DESIGN, MODELLING AND ANALYSIS OF A MULTIPLE INPUT BUCK BOOST SWITCHED CAPACITOR BASED CONVERTER

A THESIS

submitted by

CHIKKU ABRAHAM

for the award of the degree

of

DOCTOR OF PHILOSOPHY

DIVISION OF ELECTRONICS AND COMMUNICATION

SCHOOL OF ENGINEERING

Cochin University of Science and Technology.

April 2018

THESIS CERTIFICATE

This is to certify that the thesis entitled "**DESIGN, MODELLING AND ANALYSIS OF A MULTIPLE INPUT BUCK BOOST SWITCHED CAPACITOR BASED CONVERTER**" submitted by **CHIKKU ABRAHAM** to the Cochin University of Science and Technology, Kochi for the award of the degree of Doctor of Philosophy is a bonafide record of research work carried out by him under my supervision and guidance at the Division of Electronics and Communication Engineering, School of Engineering, Cochin University of Science and Technology. The contents of this thesis, in full or in parts, have not been submitted to any other University or Institute for the award of any degree or diploma. All the relevant corrections and modifications suggested by the audience during the pre - synopsis seminar and recommended by the Doctoral committee have been incorporated in the thesis.

Dr. BABITA ROSLIND JOSE
Research Guide
Associate Professor
Division of Electronics and Communication Engineering
School of Engineering
CUSAT, 682 022

Place: Kalamassery
Date: April 2018

To God Almighty, my strength

To My father and mother, my inspiration

To My family Surya, George and Hanna, my love

To My research guide, all my teachers and friends, my sincere thanks

DECLARATION

I hereby declare that the work presented in the thesis entitled "**DESIGN, MODELLING AND ANALYSIS OF A MULTIPLE INPUT BUCK BOOST SWITCHED CAPACITOR BASED CONVERTER**" is based on the original research work carried out by me under the supervision and guidance of **Dr. Babita Roslind Jose**, Associate Professor, for the award of degree of Doctor of Philosophy with Cochin University of Science and Technology. I further declare that the contents of this thesis in full or in parts have not been submitted to any other university or institute for the award of any degree or diploma.

Place: Kalamassery   **Chikku Abraham**

Date: April 2018

ACKNOWLEDGEMENTS

ABSTRACT

DC - DC converter forms the heart of any electrical or electronic circuit for lowering, raising, inverting or conditioning the output voltage from the available input voltage. Switched Mode Power Supplies(SMPS) are the widely used converters in this segment. In any modern SMPS an energy storage element is included to transfer the energy from source to load. Inductors are the widely accepted storage element in most of the present day SMPS. Inductors are capable of carrying larger currents by virtue of its construction in large power converters. However, when it comes to small converters inductors which are bulky and heavy often restrict the application in an on chip miniaturization circuit. Capacitor, which is another energy storage element, because of its high energy density and low equivalent series resistance compared to inductors, is promising for efficient on chip application. Switched capacitor converters (SCC) that are using only switches and capacitors popularly known as flying or charge pump capacitors are gaining popularity in on die power management boards.

In this thesis, after a brief literature survey, few generic switched capacitor converters that can operate in buck or boost modes are verified through simulation and hardware throwing light to the feasibility and potential of these converters. Usually SCC are found to operate from single source. However, if the converter can be made to operate from multiple sources and force the flying capacitors charging and discharging to be completed in one switching cycle, energy utilization of both sources can be tapped. The merits of elimination of bulky inductor and utilization of multiple sources, has resulted in this thesis, the development of new series parallel Switched Capacitor Converter (SCC) topology capable of operating off two independent input sources and generating target output voltage in buck or boost mode. The converter with only 9 switches, 5 diodes and 2 flying or charge pump capacitors can deliver 11 voltage conversion ratio or gain at the output. Operation principle, voltage conversion ratios (VCR), modelling considerations in different operation modes and extensive loss analysis are derived. The converter is robust and may be operated off one or two input sources, having the ability to change conversion ratio over a wide range. The proposed model assumes that the

conduction losses are proportional to the average current flowing through each of the charge pump capacitor in a switching phase. Capacitor current instantaneous waveform in the complete charge, partial charge and no charge modes are captured in simulation and experiment. Model predicted equivalent resistance, output voltage and instantaneous capacitor current waveform concur excellently with simulated and experimental values, rendering the new converter as an excellent candidate for two and single input source applications. An extension of the converter VCR, again with only 9 switches and 2 flying or charge pump capacitors, eliminating the 5 diodes, but delivering another two more output voltage conversion ratio or gain extending from 11 to 13, at the output has been verified. Furthermore, with the addition of one more switch, thus altogether 10, an inversion mode of operation is also realized increasing the possible VCRs to 15 in total, qualifying the converter to work in a wide range of output voltages operating from two independent sources. The elimination of 5 diodes is possible if CMOS switches are used in place of MOSFET switches. An implementation of the proposed converter using CMOS switches is verified for all the 15 modes which will not only improve the efficiency but also reduce the circuit size. Another demand of any good converter is its regulation capability. In inductor based converter this is achieved by varying the duty ratio of switching. Regulation in the proposed SC converter is implemented in two ways. Firstly, by varying the frequency at which the switches are turned on and off, the equivalent resistance of the converter varies and in turn the load voltage can be regulated. Secondly, by selecting a particular voltage conversion ratio the converter is made to restructure its topology by gating the switches in a predefined logic to obtain the required output voltage. Both the methods are verified in the prototype and an application to power white LEDs utilizing two input sources, one of which a renewable energy source (solar) is also demonstrated.

TABLE OF CONTENTS

LIST OF FIGURES

xiii

LIST OF TABLES

ABBREVIATIONS

AC	Alternating Current
ASCII	American Standard Code for Information Interchange
CMOS	Complementary Metal Oxide Semiconductor
CP	Charging Phase
CS	Charge State
CSTS	Charge State Transfer State
DC	Direct Current
DP	Dumping Phase
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	Electro Magnetic Interference
ESR	Equivalent Series Resistance
FC	Full Charge
FSL	Fast Switching Limit
IC	Integrated Circuits
IGBT	Insulated Gate Bipolar Transistor
ITRS	International Technology Roadmap for Semiconductors
KVL	Kirchoff's Voltage Law
LED	Light Emitting Diode
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
NC	No Charge
PC	Partial Charge
PCB	Printed Circuit Board
PFM	Pulse Frequency Modulation
SCC	Switched Capacitor Converter
SIP	System In Package
SMPS	Switched Mode Power Supplies
SoC	System On Chip
SSL	Slow Switching Limit

TS	Transfer State
VCR	Voltage Conversion ratio
VSS	Variable Structure System
ZCS	Zero Current Switching

NOTATIONS

C_{CS} Equivalent capacitance in charge state

C_{filter} or C_0 Filter capacitor

C_{fly1} or C_1 Flying capacitor 1

C_{fly2} or C_2 Flying capacitor 2

C_{TS} Equivalent capacitance in transfer state

$d\boldsymbol{q}_{CP}^{x}$ Differential values of Electric charge during the charging phase in x^{th} flying capacitor

$d\boldsymbol{q}_{DP}^{x}$ Differential values of Electric charge during the dumping phase in x^{th} flying capacitor

$dq_{CP,Vs}$ Differential values of electric charges at the input terminal during charging phase

$dq_{CP,VLoad}$ Differential values of electric charges at output terminal during charging phase

$dq_{DP,Vs}$ Differential values of electric charges at input terminal during dumping phase

$dq_{DP,VLoad}$ Differential values of electric charges at output terminal during dumping phase

dq_{Vs} Differential values of electric charges at input terminal

dq_{VLoad} Differential values of electric charges at output terminal

ESR_{CS} Flying capacitor equivalent series resistance in charge state

ESR_{TS} Flying capacitor equivalent series resistance in transfer state

I_{Cavi} Average flying capacitor current in any operating phase "i"

$I_{Load,avg}$ or I_{out} Average load current

$I_{s,avg}$ or I_{in} Average input current

λ_{CS} Ratio $\frac{t}{RC}$ in charge state

λ_{i} Ratio $\frac{t}{RC}$ in any operating phase "i"

λ_{TS}	Ratio $\frac{t}{RC}$ in transfer state
Φ_{CS}	Proportionality factor in charge state
Φ_i	Proportionality factor connecting charge and transfer states
Φ_{TS}	Proportionality factor in transfer state
P_{Routi}	Power dissipated in the output resistance in any operating phase "i"
R_{CS}	Switch ON state resistance in charge state
$R_i C_i$	RC product in any operating phase "i"
R_{load} or R_L	Load resistance
R_{on}	Switch ON state resistance
R_{outCS}	Modeled converter resistance in charge state
R_{outTS}	Modeled converter resistance in transfer state
R_{out}	Switched capacitor modeled equivalent resistance
$R_{S1} - R_{S10}$	Switch ON state resistance
R_{TS}	Switch ON state resistance in transfer state
S1-S10	Transistor switches
S_{Batt}	Switch connected to battery source
$S_{CS} R_{on}$	Switch ON state resistance in charge state
S_{Solar}	Switch connected to Solar source
$S_{TS} R_{on}$	Switch ON state resistance in transfer state
T_{CS}	Time period in charge state
T_i	Time period in any operating phase "i"
T_{TS}	Time period in transfer state
V_{Cfly1}	Flying Capacitor 1 Voltage
V_{Cfly2}	Flying Capacitor 2 Voltage
V_{diode}	Total modeled diode voltage drop
$V_{diodeCS}$	Modeled diode voltage drop in charge state
$V_{diodeTS}$	Modeled diode voltage drop in transfer state
V_{in}	Source Voltage
V_{in1}	Source Voltage 1
V_{in2}	Source Voltage 2

V_{Load} or V_{out} Load Voltage

V_s Gain Voltage after conversion at the secondary in the SCC model

W_{CP} Energy consumed during the charging phase

W_{DP} Energy consumed during the dumping phase

W_{Routi} Energy consumed by the output resistance in any operating phase "i"

W_T Total energy consumed in one complete cycle

CHAPTER 1

INTRODUCTION

Switched capacitor converters (SCC) are gaining in popularity during the last decade and a half. Comprised only from switches and capacitors this family of power converters provides many options to create large conversion ratios in both step up and step down modes. The lack of magnetic components is yet another advantage of this family, rendering it as an excellent candidate for on chip integration. With the growing demand for power processing and miniaturization in the fields of communications and renewable energy harvesting, a fully integrated voltage regulator with tight regulation, capable to operate from the same global power supply is gaining more and more attention. This chapter briefs the need for SCC, the purpose and objectives of this research work. Chapter organization of the thesis is also included in this chapter.

1.1 Background: Need for Switched Capacitor Converters (SCC)

Power converters are an inevitable part of any electrical or electronic gadget. It is usually connected between the source and load. There are different topologies of power converters available in the market with isolation and non isolation. The buck, boost, buck-boost, Cuk, Sepic are few such non isolated converters and the forward, flyback, push pull, half bridge and full bridge are some of the isolated converters derived from the basic buck or buck boost converters. All these converters use an energy transfer element and inductor is the popular choice due to its high current carrying capability in high power applications. Thus the switched inductor based converters are good choice for high power applications and in requirements where output voltage regulation is important (Mohan *et al.*, 2003). However, the switched inductors are bulky for on chip integration in power converters and associated magnetics cause Electro Magnetic Interference (EMI) at varied switching frequencies. Eliminating the inductor is one solution for such problems.

System integration and very large scale integrated circuit technology has matured and growth has been exponential over the last decade. Customized System on Chip (SoC) and System in Package (SIP) designs are replacing the conventional standard circuit designs enabling system integration to miniaturize the on board size, allowing parallelism and efficient PCB area usage. This has been reported in the 2015 International Technology Road map for Semi conductors (ITRS2.0, 2015). Many IC and chip manufacturers have come out with solutions since last decade to address this issue. Many functions are integrated into a system on chip application with reduction in size and space, however the power distribution to the boards at different voltage levels from a global input supply has not shrunk in form factor and integration. The need for reducing the PCB area used by the power management units which works from a global input supply and delivering different output voltages is illustrated as an example in the apple series iPhone 3GS, iPhone 4S and iPhone 5 reported in a recent work published in (Le, 2015). The three boards are shown in figure 1.1 (a - c). Here the power management system shown in red boxes have not shrunk in size compared to the SoCs mainly due to the dependency on inductor as an energy transfer element. Using capacitor instead of inductor to transfer energy is thought of by researchers as an alternative to the above problems and SCC has gained significance.

Switched-capacitor (SC) DC - DC power converters are a novel set of DC - DC power converters drawing attention of industry and researchers. They are implemented by a combination of switches and capacitors. The capacitors are made to charge and discharge through different paths producing an output voltage that is proportional to the input voltage. The presence of inductors, magnetic storage elements and transformers make the traditional converters bulky, less efficient and decreases power density. Since SC converters only use switches and capacitors it offers high power density, small size and more importantly Integrated Circuit (IC) implementation potential is large. Through different combinations of switches and capacitors as well as proper control methods, SC converters are able to produce an output voltage that may be higher or lower or level shifted multiple input multiple output voltages can be realized. SC power electronics are well suited for low power supplies or small output power applications where no DC - DC isolation between the input and output is necessary (Sanders *et al.*, 2013).
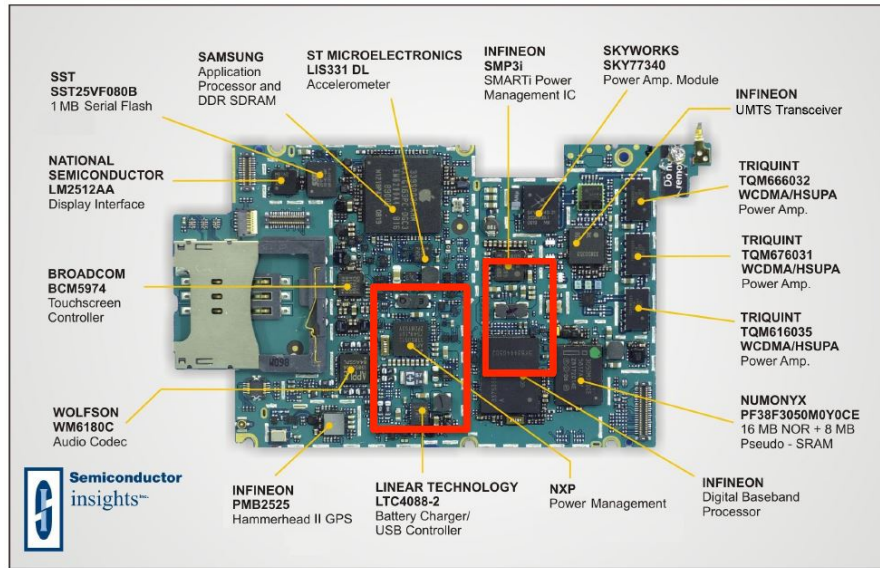
(a)
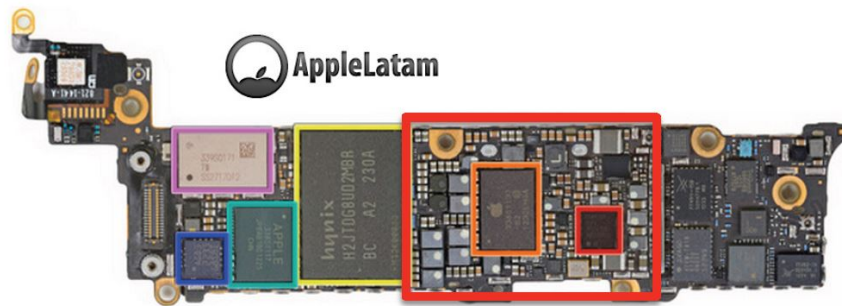
(b)
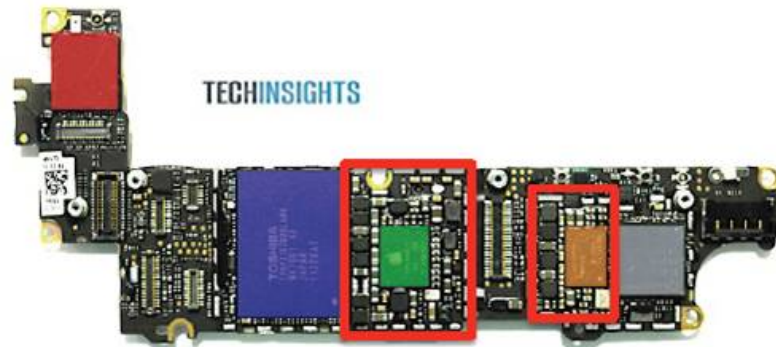
(c)

Figure 1.1: Apple iPhone Boards (a) 3S (b) 4S (c) 5S (Le, 2015)

1.2   Purpose and Objectives of the Research

The purpose of this research work is to develop a novel SC converter topology with the following objectives.

1. To explore various existing SCC topologies.

2. To Propose a new SC converter topology with less switches and capacitors which can operate off two independent sources delivering more output Voltage Conversion Ratios (VCR) than the existing ones.

3. Study the regulation methods and ripple in the output voltage of the new converter.

4. Provide good theoretical framework for the new converter topology by developing a mathematical model.

5. Simulation studies on the proposed topology and verify with the mathematical model for accuracy.

6. Development of a prototype and validating experimentally the new converter topology for the various VCR proposed.

7. Comparing the model derived, simulated and experimental results for validating the output of the converter.

8. Explore the possibility of implementation of new SC converter using CMOS switches and propose additional VCRs.

9. To power white LEDs using the new converter operating from two independent input sources (battery and solar) by sensing solar energy and utilizing it to the maximum.

1.3   Organization of the Thesis

Chapter 1 gives the motivation and purpose of the research work along with the organization of thesis.

Chapter 2 focus on the fundamentals of a SC converter, its equivalent circuit and few basic types available in literature. A detailed literature survey about the various topologies in both hard and soft switched category along with a few commercially available SC converters voltage regulator is also discussed in this chapter.

Chapter 3 investigates a dual input single output voltage SCC topology through simulations. The topology presented is powered by two input sources using only five components and producing an output voltage which is the sum, difference, double, half or inverting combination of the sources. This topology is however, lacking the ability to change the gain, forcing an operation at a single conversion ratio, and sacrificing efficiency once a regulation over wider range is needed.

Chapter 4 presents a dual input variable output voltage SCC that can be operated in step down mode and unity mode. The feature of the converter is that it can be selectively switched between two input sources one being a solar source. Since inductors are eliminated in the circuit topology the converter is light in weight and size. Simulation studies and hardware realization of the converter are reported here.

Chapter 5 enumerates the new multiple input multiple output buck boost based DC - DC SCC that is designed to operate off two independent sources and delivering multiple output voltages by intelligent gating and variable circuit structure. A complete accurate methodology for theoretically and mathematically modelling the new converter using the average current conduction loss model is developed and detailed in this chapter. Subsequently in the chapter, the model derived, simulated and experimental results along with efficiency of the proposed converter for three different frequencies are reported. An in depth analysis of flying capacitor current waveform, which is the heart of SCC, is captured through simulation and experiments and presented in this chapter.

Chapter 6 reports the extension of possible new VCRs and implementing the same converter using CMOS switches. Furthermore, the capability of the new converter to work in tandem between two sources of input power which are battery and solar to power a string of LED's is presented. The input voltage is sensed between solar and battery. If the solar voltage drops down to less than a threshold value the LED's are

powered completely by the battery. Hence maximum utilization of solar energy is ensured by the proposed multiple input multiple output SCC. Two regulation techniques are briefly discussed in this chapter, the variable voltage VCR and variable frequency control regulation method.

Chapter 7 concludes the entire work highlighting the key contributions and put forward few suggestions for future work.

CHAPTER 2

REVIEW OF SWITCHED CAPACITOR BASED CONVERTERS

The requirement of any switching mode power converter is to provide a regulated output voltage (DC or AC) at different levels across the load even though the input voltage or load may vary. Thus a control strategy is to be properly designed for adjusting the switching topologies for efficient regulation. As mentioned in the introduction, SC converters uses only capacitors and switches thereby eliminating the inductor and the associated magnetics. Moreover, integrated capacitors can achieve higher capacitance density and low ESR. Wherever a wide range of variable voltage is required with high efficiency, switched regulators are preferred. SC converters were traditionally used to provide programmable voltages to memories but catering to only very few watts of power. This chapter surveys the latest developments in SCC research and later discuss the operating principle, equivalent circuit model and few generic topologies with SCC regulators introduced by leading electronic manufacturers.

2.1 Operating Principles of Switched Capacitor Converters (SCC)

A SCC can be thought of as a power converter which consists of only switches and capacitors. The switches are controlled in such a way that the capacitors are charged and discharged through different paths, producing an output voltage as fixed fraction of the input voltage. The different combination of switches and capacitors result in different topologies which can produce step up, step down or polarity reversal of the input voltage. As the operation of switched capacitor is characterized by repetitive change in circuit structure, it is identified as a Variable Structure System (VSS). In Figure 2.1, it can be seen that there are three ports to which a voltage source, current source or load can be connected. This connection can be expanded for increasing the

conversion ratio as the requirements demand. Few current trends in SCC research trends can be found in (Nguyen *et al.*, 2017; He *et al.*, 2016).
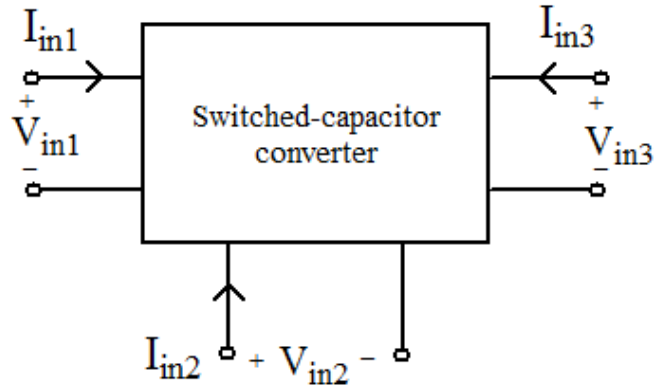
Figure 2.1: A SCC with 3 ports

2.1.1   A Step Up Switched Capacitor Converter

To explain the basic working of a step up and step down SCC (Van Breussegem and Steyaert, 2012) is taken as reference. In Figure 2.2a, a step up SCC converter is shown. By turning on and turning off the switches to change the connection of flying capacitors, they can be charged or discharged and therefore the charges can be dumped into or removed from the output of the converter. Therefore these types of converters are also called charge pump converters. There are two phases or states namely Charge State (CS) and Transfer State (TS) in one complete cycle of operation. Two types of capacitors are used in switched capacitor converter; charge pump or flying capacitors and output filter capacitor or buffer capacitors or bypass capacitors. Flying capacitors are the charge transferring capacitors whereas the output buffer capacitor influences the start-up behavior and steady state characteristics of the converter and does not take part in charge transfer. Referring to Figure 2.2a, during the charge phase CS, diode D_1, flying capacitor C_{fly} and turning on the switch SW_1, C_{fly} will charge to input voltage source V_{in}. In the next phase, TS, gating SW_2, V_{in} is connected in series with already charged C_{fly} to establish an output voltage $V_{out} \equiv 2V_{in}$ across the load R_L, through the diode D_2. The second type of capacitor used in this circuit is C_{out} used to maintain the load voltage constant, ripple free and to supply the load current during the CS when C_{fly} is disconnected from the load. Here the diodes can be replaced with switches and appropriate switching scheme can be devised to obtain the required step up output. The

equivalent circuit during the CS and TS modes are shown in Figure 2.2b. It can be seen that during CS the flying capacitor charges to input voltage V_{in} and in TS C_{fly} is connected in series with V_{in} to deliver a step up voltage of $2V_{in}$. Another step up SCC for obtaining high voltage gain can be found in (Abutbul *et al.*, 2003; Liang *et al.*, 2012).

(a)

(b)
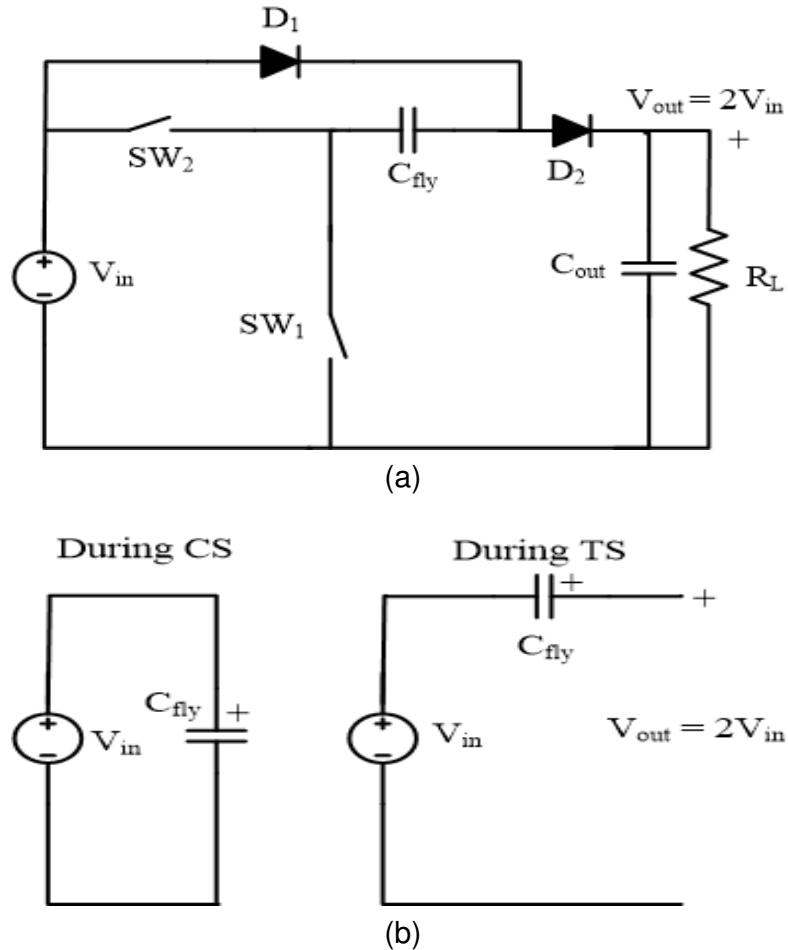
Figure 2.2: Step Up Switched Capacitor Converter (a) Circuit Topology (b) Equivalent Circuit Structure during CS and TS modes

2.1.2 A Step Down Switched Capacitor Converter

In this section, a step down or buck type SCC is explained. The circuit topology of the converter is shown in Figure 2.3a. During the charge phase CS, input voltage V_{in}, SW_1, flying capacitor C_{fly1} and diode D_1 gets connected to the second flying capacitor C_{fly2}. Thus both the capacitors get charged to $V_{in}/2$ volts. In the TS mode , switch SW_2 is gated and diode D_2 conducts. The flying capacitors voltage $V_{in}/2$ is now connected in parallel and delivering the load current. The voltage across the parallel combination

9

which is also the output voltage is given by $V_{out} \equiv V_{in}/2$ volts. The equivalent circuit and the voltage across the flying capacitors are shown in Figure 2.3b. More step down or Buck SC based converters can be found in (Chang *et al.*, 2010; Ben-Yaakov and Evzelman, 2009; Kilani *et al.*, 2016)
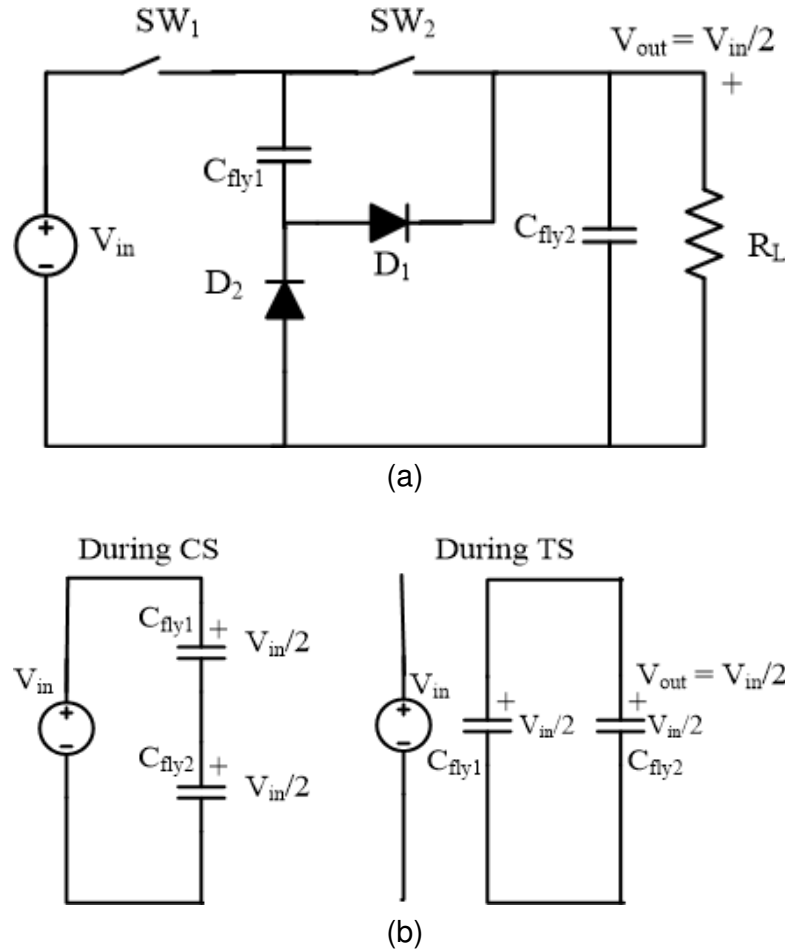
Figure 2.3: Step Down SC Converter (a) Circuit Topology (b) Equivalent Circuit Structure during CS and TS modes

2.2 Switched Capacitor Converter Model

A SCC can be basically modeled as an ideal transformer with turns ratio n, the unloaded conversion ratio and R_{out} the equivalent converter resistance (Henry and Kimball, 2011; Seeman, 2009) as shown in Figure 2.4. Here, V_{in} is the input voltage and V_{out} is the actual output voltage and V_s is the targeted secondary voltage after conversion, or no load output voltage. The switches used in SC converters are usually MOSFETs that could be treated as the ON state resistance $R_{ds}(ON)$ during their conduction state that influences the output voltage and contributes to the conduction losses, which in turn af-

10
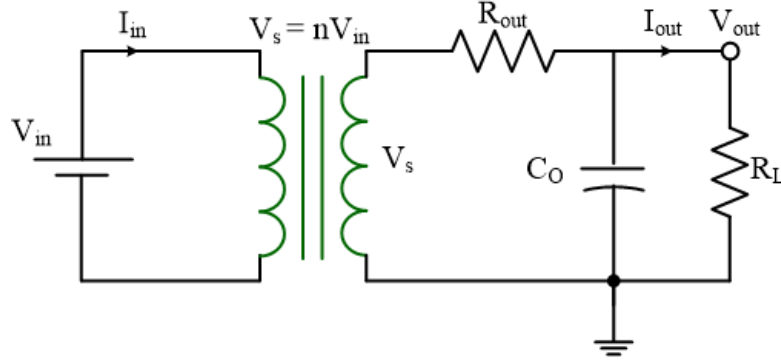
Figure 2.4: A SCC Equivalent Circuit Model

fect the efficiency. Equivalent series resistance (ESR) of the capacitors also adds to SCC conduction losses. Therefore the model has to take into account both switch resistances and capacitors ESR to determine the equivalent converter resistance. If voltage drop devices are used, such as diodes, the diode losses as a result of forward voltage drop needs to be included in the model. This model is used later in the newly proposed converter for detailed analysis.The efficiency of an SCC can be expressed by the equation 2.1 (Evzelman and Ben-Yaakov, 2013; Seeman and Sanders, 2008).

$$\eta = \frac{V_{out}}{nV_{in}} = \frac{V_{out}}{V_s} \tag{2.1}$$

2.3 Developments in SCC Research over the Last One and Half Decades

Switched-capacitor (SC) DC-DC power converters are gaining popularity and interest for researchers who are primarily looking for ease of integration and less space. An intelligent connection of capacitors and switches forcing the capacitors to charge and discharge through different paths can generate output voltage that can be stepped up or down. The main disadvantage in integration and size of conventional converters is the presence of bulky space consuming elements such as inductors and transformers. This can also decrease the power density. Author found in (Ioinovici, 2001), one of the early SCC researchers, reported that since SC converters only use switches and capacitors power density is more, miniature circuit size and all of these advantages can ease IC implementation. Few early switched capacitor steady state analysis, a step up converter based on SCC and focus on SCC with emphasis on efficiency, regulation and

11

ripple can be seen in (Ngo and Webster, 1994; Zhu and Ioinovici, 1996; Mak *et al.*, 1995). Another interesting early analysis on lossless SCC and the performance of SCC can be found in (Tse *et al.*, 1995; Makowski and Maksimovic, 1995). SCC belong to the family of new generation converters as an alternative to the conventional inductor based buck, boost or buck boost converters. These converters are applied in all-purpose LED lighting (Lee *et al.*, 2016; Sanders and Kline, 2016; Wong *et al.*, 2017), indoor and outdoor lighting, portable hand-held devices (Lei *et al.*, 2017, 2016*a*), flash memory, flash lighting (Dagan *et al.*, 2014; Sako *et al.*, 2016) and in many medical gadgets (Narayanasamy *et al.*, 2017; Pandey *et al.*, 2017). A comparison between the performance of an inductor based converter and a switched capacitor converter is described in (Seeman *et al.*, 2010; Ye and Cheng, 2017*b*) where the switches and reactive elements are analyzed in terms of the limits of utilization. This limit is defined in terms of the ratio of output power with respect to the energy stored in inductor or capacitor. The authors also discussed about the regulation strategies that can be adopted. SC converters are also finding interest in hybrid vehicle applications (Amjadi and Williamson, 2010; Chau and Chan, 2007), battery charging balancing (Baughman and Ferdowsi, 2008; Pascual and Krein, 1997; Kim *et al.*, 2014) and energy harvesters due to its low size (Jung *et al.*, 2014*b,a*). Switched capacitor converter research has also been in the field of biomedical applications which demand safe power in milli/micro watt ranges (Huang and Oberle, 1998; Wong *et al.*, 2004; Chandrakasan *et al.*, 2008). Application of SCC in AC circuits for multilevel inverters can be found in (Sano and Fujita, 2008).

2.3.1 Common Switched Capacitor Converter Topologies

Few common SCC topologies are discussed in this section and most of the other topologies have generated from one or more combinations of the fundamental generic topology. The proposed converter in this thesis is derived from the generic series - parallel topology. Some of the topologies of interest are,

1. Dickson topology

2. Fibonacci topology

3. Ladder topology

4. Series - Parallel topology

Dickson Topology

Dickson converter, widely used in ac circuits as a voltage multiplier, is a two state converter proposed by (Dickson, 1976; Van Breussegem and Steyaert, 2012). This converter is actually a step up converter and originated as an extension of the Grienacher multiplier circuit. In AC circuits very high voltages were needed for conducting particle physics experiments as well as insulation testing in electrical engineering. Grienacher multiplier is popularly known by the name Cockroft - Walton voltage multipliers. When the requirement of high voltages greater than 10 V (with respect to the on - chip voltages) were needed, the Cockroft - Walton voltage multiplier was modified by Dickson to propose a new topology in SCC called the Dickson topology. In Cockroft - Walton voltage multiplier, the charge pump capacitors were connected in series but in Dickson topology the capacitors are connected in parallel which reduces the effect of stray capacitors. The need for high voltage in on chip applications are to write or erase data. Later, this converter topology found application in implementing "on chip" for stepping up voltage since the circuit is composed of only switches. The circuit diagram of a Dickson step up SCC is shown in Figure 2.5. More control and applications of Dickson converter can be found in (Dickson, 1980; Lei *et al.*, 2016*b*).
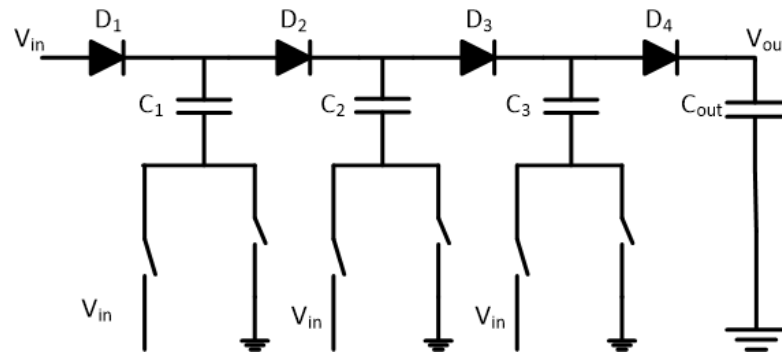
Figure 2.5: Dickson SCC Topology

In Figure 2.6a and Figure 2.6b the circuit states during CS and TS are shown. It can be seen that the diodes D_1 and D_3 conduct during CS and transfers charge to the load. In TS diode D_2 and D_4 conduct and D_1 and D_3 blocks. The charge pump or flying capacitor C_1, C_2 and C_3 potential is altered by triggering the switches. In advanced form of Dickson SCC, the diodes are replaced by active switches.
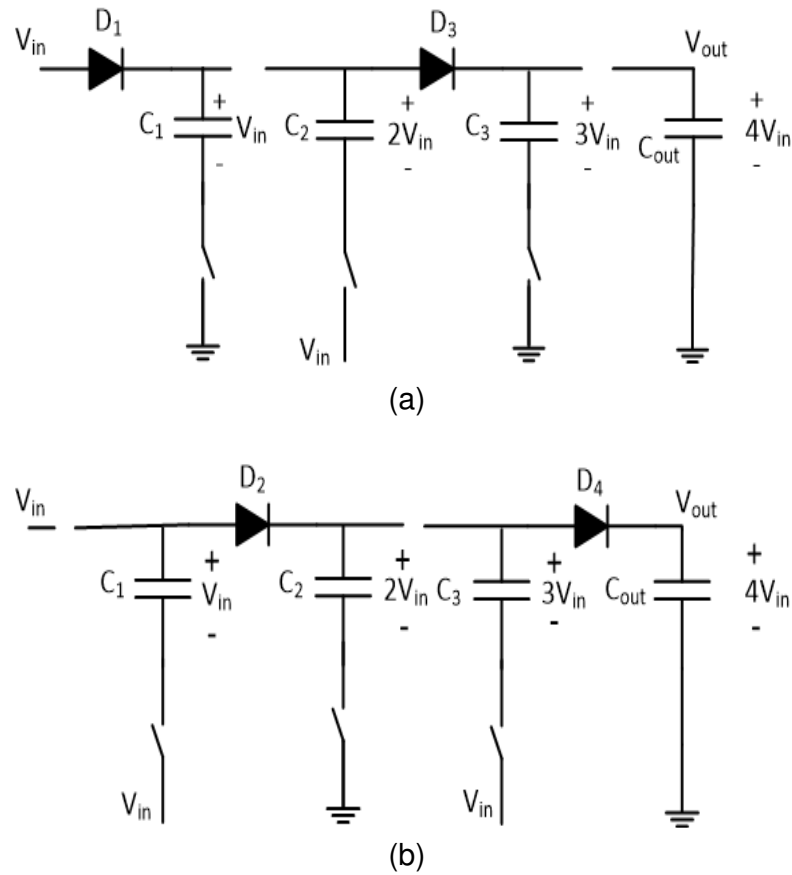
Figure 2.6: Dickson SCC Topology Circuit States (a) Charge State (CS) (b) Transfer State (TS)

Fibonacci Topology

A Fibonacci SCC is another topology which gives the higher conversion modes with two states CS and TS (Kushnerov and Ben-Yaakov, 2013; Kushnerov, 2014). The Fibonacci series is represented by the number series 1, 1, 2, 3, 5, 8, 13, 21.... In one stage the circuit comprises of three switches and one capacitor. If we add more stages of this combination "n" stages can be obtained with proper gating of the switches. Referring to the circuit topology of a Fibonacci topology in Figure 2.7, one cell in the stage is clocked opposite from the cell before it. Here there are three such cells and can be extended to "n" stages. The switches designated odd numbers are clocked in CS state and the one with even numbers triggered in TS state. Detailed analysis of a Fibonacci converter can be found in (Seeman, 2009; HARADA *et al.*, 1992).

A binary and Fibonacci SCC topology can be a good combination for getting step up and step down voltage levels. A resonant version of it can be found in (Hamo *et al.*, 2012) featuring a bidirectional medium power transfer capability. The resonant inductor
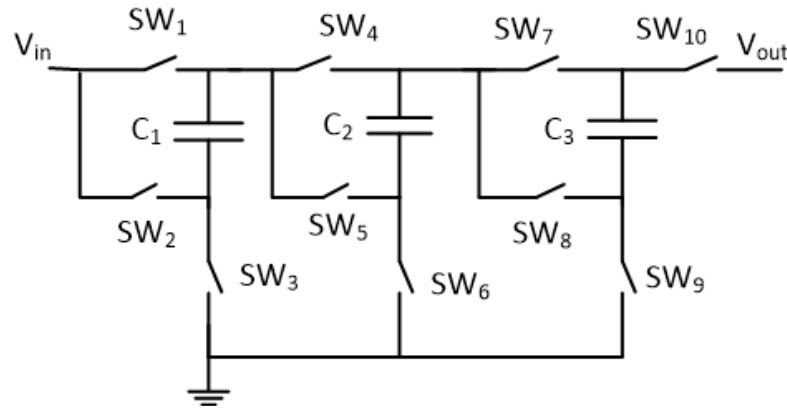
Figure 2.7: Fibonacci SCC Topology

is realized using the stray inductance without addition of another inductor. The switches include two N channel MOSFETS connected to common source and common gate. This arrangement will prevent the unwanted conduction in the reverse direction when the switches are off. Using 3 flying capacitors, 13 conversion ratios in the fractional range is realized in the referred work.

Ladder Topology

Ladder converter is comprised of two sets of series capacitor that can charge from the input supply during charging in the first phase and discharging through the load in the second phase. With "n" flying capacitors a conversion ratio of $\frac{2}{n+3}$ can be achieved. Another advantage of a ladder topology is that it is a multi output converter since the output DC can be taken from different points. To operate SCC in high voltage levels ladder topology can be an option.

A variation from the generic ladder topology to an improved version that can handle few kilovolts as well as the resonant version can be found in (Lopez *et al.*, 2012; Dias and Lazzarin, 2016). The circuit illustration of a Ladder topology is given in Figure 2.8. Here the flying capacitors C_1, C_2 and C_3 are connected to the input voltage V_{in} by the proper sequencing of turning on and off the switches. The intermediate points where DC voltage tapping can be taken is marked as V_{int}. This topology though has many advantages it requires large number of switches. A solar photovoltaic application of ladder topology can be found in (Kesarwani and Stauth, 2012).

Figure 2.9a and Figure 2.9b shows how different voltages can be tapped through
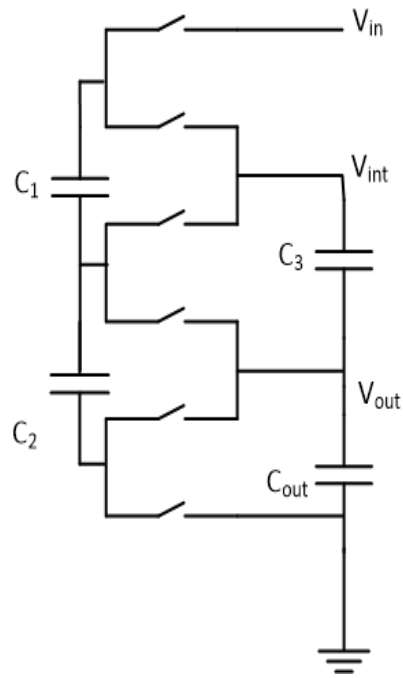
Figure 2.8: Ladder SCC Topology

(a)   (b)
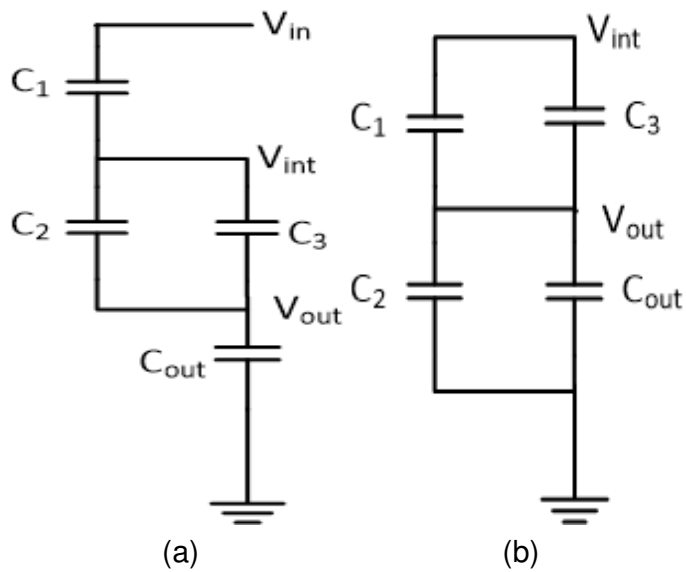
Figure 2.9: Ladder SCC Topology (a) Intermediate DC Tapping Solution 1 (b) Interme-
        diate DC Tapping Solution 2

intermediate stages by the reconnection of capacitor in sliding mode by triggering the
relevant switches. In solution 1, C_1 is in series with C_2 and C_3 in parallel, where as in
solution 2, C_1 and C_3 are in parallel, similarly C_2 and C_{out}.

Series - Parallel Topology

Series - Parallel topology is a simple and straight forward converter type. The capacitors are charged parallel in charge state (CS) and discharged to the load in series during the transfer state or (TS). Figure 2.10a shows the circuit diagram of the series - parallel topology and Figure 2.10b in CS and TS modes for a step up voltage conversion ratio (VCR) of 3.

(a)

(b)
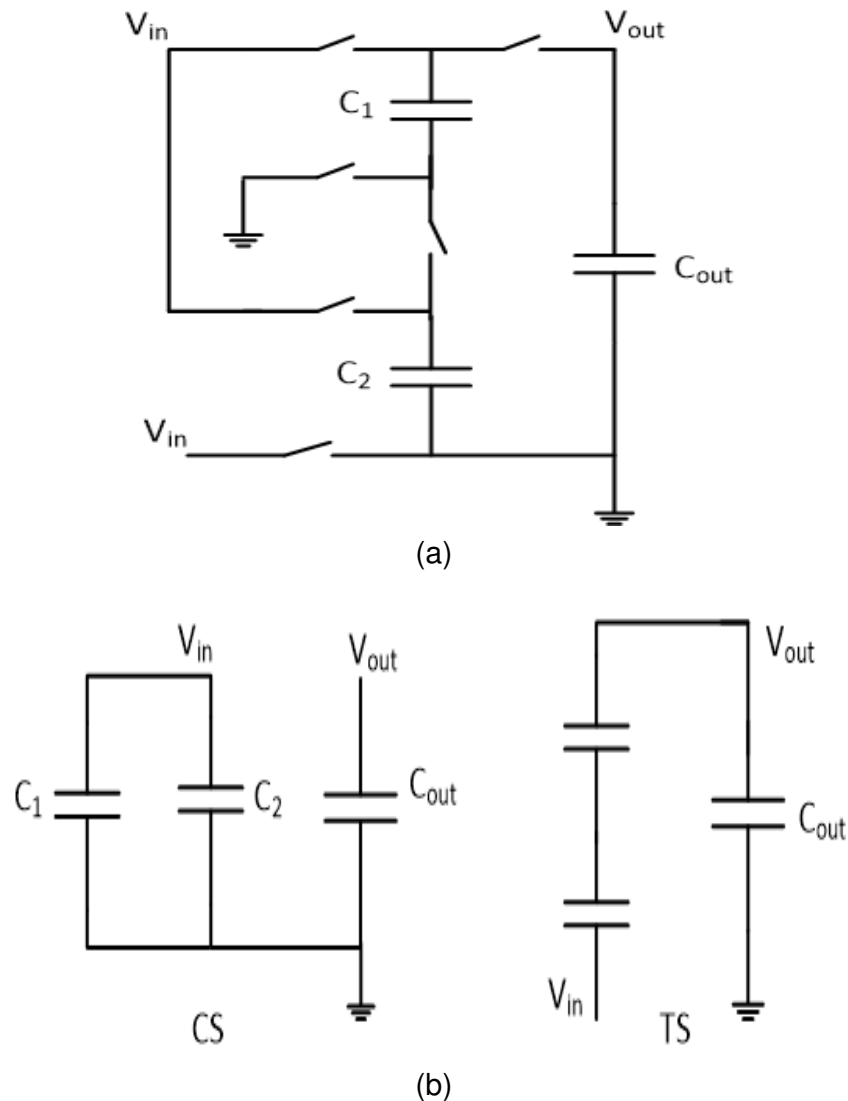
Figure 2.10: Series - Parallel SC Converter for VCR of 3 (a) Circuit Topology (b) Equivalent Circuit Structure during CS and TS modes

Another derivative of the series - parallel converter consists of charging the flying capacitors in series and then discharging it in parallel as seen in (Myono, 2004). Usually this mode gives a step down operation. In the proposed new converter in this thesis the inspiration was derived from the series - parallel converter topology for obtaining both buck and boost modes of operation from two sources. The detailed topology and

working principle is explained in later half of the thesis.

2.3.2   A Dual Input Switched Capacitor Converter

The research work reported by (Yuanmao and Cheng, 2012; Guo *et al.*, 2014) discusses a dual input SC converter with six voltage conversion ratios (VCR) alongside with the resonant switching to decrease the switch stress. To switch between any of the desired six conversion ratios the converter operates with only two switches, two diodes, one flying capacitor and a filter capacitor. However, the circuit topology has to be changed for each of the conversion ratios and all modes cannot be realized within one circuit.It is powered by two input sources using only five components and producing an output voltage which is the sum, difference, double, half or inverting combination of the sources. This topology is however, lacking the ability to change the gain, forcing an operation at a single conversion ratio, and sacrificing efficiency once a regulation over wider range is needed. A resonant version with reduced switch stress, and an extension to include multiple sources summation circuit and subtraction circuit can be found in (Yuan-mao and Cheng, 2013). As mentioned above, the addition of inductor partially defeats the whole purpose of miniaturization friendly converter. A SCC that accepts 3 input voltages and provide different output level and stages can be found in the patent (Oraw and Kumar, 2010) using 14 switches and 3 flying capacitors. Another SCC that accepts dual input voltage rail can be found in (Miller *et al.*, 2002).

2.3.3   Resonant Switched Capacitor Converter

Earlier, a resonant SC converter has been proposed in (Yeung *et al.*, 2004). A CMOS based DC-DC switched capacitor patent using an inductor limiter can be found in (Forbes and Ahn, 2002). The switches in normal SCC topologies works in the hard switched mode. To operate the switches in the soft switch mode a small resonant inductor is added. The resonant switching has been introduced to increase efficiency of SC DC to DC converters. A very small inductor is added to create a resonant turn-on and turn-off when the transistors are switched on or off, respectively. Zero-current switching condition in both switching on and off is obtained so that both switched loss and electromagnetic interference are low. Transistor current is limited by the small resonant

inductor. Topologies were proposed for 1/2 -mode, 1/3-mode and 1/4-mode step-down converters as well as the corresponding step-up counterparts. However, in (Ioinovici *et al.*, 2006, 2007), the author critically evaluates and comments on the work cited by (Law *et al.*, 2005; Yeung *et al.*, 2004) disagreeing that the introduction of an inductor to provide resonance will reduce the merits of a SC converter, which is true since all the efforts in SCC research has been to eliminate the magnetics and its associated disadvantages. Coupled inductor along with switched capacitor techniques are also gaining popularity for obtaining high voltage gain (Hsieh *et al.*, 2012; Stauth *et al.*, 2013).

Several research work in the recent years has progressed in the resonant switched capacitor even though it poses the question of addition of inductor. The focus on a resonant operation to charge and discharge the capacitor during zero voltage or zero current through the switches than forcing it to periodically perform the charging and discharging is discussed in (Shoyama *et al.*, 2004; Cervera *et al.*, 2017*b*,*a*). The efficiency of the converter deteriorate during the forced operation and therefore limits it to use in small current applications. High efficiency even at high current output is the advantage of resonant operated switched capacitor converters than conventional SCC. A buck type resonant converter is taken as an example and the complete analysis and experimentation has been discussed. Another quasi resonant converter is detailed in (Yuanmao *et al.*, 2012) that can be used to equalize the charging of a series string battery management system. There is always an unbalance in the battery cell voltage and quasi resonant tank designs can overcome this problem to increase the system efficiency. Another resonant switched converter known as zero current switching resonant converter is proposed in (Lee *et al.*, 2005; Ye and Cheng, 2017*a*). This converter enables bidirectional power flow and features all the advantages of normal SCC with reduced current stress on the switches. A resonant SCC voltage multiplier to deliver a steep voltage gain is given (Rosas Caro *et al.*, 2015). High voltage gain is realized by serially charging the capacitor with the voltage of capacitors that already have been charged in the previous state. To make the input current continuous a small inductor is added and this will wipe out the resonant current from all the switches. A zero-current-switching (ZCS) Bidirectional Interleaved Switched-Capacitor (BISC) *DCDC* converter is proposed in (Choi *et al.*, 2016). Another feature of the converter is that it uses the stray inductance in the circuit for resonance purpose to achieve zero current switching. This converter presents high

voltage gain along with bidirectional power flow. The interleaved approach has been used in SCC circuits to increase the current rating and also to reduce the ripple as reported in another work by (Han *et al.*, 2006). An interleaved discharging approach was used to reduce the output ripple in switched-capacitor-based step-down dc-dc converters. This method takes full advantage of structure of step-down SC DC-DC converter. Unlike ordinary interleaving technique it does not need any extra converter cells to be connected in parallel. Moreover this method does not need some extra driving signals for the switches, but simple flip-flops and similar circuits are enough. This method also provides flexibility in optimizing the design of SC DC-DC converters. With this method capacitance of the output filter could be reduced for lower cost and higher power density. In addition, switching frequency could be reduced for higher efficiency which is possible because of the reduced switching losses. The efficiency is improved due to decrease in discharging period of capacitors and hence conduction losses. The steady state performance was analyzed using charge conservation method.

A unified modelling methodology is explained by (Hamo *et al.*, 2015*b*) to study the losses in resonant SCC that is operating in zero current switching (ZCS) mode. The switches are turned off naturally when zero current state is achieved and is termed as self commutation. The SCC which can be modeled as R_{out} the equivalent converter resistance in figure 2.4 is derived based on the concept that a single conduction path exists for the resonant current. This concept is extended to model the losses by assuming that the current is divided among several conduction meshes. Another work reported by (Hamo *et al.*, 2015*a*) introduces an active method for ZCS resonant switched capacitor converters (SCC) that can operate over wide range. A binary SCC is selected for the demonstration and due to soft switching operation high efficiency is achieved.

2.3.4 Switched Capacitor Converter Based Industrial Regulators and Drivers

A wide variety of SCC regulators and drivers have been introduced in the market by different manufacturers. This section introduces a few of them. (LM2788, 2013) is a 120 mA high efficiency step down switched capacitor voltage converter of Texas instruments. It is a step down converter with the output options of 1.5, 1.8 and 2.0 V

for an input range of 2.6V to 5.5 V. This regulator uses two 1 μF flying/charge pump capacitors and two 10 μF filter capacitors with no inductors, making the size compact. Standard protection features like soft start mechanism, over temperature and over current is provided. From the operational end this converter features fractional gain, Pulse Frequency Modulation (PFM) for regulation and auto gain selection to improve overall efficiency. A detailed explanation on the selection of output capacitor and flying capacitor is also given in the data sheet. This converter with line and load regulation is also known as a Three Charge Pumps in One SC converter. This regulator finds application in cellular phones, portable electronic equipments and hand held instrumentation.

A switched capacitor voltage converter regulators of Texas instruments is given in (LT1054, 2015). It can operate in an input voltage range of 3.5 V to 15 V delivering 100 mA to the load at -5 V. It provides regulation for both the change in input voltage and output current with protection like external shutdown. It is one of the first SC converter to provide regulation feature. (LTC1044, 2011) is a switched capacitor voltage regulator presented by linear technologies that can provide 200 μA. It can be applied as a voltage inverter at -5 V, positive and negative voltage doubler or a divider. The theory of how LTC1044 works can be explained with a basic SCC building block. Consider the circuit in Figure 2.11. When the switch is in position 1 the capacitor C_{fly} charges to V_1 which is the charge state (CS) and in position 2 the stored charge is dumped to voltage V_2 which is the transfer state (TS). The charge on C_{fly} during CS will be,
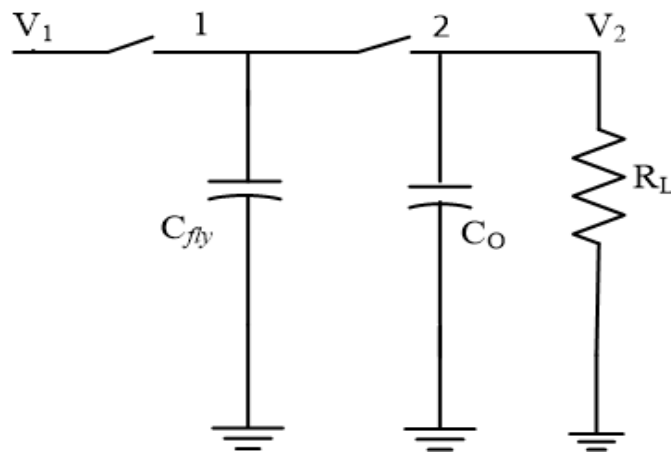
Figure 2.11: SCC Building Block

$$Q_{CS} = C_{fly}V_1 \tag{2.2}$$

During TS it will be,

$$Q_{TS} = C_{fly}V_2 \tag{2.3}$$

The total charge transferred in the CS and TS phases are,

$$\Delta Q = Q_{CS} - Q_{TS} = C_{fly}(V_1 - V_2) \tag{2.4}$$

The switch is turned on and off with a frequency of "f" cycles per second, then the current is,

$$I = f\Delta Q \tag{2.5}$$

$$I = fC_{fly}(V_1 - V_2) \tag{2.6}$$

If Equation 2.6 is expressed in terms of ohms law,

$$I = \frac{V_1 - V_2}{\frac{1}{fC_{fly}}} \tag{2.7}$$

$$I = \frac{V_1 - V_2}{R_{Equiv}} \tag{2.8}$$

Equation 2.8 shows that the equivalent resistance R_{Equiv} or generally defined as R_{out} in Figure 2.4 is dependent on the switching frequency "f" and the value of the flying or charge pump capacitor C_{fly}. Thus the challenge to model a complex SCC with more flying capacitors is to find out R_{Equiv} as shown in Figure 2.12.
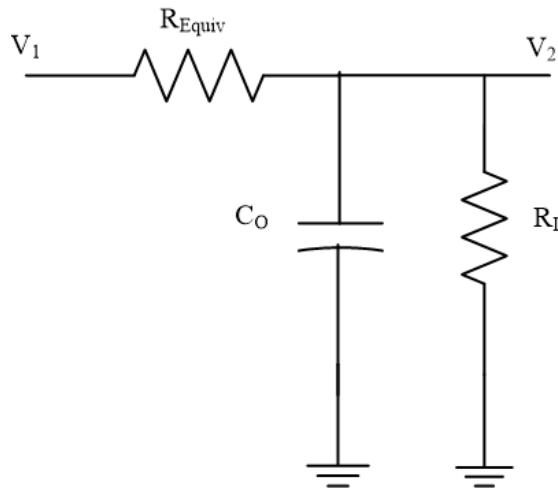
Figure 2.12: SCC Practical Equivalent Circuit Representation

IC introduced by Maxim integrated products (Max1910, 2004) are 1.5x / 2x gain high efficiency white LED Charge Pumps with a regulated voltage or current up to 120 mA from an unregulated input supply 2.7 V to 5.3 V. Input ripple is minimized by a unique regulation scheme that maintains a fixed 750 Hz switching frequency over a wide load range and is widely used for portable electronic equipments. There are 7
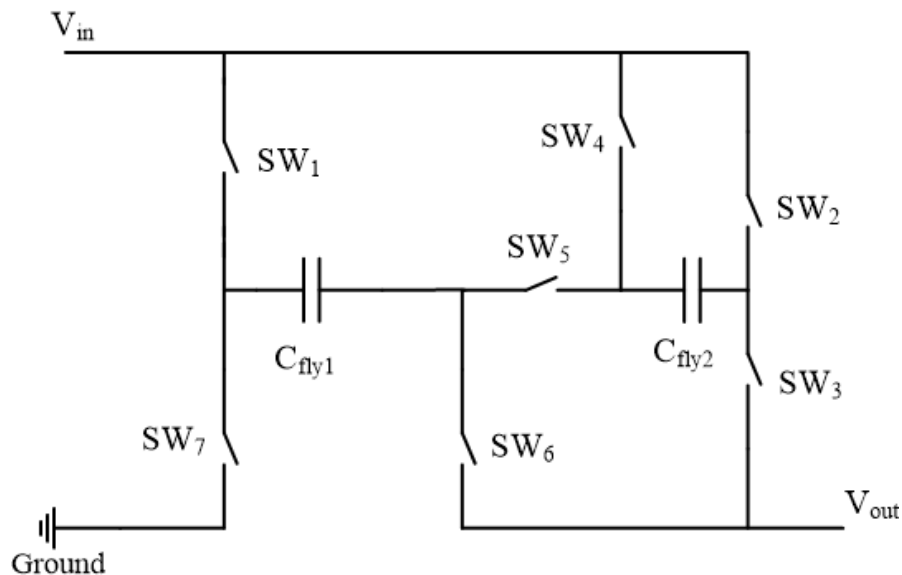
Figure 2.13: Circuit Diagram of MAX1910 with Switches and Flying Capacitors

switches and 2 flying or charge pump capacitors excluding the filter capacitors for two step up modes of 1.5x / 2x gain modes with options of only one input source voltage as shown in Figure 2.13. When the converter operates in 1.5x gain mode switches SW_2, SW_5 and SW_7 are ON while SW_1, SW_3, SW_4 and SW_6 are OFF during the charging state (CS). In transfer state (TS), SW_1, SW_3, SW_4 and SW_6 are ON while SW_2, SW_5 and SW_7 are OFF. Similarly in 2x gain mode, SW_3, SW_4, SW_5 and SW_7 are ON while, SW_1, SW_2 and SW_6 are OFF. Again in TS, SW_1, SW_2 and SW_6 are ON while SW_3, SW_4, SW_5 and SW_7 are OFF. Thus by clocking the switches in the predetermined sequence gain in boost mode of 1.5x or 2x is possible. When the input voltage falls below a threshold value, the converter switches to 2x gain mode to stabilize the output which is a doubler circuit operation. If this converter has to be used for two sources, then one more of this converter has to be connected in parallel making the switch count 14, 4 flying capacitors amounting to 18 components. The focus of this research work is to develop a novel converter that can feature the multiple gain options, operating off two independent sources, but with reduced switch count and MAX1910 is one of the reference converter in developing the proposed novel converter. The applications of

this IC is in LED back lighting, personal digital assistants (PDA), MP3 players. More industrial regulators can be found in (LMZ12001, 2010; REG71027, 2015). Inductor based industrial buck/buck-boost converters in use can be found in (LTC3115-1, 2012; FAN8301, 2008).

2.3.5 SCC Implementation using CMOS Technology

For low power applications SCC voltage regulators are being implemented using CMOS technology due to the low on board size and ease of integration. Such regulators for on board power management may consist of various power supply rails. Few such regulators are discussed in (Milliken *et al.*, 2007; Chang *et al.*, 2010; Gregoire, 2006; Le *et al.*, 2010). Another area of switched capacitor converter is in the development of filters in electronics engineering. It utilizes the advantage of variable frequency method to achieve a variable resistance. Such different types of filters are discussed in (Serra *et al.*, 2017; Wang *et al.*, 2017; Psychalinos *et al.*, 2016; Chen and Hashemi, 2016).

2.4 Summary of Switched Capacitor Converters

Advantages

- Unlike traditional inductor based converters, it does not contain any magnetic elements such as inductors, transformers etc and are also called inductorless converters.

- As the bulkiest component, inductor is discarded from the circuit, a switched capacitor DC / DC converter can be composed into thin circuit configuration.

- SCC are compact and have light weight.

- Due to absence of the magnetic elements EMI effects are less.

- Due to absence of inductors and transformers the complete integration of switched capacitor topology using integrated circuit technology is possible.

- It can support high power density compared to traditional converters for a given conversion ratio.

- Switched capacitor converters are ideal for "on die" power conversion as it requires no special processing steps and does not increase input output utilization.

- Through simple control methods, regulation over many magnitudes of output power is possible while maintaining high efficiency.

Limitations

- Only finite number of fixed conversion ratios can be obtained with a particular switched capacitor converter.

- SCC are suitable only in low power applications. Inductor based converters can carry more current hence suited in high power applications.

- They are less efficient than ordinary buck or boost converters since any arbitrary conversion ratio is obtained by varying duty cycle ratio. However multiple fractional gain configurations can be used to maximize conversion efficiency.

- They have more number of switches than magnetic based converters causing increased switching losses but the proper design and optimization techniques when suitably used can decrease the switching losses.

- Due to the equivalent series resistances of the capacitors, more ripples are produced in the output voltage.

- When capacitor is charged by a voltage source whose magnitude differs from the initial voltage of the capacitor, then fixed amount of energy is lost.

Applications

- The switched capacitor DC/DC converters are widely used in portable electronic devices due to its thin circuit configuration.

- It is used for white LED supplies in backlit color display applications.

- Since they can support increased power density for a fixed conversion ratio compared to traditional converters, they are best suited for on-die power conversion.

- SC converters are ideal for integrated implementations, as common integrated inductors are not suitable for power electronic applications.

- Switched capacitor converter is used as high voltage hybrid converter for an autonomous micro air vehicle.

- It is used as power management IC for wireless sensor nodes.

- They can be used to power numerous power domains in the microprocessor and multi-core microprocessor application with different sleep state.

CHAPTER 3

SIMULATION STUDIES ON A FEW BASIC SWITCHED CAPACITOR CONVERTERS (SCC)

In this chapter, few basic switched capacitor converters belonging to the series parallel topology discussed in Chapter 2 and (Yuanmao and Cheng, 2012), are simulated to realize its potential. The circuit is rigged in a power electronics software PSIM for simulation. Mathematical modelling of the converter is not attempted in the basic topologies since the interest was in understanding the working principle, verification and assess the potential for realization. Altogether five converter topologies have been demonstrated in this chapter which are doubler, half, inverted, adder and subtractor. The first three converters are working with single source providing a SCC doubler topology, half topology and inverting topology. The next two topologies cover addition and subtraction of voltage levels when operated off two sources. The basis for the need of developing a much more simple converter based on SCC principle is warranted as an outcome of the simulation studies in this chapter.

3.1 Simulation Studies on a SCC Voltage Doubler (Boost) Topology

There are many applications that require twice the input voltage at the output and traditionally this has been accomplished with the help of inductor based boost converters. However, better efficient compact converters can be realized using SC converter for the same application in low power requirements. The advantages of inductor based boost converter is the ease of realizing any arbitrary conversion ratio between one and two. This happens to be a disadvantage of SC converter presented here but if the application demands only one mode like the boost doubler voltage, SC converter is a potential choice. The circuit diagram of a voltage doubler is shown in Figure 3.1. There are altogether 5 components namely switches SW_1, SW_2, diodes D_1, D_2, flying capacitor

C_1 and C_2 the filter capacitor. The load is selected here as 300 Ω. When SW$_1$ is turned on during the charging phase (CS), the flying capacitor C_1 charges to the input voltage of source V_{s1}, which is to be 24 V. In the next phase called transfer phase (TS) switch SW$_2$ is turned on and SW$_1$ is turned off. Now the already charged flying capacitor voltage in series with the source, supplies the load through D_2 delivering 48 V across the load, if the switches and capacitors are ideal. The input and output voltage V_{in} and
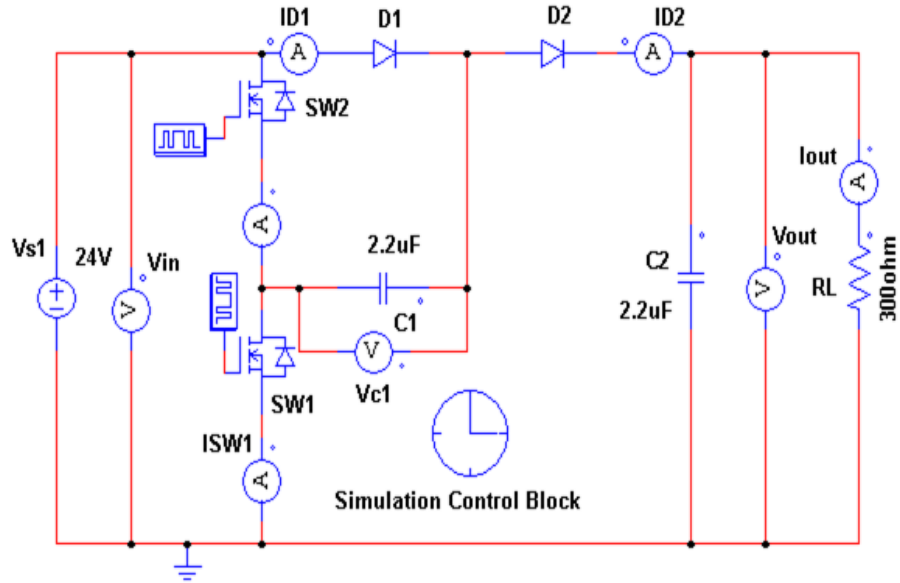
Figure 3.1: A SCC Voltage Doubler

V_{out} respectively are shown in Figure 3.2. The input voltage is selected as 24 V and switching frequency is taken as 100 kHz. The load resistance is taken as 300 Ω since SCC generally is used to power low power electronic gadgets in the range of mA to 1 A. The output load voltage V_{out} is measured as 47 Volts. Thus this topology can generate a voltage equal to twice the input voltage acting as a boost converter. The flying capacitor output voltage V_{c1} waveform in shown in Figure 3.3. The flying capacitor charges nearly to the source voltage of 24 V and later the source in series with V_{c1} delivers 47 V across the load. The flying capacitor forms the energy storing and transferring element in SCC. In this simulation, the flying capacitor and filter capacitor values both are arbitrarily taken as 2.2 μF. During CS, the filter capacitor need to deliver the load. A detailed discussion on the effect of output voltage in selection of flying capacitor and filter capacitor values is discussed in Chapter 5. The switch current and diode current pattern can be of interest to understand the stress on them. The switch and diode current waveform through SW$_1$ and D_1 are shown in Figure 3.4 and the current pattern through SW$_2$ and D_2 are shown in Figure 3.5. It can be seen that the initial stress on
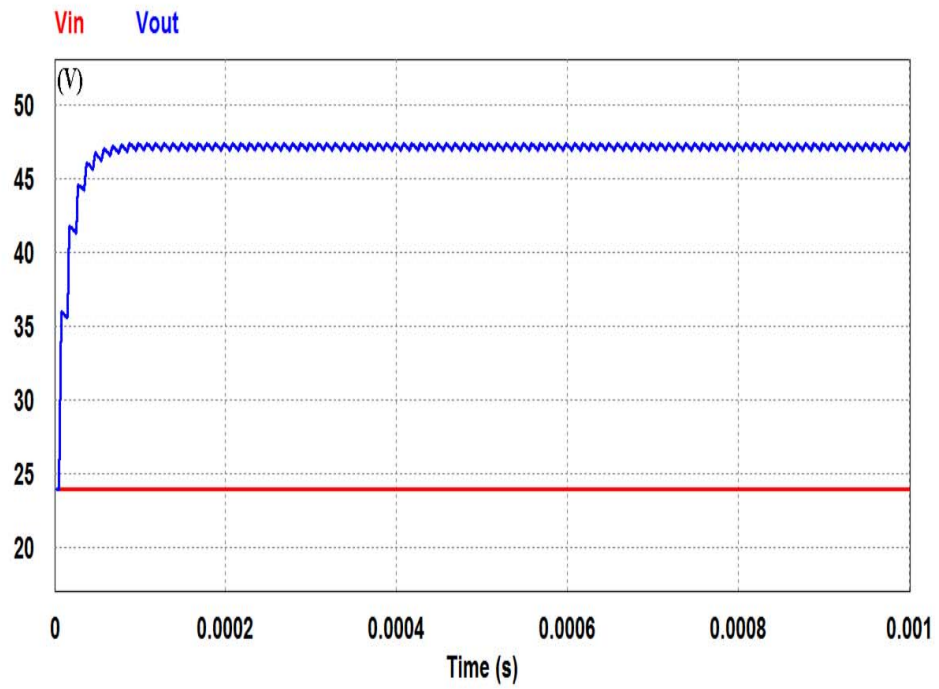
Figure 3.2: Simulated Voltage Waveforms Measured Across Source and Load for Doubler Circuit
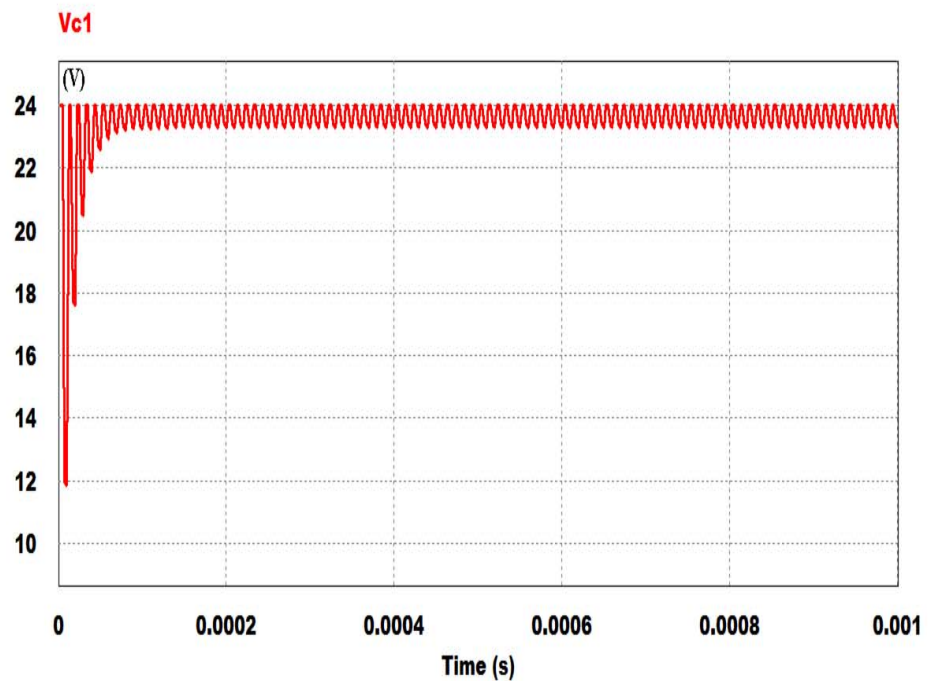
Figure 3.3: Simulated Voltage Waveforms Measured Across Flying Capacitor for Doubler Circuit

switch 2 and diode 2 is less compared to switch 1 and diode 1 respectively, though all the switches are hard switched which can create electro magnetic interference and can

reduce converter life. Since the load current delivered is small and around 16 mA hard switched SCC can also be used. Higher switch stress can be reduced by introducing resonant circuit by adding an inductor. When the current dealt is very high this may be a good option but defeats the very basic purpose of SCC when an inductor is added. The circuits simulated in the initial stage of research reported in this chapter, has been to basically understand the concept and hence load current was fixed at very low value. Higher load current in the range of 250 mA can be realized by reducing the load. In Chapter 6, a hardware implementation of a SCC is realized by powering white LEDs.
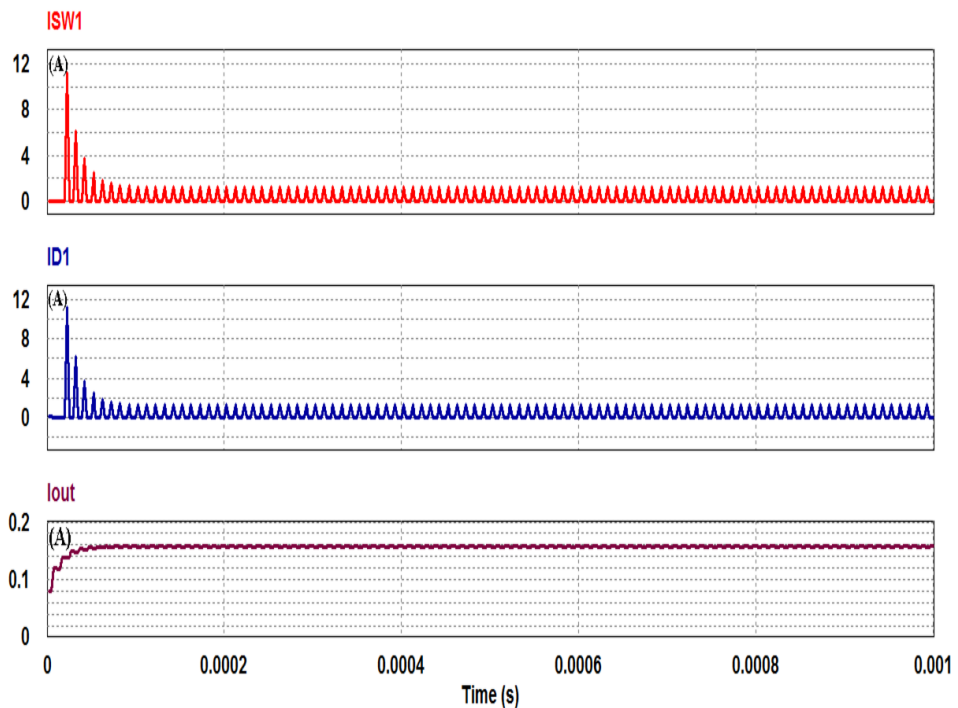
Figure 3.4: Simulated Switch 1, Diode 1 and Load Current Waveforms for Doubler Circuit

3.2 Simulation Studies on a SCC Voltage Half (Buck) Topology

There are many applications that require buck or reduced voltage. An inductor based buck converter is the choice of power electronic engineers and many forms of such converter in isolated and non isolated modes are available. SC converter due to its low weight and size can replace a buck inductor based converter. The circuit diagram of a

29
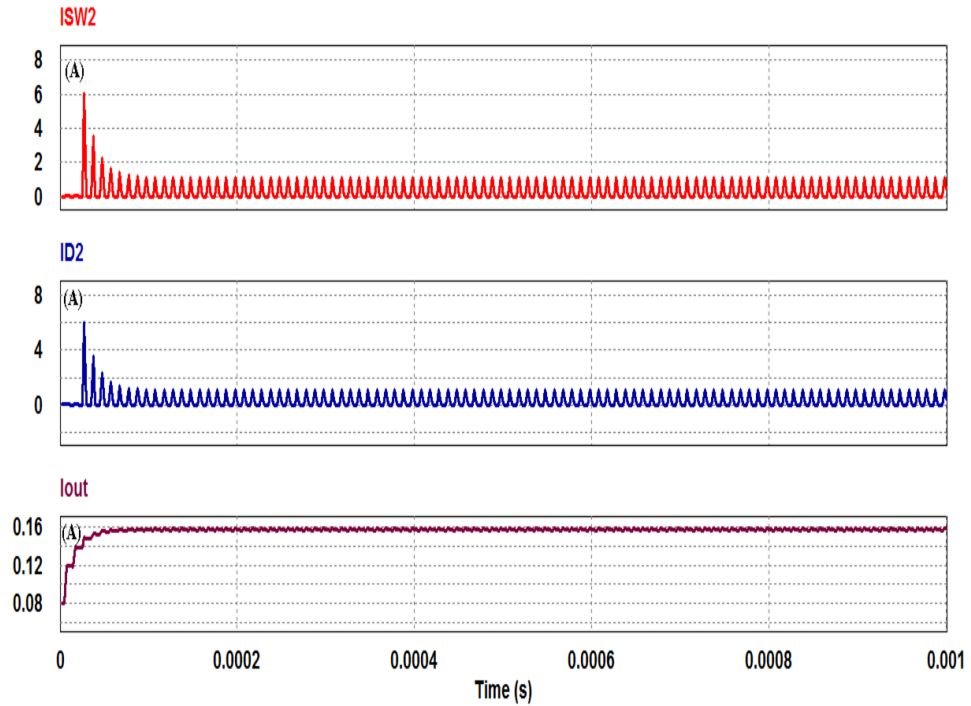
Figure 3.5: Simulated Switch 2, Diode 2 and Load Current Waveforms for Doubler Circuit

voltage half circuit is shown in Figure 3.6. There are altogether 5 components namely switches SW_1, SW_2, diodes D_1, D_2 and flying capacitor C_1 as in the doubler above. C_2 forms the filter capacitor. The load is selected here as 75 Ω to drive minimum current as the voltage expected is only 12 V for an input voltage of 24 V. When SW_1 is turned on during the charging phase (CS), the flying capacitor C_1 charges to half of the input voltage of source V_{s1} which is 12 V, in series with diodes D_1 through load. In the next phase called transfer phase (TS) switch SW_2 is turned on and SW_1 is turned off. Now the already charged flying capacitor voltage connects in parallel to the load through D_2, which is now forward biased delivering 12 V across the load, if the switches and capacitors are ideal. The input and output voltage V_{in} and V_{out} respectively are shown in Figure 3.7. The input voltage is selected as 24 V and switching frequency is taken as 100 kHz. The load resistance is taken as 75 Ω. The output load voltage V_{out} is measured as 11.8 Volts which is almost half of the input voltage. Thus this topology can generate a voltage equal to half the input voltage acting as a buck converter. The flying capacitor output voltage V_{c1} waveform is shown in Figure 3.8. The flying capacitor charges nearly to half of the source voltage of 24 V through SW_1 which is 11.8 V and later V_{c1} delivers 11.8 V across the load. The diode D_1 automatically will be reverse biased when SW_2
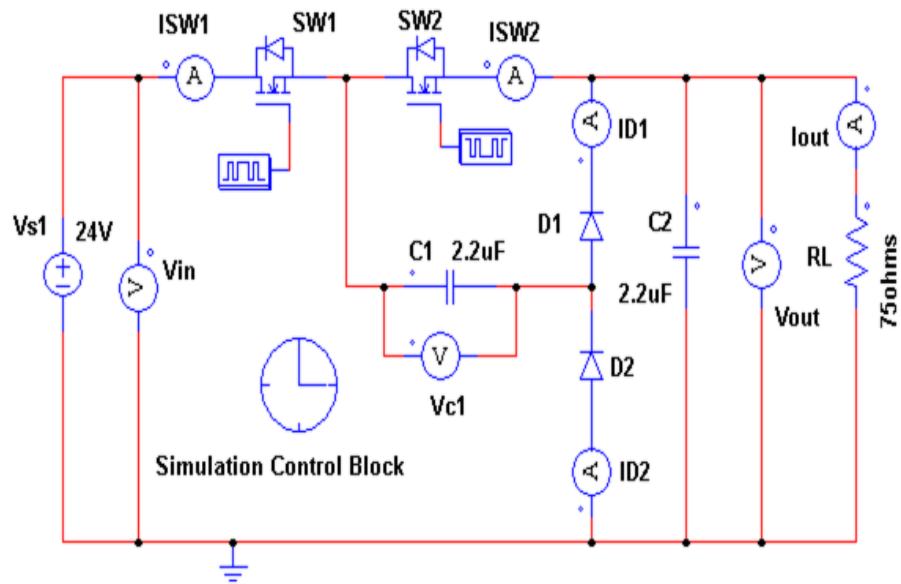
Figure 3.6: A SCC Voltage Half Circuit
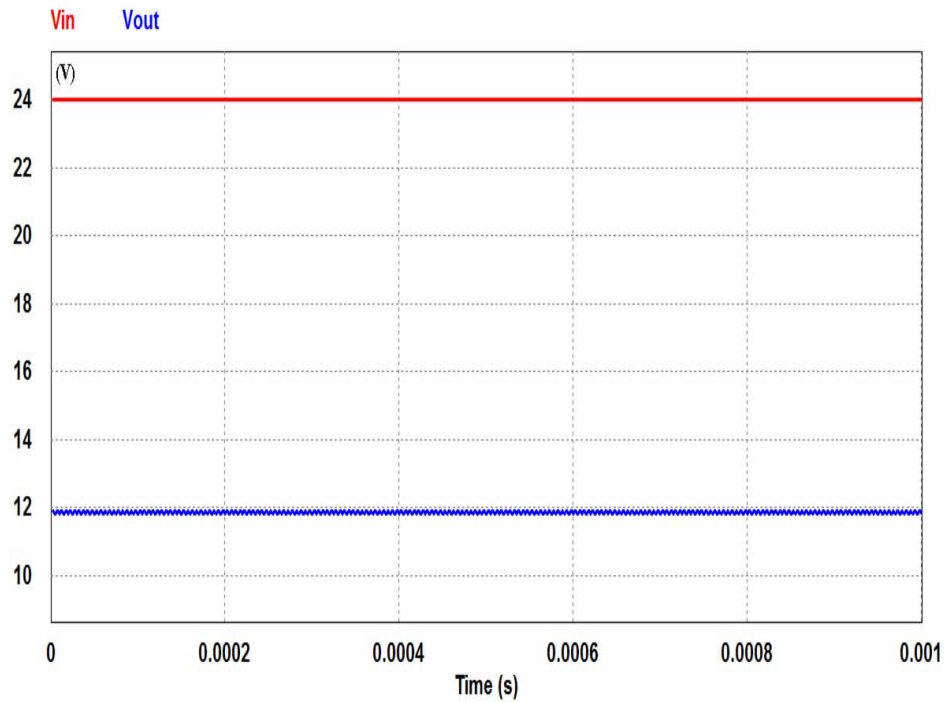
Figure 3.7: Simulated Voltage Waveforms Measured Across Source and Load for Half Circuit

is turned on in TS. At the same time, D_2 turns on and switch SW_2 and diode D_2 now connects the flying capacitor V_{c1} in parallel to the load and the voltage to which V_{c1} has been charged during CS is 11.8 V. The flying capacitor and filter capacitor values both are taken as 2.2 μF and a high value for filter capacitor is preferred if reduced ripple is a mandate. As a next step, the switch current and diode current pattern is studied for the

31
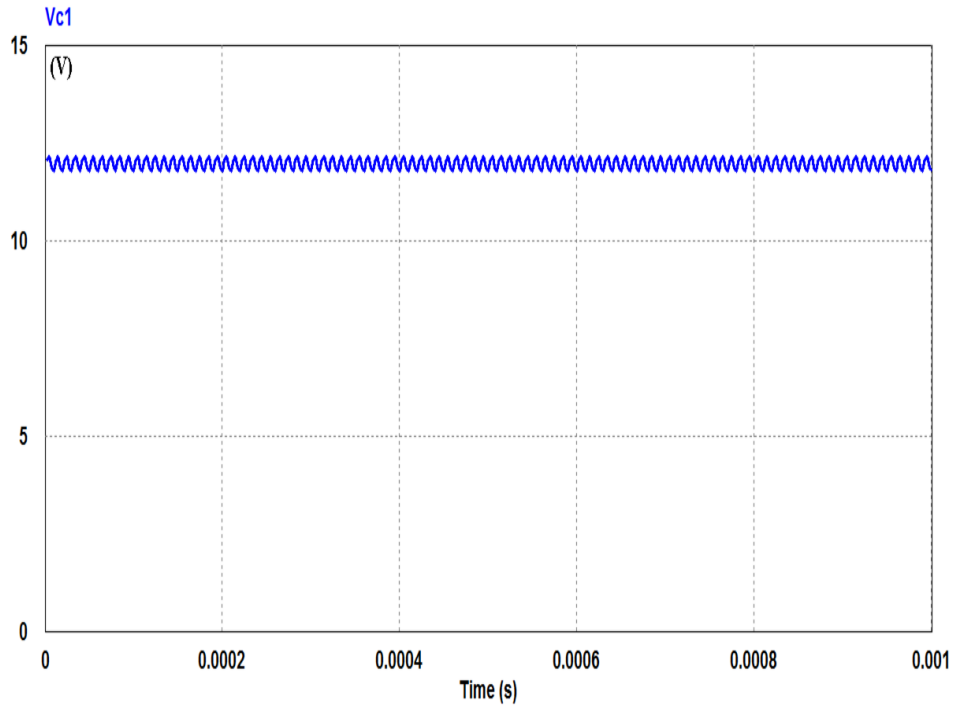
Figure 3.8: Simulated Voltage Waveforms Measured Across Flying Capacitor for Half Circuit

half circuit. The switch and diode current waveform through SW_1 and D_1 are shown in Figure 3.9 and the current pattern through SW_2 and D_2 are shown in Figure 3.10. The load current in both doubler and half circuit is maintained at 16 mA by adjusting the load resistance as 300 Ω and 75 Ω since the output voltages are 47 V and 11.8 V respectively. A close observation of initial spike on the switches, diodes currents in doubler circuit of Figure 3.4 and Figure 3.5 compared to the currents on the switches of half circuit shows that in half circuit the spike is much less and both the switches, diodes currents in CS and TS follows same pattern.

3.3   Simulation Studies on a SCC Inverted Topology

There has been demand in application that require a negative polarity voltage at the output with respect to the positive reference. SC converter can provide a solution for such requirements. The circuit diagram to generate an inverting voltage at the output is shown in Figure 3.11. All the topologies that are being discussed in this chapter uses 5 components namely switches SW_1, SW_2, diodes D_1, D_2 and flying capacitor C_1. Similarly C_2 forms the filter capacitor. The load is selected here as 100 Ω to drive a

32
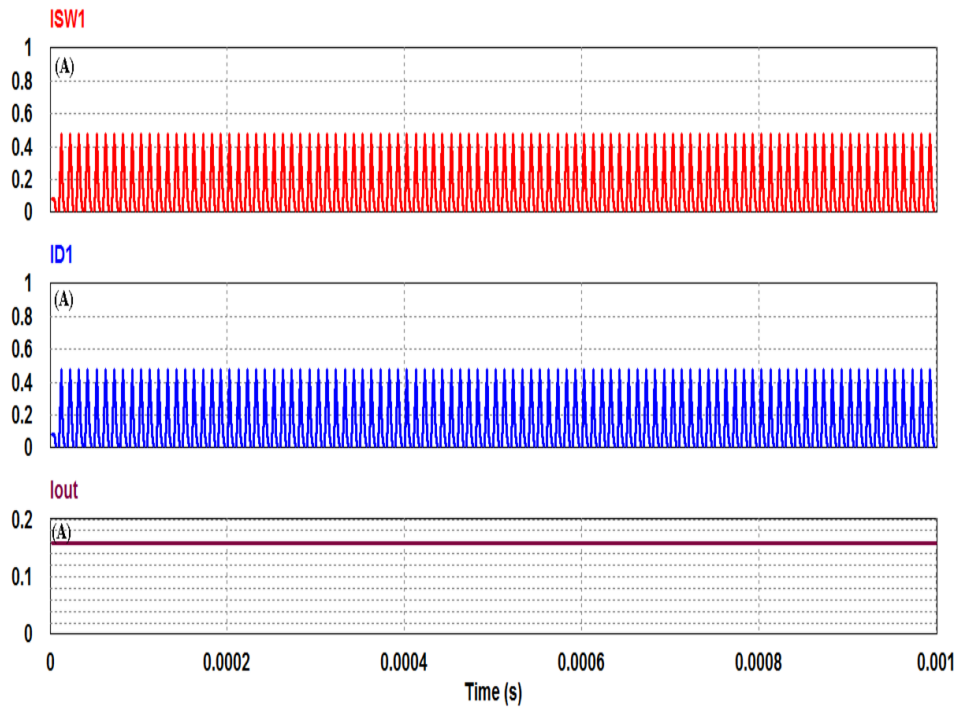
Figure 3.9: Simulated Switch 1, Diode 1 and Load Current Waveforms for Half Circuit
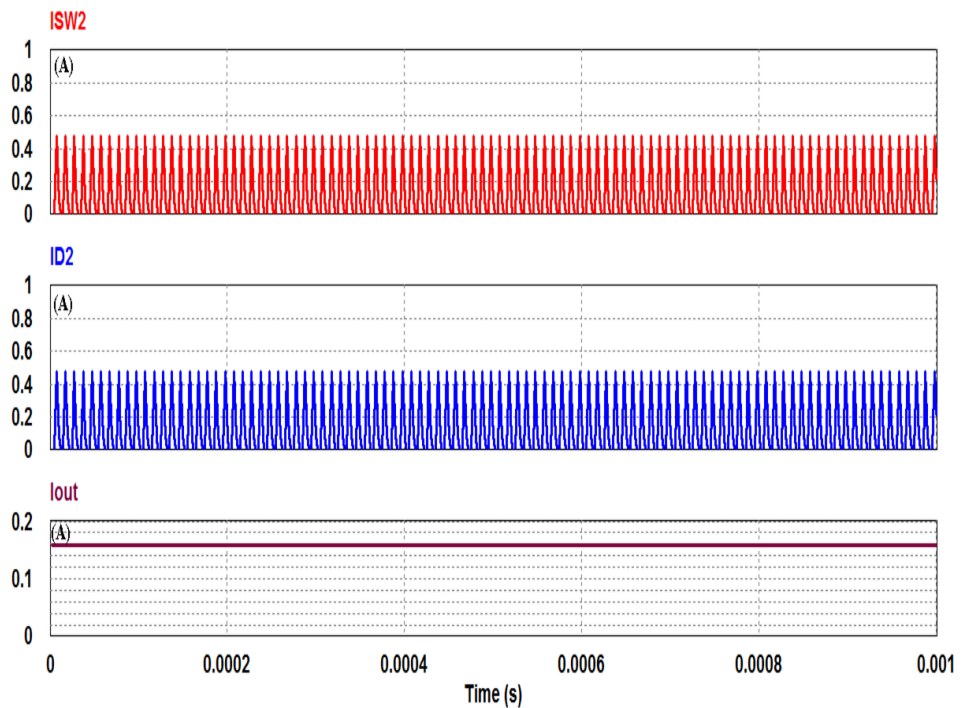
Figure 3.10: Simulated Switch 2, Diode 2 and Load Current Waveforms for Half Circuit

negative current and the voltage expected is -24 V for an input voltage of 24 V. When SW$_1$ is turned on during the charging phase (CS), the flying capacitor C_1 charges to the input voltage of source V_{s1} which is 24 V, in series with diodes D_1 to the ground. The

left plate of the capacitor is charged with a positive polarity. In the next phase called transfer phase (TS), switch SW_2 is turned on and SW_1 is turned off. Now the already charged flying capacitor voltage connects in parallel to the load through D_2, which is now forward biased delivering -24 V across the load, if the switches and capacitors are ideal. The input and output voltage V_{in} and V_{out} respectively are shown in Figure
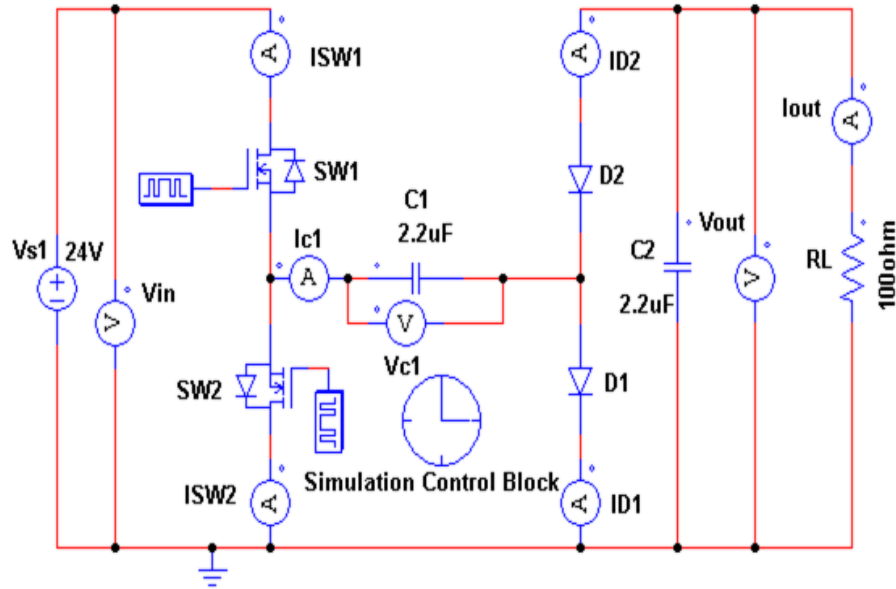
Figure 3.11: A SCC Voltage Inverting Circuit

3.12. The input voltage is selected as 24 V and switching frequency is taken as 100 kHz. The load resistance is taken as 100 Ω. The output load voltage V_{out} is measured as -23 Volts which is negative of the input voltage. The simulation control block can be used to control the run time. Here the simulation is run for 2 ms. Thus this topology can generate a voltage which is almost negative with respect to input voltage acting as a inverting converter. The flying capacitor output voltage V_{c1} and the output voltage waveform V_{out} is shown in Figure 3.13. The flying capacitor charges nearly to the source voltage of 24 V through SW_1 which is around 23.4 V and later V_{c1} delivers around -22.6 V across the load. The diode D_1 automatically will be reverse biased when V_{c1} is fully charged because the right plate of the flying capacitor is negative. Now when SW_2 is turned on in TS, at the same time D_2 turns on and switch SW_2 and diode D_2 now connects the flying capacitor V_{c1} in parallel to the load and the voltage to which V_{c1} has been charged during CS is 23 V. The flying capacitor and filter capacitor values both are taken as 2.2 μF and a high value for filter capacitor can be selected if reduced ripple is desired. This will also increase the average output voltage. The switch current and diode current pattern is studied next for the inverting circuit. The switch and diode

34
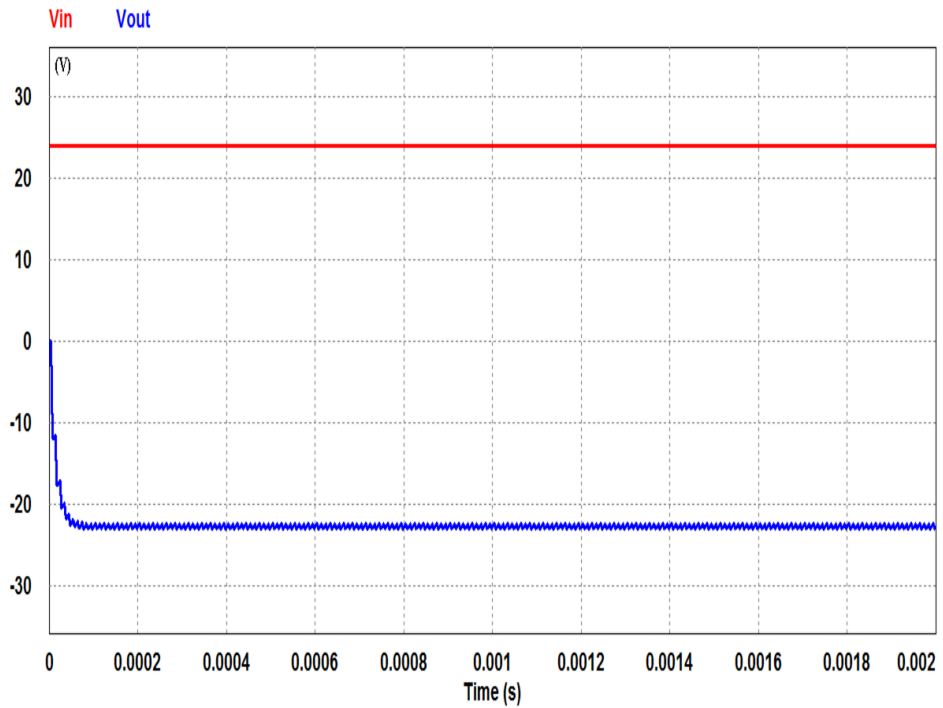
Figure 3.12: Simulated Voltage Waveforms Measured Across Source and Load for Inverting Circuit
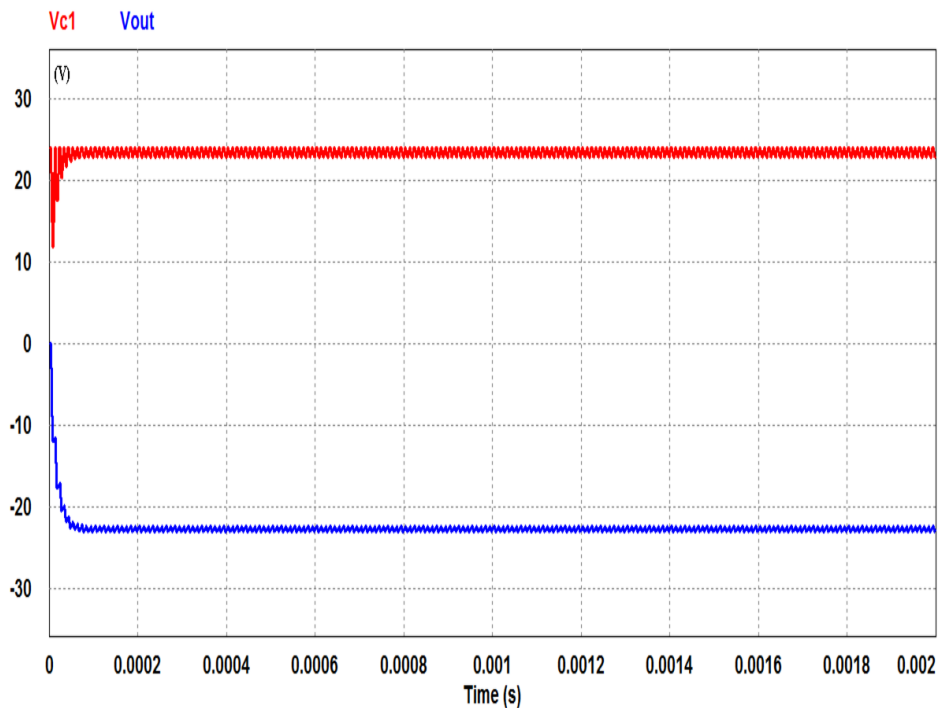
Figure 3.13: Simulated Voltage Waveforms Measured Across Flying Capacitor for Inverting Circuit

current waveform through SW_1, D_1 and flying capacitor current waveform I_{c1} are shown in Figure 3.14. The current pattern through SW_2 and D_2 are shown in Figure 3.15. The

35

load current is measured as -225 mA when the load resistance is selected as 100 Ω. The capacitor current waveform is of importance since the frequency of switching decides the amount of time that the flying capacitor gets to completely charge or partially charge to the voltage applied across it. The theory that average capacitor current should be zero in one switching cycle is also verified as can be seen from the waveform in Figure 3.14. A detailed study on the capacitor current waveforms is discussed in Chapter 5 in the proposed new flexible and efficient converter with more conversion ratios that can be realized from one single circuit.
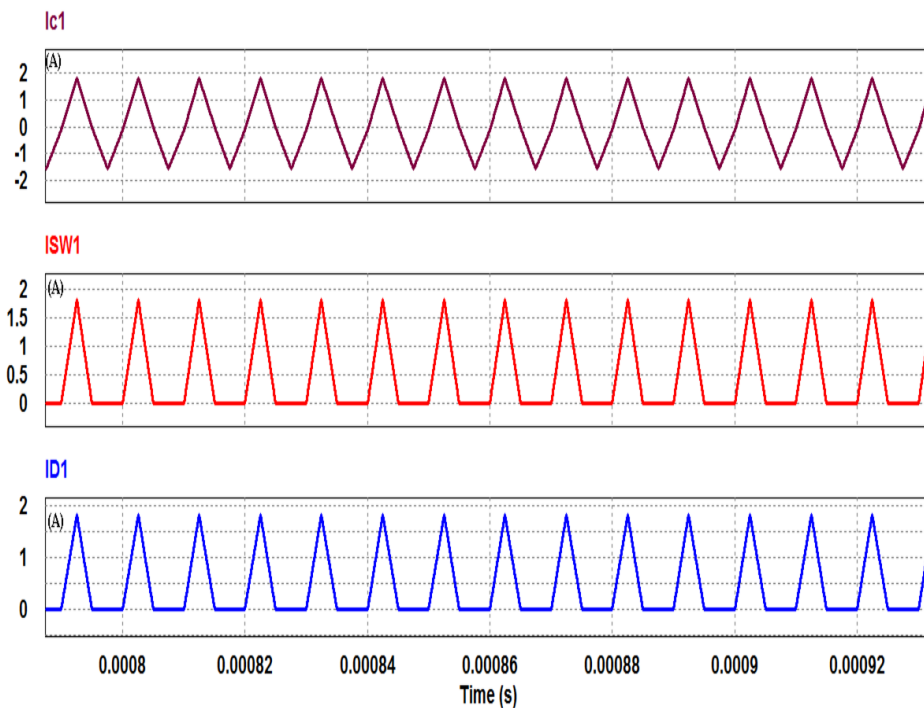
Figure 3.14: Simulated Flying Capacitor Current, Switch 1 and Diode 1 Waveforms for Inverting Circuit

3.4   Simulation Studies on a SCC Dual Source Adder Topology

When two or more sources are to be utilized, summation circuit presented in Figure 3.16 can be useful. Here the flying capacitor of SCC circuit is used to charge from one source and transfer in series with the second source to the load. The summation or adder topology also uses switches SW_1, SW_2, diodes D_1, D_2, flying capacitor C_1 and
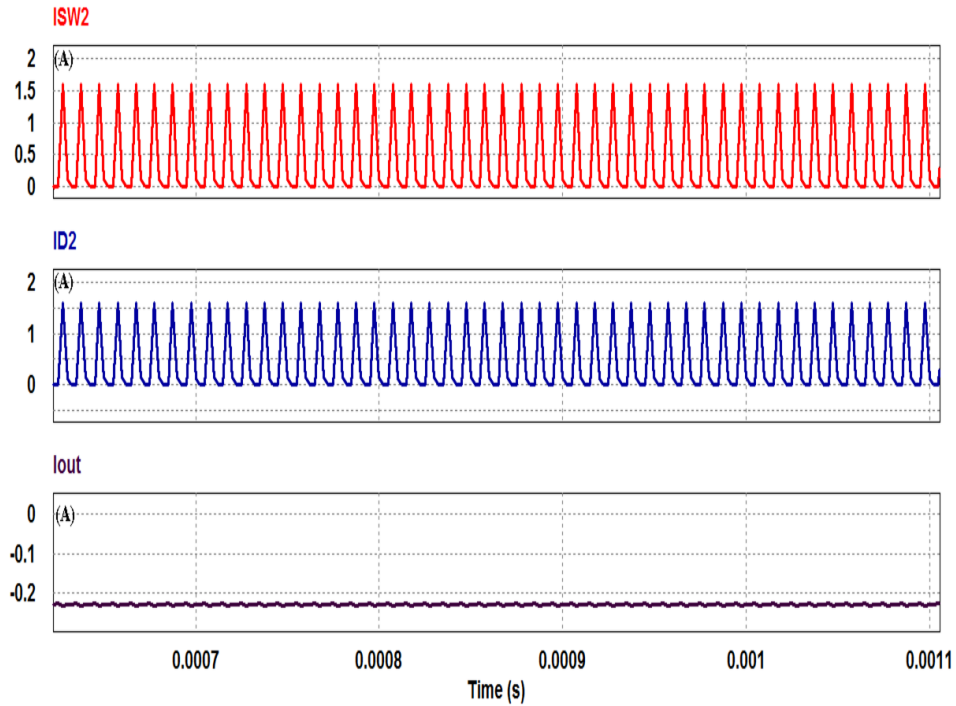
Figure 3.15: Simulated Switch 2, Diode 2 and Load Current Waveforms for Inverting
Circuit

C_2 forms the filter capacitor. The load is selected here as 300 Ω to drive a reasonable current and the voltage expected is 36 V for an input voltage of V_{s1} 24 V and V_{s2} 12 V being the two sources respectively. When SW_1 is turned on during the charging phase (CS), the flying capacitor C_1charges to the input voltage of source V_{s1} which is 24 V, in series with diodes D_1 to the ground. The left plate of the capacitor is charged with a positive polarity. In the next phase called transfer phase (TS), switch SW_2 is turned on and SW_1 is turned off. Now the already charged flying capacitor voltage connects in series with the second source V_{s2} to the load through D_2, which is now forward biased delivering 36 V across the load, if the switches and capacitors are ideal. The two input voltages and the simulated output voltage V_{in1}, V_{in2} and V_{out} respectively are shown in Figure 3.17. The input voltages are selected as 24 V and 12 V, switching frequency is taken as 100 kHz. The load resistance is taken as 300 Ω. The output load voltage V_{out} is measured as 36 Volts which is summation of the two input voltages. The simulation control block can be used to control the run time and is run for 2 ms. Thus this topology can generate a voltage which is summation of two input voltages acting as a adder SC converter. The flying capacitor output voltage V_{c1} and the two input voltage waveforms are shown in Figure 3.18. The flying capacitor charges nearly to the source voltage of

37
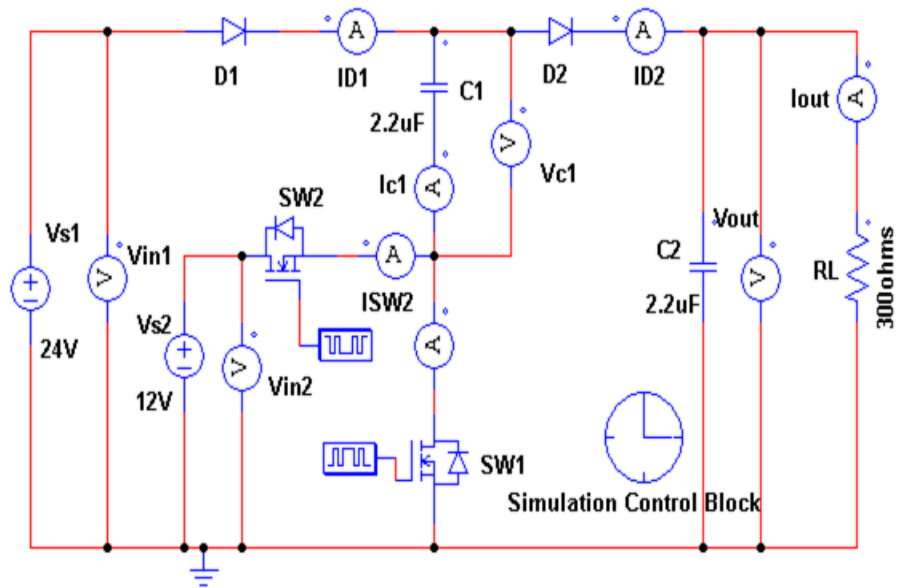
Figure 3.16: A SCC Voltage Adder Circuit
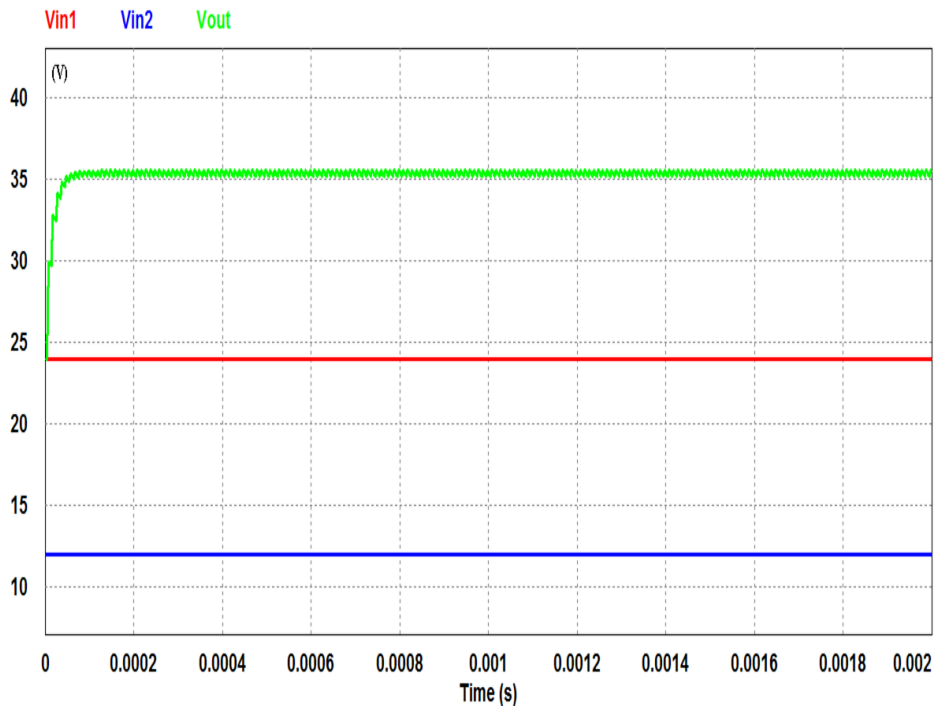
Figure 3.17: Simulated Voltage Waveforms Measured Across Two Sources and Load for Adder Circuit

24 V through SW_1 and later V_{c1} delivers around 22.8 V in series with the second source voltage of 12 V to the load. The diode D_1 automatically will be reverse biased when V_{c1} is fully charged. Now when SW_2 is turned on in TS, at the same time D_2 turns on and switch SW_2 and diode D_2 now connects the flying capacitor V_{c1} in series to the load connecting the second source and the voltage to which V_{c1} has been charged during

CS is 24 V. Thus 36 V is obtained at the output. A large ripple is seen in the flying capacitor voltage waveforms. This can be reduced by selecting a slightly higher value above 2.2 μF as the filter capacitor value. Similarly a high value for filter capacitor can be selected if ripple is high in output voltage. The switch current and diode current
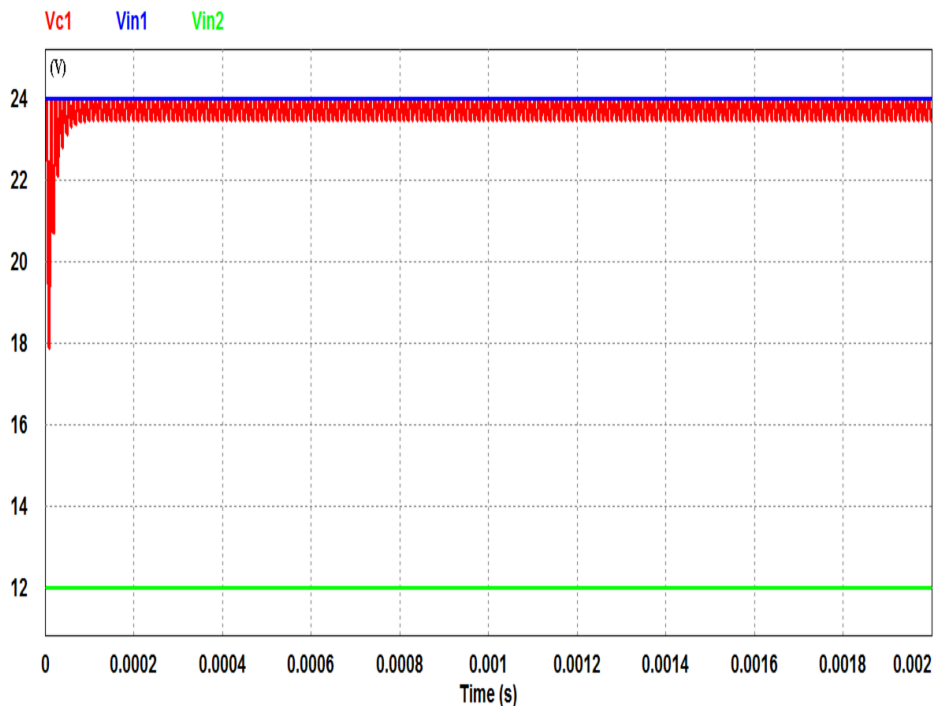
Figure 3.18: Simulated Voltage Waveforms Measured Across Flying Capacitor for Adder Circuit

pattern is studied next for the adder circuit. The switch and diode current waveform through SW_1, D_1 and flying capacitor current waveform I_{c1} are shown in Figure 3.19. The current pattern through SW_2 and D_2 are shown in Figure 3.20. The load current is measured as 120 mA when the load resistance is selected as 300 Ω. The current spikes in the switches and diodes are seen to be approximately 800 mA. It can be seen, by verifying the capacitor current waveform in Figure 3.19, that the Ampere second balance is satisfied since the average capacitor current is zero. The converter simulated and realized in this chapter fall under the category of hard switched SCC. One possible solution to reduce the switch stress is to use a small inductor and make the converter to be a resonant converter. However, it may reduce the advantages offered by inductor less topology.
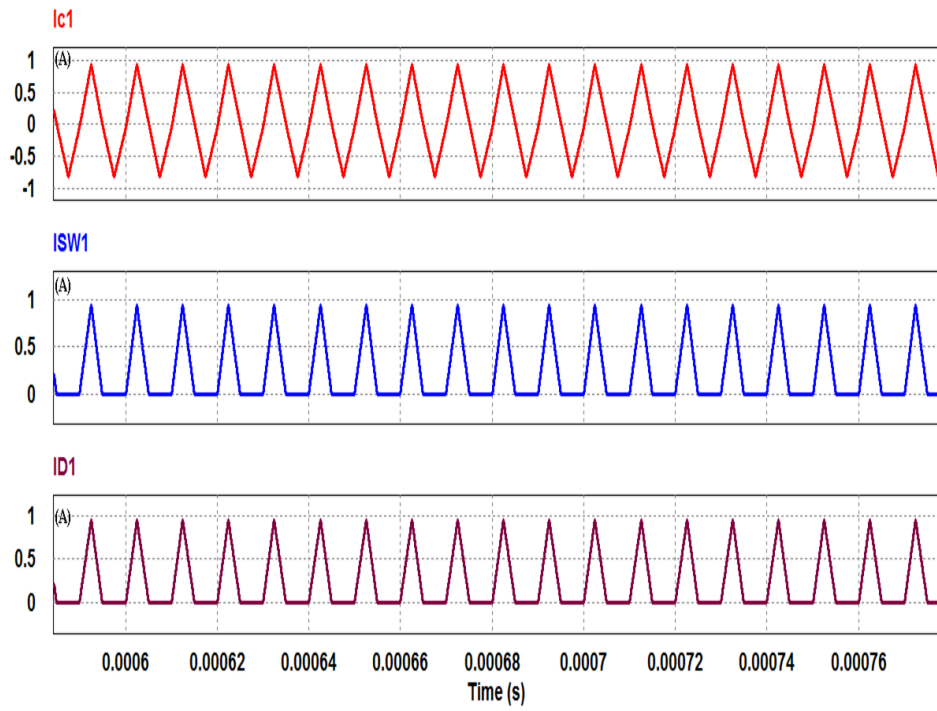
Figure 3.19: Simulated Flying Capacitor Current, Switch 1 and Diode 1 Waveforms for Adder Circuit
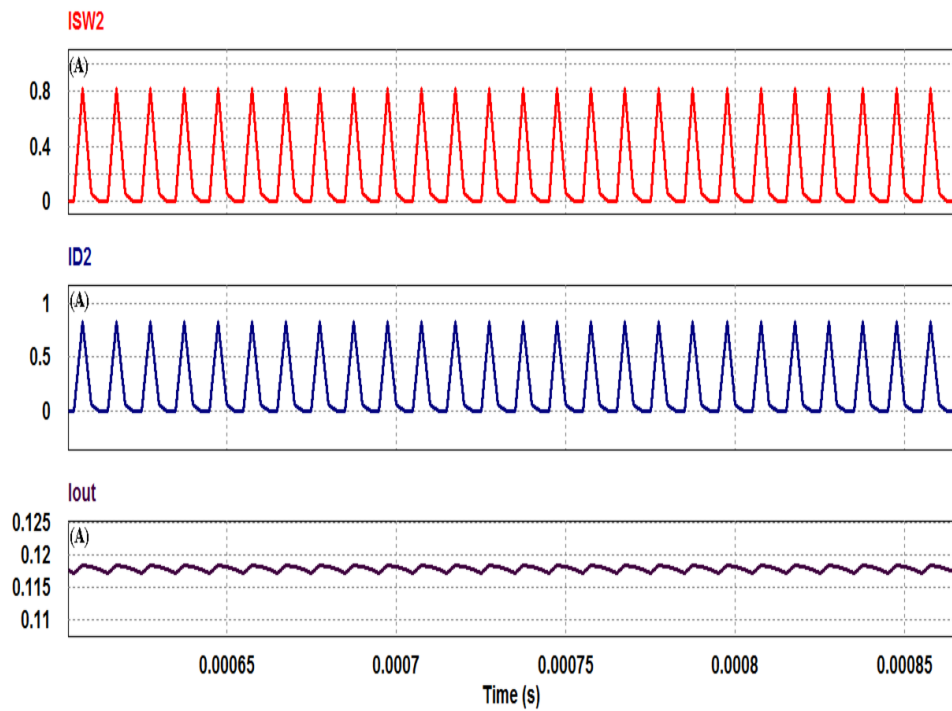
Figure 3.20: Simulated Switch 2, Diode 2 and Load Current Waveforms for Adder Circuit

3.5 Simulation Studies on a SCC Dual Source Subtraction Topology

Another configuration that can be realized using the switches SW_1, SW_2, diodes D_1, D_2, flying capacitor C_1 and C_2 the filter capacitor is the subtraction circuit presented in Figure 3.21. Here the flying capacitor of SCC circuit is used to charge to the difference between the two sources. The load is selected here as 50 Ω to drive a low current and the voltage expected is 5 V for an input voltage of V_{s1} 15 V and V_{s2} 10 V, being the two sources respectively. Here the flying capacitor C_1 is connected between the two sources through SW_1 and D_1. When SW_1 is turned on during the charging phase (CS), the flying capacitor C_1 charges to the difference of the input voltage of source V_{s1} and V_{s2} which is 5 V, in series with diode D_1. In the transfer phase (TS), switch SW_2 is turned on and SW_1 is turned off. Now the already charged flying capacitor voltage connects in parallel to the load through D_2, which is now forward biased delivering 5 V across the load, which is the difference between the two sources. The two input voltages V_{in1}, V_{in2}
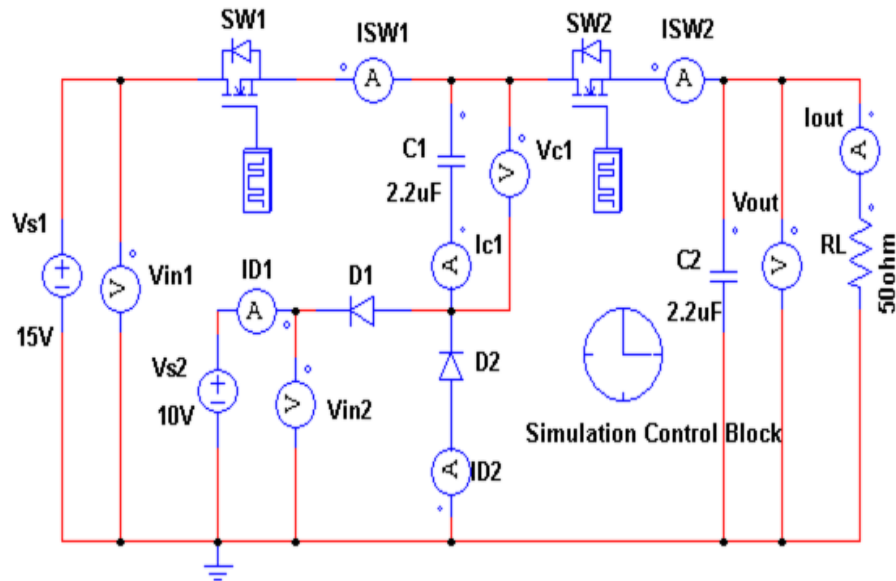
Figure 3.21: A SCC Voltage Subtraction Circuit

and the simulated output voltage V_{out} respectively are shown in Figure 3.22. The input voltages are selected as 15 V and 10 V with a switching frequency of 100 kHz. The load resistance is taken as 50 Ω since the expected output voltage is only 5 V. The output load voltage V_{out} is measured as 4.5 V which is difference of the two input voltages. The simulation run time is 2 ms. Thus this topology can generate a voltage which is

difference of two input voltages acting as a subtraction SC converter. The drop of 0.5 V is due to the drop across the MOSFET switches due to the $R_{DS}(ON)$ and also due to the forward voltage drop in the two diodes D_1 and D_2 used in the circuit.A higher output voltage nearly 5 V can be achieved if the flying capacitor value or the switching frequency is increased. The flying capacitor output voltage V_{c1} and the output voltage
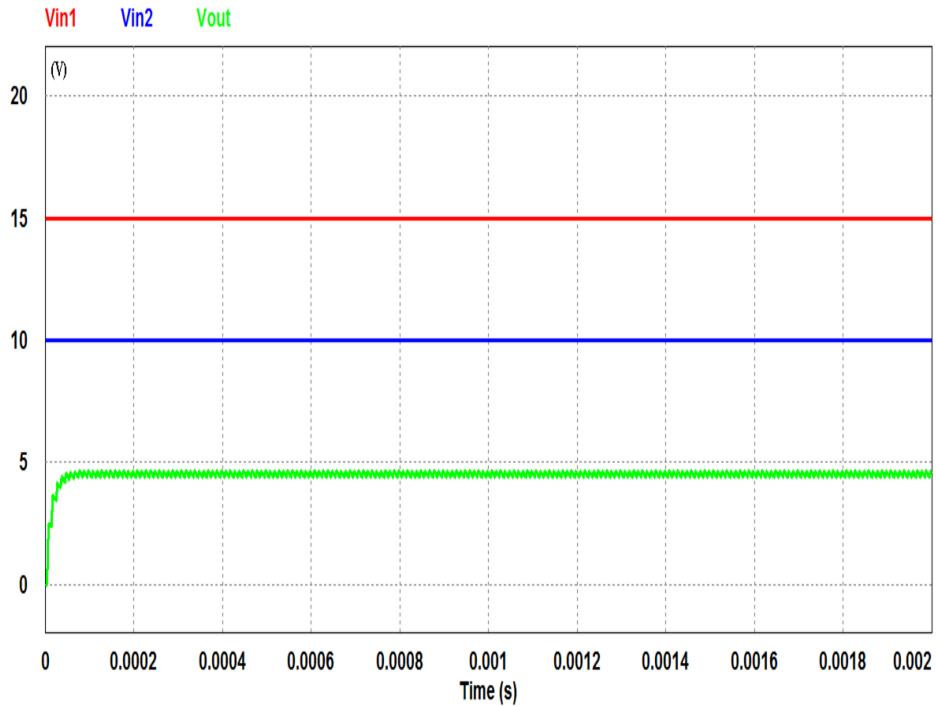
Figure 3.22: Simulated Voltage Waveforms Measured Across Two Sources and Load for Subtraction Circuit

waveform V_{out} is shown in Figure 3.23. The flying capacitor charges nearly to the difference of source voltages of around 4.8 V through SW_1 and D_1. Later V_{c1} delivers around 4.5 V in parallel to the load. The diode D_1 automatically will be reverse biased when V_{c1} is fully charged. Now when SW_2 is turned on in TS, at the same time D_2 turns on and switch SW_2 and diode D_2 now connects the flying capacitor V_{c1} in parallel to the load delivering 4.5 V the difference between the two input voltages of 15 V and 10 V. A large ripple is seen in the flying capacitor voltage and output voltage waveforms as seen in Figure 3.23. This can be reduced by selecting a slightly higher value above 2.2 μF as the filter capacitor value. Similarly a high value for filter capacitor can be selected if ripple is high in output voltage. In all the topologies presented here, the filter capacitor and flying capacitor values are taken as the same. The switch, diode current waveform through SW_1, D_1 and flying capacitor current waveform I_{c1} are shown in Figure 3.24.

42
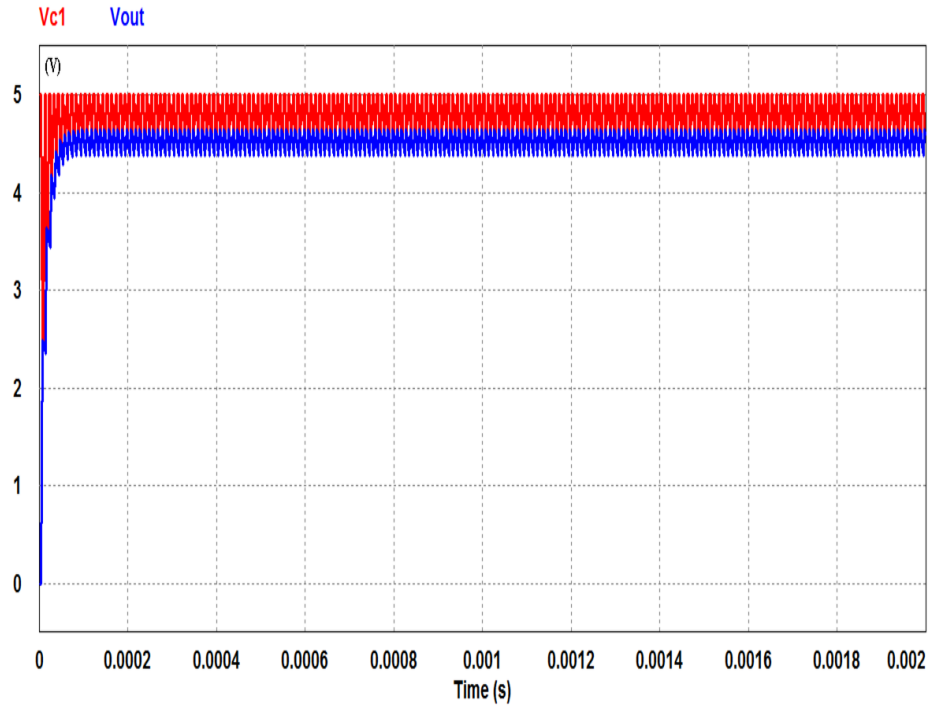
Figure 3.23: Simulated Voltage Waveforms Measured Across Flying Capacitor for Subtraction Circuit

The current pattern through SW_2 and D_2 are shown in Figure 3.25. The load current is measured as 90 mA when the load resistance is selected as 50 Ω. The current spikes in the switches and diodes are seen to be less than 1 A in steady state. It can be seen, by verifying the capacitor current waveform in Figure 3.24, that the Ampere second balance is satisfied since the average capacitor current is zero in steady state.

3.6 Conclusion

This chapter presented few basic SCC topologies that can operate as a doubler, half, inverting, adder and subtraction circuits. All the topologies have been simulated and the output voltage and current waveforms, flying capacitor voltage and current waveforms, switch and diode current waveforms have been verified. The advantage of these topologies are it uses only 5 components to achieve any of the conversions. However the major disadvantage is that the circuit cannot be used as a variable structure topology by which all the conversion ratio can be realized in one single topology. The converter discussed in Chapters 5 and 6 are developed to be more flexible and user friendly with the ability to generate more VCRs. Another aspect is the regulation of output voltage.
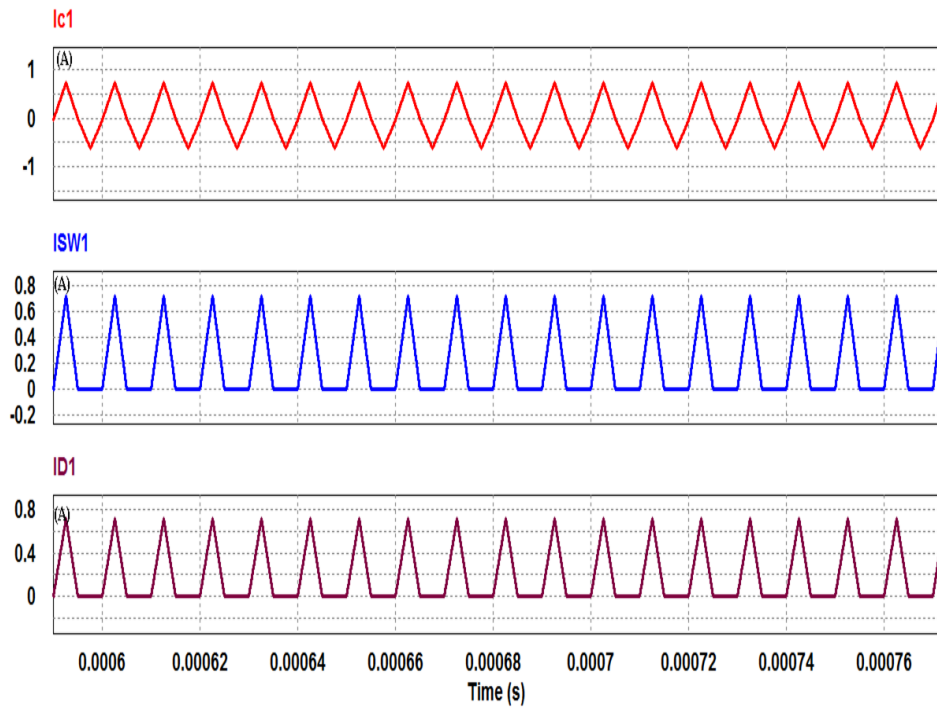
Figure 3.24: Simulated Flying Capacitor Current, Switch 1 and Diode 1 Waveforms for Subtraction Circuit
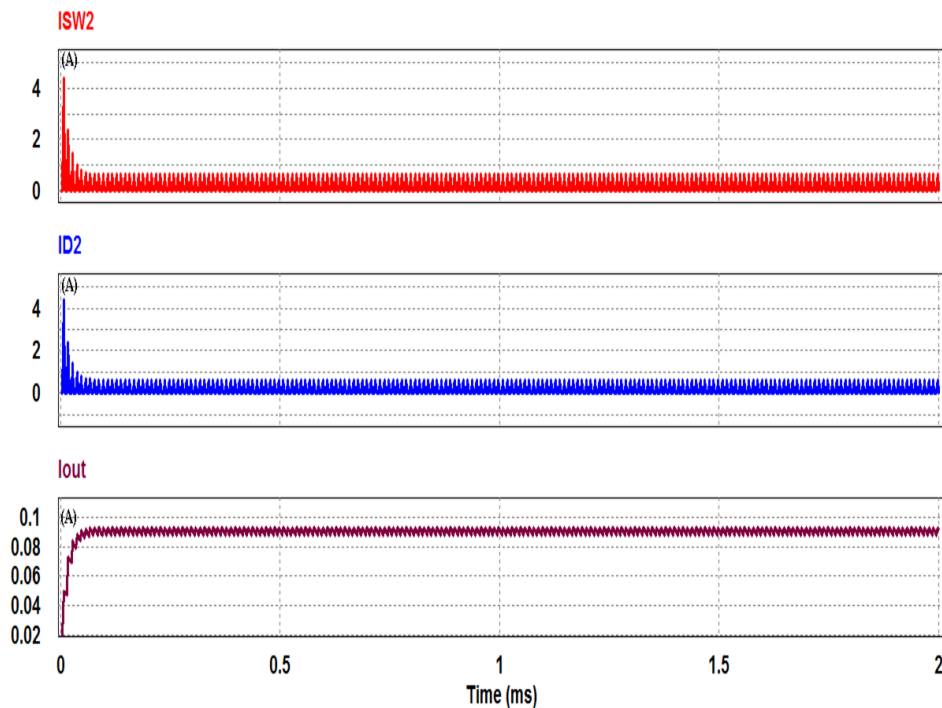
Figure 3.25: Simulated Switch 2, Diode 2 and Load Current Waveforms for Subtraction Circuit

The converter presented in Chapter 6 addresses the possible regulation mechanism in SCC.

CHAPTER 4

A DUAL INPUT VARIABLE OUTPUT BUCK BASED SWITCHED CAPACITOR CONVERTER

This chapter presents a dual source variable output switched capacitor that can be operated in step down mode. The feature of the converter is that it can be selectively switched between two input sources if one needs a solar source. Since inductors are eliminated in the circuit topology the converter is light in weight and size. Also EMI issues are minimal due to the absence of inductors. The converter working in the No Charge (NC) mode or Fast Switching Limit (FSL) (explained in detail in Section 4.2) is used to develop the mathematical model using the differential charge analysis method. Using this model the equivalent resistance of the converter due to the influence of switch resistance can be found out. PSIM simulation of the converter gives satisfactory results and a laboratory prototype has been set up for experimental validation using the locally available components. The converter input is fixed at 12 V which can be from a battery source or if wanted a solar source. The output variable voltage gain obtained is $\frac{1}{3}$, $\frac{1}{2}$, $\frac{2}{3}$ and unity with respect to the input. The application of this converter can be in portable electronic devices or a processor for future which need three buck voltage levels typically in active, standby and sleep mode.

4.1 Description and Working of the Proposed Buck Based SC Converter

A SC converter capable of delivering three buck gain and one unity gain configurations depending on the gating sequence of the switches is shown in Figure 4.1. It consists of two flying capacitors C_{fly1}, C_{fly2} and an output filter capacitor C_{Filter}. The switches S_1 to S_{10} are switched in order to change the connection of flying capacitors so that capacitors can be charged and discharged through different paths in order to obtain desired voltage at the output of converter. Before operating the converter,

switches S_{Batt} or S_{Solar} is triggered. The decision can be taken by sensing battery or solar input. This decision can be made depending upon the availability of solar energy. The switches are controlled using two complementary triggering pulses. Accordingly
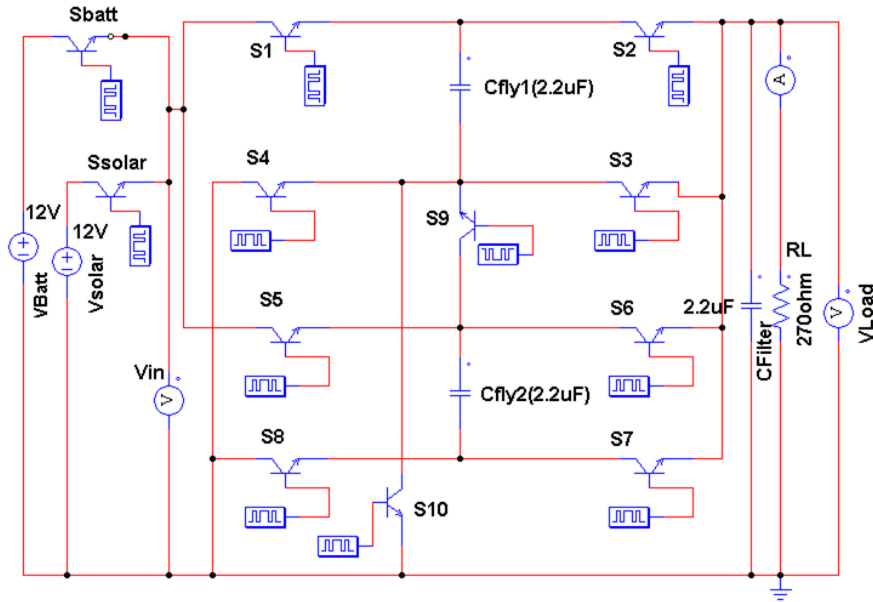
Figure 4.1: Circuit Model of the Proposed Buck Based SC Converter

it has two phases: Charging Phase (CP) and Dumping Phase (DP). By varying how the switches are clocked, according to a particular switch configuration, four different gains $\frac{1}{2}$, $\frac{1}{3}$, $\frac{2}{3}$ and 1 can be obtained by this multi - topology converter. The Voltage Conversion Ratios (VCR) or in other words voltage gain and their switching configurations are given in Table 4.1. Referring to Equation 4.1 "d" and "T" denote the duty factor and

Table 4.1: Switch Pulsing Sequence for Different VCR or Gain Modes

Switch	$\frac{1}{3}$	$\frac{1}{2}$	$\frac{2}{3}$	$\frac{1}{1}$
S_1	CP	CP	CP	CP
S_2	DP	DP	DP	DP
S_3	-	CP	CP	CP
S_4	DP	DP	-	-
S_5	-	CP	CP	-
S_6	DP	DP	-	-
S_7	CP	CP	CP	-
S_8	DP	DP	DP	-
S_9	CP	-	DP	-
S_{10}	-	-	-	DP

46

period of triggering pulses respectively. The duty cycle is taken as 50 percent.

$$T = CP + DP$$
$$CP = dT \qquad (4.1)$$
$$DP = (1 - d)T$$

In Table 4.1, CP indicates the switches that are on during the charging phase and DP indicates the switches on during the dumping phase. Accordingly there exist two equivalent circuits during steady state of topologies for each gain configurations. The verification of output voltages has been done using PSIM for simulation and a small laboratory prototype is developed in breadboard where the switches are controlled using pulses obtained from an astable multivibrator.

4.1.1 Reduced Circuit Structure and Explanation for VCR One by Three

Consider the gain configuration $\frac{1}{3}$ meaning output voltage is one third of the input voltage. From Table 4.1 we can see that the switches S_1, S_7 and S_9 are on during the charging phase CP and switches S_2, S_4, S_6 and S_8 are on during dumping phase DP. The switched circuits of charging and dumping phase are shown in Figure 4.2. Then by KVL following equations can be written. The flying capacitors are charged in series through switches S_1, S_9 and S_7 according to the equations,

$$V_{Cfly1} = V_{Cfly2} = \frac{V_s - V_{load}}{2}$$

In dumping phase, through switches S_2, S_4, S_6 and S_8, the flying capacitors C_{fly1} and C_{fly2} are connected in parallel with the load. The voltages of C_{fly1} and C_{fly2} are,

$$V_{Cfly1} = V_{Cfly2} = V_{load}$$

In steady state, combining the above two equations will result in $\frac{1}{3}$ of the input at the output as shown below by Equation 4.2.

$$\frac{V_{load}}{V_s} = VCR = \frac{1}{3} \qquad (4.2)$$

(a)

(b)
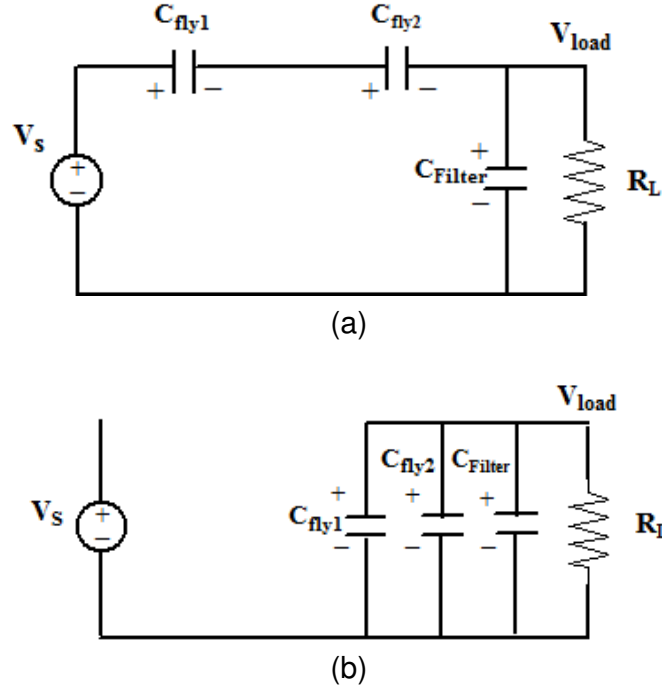
Figure 4.2: Circuit States for VCR $\frac{1}{3}$ (a) During Charging Phase CP (b) During Dumping Phase DP

4.1.2 Reduced Circuit Structure and Explanation for VCR One by Two

Consider the gain configuration $\frac{1}{2}$ meaning output voltage is one half of the input voltage. From Table 4.1 we can see that the switches S_1, S_3, S_5 and S_7 are on during the charging phase CP and switches S_2, S_4, S_6 and S_8 are on during dumping phase DP. The switched circuits of charging and dumping phase are shown in Figure 4.3. In this gain mode, during CP the flying capacitors are connected in parallel which is connected in series with the load deliver the required output voltage. By applying KCL in the Figure 4.3,

$$V_{cfly1} = V_{cfly2} = V_s - V_{load}$$

During DP, the capacitors are connected in parallel with the load satisfying the following equation

$$V_{cfly1} = V_{cfly2} = V_{load}$$

In steady state, both relations will hold. Combining both the equations in steady state result in,

$$\frac{V_{load}}{V_s} = VCR = \frac{1}{2} \tag{4.3}$$

48
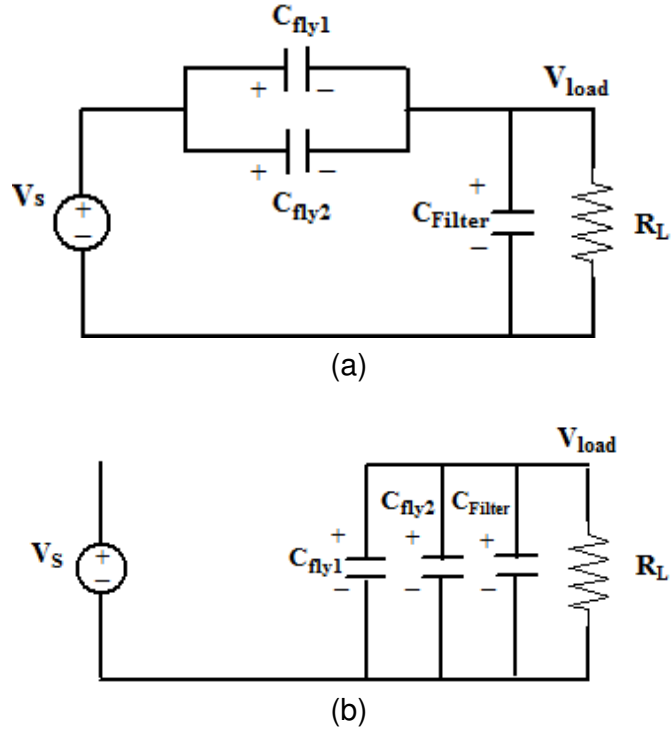
Figure 4.3: Circuit States for VCR $\frac{1}{2}$ (a) During Charging Phase CP (b) During Dumping Phase DP

,

This means $\frac{1}{2}$ of the input voltage is obtained at the output.

4.1.3 Reduced Circuit Structure and Explanation for VCR Two by Three

Consider the gain configuration $\frac{2}{3}$ meaning output voltage is two third of the input voltage. The switches S_1, S_3, S_5 and S_7 are on during the CP and S_2, S_9 and S_8 are on during DP. The switched circuits of charging and dumping phase are shown in Figure 4.4. The flying capacitors are connected in parallel first then the flying capacitors are made to reconnect in series with the load. By applying KCL in the Figure 4.4 satisfying the following equation the VCR can be verified.

$$V_{cfly1} = V_{cfly2} = V_s - V_{load}$$

During dumping phase, the capacitors are connected in series with the load satisfying the following equation,

$$V_{cfly1} = V_{cfly2} = \frac{1}{2}V_{load}$$

49
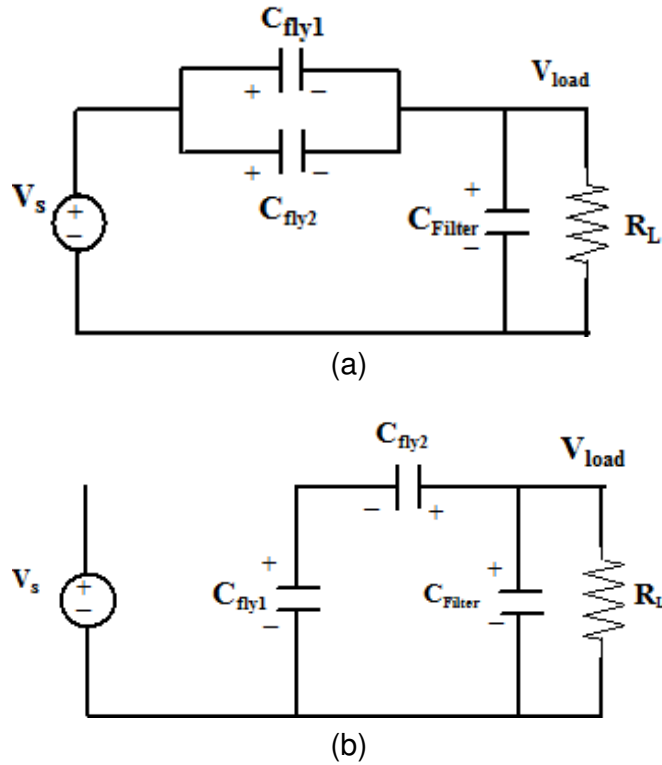
Figure 4.4: Circuit States for VCR $\frac{2}{3}$ (a) During Charging Phase CP (b) During Dumping Phase DP

In steady state, both relations will hold. Combining equations will result in,

$$\frac{V_{load}}{V_s} = VCR = \frac{2}{3} \tag{4.4}$$

This means $\frac{2}{3}$ of the input voltage is obtained at the output.

4.1.4 Reduced Circuit Structure and Explanation for VCR One by One

Consider the gain configuration $\frac{1}{1}$ meaning output voltage is same as that of the input voltage. From Table 4.1 we can see that the switches S_1 and S_3 are on during the charging phase CP, making the capacitor C_{fly1} charge into the V_{load}. The switched circuits of charging and dumping phase are shown in Figure 4.5. This occurs according to the following equation by applying KVL,

$$V_{cfly1} = V_s - V_{load}$$
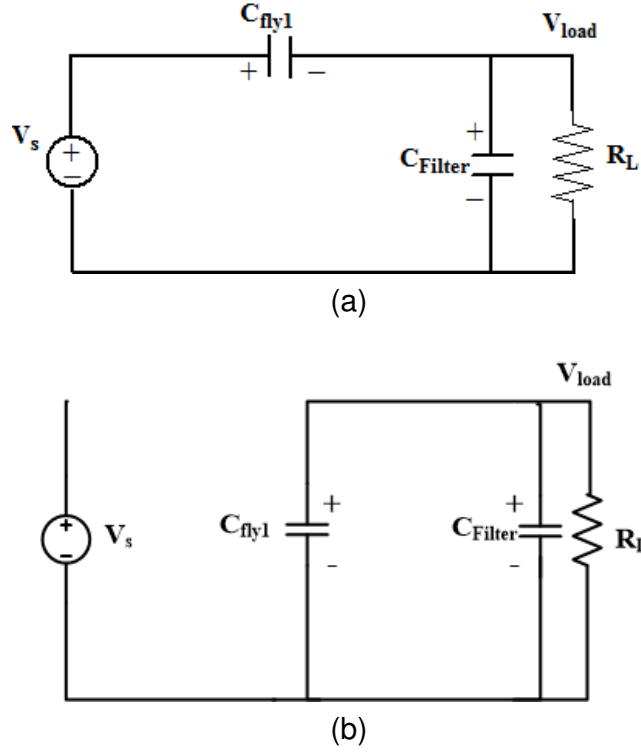
Figure 4.5: Circuit States for VCR 1/1 (a) During Charging Phase CP (b) During Dumping Phase DP

The switches S_2 and S_{10} are on during the dumping phase DP, making the capacitor C_{fly1} discharge into the V_{load} from the input. Thus the following equation is satisfied,

$$V_{cfly1} = V_{load} - V_s$$

As in the steady state, both the equations are satisfied we get,

$$\frac{V_{load}}{V_s} = VCR = 1 \tag{4.5}$$

Thus we can see that conversion ratio 1:1 is obtained using this particular switch configuration in this topology. The proposed converter depending on which gain or VCR is required can be made to clock to connect the flying capacitors in the combination mentioned in Table 4.1 to achieve $\frac{1}{2}$, $\frac{1}{3}$, $\frac{2}{3}$ and 1. In general, the proposed converter is a buck based SCC realization with the absence of inductors. Another important feature of the proposed converter referring to Figure 4.1 is that it can be switched between battery and solar source as the user may define giving flexibility to use multiple sources.

4.2   General Modelling and Analysis Framework for SCC

It is very important to model any power converters for analyzing the performance parameters like losses, efficiency and regulation. There are many models discussed in the literature and this section gives an overview of few of them. The accepted model in the SCC literature to represent SCC is shown in Figure 4.6. When the converter is loaded there will be a voltage drop across R_{out} due to switch resistance and charge transfer losses in the flying capacitors. An exact model will be able to represent R_{out} with reasonable accuracy. When the circuit structure is variable between different phases calculating and summing up the equivalent resistances become more complex. Moreover, the converter may be subjected to different frequencies at which the switches are pulsed to obtain the required VCR and that too in different duty cycles *"d"*. Three models are discussed next based on (Van Breussegem and Steyaert, 2012), (Seeman, 2009) and (Evzelman and Ben-Yaakov, 2013).

The authors (Van Breussegem and Steyaert, 2012) discuss different analysis techniques that are used for analyzing switched capacitor DC - DC converters. The important analysis techniques are charge flow analysis, charge balance analysis and branch analysis. They are used to find the most predominant model; the output impedance model. Charge flow analysis is for identifying the role of different components in the conversion block. Based on this analysis the charge flow vectors are extracted, which play an important role in the modelling and design techniques. They qualify the capacitive converter performance and enable an objective comparison of the converter topologies. Charge balance analysis is based on the law of charge conservation. It deals with absolute amount of charge in the circuit in contrast with charge flow analysis that deals with change in charge on the components. For more complex converter topologies for which other methods becomes exhaustive, a method to determine the output impedance based on the Tellegans theorem called branch analysis is used. It involves two approximates of the output impedance.

The analysis of the proposed converter in this chapter follows the theory that differential values of electric charges in the capacitors used in the circuit during the Charging Phase (CP) and Dumping Phase (DP) is zero. Then the average current is equated by di-

viding the charge by time. However the model developed using the above technique, in the early phase of this research is only partial, therefore incomplete, owing to the fact it addresses only one of the boundaries of operation or transition state of the circuit which is the FSL or NC analysis technique developed by (Seeman, 2009) and (Evzelman and Ben-Yaakov, 2013) respectively detailed in later sections. In the novel converter that has been developed in the later stages of research and discussed in the next chapter, the limitations in respect to the need for more VCR or output voltage gains in both buck and boost modes, as well as a more accurate model development is realized increasing the flexibility of the new converter for the targeted applications.

The model proposed in (Seeman, 2009) is a widely accepted complete model to study the SC converter dynamics. This model included two impedance analysis namely the FSL and Slow Switching Limit Impedance (SSL), adding the two by an approximation method results in finding a more accurate output resistance R_{out} denoted in the model shown in Figure 2.4. The FSL and SSL modes clearly capture the effect of switching frequency on switch resistance and capacitor ESR which is accurately modeled in this analysis technique.

In the SSL analysis corresponding to larger time periods or low frequency, the capacitor current is not constant. The effect of finite resistances of the switches and capacitors are minimal. Hence in this case R_{out} is influenced largely by switching frequency and the flying capacitor values.

In the FSL analysis corresponding to smaller time periods and high frequencies the on state switch resistance, ESR of capacitors influence largely the R_{out} and hence it affects the efficiency considerably. FSL limit is characterized by constant current flowing through the capacitors.

In each of these limits a charge multiplier vector needs to be found. This vector corresponds to charge flows into the flying capacitors once the respective switches are clocked in a particular phase. The charge multiplier vectors can be calculated by applying KCL into the respective capacitor or voltage source into which the charge flows. Thus SSL and FSL is calculated which represents R_{out} the equivalent resistance. The

same theory can be applied for two phase or multiphase circuits which can be verified for details from the cited reference (Seeman, 2009).

It has been proposed in (Evzelman and Ben-Yaakov, 2013), an average current focused modelling of the conduction and charge flow losses to develop R_{out}. This analysis is derived from the basic circuit theory concept of approximating the SCC circuit in any operating phase to a first order RC circuit. The concept of Complete Charge (CC), Partial Charge (PC) and NC boundaries has been developed. The CC and PC corresponds to SSL and FSL limits proposed in (Seeman, 2009). This technique is used to completely model and analyze the novel multiple input variable output buck boost switched capacitor based converter and hence will be treated in detail in the next chapter.

4.2.1 Theoretical Analysis of Dual Input Buck SCC for VCR One by Three

The mathematical analysis performed here is based on (Van Breussegem and Steyaert, 2012; Eguchi *et al.*, 2011) focusing the differential charge analysis. The following assumptions are made in general for all modes in developing the analysis.

1. The converter is assumed to be operating in the FSL or NC mode.
2. Parasitic elements are negligibly small.
3. Time constant is much larger than the period of clock pulses.
4. Assuming all the denoted switch resistances are equal and let each be equal to R_S.

The equivalent circuit of switched capacitor power converter is shown in Figure 4.6, where R_{out} is the switched capacitor modeled resistance, "n" is the turns ratio of ideal transformer which is the VCRs, and $V_{s,avg}$ and $V_{load,avg}$ are the average value of input and output voltages respectively.

The equivalent circuit for modelling the converter to develop R_{out} is shown in Figure 4.7. R_{S1}, R_{S2}, R_{S3}, R_{S4}, R_{S5}, R_{S6}, R_{S7}, R_{S8}, R_{S9}, and R_{S10} denotes the on state resistance of the switches S_1 to S_{10} respectively. Differential values of electric charges during
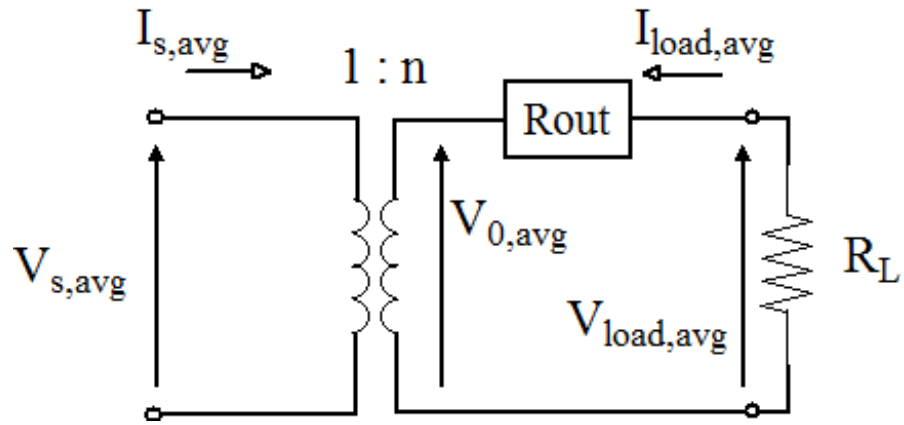
Figure 4.6: Instantaneous Equivalent Circuit Model
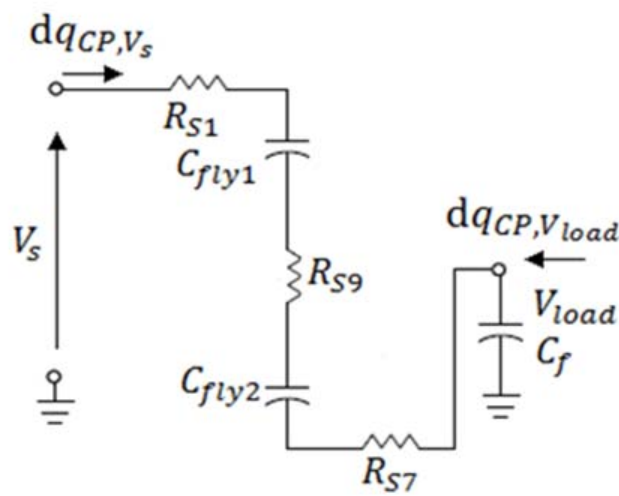
(a)
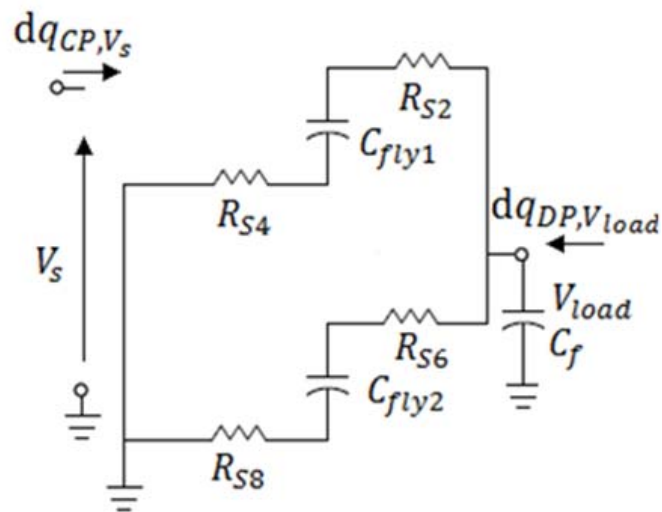
(b)

Figure 4.7: Equivalent Circuit States for VCR $\frac{1}{3}$ (a) During Charging Phase CP (b) During Dumping Phase DP

steady state of circuit is C_x where x = {1, 2, 3} satisfy,

$$dq_{CP}^x + dq_{DP}^x = 0 \tag{4.6}$$

where dq_{CP}^x and dq_{DP}^x denote electric charges during charging phase (CP) and dumping phase (DP) respectively in the two flying capacitors and buffer or filter capacitor that participates in the charge transfer. During charging phase, differential values of electric charges in input and output terminals dq_{CP,V_s} and $dq_{CP,V_{load}}$ are given by,

$$dq_{CP,Vs} = dq_{CP}^1 = dq_{CP}^2$$

$$dq_{CP,VLoad} = dq_{CP}^3 + dq_{CP}^1 = dq_{CP}^3 + dq_{CP}^2 \tag{4.7}$$

During dumping phase, differential values of electric charges in input and output state terminals, dq_{DP,V_s} and $dq_{DP,V_{load}}$ are given by,

$$dq_{DP,Vs} = 0$$

$$dq_{DP,VLoad} = dq_{DP}^1 + dq_{DP}^2 + dq_{DP}^3 \tag{4.8}$$

The average value of currents at input and output, $I_{s,avg}$ and $I_{load,avg}$ are given by,

$$I_{s,avg} = (dq_{CP,Vs} + dq_{DP,Vs})/T \equiv dq_{Vs}/T$$

$$I_{load,avg} = (dq_{CP,Vload} + dq_{DP,Vload})/T \equiv dq_{Vload}/T \tag{4.9}$$

Where dq_{V_s} and $dq_{V_{load}}$ are electric charges in input terminal and output terminal respectively. From Equations (4.7), (4.8) and (4.9),

$$I_{s,avg} = dq_{CP}^1/T = dq_{CP}^2/T \tag{4.10}$$

$$I_{load,avg} = (dq_{CP}^3 + dq_{CP}^1 + dq_{DP}^1 + dq_{DP}^2 + dq_{DP}^3)/T$$

From Equation (4.6), $I_{load,avg} = (-2dq_{CP}^1 - dq_{CP}^2)/T$

$$I_{load,avg} = (-3dq_{CP}^1)/T = (-3dq_{DP}^1)/T \tag{4.11}$$

From Equations (4.10) and (4.11) the relation between input and output currents is obtained as,

$$I_{s,avg} = -\frac{1}{3}I_{load,avg} \tag{4.12}$$

The energy consumed by resistances in Figure 4.7 during one complete cycle, W_T can be expressed as,

$$W_T = W_{CP} + W_{DP} \tag{4.13}$$

Where,

$$W_{CP} = \frac{3R_s}{CP}(dq_{CP}^1)^2 \tag{4.14}$$

$$W_{DP} = \frac{2R_s}{DP}(dq_{DP}^1)^2 + \frac{2R_s}{DP}(dq_{DP}^2)^2 \tag{4.15}$$

From Equations (4.6), (4.7), (4.8), (4.9) and (4.12), consumed energy (4.14) and (4.15) can be rewritten as,

$$W_{CP} = \frac{R_s}{3dT}(dqV_{load})^2$$

$$W_{DP} = \frac{4R_s}{9(1-d)T}(dqV_{load})^2$$

$$W_T = \frac{R_s}{3dT}(dqV_{load})^2 + \frac{4R_s}{9(1-d)T}(dqV_{load})^2$$

Thus,

$$W_T = \frac{1}{3T}(dqV_{load})^2\frac{9+3d}{27d(1-d)}R_s \tag{4.16}$$

The consumed energy W_T in Figure 4.6 is given by,

$$W_T = \left(\frac{dqV_{load}}{T}\right)^2 R_{out}T \tag{4.17}$$

Equating values of W_T from Equations (4.17) and (4.16), switched capacitor resistance for gain configuration $\frac{1}{3}$ is given by,

$$\left(\frac{dqV_{load}}{T}\right)^2 R_{out}T = \frac{1}{3T}(dqV_{load})^2\frac{9+3d}{27d(1-d)}R_s$$

$$R_{out} = \frac{9+3d}{27d(1-d)}R_s \tag{4.18}$$

The equivalent circuit shown in Figure 4.6 can be expressed with determinants using

57

kettenmatrix. The determinants are,

$$
\begin{bmatrix} V_{s,avg} \\ I_{s,avg} \end{bmatrix} = \begin{bmatrix} \frac{1}{n} & 0 \\ 0 & n \end{bmatrix} \begin{bmatrix} V_{0,avg} \\ I_{load,avg} \end{bmatrix}
\tag{4.19}
$$

$$
\begin{bmatrix} V_{0,avg} \\ I_{load,avg} \end{bmatrix} = \begin{bmatrix} 1 & R_{out} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_{load,avg} \\ -I_{load,avg} \end{bmatrix}
\tag{4.20}
$$

where $n = \frac{1}{3}$. From (4.19) and (4.20) the power efficiency can be written as,

$$
\eta = \frac{R_L \left(I_{load,avg}\right)^2}{R_L \left(I_{load,avg}\right)^2 + R_{out} \left(I_{load,avg}\right)^2}
$$
$$
= \frac{R_L}{R_L + R_{out}}
\tag{4.21}
$$

The optimal value of duty factor can be obtained by,

$$
\frac{dR_{out}}{d(d)} = 0
\tag{4.22}
$$

$$
\frac{d}{d(d)} \left(\frac{9 + 3d}{27d(1 - d)} R_s \right) = 0
$$

$81d^2 + 486d - 243 = 0$ and $0 < d < 1$. On solving we get, $d = -6.46$ and $d = 0.46$ Thus from Equations (4.18) and (4.22) the optimal duty factor for gain configuration is $d \simeq 0.46$.

4.2.2 Theoretical Analysis of Dual Input Buck SCC for VCR One by Two

The equivalent circuit for modelling the converter is shown in Figure 4.8. The switches participating in CP are R_{S1}, R_{S3}, R_{S5}, R_{S7}, in DP R_{S2}, R_{S4}, R_{S6}, R_{S8} take part as can be seen from the equivalent circuit connecting the respective flying capacitors. During charging state CP, differential values of electric charges in input and output terminals, dq_{CP,V_s} and $dq_{CP,V_{load}}$ are given by,

$$
dq_{CP,V_s} = dq_{CP}^1 + dq_{CP}^2
\tag{4.23}
$$
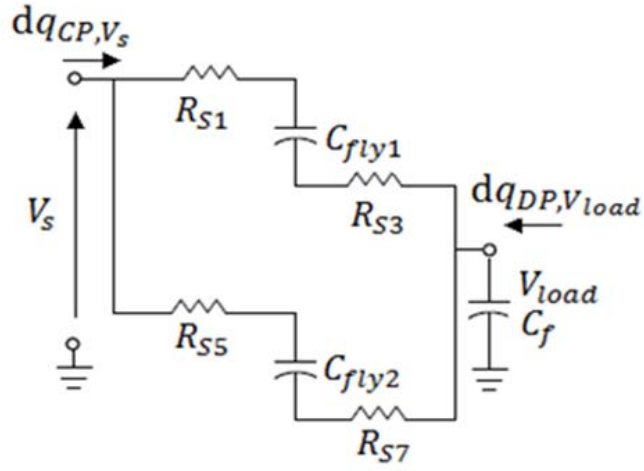
(a)
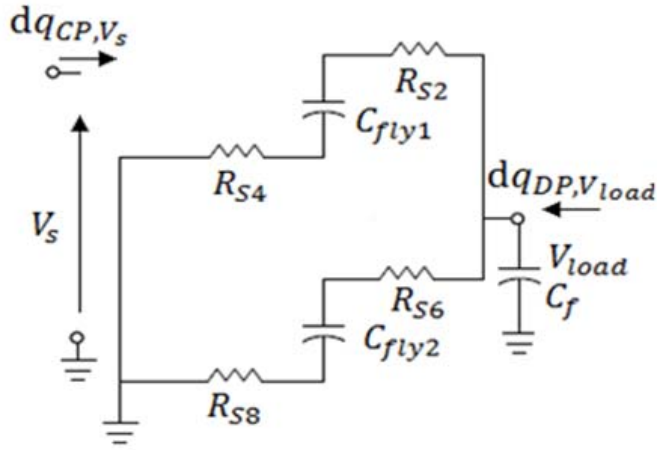
(b)

Figure 4.8: Instantaneous Equivalent Circuit States for VCR $\frac{1}{2}$ (a) During Charging Phase CP (b) During Dumping Phase DP

$dq_{CP,V_{load}} = - (\, dq_{CP}^1 + dq_{CP}^2) + \, dq_{CP}^3$. During dumping state DP, differential values of electric charges in input and output terminals, dq_{DP,V_s} and $dq_{DP,V_{load}}$ are given by,

$$dq_{DP,V_s} = 0$$

$$dq_{DP,V_{load}} = dq_{DP}^1 + dq_{DP}^2 + dq_{DP}^3 \qquad (4.24)$$

By substituting (4.6), (4.23) and (4.24) into (4.9) the relation between input and output currents is obtained as,

$$I_{s,avg} = -\frac{1}{2}I_{load,avg} \qquad (4.25)$$

59

The energy consumed by resistances in Figure 4.8 during one complete cycle, W_T can be expressed as,

$$W_T = W_{CP} + W_{DP} \tag{4.26}$$

Where,

$$W_{CP} = \frac{2R_s}{CP}(dq^1_{CP})^2 + \frac{2R_s}{CP}(dq^2_{CP})^2$$

$$W_{DP} = \frac{2R_s}{DP}(dq^1_{DP})^2 + \frac{2R_s}{DP}(dq^2_{DP})^2$$

From (4.6), (4.23) and (4.24), consumed energy (4.26) can be rewritten as,

$$W_T = \frac{R_s}{4dT}(dq_{V_{load}})^2 + \frac{R_s}{4(1-d)T}(dq_{V_{load}})^2 \tag{4.27}$$

Equating values of W_T from Equations (4.17) and (4.27), Switched capacitor resistance for gain configuration $\frac{1}{2}$ is given by,

$$R_{out} = \frac{1}{4d(1-d)}R_s \tag{4.28}$$

From Equations (4.28), the equivalent circuit can be redrawn as in Figure 4.6 where VCR of $n = \frac{1}{2}$ is realized. The power efficiency is obtained from Equation (4.21), and the optimal duty factor is obtained as $d = 0.5$. By following a similar procedure as in Equation (4.20) the Kettenmatrix can be developed.

4.2.3 Theoretical Analysis of Dual Input Buck SCC for VCR Two by Three

The equivalent circuit for modelling the converter is shown in Figure 4.9. The switches participating in CP are R_{S1}, R_{S3}, R_{S5}, R_{S7} and in DP R_{S2}, R_{S8}, R_{S9} take part as can be seen from the equivalent circuit connecting the respective flying capacitors.

During charging state CP, differential values of electric charges in input and output terminals, dq_{CP,V_s} and $dq_{CP,V_{load}}$ are given by, $dq_{CP,V_s} = dq^1_{CP} + dq^2_{CP}$ and,

$$dq_{CP,V_{load}} = -(dq^1_{CP} + dq^2_{CP}) + dq^3_{CP} \tag{4.29}$$

During dumping state DP, differential values of electric charges in input and output
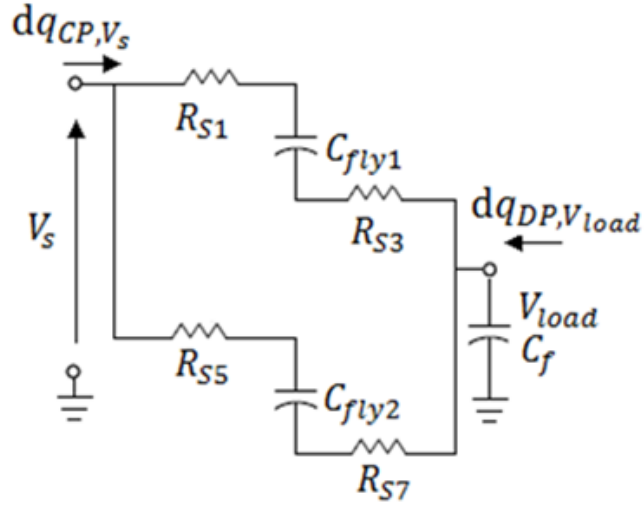
(a)
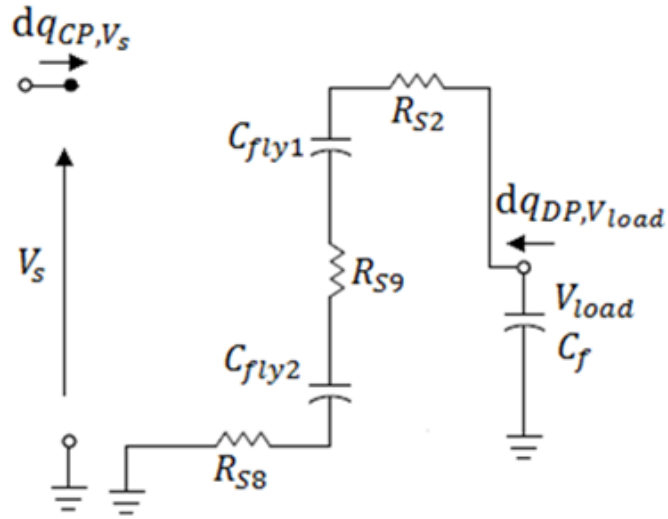
(b)

Figure 4.9: Instantaneous Equivalent Circuit States for VCR $\frac{2}{3}$ (a) During Charging Phase CP (b) During Dumping Phase DP

terminals, dq_{DP,V_s} and $dq_{DP,V_{load}}$ are given by,

$$dq_{DP,V_s} = 0$$

and,

$$dq_{DP,V_{load}} = dq_{DP}^1 + dq_{DP}^3 = dq_{DP}^2 + dq_{DP}^3 \qquad (4.30)$$

By substituting (4.6), (4.29) and (4.30) into (4.9) the relation between input and output currents is obtained as,

$$I_{s,avg} = -\frac{2}{3}I_{load,avg} \qquad (4.31)$$

61

The energy consumed by resistances in Figure 4.9 during one complete cycle, W_T can be expressed as,

$$W_T = W_{CP} + W_{DP} \tag{4.32}$$

Where,

$$W_{CP} = \frac{2R_s}{CP}(dq^1_{CP})^2 + \frac{2R_s}{CP}(dq^2_{CP})^2$$

$$W_{DP} = \frac{3R_s}{DP}(dq^1_{DP})^2$$

From Equations (4.6), (4.29) and (4.30), consumed energy can be rewritten as,

$$W_T = \frac{4R_s}{9dT}(dq_{V_{load}})^2 + \frac{R_s}{3(1-d)T}(dq_{V_{load}})^2 \tag{4.33}$$

Equating values of W_T from Equations (4.17) and (4.33), Switched capacitor resistance for gain configuration $\frac{2}{3}$ is given by,

$$R_{out} = \frac{12 - 3d}{27d(1-d)}R_s \tag{4.34}$$

From Equations (4.34), the equivalent circuit can be redrawn as in Figure 4.6 where VCR of $n = \frac{2}{3}$ is realized. The power efficiency is obtained from Equation (4.21), and the optimal duty factor is obtained as d = 0.54. By following a similar procedure as in Equation (4.20) the Kettenmatrix can be developed.

4.3 Discussions on Limitations of the Model Developed using the Differential Charge Analysis

As discussed in Section 4.2 the differential charge analysis used to develop the model for R_{out} referred in Figure 4.6 is partial and hence incomplete. This method was developed in the initial phase of the research and in next chapter a more accurate method using the average current conduction model has been derived to model R_{out} in the newly developed converter. The advantages and disadvantages of this analysis are,

1. The Equations (4.2), (4.3), (4.4) and (4.5) are valid to define the connections of flying capacitors to obtain a particular VCR.

2. The Equations (4.18), (4.28) and (4.34) have limitations due to the fact that the ESR of the flying capacitors are not modeled as part of the equivalent circuit resistances in Figures 4.7, 4.8 and 4.9. This will affect the calculation of R_{out} in the main model parameter.

3. Another limitation of Equation (4.18), (4.28) and (4.34) is the absence of the flying capacitor term C_{fly}. This term which can be seen in the Equations (2.7) and (2.8) in the industrial SCC regulators discussed in chapter 2, is a very important parameter in the design of SCC. It may be noted that the frequency term is embedded in Equation (4.18) and (4.28) since duty ratio "d" is proportional to the time period "T" and hence frequency "f". The theory that $R_{out} \propto \frac{1}{fC}$ should be the basis of any SCC model, where "f" is the switching frequency and "C" the flying capacitor and filter capacitor equivalent capacitance.

4. Equation (2.1) holds good to calculate the efficiency and Equation (4.28) gives good insight into the method.

5. Even with the limitations and inaccuracy, the attempt to model and analyze using this method as a first step helps in refining further the analysis presented in subsequent chapters giving a very accurate model and results.

4.4 PSIM Based Simulations of the Proposed Converter

The PSIM software is used as the simulation platform in order to check the validity of the proposed converter. The circuit is simulated for an input voltage of 12 V and the output options available are 4 V, 6 V, 8 V and 12 V respectively for the gain configuration $\frac{1}{3}$, $\frac{1}{2}$, $\frac{2}{3}$ and unity. According to the required gain configuration the clocking pulses are provided at the desired frequency and the waveforms of input voltage, output voltage and load currents have been obtained. The circuit is simulated for a load of 270 Ω such that the load current varies in the range of 10 mA to 50 mA. The switching frequency is taken as 2 kHz and duty cycle is set at 50 percent. The circuit is rigged as shown in Figure 4.1.

The value of flying capacitors C_{fly1} and C_{fly2} and filter capacitor C_{Filter} is taken as each of 2.2 μF. The switches used here are simple BJTs whose on state resistance is set to zero. Similarly the ESR of the capacitors are not accounted as this parameter is absent in the mathematical modelling as indicated above. Therefore the attempt in this simulation study is basically to validate the working of the converter producing the required buck output of gain configuration $\frac{1}{3}$, $\frac{1}{2}$, $\frac{2}{3}$ and unity. To interchange between sources, switches S_{Batt} or S_{Solar} is triggered based on selection.

4.4.1 Simulation Results for VCR of One by Three

The simulation results for VCR $\frac{1}{3}$ is shown in Figure 4.10. The input voltage of the converter is selected as 12 V which can be from solar source or battery as can be seen from the first waveform. The second waveform shows the output voltage which is as desired equal to 4 V. The third waveform is the the output current which is equal to 15 mA. By inspection it can be seen that the output voltage is one - third of the input given qualifying for a buck converter operation.

4.4.2 Simulation Results for VCR of One by Two

The simulation results for VCR $\frac{1}{2}$ is shown in Figure 4.11. The input voltage of the converter is selected as 12 V which can be from solar source or battery as shown in the first waveform. The second waveform shows the output voltage which is as desired equal to 6 V. The third waveform is the the output current which is equal to 22 mA. By inspection it can be seen that the output voltage is one - half of the input given justifying a buck converter operation.

4.4.3 Simulation Results for VCR of Two by Three

The simulation results for VCR $\frac{2}{3}$ is shown in Figure 4.12. The input voltage of the converter is selected as 12 V which can be from solar source or battery as shown in the first waveform. The second waveform shows the output voltage which is as desired equal to 8 V. The third waveform is the the output current which is equal to nearly 30 mA. By inspection it can be seen that the output voltage is two - third of the input given,
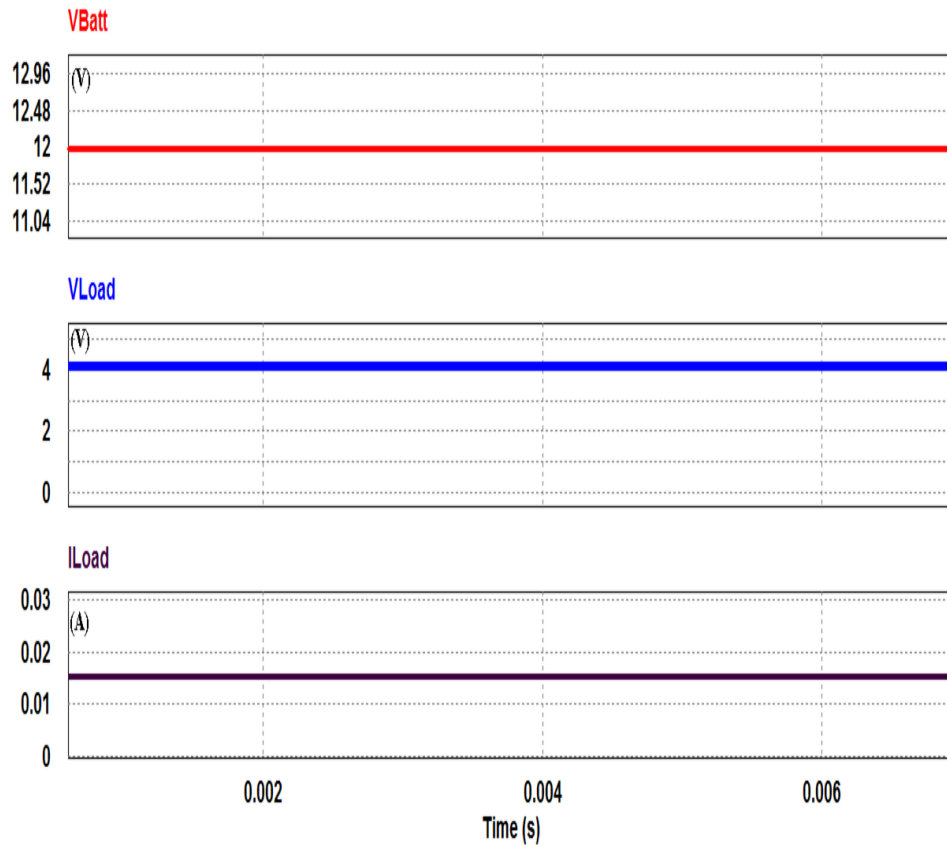
Figure 4.10: Simulated Waveforms for VCR $\frac{1}{3}$ - Input Voltage (V_{Batt}) Volts, Output Load Voltage (V_{Load}) and Load Current I_{Load}

qualifying for a buck converter operation.

4.4.4 Simulation Results for VCR of 1/1

The simulation results for VCR $\frac{1}{1}$ is shown in Figure 4.13. The input voltage of the converter is selected as 12 V which can be from solar source or battery as shown in the first waveform. The second waveform shows the output voltage which is as desired equal to 12 V. The third waveform is the the output current which is equal to nearly 45 mA. By inspection it can be seen that the output voltage is that of the input given, thus being a unity gain converter.
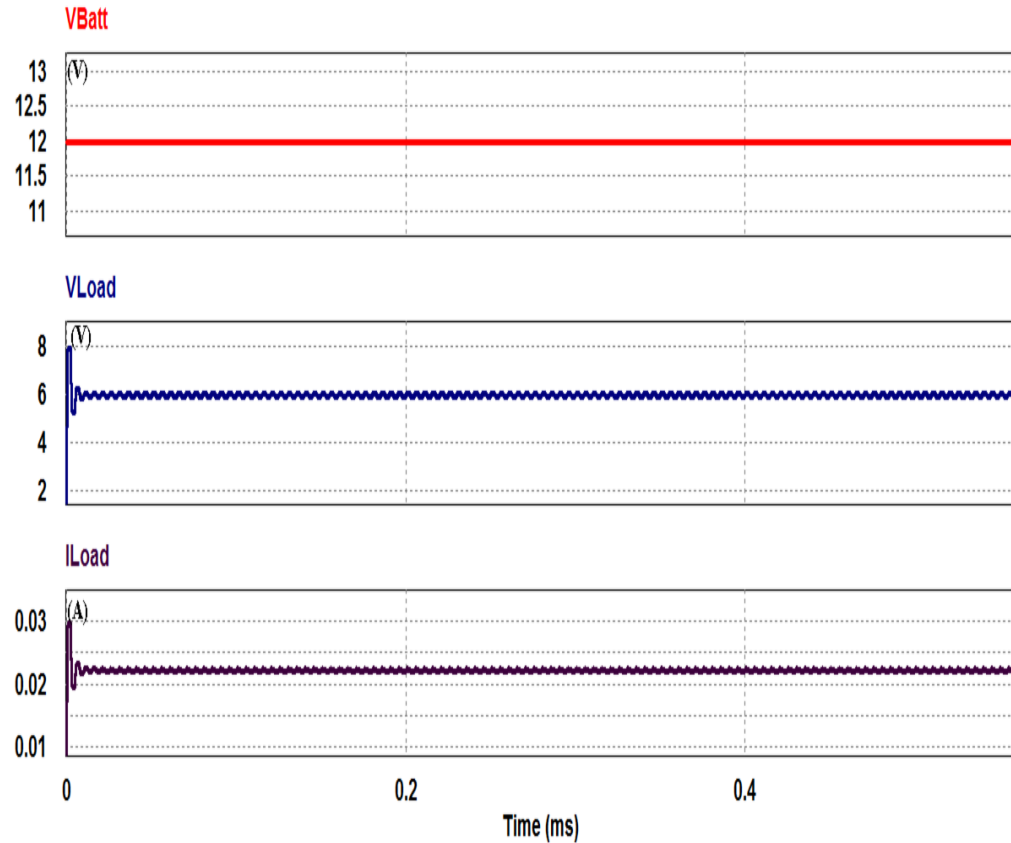
Figure 4.11: Simulated Waveforms for VCR $\frac{1}{2}$ - Input Voltage (V_{Batt}) Volts, Output Load Voltage (V_{Load}) and Load Current I_{Load}

4.5 Development of a Laboratory Prototype for Experimental Verification of the Proposed Converter

For laboratory experimental verification, locally available transistor switches BC107 is used as switches. The output power requirement in the anticipated application of these converters is in mW range typical for LED's. The flying capacitors and the bypass capacitor are of electrolytic type and are assumed to be of same value for the proper charge division during the operation of topology in different modes. Optocouplers are used for isolation between power circuit and gating circuit. The load resistance R_L is taken as 270 Ω and value of the flying capacitor as 2.2μF. The astable multivibrator which produce the gating control signals are composed of the capacitors, resistors and switches are composed of transistor BC107. Taking the capacitor value as 2.2μF and required triggering pulse frequency as 2 kHz and taking the value of capacitor time constant and capacitor charging time equal, the value of resistor used in astable multi-

66
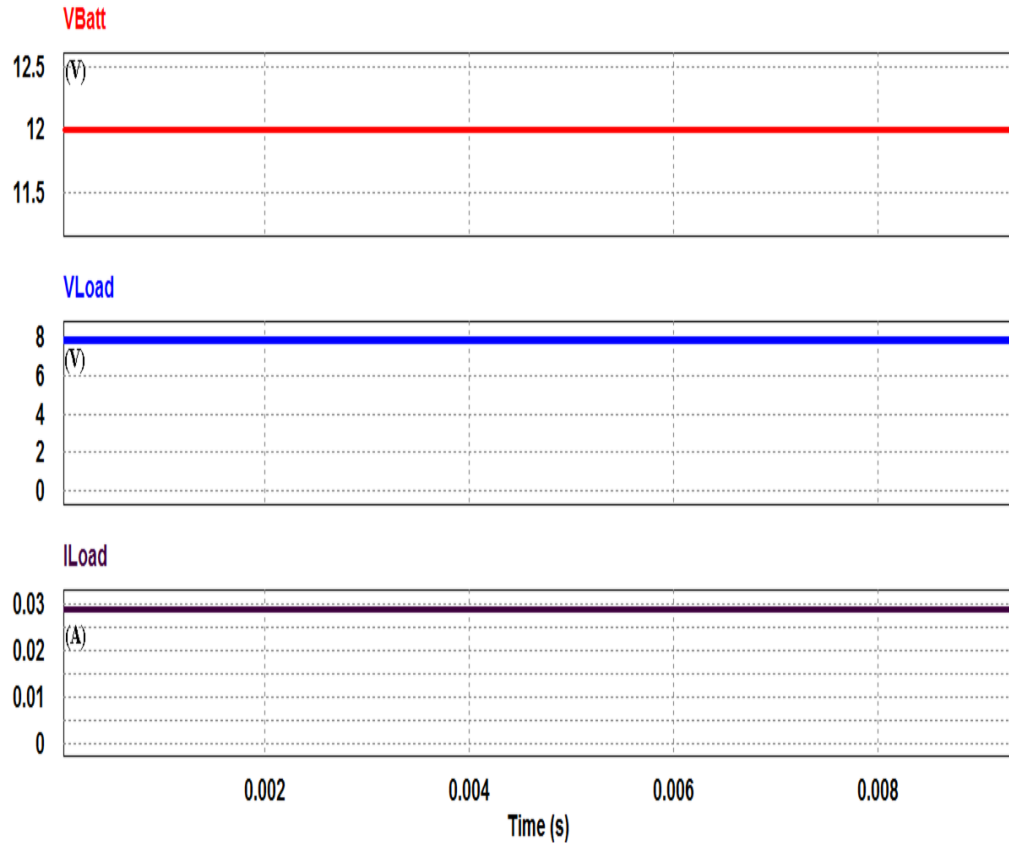
Figure 4.12: Simulated Waveforms for VCR $\frac{2}{3}$ - Input Voltage (V_{Batt}) Volts, Output Load Voltage (V_{Load}) and Load Current I_{Load}

vibrator is obtained as 82 kΩ with an additional resistance of 680 Ω to limit the output current supplied to the optocouplers. As an example, for gain configuration 3:1 the input given is 12 V and output voltage is one - third of the input that is equal to 4 V. Thus the output current and output power are, $I = V/R$ = 14.8 mA, $P = VI$= 59.25 mW. Similarly all the values in other VCR can also be found out.

The most important three gain configuration namely $\frac{1}{3}$, $\frac{1}{2}$, $\frac{2}{3}$ has been experimentally verified as this converter is assumed to be a buck or step down converter and moreover unity gain is direct supply of input. Hence only nine switches are required and can be called as a triple ratio SCC based buck converter. The input source can be from a solar panel if switch S_{Solar} is selected. In this work, battery is selected as input for experimental verification. Two DC regulated variable power supplies of 0 - 30 V available in laboratory are used. One is used for providing a DC input of 12 V to the proposed multi - gain converter circuit and other for providing 5 V DC input to the astable multivibrator. The digital storage oscilloscope DSO - 5100A is used to view the input and output
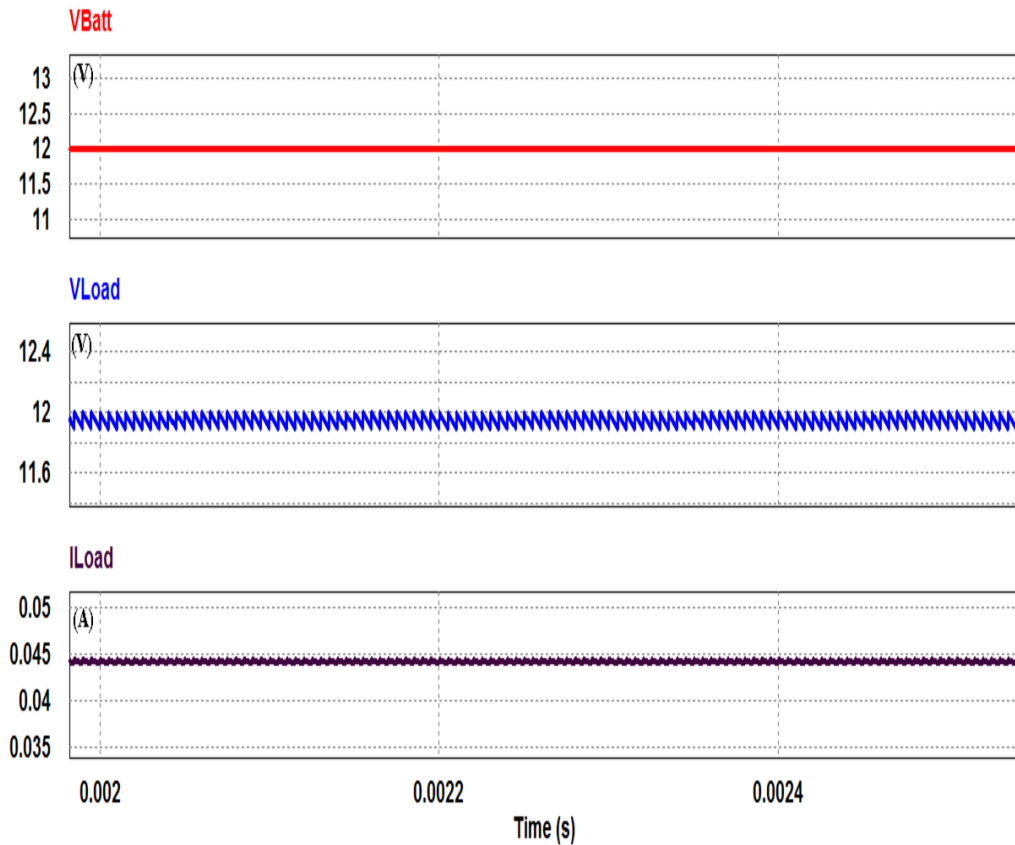
Figure 4.13: Simulated Waveforms for VCR 1/1 - Input Voltage (V_{Batt}) Volts, Output
Load Voltage (V_{Load}) and Load Current I_{Load}

voltages.

4.5.1 Experimental Verification of Output Voltages of the Proposed Converter

The hardware is rigged up in breadboard as shown in Figure 4.14 and the waveforms
for all the VCR gain configuration has been verified. The trigger pulses for the switches
are as shown in Figure 4.15. The plots for the input of 12 V and output voltage of 4 V,
6 V and 8 V which is corresponding to $\frac{1}{3}$, $\frac{1}{2}$, $\frac{2}{3}$ are shown in Figure 4.16.

The voltage per division is set to 5 V. It can be viewed from Figure 4.16a that for an
input of 12 V one third of the input that is 4 V is obtained at the output as anticipated in
the simulation results shown in Figure 4.10. Slight ripple is seen in the output waveform
which can be eliminated by using a higher size filter capacitor or by increasing the
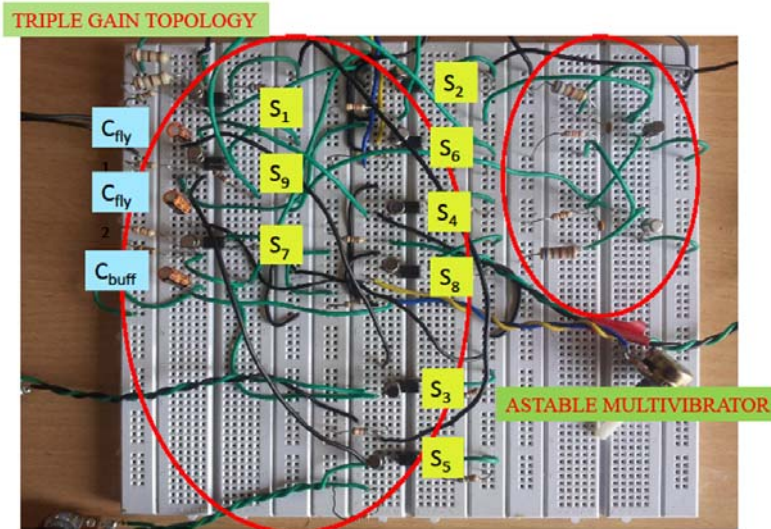
Figure 4.14: Hardware Prototype with all the switches and flying capacitors
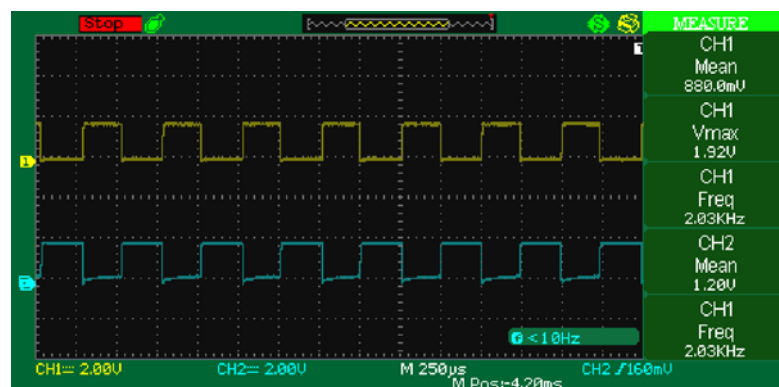
Figure 4.15: Trigger pulses with Duty Cycle 0.5

switching frequency. Similarly Figure 4.16b and Figure 4.16c show an output voltage of 5.8 V and 8 V for an input of 12 V validating the other two gain modes of $\frac{1}{2}$ and $\frac{2}{3}$ with good agreement with simulation results of Figure 4.11 and 4.12. In general the ripples seen can be mitigated by increasing the switching frequency.

4.6   Conclusion

In this chapter, a novel SC based buck converter is presented which is capable of generating $\frac{1}{3}$, $\frac{1}{2}$, $\frac{2}{3}$ and unity, all in step down voltage or buck mode. The novelty claimed in this circuit is the capability to operate from two independent sources with additional gain mode of unity. Another feature is that, the required VCR is obtained without the inductor which promise a better space utilization for on chip implementation. An attempt was made in the crude form to model and present a mathematical model using
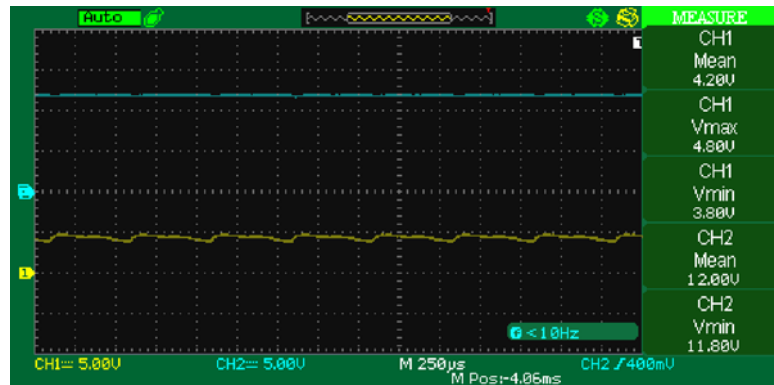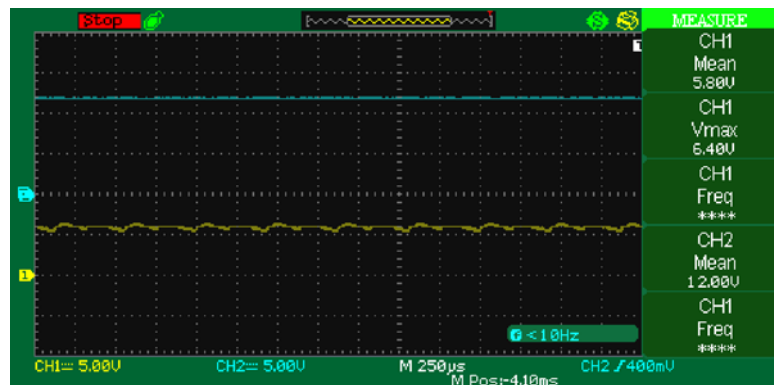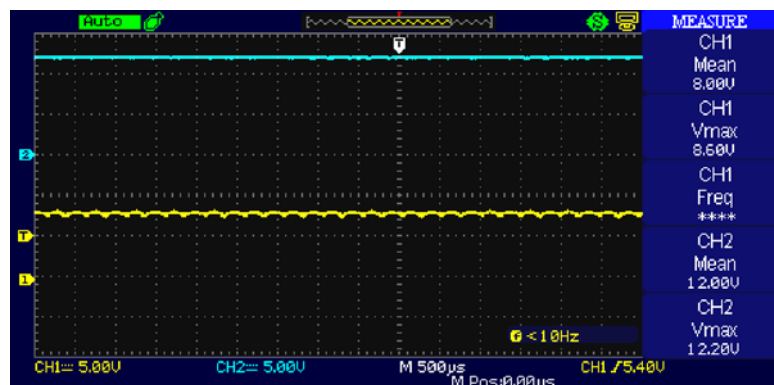
Figure 4.16: Experimental Output Voltage Waveforms for VCR $\frac{1}{3}$, $\frac{1}{2}$ and $\frac{2}{3}$

the differential charge analysis technique which do not represent the exact model as the ESR of the capacitors and the flying capacitor values are absent. Also some circuits will have diodes present in the charging or dumping phase, whose model is also to be incorporated in the analysis. The output voltages ideally will be slightly less than the input voltage due to the losses in the switches, diodes if any and ESR of the capacitor. However the focus of the simulation and experimental work was to verify, gain insight into the SC converter domain and understand the possibility of SC based buck converter implementation which is promising.

Having understood the limitations and flaws of the analysis along with the inaccuracy in the model a new and better analysis method which could give an accurate model was surveyed. Extending the possibilities of both buck and boost modes in a single circuit itself with same or lesser number of switches was another focus to increase flexibility in the converter. Thus in the next stages of the research, reported in subsequent chapters, a new multiple input multiple output DC - DC SCC that can operate off two independent sources and deliver multiple output voltages by intelligent gating to establish a variable circuit structure that can give the targeted output which is buck - boost based is presented.

CHAPTER 5

A NEW MULTIPLE INPUT VARIABLE OUTPUT BUCK - BOOST BASED SERIES - PARALLEL SWITCHED CAPACITOR CONVERTER

A new series - parallel Switched Capacitor Converter (SCC) topology capable of operating off two independent input sources and generating target output voltage in buck or boost mode is presented in this chapter. Operation principle, conversion ratios, modelling considerations in different operation modes and extensive loss analysis are derived. The converter is robust and may be operated off one or two input sources, having the ability to change conversion ratio over a wide range in buck or boost mode. The proposed model assumes that the conduction losses are proportional to the average current flowing through each of the charge pump capacitor in a switching phase. Capacitor current instantaneous waveform in the complete charge, partial charge and no charge modes are captured in simulation and experiment. Model predicted equivalent resistance, output voltage and instantaneous capacitor current waveform concur excellent with simulated and experimental values, rendering the new converter as an excellent candidate for two and single input source applications. The model of the converter is accurately derived and represented as an equivalent output resistance R_{out}. One possible method of regulating the output voltage is by varying R_{out} by changing the switching frequency and this method of regulation is also detailed in this chapter.

5.1 Architecture of the Proposed Buck - Boost Based SCC

In this work, a converter capable to utilize two input sources simultaneously is presented. Renewable energy sources like solar panels or combination of energy storage and solar panel resources can be tapped using the presented converter. The architecture of the converter is shown in Figure 5.1 The converter has a capability to reconfigure its
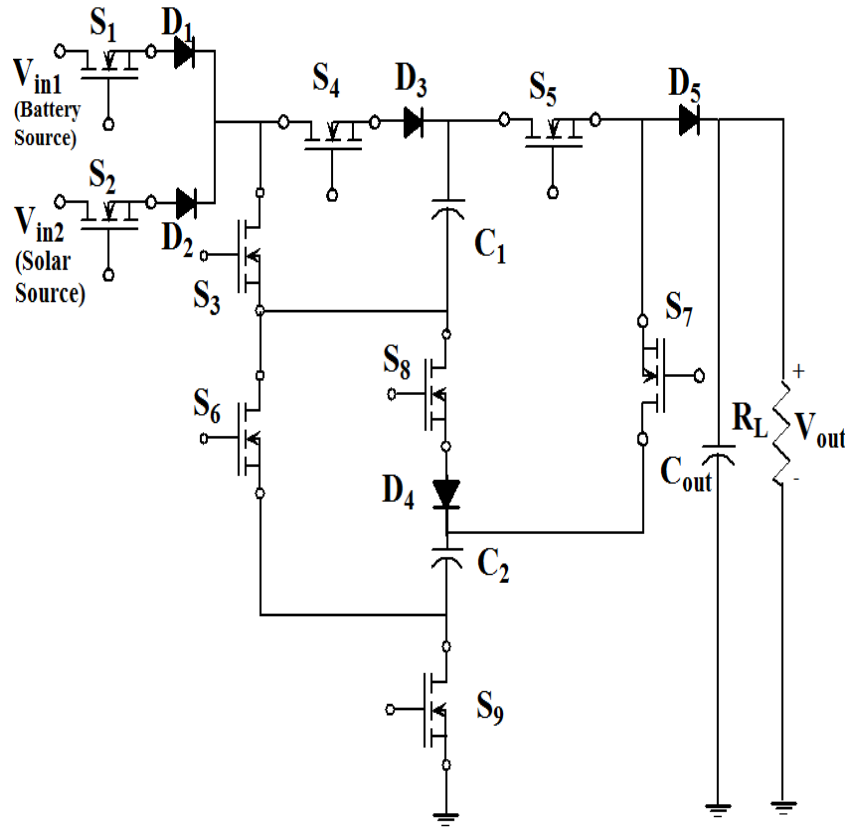
Figure 5.1: Architecture of the Proposed Multiple Input Multiple Output Buck - Boost SCC

gain using variable circuit structure by selectively activating converter switches. The same switches and capacitors are reused and connected in a predetermined pattern to generate the required output voltage optimizing the usage of the components. The converter uses 2 flying capacitors, 9 active switches and five diodes to achieve the required output with the capability to deliver 11 gain modes or Voltage Conversion Ratios (VCR) at the output. Five diodes are used to suppress the unwanted conduction of antiparallel diode in MOSFETs. The topology is developed based on the series parallel generic topology discussed in Chapter 2. The architecture based on selectively switching making the converter to adopt a variable structure to obtain the required VCR. Eleven gain modes can be derived from this architecture when judiciously selecting the source. One source in this architecture is taken as battery and the second one a solar source. This gives a very convenient method of using both according to the availability of sunlight.

5.2 Operational States and Voltage Conversion Ratio (VCR) of the Two Input Series - Parallel Multiple Output Buck - Boost SCC Topology

The power circuit layout of a series - parallel topology switched capacitor converter capable of delivering 11 output states are shown in Figure 5.1. The switching transition of all the switches when gated is shown in Table 5.1 and eleven possible voltage conversion ratios (VCR) is presented. Tapping both the sources when solar is partially available is the state 3 in Table 5.1. When boost mode of operation is needed the switching sequence is generated to obtain state 1, 2, 4 and 5. State 1 and 2 are the doubler boost modes either from battery or solar source. Similarly state 4 and 5 will generate at the output a voltage of $\frac{3}{2}$ times the input voltage when operated from battery or solar source. State 8 and 9 enables the buck mode of operation which can give half the input voltage at output. Another state, 6 and 7 is an adder mode with output voltage being the sum of the voltages of one source and half of the other one. State 10 and 11 are unity gain modes in which output voltage is the same as input voltage. For a particular output voltage requirement, the predetermined gating sequence has to be generated to control the switches. There are two states in one cycle of operation of the converter for any desired output voltage. The duty ratio for simplicity is taken as 50 % and only two phase clocking is used. During the charging state (CS) the charge pump capacitors or flying capacitors C_1 and C_2 charges from the source and in the transfer state (TS) the stored charge is transferred to the load as shown in Figure 5.2 referring to state 6 in Table 5.1. This mode is selected as a sample mode in the entire analysis for developing a theoretical framework for modelling. However, a similar approach can be taken to understand other VCRs in Table 5.1. The way in which the charge pump or flying capacitors are charged and later discharged is realized by intelligent control and configuration of the 9 switches.

Table 5.1: States of Operation and VCR for Targeted Output Voltage Along with Switching Sequence in Charge and Transfer States

State	VCR	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	D_1	D_2	D_3	D_4	D_5
1	$V_{in1} \times 2$	CSTS	-	TS	CS	TS	CS	-	-	CS	CSTS	-	CS	CS	TS
2	$V_{in2} \times 2$	-	CSTS	TS	CS	TS	CS	-	-	CS	-	CSTS	CS	CS	TS
3	$V_{in1} + V_{in2}$	CS	TS	TS	CS	TS	CS	-	-	CS	CS	TS	CS	-	TS
4	$V_{in2} \times 1.5$	-	CSTS	TS	CS	TS	TS	TS	CS	CS	-	CSTS	CS	CS	TS
5	$V_{in1} \times 1.5$	CSTS	-	TS	CS	TS	TS	TS	CS	CS	CSTS	-	CS	CS	TS
6	$V_{in2} + (V_{in1} \times 0.5)$	CS	TS	TS	CS	TS	TS	TS	CS	CS	CS	TS	CS	CS	TS
7	$V_{in1} + (V_{in2} \times 0.5)$	TS	CS	TS	CS	TS	TS	TS	CS	CS	TS	CS	CS	CS	TS
8	$V_{in1} \times 0.5$	CS	-	-	CS	TS	TS	TS	CS	CSTS	CS	-	CS	CS	TS
9	$V_{in2} \times 0.5$	-	CS	-	CS	TS	TS	TS	CS	CSTS	-	CS	CS	CS	TS
10	V_{in1}	CS	-	-	CS	TS	CSTS	-	-	CSTS	CS	-	CS	-	TS
11	V_{in2}	-	CS	-	CS	TS	CSTS	-	-	CSTS	-	CS	CS	-	TS
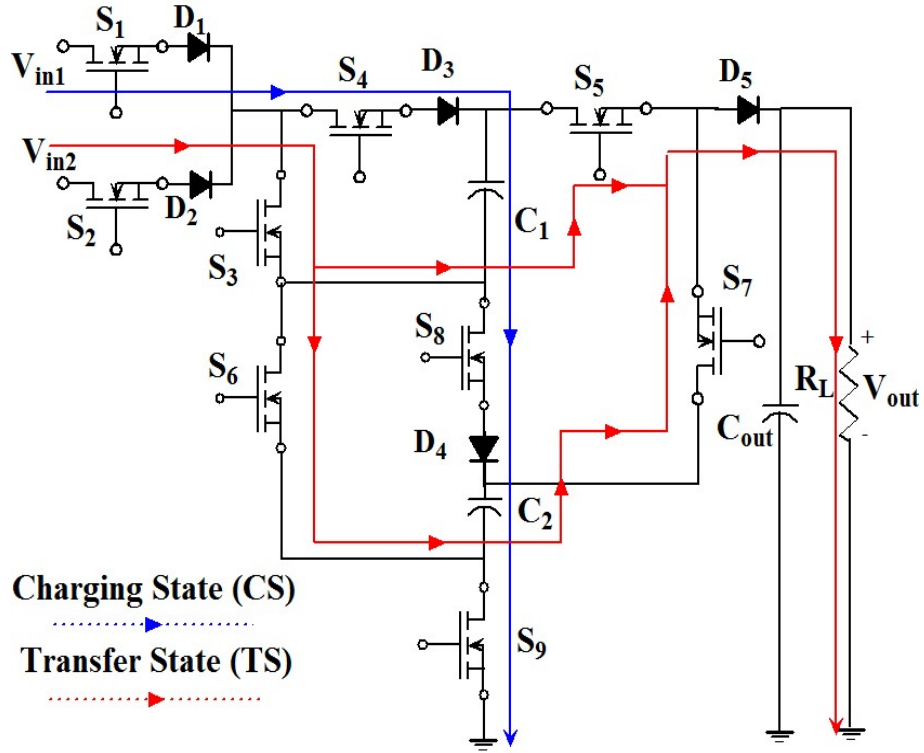
Figure 5.2: Circuit Topology of the Two Input Series - Parallel Buck - Boost based SCC Showing the Charging and Discharging Paths in State 6

5.3 Theoretical Considerations and Definitions

A SCC can be basically modeled as an ideal transformer with turns ratio 'n', the unloaded conversion ratio and R_{out} the equivalent converter resistance as shown in Figure 5.3. Here, V_{in} is the input voltage and V_{out} is the actual output voltage and V_s is the targeted secondary voltage after conversion, or no load output voltage and V_{diode} is the modeled diode losses. The same model has been introduced in Chapter 2 and Chapter 4. The equivalent circuit of the model shown in Figure 2.4 in Chapter 2 is correct without diodes in the circuit. Further, the mathematical modelling was incomplete in Chapter 4 and the advantages and disadvantages has been completely discussed in Section 4.6. The theoretical framework developed in this chapter for the derivation of a complete mathematical expression for R_{out} including diode losses forms the complete model hence is accurate as shown in Figure 5.3. The switches used in SC converters are usually MOSFETs that could be treated as the ON state resistance $R_{ds}(ON)$ during their conduction state that influences the output voltage and contributes to the conduction losses, which in turn affect the efficiency. Equivalent series resistance (ESR) of the

capacitors also adds to SCC conduction losses. Therefore the model has to take into account both switch resistances and capacitors ESR to determine the equivalent converter resistance. If voltage drop devices are used, such as diodes or IGBTs, the diode losses as a result of forward voltage drop needs to be included in the model.
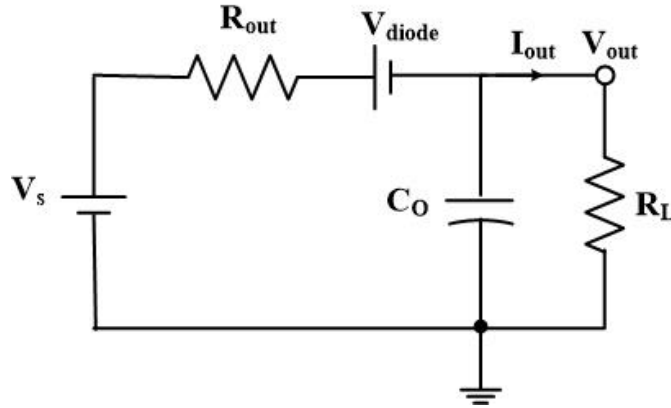
Figure 5.3: A SCC Complete Steady State Equivalent Circuit Model

A detailed discussion and insight about the influence of switch resistance on losses and efficiency of a SCC can be found in (Law *et al.*, 2005; Ioinovici *et al.*, 2006). In (Ioinovici *et al.*, 2006) the authors conclude that the switch resistance does not affect in the charging phase circuit efficiency but it does affect the transfer circuit efficiency. A detailed mathematical model presented in (Ben-Yaakov, 2012; Cheung *et al.*, 2010) illustrates how switch resistance and capacitor ESR take part in conduction losses and affect efficiency. The optimal switch resistance to meet a certain specification and the influence of switch resistance can be found in (Ben-Yaakov and Evzelman, 2012; Evzelman and Ben-Yaakov, 2013) . The efficiency of an SCC (Seeman, 2009; Evzelman and Ben-Yaakov, 2013) can be expressed by the Equation (5.1)

$$\eta = \frac{V_{out}}{n.V_{in}} = \frac{V_{out}}{V_s} \tag{5.1}$$

In the model proposed in (Evzelman and Ben-Yaakov, 2013), the conduction losses are expressed as the average current flowing through the charge pump capacitors in each switching phase. Here the sub circuits in charging and discharging phase of the charge pump capacitors are developed and approximated as first order RC network. The charging and discharging equivalent resistances determined along with diode losses are added to get the total converter equivalent resistance R_{out}.

5.4 Development of Equivalent Circuit and Analysis of the Proposed SC Converter

The model derivation is demonstrated on the SC converter in state 6 for a VCR of $V_{in2} + (V_{in1}\mathbf{x}0.5)$ utilizing both sources, but the general steps are the same for the other conversion ratios. In any operating phase "i" of the SCC corresponding to a time period "T_i", if the charging and discharging process is fully completed then the converter is operating in the CC (Complete Charge) state or SSL (Slow Switching Limit). Similarly if the charging and discharging is partially completed then it is operating in the PC (Partial Charging) state. Finally if the capacitor current is constant then it is operating in the NC (No charging) or FSL (Fast Switching Limit). The equivalent resistance of the sub circuit operating in any of the state NC, PC or CC is dependent on "T_i" and "R_iC_i", where "R_i" is the equivalent reduced resistance of all the participating switches, the flying capacitor ESR and "C_i" is the value of the equivalent capacitance in Farads corresponding to time period "T_i" during the "i^{th}" operating state defined as CS or TS in this work.

From Table 5.1, in state 6, switches S_1, S_4, S_8, S_9, D_1, D_3 and D_4 are conducting in the charging state (CS) and S_2, S_3, S_5, S_6, S_7, D_2 and D_5 conduct in the transfer state (TS). In Figure 5.2 the corresponding switches, diodes and flying capacitors participating in the charging state (CS) and transfer state (TS) are shown. Based on the SCC model in Figure 5.3, if the "R_{out}" or the equivalent series resistance can be found in both CS and TS states along with the diode voltage drops, then the output voltage across the load can be calculated. Equivalent circuit resistances "R_{CS}" and "R_{TS}" during CS and TS are developed and are shown in Figure 5.4. In Figure 5.5 the reduced equivalent circuit, which reduces the entire CS and TS modes to a first order RC circuit model is shown. Here, the on state resistances of the switches are denoted as S_nR_{on} where "n" denotes the switch participating in that state. The capacitor equivalent series resistance (ESR) is shown as R_{ESR1} or R_{ESR2} where 1 or 2 in the suffix denotes the flying capacitor 1 or 2 participating in that state.

Since the two states have different circuit structure, the proportionality factor "Φ_i" which is the ratio of the average sub circuit currents to the output current in each of the
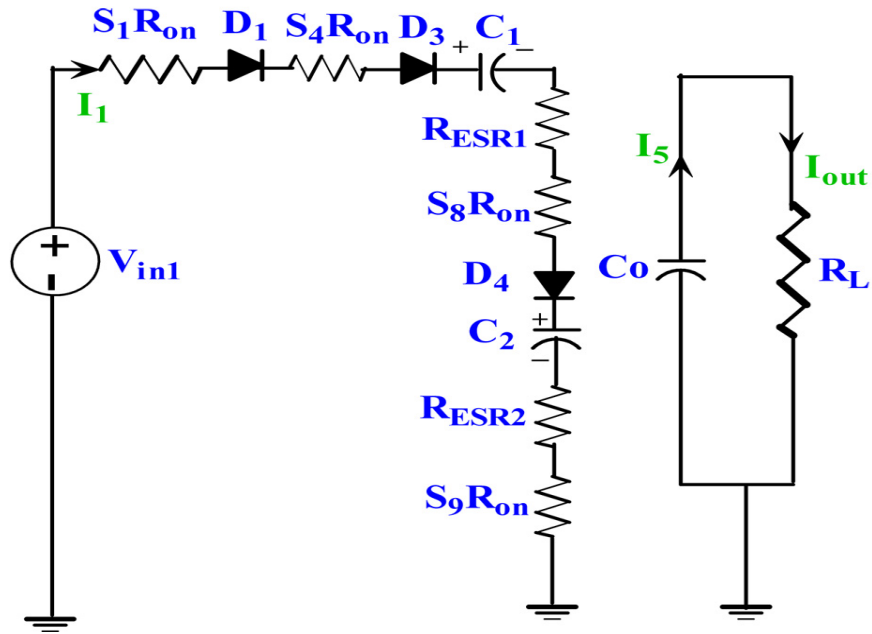
(a) Actual Equivalent Circuit in CS
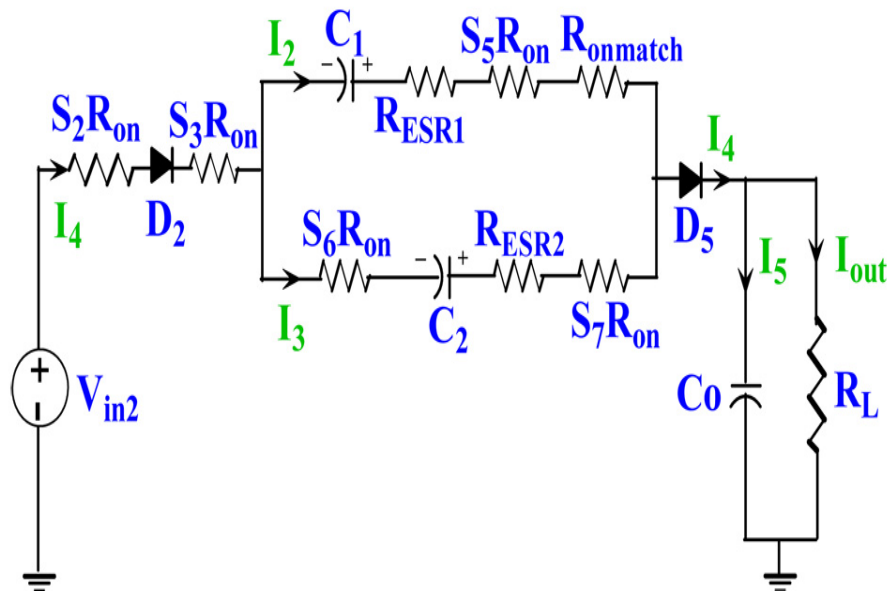
(b) Actual Equivalent Circuit in TS

Figure 5.4: Equivalent Circuits in State 6 for a VCR of $V_{in2} + (V_{in1}x0.5)$ in CS and TS Modes
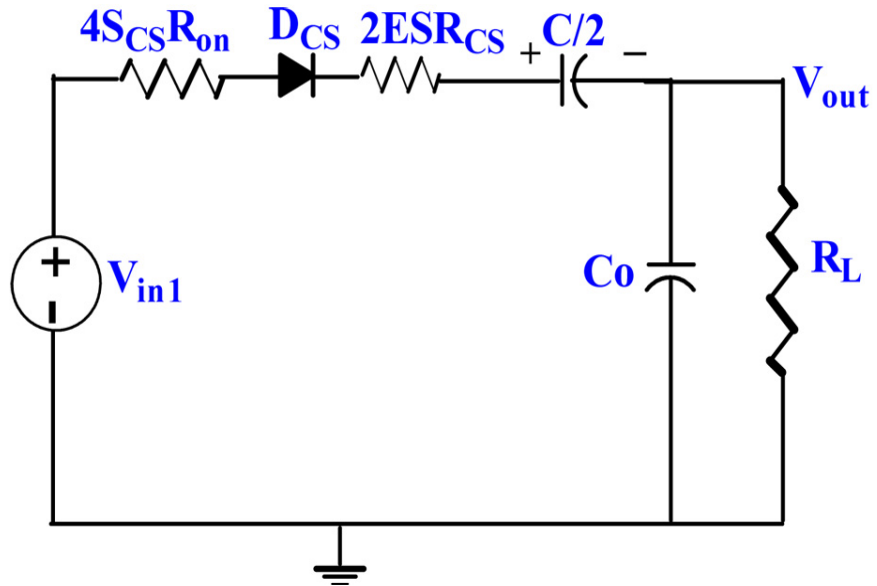
(a) Reduced Equivalent Circuit in CS
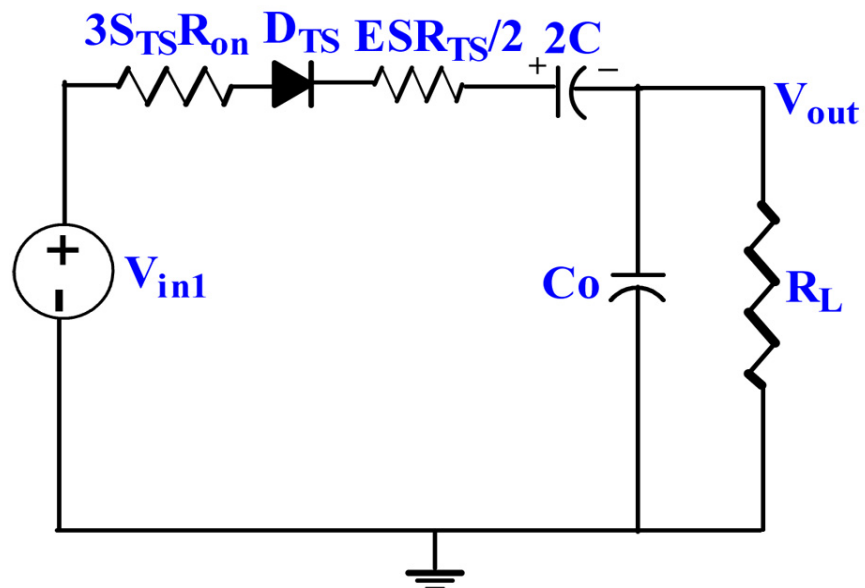
(b) Reduced Equivalent Circuit in TS

Figure 5.5: Reduced Equivalent Circuits in State 6 for a VCR of $V_{in2} + (V_{in1}\mathbf{x}0.5)$ in CS and TS Modes

"*i*" operational states, CS or TS in this work, is found by KCL. Diode conduction losses can be modeled as a voltage source V_{diode} which is equivalent to the average forward voltage drops of all the diodes in the circuit multiplied by the factor "Φ_i".

5.4.1 Analysis of First Order RC Circuits

A brief explanation on the model derivation based on first order RC approximation can be understood referring to Figure 5.6. At time "$t \geq 0$" the instantaneous value of the
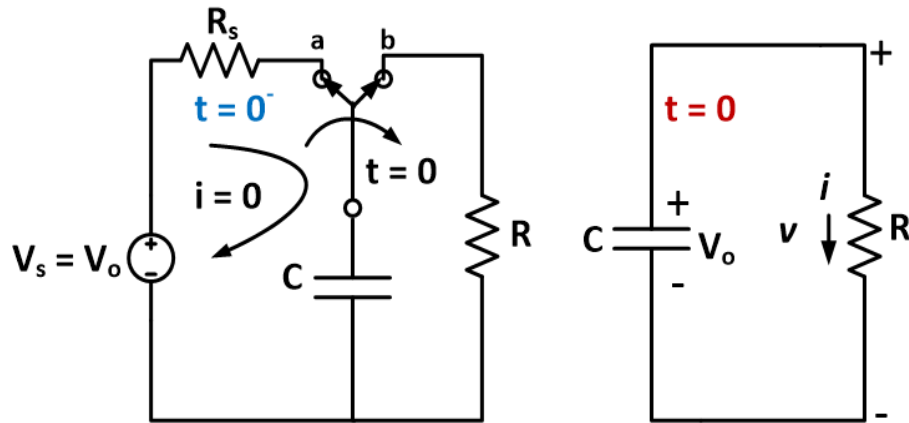
Figure 5.6: First Order RC Circuit Model

voltage can be written as shown in Equation 5.2.

$$v(t) = v(0^+)e^{-\frac{t}{RC}} = V_o e^{-\frac{t}{RC}} \tag{5.2}$$

As a next step the instantaneous current expression is derived as shown in Equation 5.3.

$$i(t) = \frac{v(t)}{R} = \frac{V_o}{R}e^{-\frac{t}{RC}} \tag{5.3}$$

Expression for the instantaneous power shown in Equation 5.4, is the product of voltage and current obtained from Equations 5.2 and 5.3. Multiplying with time gives the expression for energy consumed in the first order RC network, shown in Equation 5.5.

$$p(t) = v(t)i(t) = \frac{V_o^2}{R}e^{-\frac{2t}{RC}} \tag{5.4}$$

$$w(t) = \int_0^t p(t).d(t) = \frac{1}{2}CV_o^2(1 - e^{-\frac{2t}{RC}}) \tag{5.5}$$

From Equation 5.5, the expression for energy pertaining to the modeled R_{out} of Figure 5.3 can be obtained. Applying it to Figure 5.5, the energy expression for state 6 can be derived as Equation 5.6, considering the voltage across any flying capacitor is ΔV_i, where λ_i is the ratio $\frac{t}{RC}$.

$$W_{Routi} = \frac{1}{2} C_i \Delta V_i^2 (1 - e^{-2\lambda_i}) \tag{5.6}$$

From fundamentals the following Equations 5.7 and 5.8 can be written.

$$q_i = C_i \Delta V_i (1 - e^{-2\lambda_i}) \tag{5.7}$$

The average capacitor current I_{Cavi} expression is determined from Equation 5.7.

$$I_{Cavi} = \frac{q_i}{T_{CS} + T_{TS}} = q_i f_s \tag{5.8}$$

Equations 5.7 and 5.8 can be rearranged to obtain a relationship between the difference in voltage and the average capacitor current as shown in Equation 5.9.

$$\Delta V_i = \frac{I_{Cavi}}{f_s C_i (1 - e^{-2\lambda_i})} \tag{5.9}$$

Finally energy expression Equation 5.10, can be derived which helps in developing the equivalent resistance R_{out} to model the SCC shown in Figure 5.3.

$$W_{Routi} = I_{Cavi}^2 \cdot \frac{1}{f_s} \frac{1}{2 f_s C_i} \frac{(1 + e^{-2\lambda_i})}{(1 - e^{-2\lambda_i})} \tag{5.10}$$

5.4.2 Assumptions for Analyzing the Equivalent Circuits

The major assumptions made while analyzing the equivalent circuits are,

1. The parallel capacitors are treated as single capacitor reducing the sub circuits to a first order RC network in both CS and TS states.

2. The filter capacitor C_0 is having much larger values compared to the flying or charge pump capacitors.

3. A charge pump capacitor will participate in both CS and TS states.

4. The duty cycle of operation in CS and TS will be 50%.

5. The MOSFET switch on state resistance is the same for all the switches used and the charge pump capacitors have the same value of capacitance and ESR.

6. All the diodes used are identical, with identical forward voltage drop.

7. All eleven states in Table 5.1 correspond to operation of the SCC in hard switching case and both the input voltages V_{in1} and V_{in2} are assumed to be identical for simplicity of the analysis.

5.5 Model Derivation of the Proposed Converter

In a hard switched SCC, the equivalent resistance R_{outi} in the "i^{th}" operational state, CS or TS, can be derived based on the approximation that the circuit behaves like a first order RC circuit. Referring to Figure 5.5, in any operational phase "i" the current exhibits an exponential waveform. The power loss "P_{Routi}" as a function of average sub circuit capacitor current "I_{Cavi}" can be inferred from energy expression of Equation (5.10) and is given by,

$$P_{R_{outi}} = I_{C_{avi}}^2 \cdot \frac{1}{2 f_s C_i} \frac{(1 + e^{-\lambda_i})}{(1 - e^{-\lambda_i})} = I_{out}^2 \cdot \phi_i^2 \cdot \frac{1}{2 f_s C_i} \coth(\frac{\lambda_i}{2}) = I_{out}^2 R_{outi} \qquad (5.11)$$

Where "f_s" is the switching frequency, "C_i" is the flying capacitors or charge pump capacitors participating in that state and $\lambda_i = \frac{T_i}{R_i C_i}$. A proportionality factor "Φ_i", the ratio between the average sub circuits current "I_{Cavi}" and the average output current "I_{out}" in the steady state, connects between CS and TS states. This factor can be found by applying KCL referring to Figure 5.4.

The switching sub circuit in CS is shown in Figure 5.4a. Following the assumptions stated in Section 5.4.2, the sub circuit reduces to a first order RC circuit as shown in Figure 5.5a where the equivalent R_{CS} and C_{CS} is derived for the time period denoted as T_{CS}. Following the same assumptions, the sub circuit in TS of Figure 5.4b reduces to a first order RC circuit with the flying capacitors connected in parallel reduced to a single capacitance C_{TS} and equivalent resistances modeled into a single resistance R_{TS} for the

time period T_{TS} as shown in Figure 5.5b. Next Φ_i is calculated. Φ_i, is the proportionality factor that links the sub circuit currents I_1 and I_4 in Figures 5.4a and 5.4b respectively to the average output current I_{out}. Thus all the parameters in Equation (5.11) for CS and TS are found separately and added together to get the equivalent resistance. The diode conduction losses are modeled separately after obtaining R_{out}. Referring to Figures 5.4a and 5.4b the following equations are obtained. Applying charge balance for the flying capacitors C_1 and C_2 Equations (5.12) and (5.13) can be formulated.

$$I_1 - I_2 + 0I_3 + 0I_4 + 0I_5 = 0 \tag{5.12}$$

$$I_1 + 0I_2 - I_3 + 0I_4 + 0I_5 = 0 \tag{5.13}$$

Applying KCL at the nodes in the capacitor parallel path where currents I_2, I_3 meets and at node where I_4, I_5 and I_{out} meets in Figure 5.4b during TS, Equations (5.14) and (5.15) can be written.

$$0I_1 + I_2 + I_3 - I_4 + 0I_5 = 0 \tag{5.14}$$

$$0I_1 + 0I_2 + 0I_3 + I_4 - I_5 = I_{out} \tag{5.15}$$

During CS, the filter capacitor C_0 supplies the load current such that $I_5 = I_{out}$.

$$0I_1 + 0I_2 + 0I_3 + 0I_4 + I_5 = I_{out} \tag{5.16}$$

In matrix form, Equations (5.12) to (5.16) can be written as Equation (5.17). The proportionality coefficient can be calculated from Equation (5.17).

$$
\begin{bmatrix}
1 & -1 & 0 & 0 & 0 \\
1 & 0 & -1 & 0 & 0 \\
0 & 1 & 1 & -1 & 0 \\
0 & 0 & 0 & 1 & -1 \\
0 & 0 & 0 & 0 & 1
\end{bmatrix}
\begin{bmatrix}
I_1 \\
I_2 \\
I_3 \\
I_4 \\
I_5
\end{bmatrix}
=
\begin{bmatrix}
0 \\
0 \\
0 \\
I_{out} \\
I_{out}
\end{bmatrix}
\tag{5.17}
$$

$$\phi_{CS} = \frac{I_1}{I_{out}} = \frac{I_{out}}{I_{out}} = 1 \qquad (5.18)$$

$$\phi_{TS} = \frac{I_4}{I_{out}} = \frac{2I_{out}}{I_{out}} = 2 \qquad (5.19)$$

The proportionality factor $\phi_{CS} = 1$ and $\phi_{TS} = 2$ obtained above is by considering the instantaneous values of current and to get the average current since, $T_i = T_{CS} = T_{TS} = 0.5$, Equations (5.18) and (5.19) has to be divided for half cycle. Therefore,

$$\phi_{CS} = \frac{1}{2} \qquad (5.20)$$

$$\phi_{TS} = 1 \qquad (5.21)$$

From Figure 5.5a, the equivalent resistance R_{CS} and equivalent capacitance C_{CS} during charging state (CS) are given by Equations (5.22) and (5.23),

$$R_{CS} = 4S_{cs}Ron + 2ESR_{CS} \qquad (5.22)$$

$$C_{CS} = \frac{C}{2} \qquad (5.23)$$

From Figure 5.5b, the equivalent resistance R_{TS} and equivalent capacitance C_{TS} during transfer state (TS) are given by Equations (5.24) and (5.25),

$$R_{TS} = 3S_{Ts}Ron + \frac{ESR_{TS}}{2} \qquad (5.24)$$

$$C_{TS} = \frac{2C.C_0}{2C + C_0} \qquad (5.25)$$

If T_{CS} and T_{TS} are the time period during the charging state and transfer state, then,

$$\lambda_{CS} = \frac{T_{CS}}{R_{CS}C_{CS}} = \frac{T_{CS}}{(4S_{cs}Ron + 2ESR_{CS}).(\frac{C}{2})} \qquad (5.26)$$

$$\lambda_{TS} = \frac{T_{TS}}{R_{TS}C_{TS}} = \frac{T_{TS}}{(3S_{Ts}Ron + \frac{ESR_{TS}}{2}).(\frac{2C.C_0}{2C+C_0})} \qquad (5.27)$$

From Equation (5.11),

$$R_{outCS} = \phi_{CS}^2 . \frac{1}{2f_sC_{CS}} \coth(\frac{\lambda_{CS}}{2}) = (\frac{1}{2})^2 . \frac{1}{2.f_s.\frac{C}{2}} . \coth(\frac{\lambda_{CS}}{2}) \qquad (5.28)$$

$$R_{outTS} = \phi_{TS}^2 . \frac{1}{2f_sC_{TS}} \coth(\frac{\lambda_{TS}}{2}) = (1)^2 . \frac{1}{2.f_s.(\frac{2C.C_0}{2C+C_0})} . \coth(\frac{\lambda_{TS}}{2}) \qquad (5.29)$$

Hence the equivalent R$_{out}$ of the converter to be modeled as in Figure 5.3 combining Equations (5.28) and (5.29) is,

$$R_{out} = R_{outCS} + R_{outTS}$$

$$R_{out} = \frac{1}{4.f_s.C} \coth(\frac{\lambda_{CS}}{2}) + \frac{1}{2.f_s.(\frac{2C.C_0}{2C+C_0})} . \coth(\frac{\lambda_{TS}}{2}) \qquad (5.30)$$

Following the assumption that $C_0 >> C$, Equation (5.30) can be approximated to,

$$R_{out} = \frac{1}{4.f_s.C} \left[\coth(\frac{\lambda_{CS}}{2}) + \coth(\frac{\lambda_{TS}}{2}) \right] \qquad (5.31)$$

For the state 6 corresponding to a VCR of V$_{in2}$ + (V$_{in1}$x0.5) in Table 5.1, which is typically a summation of second source with a buck mode of first source, the SCC model for R$_{out}$ is governed by Equation (5.31). A similar analysis can be followed to find the R$_{out}$ for all remaining states and VCRs. Diode conduction losses are modeled using the basic average equivalent circuit of Figure 5.3, but an equivalent diode voltage drop source, V$_{diode}$ is included. Total average voltage drop V$_{diodeCS}$ can be expressed as,

$$V_{diodeCS} = \phi_{CS}.V_{fdCS}.N_{CS} \qquad (5.32)$$

where, V_{fdCS} is the average forward voltage drop of each diode, and N_{CS} is the number of conducting diodes, D_1, D_3 and D_4 in this case as shown in Figure 5.4a. In the same manner during TS interval in Figure 5.4b,

$$V_{diodeTS} = \phi_{TS}.V_{fdTS}.N_{TS} \tag{5.33}$$

The equivalent diode conduction losses considering both CS and TS are,

$$V_{diode} = V_{diodeCS} + V_{diodeTS} \tag{5.34}$$

Using Equations (5.31) and (5.34), R_{out} and V_{diode} are calculated to finalize the model.

5.6 Discussion on Modelled, Simulated and Experimental Results

Simulations and experimental validation against the model derived output voltage values of the proposed converter in state 6 for different frequencies is presented in this section. PSIM software has been used for simulating the circuit. The parameters of the circuit used in the model, simulation trials, and experimental results are as follows. The switches S_1-S_9 used in this work for theoretical modelling, simulation and hardware referring to in Figure 5.2 are of MOSFET type manufactured by International Rectifier IRLIZ34NPbF with $R_{DS(ON)}$= 35 mΩ. To prevent unwanted conduction in the reverse direction of MOSFET's body diode, additional Schottky barrier diodes D_1-D_5 of Good - Ark 1N5817 with V_{DC} = 20 V, I_{AV} = 1 A are used. From manufacturer's data sheet an average forward voltage drop of the 1N5817 is taken as 0.3 V. The flying capacitor or charge pump capacitors C_1 and C_2 are manufactured by Keltron, rated 35 V, 22 μF with an ESR of 100 mΩ. The filter capacitor C_0 is taken as 220 μF. The load resistance R_L is taken as 68 Ω for a load current ranging between 100 mA to 150 mA at a voltage level of 7 V to 9 V. Three frequencies of 5 kHz, 27 kHz and 94 kHz with a duty cycle of 50% are evaluated.

5.6.1 Experimental Setup and Gating Circuit Specifications

The experimental setup for validation of the results is shown in Figure 5.7. The heart of the converter is the SCC board which has 9 MOSFET switches and 5 diodes. The DSPIC30F3011 generates the required sequence of gating pulse as per the selected VCRs. There is a power supply unit that supplies the required gate source voltage across the MOSFET switches to turn ON. DSPIC30F3011 is a 16 bit high perfor-
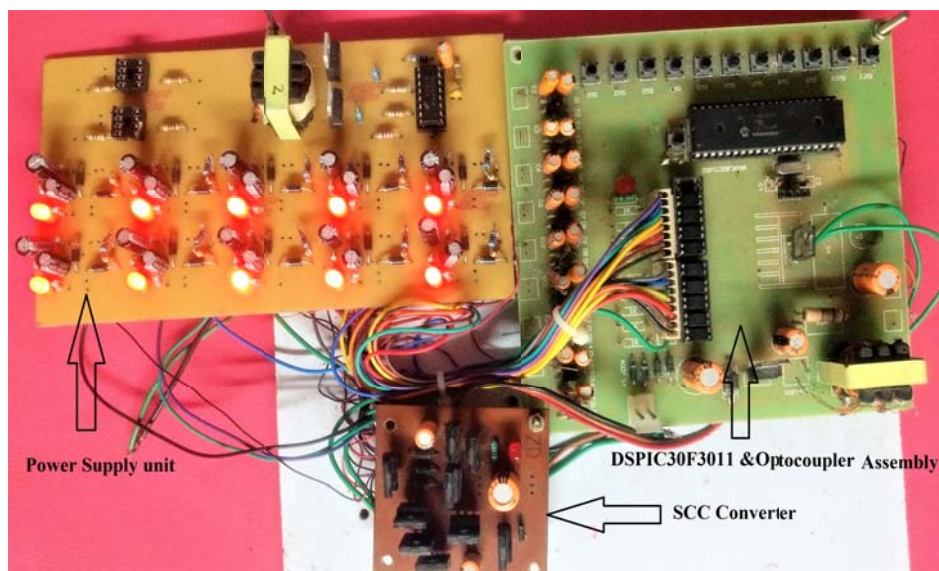
Figure 5.7: Hardware Setup of the Proposed Converter

mance digital signal controller. A detailed documentation can be found in (Microchip, 2010). The layout developed in DIPTRACE software to explain the utilization of pins of DISPIC30F3011 is shown in Figure 5.8. Pin RE0 to RE5 and RF0 TO RF4 are allocated for the mode selection switch to select the required VCRs out of the 11 presented states in Table 5.1. Pins RD2, RD0, RF6 and RF5 are reserved for frequency selection of 27 kHz, 50 kHz, 94 kHz and 100 kHz. Frequency 5 kHz is the default selection in the mode selection. All V_{ss} pins are reserved for ground and V_{dd} pins are the input supply power to the DSPIC given through a 7805 regulator. Pins 13 and 14 are for the crystal oscillator working at 20 MHz frequency. A 5 MHz clock is used here. Pins RB0 to RB8 are the output pulses generated by the controller which is the input to the optocouplers PC 817 to produce isolated gating pulses. The power supply details is shown in Figure 5.9. The output from optocoupler is connected to the gating input of the MOSFET switches fed through an SMPS oscillator at 9 V. The 9 V is generated through a 12-0-12 V transformer as shown in Figure 5.9. LED indicators are given for easy identification. The PIC program is written using MPLAB IDE assembly language.
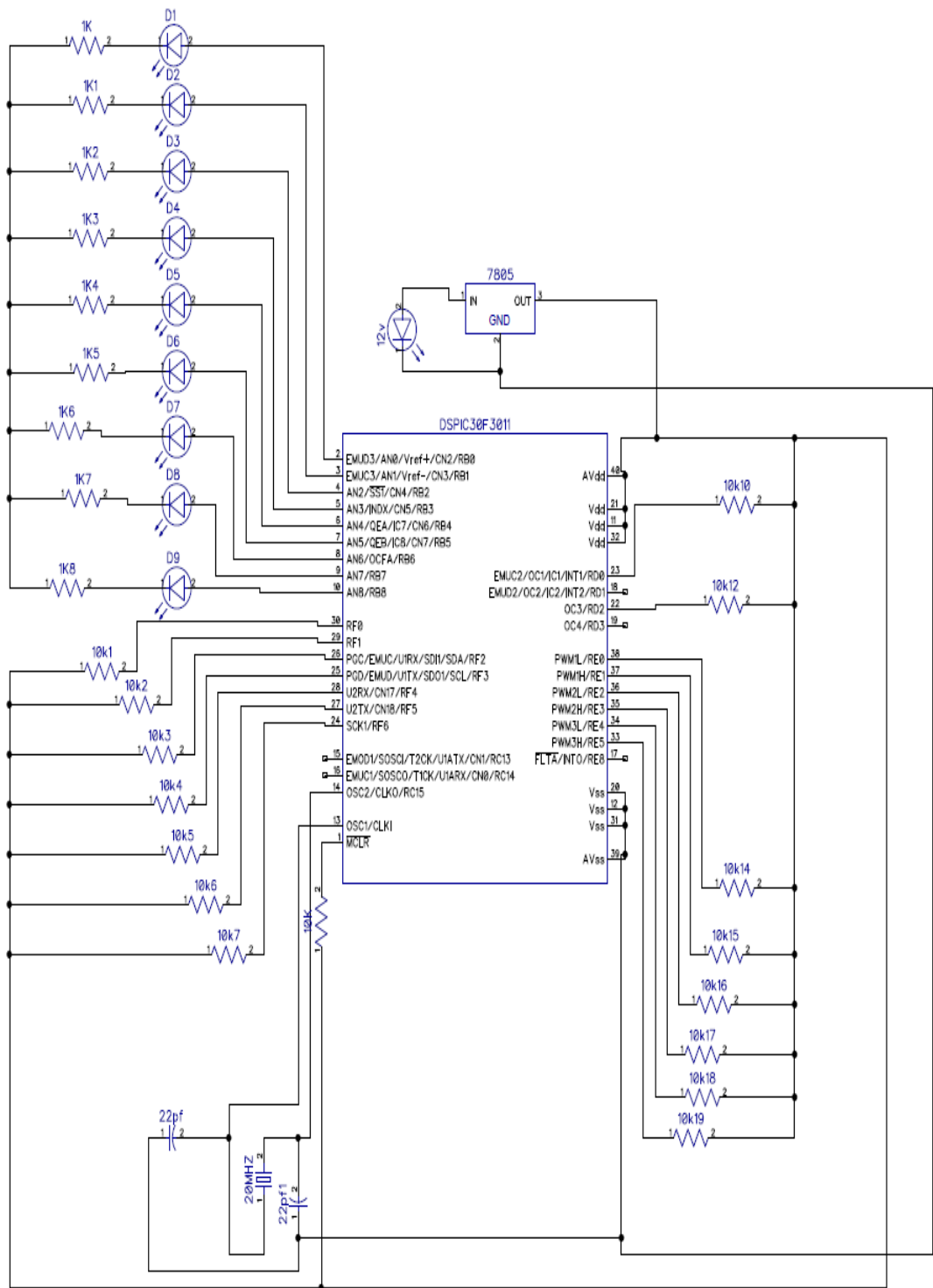
Figure 5.8: DIPTRACE Layout of DSPIC30F3011
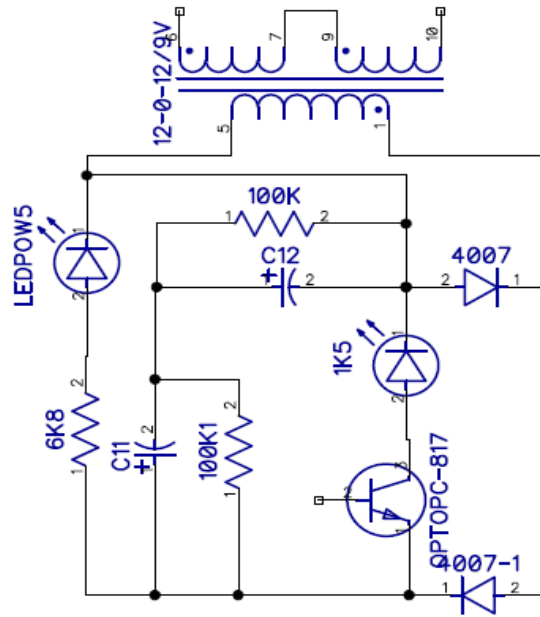
Figure 5.9: DIPTRACE Layout of Power Supply Unit

5.6.2 Analysis of Flying Capacitor Current Waveforms

The concept of Complete Charge (CC), Partial Charge (PC) and No Charge (NC) boundaries gives a thorough understanding of the flying capacitor transition states and behavior. This analysis is derived from the basic circuit theory concept of approximating the SCC circuit in any operating phase to a first order RC circuit. This technique is used to completely model and analyze the converter discussed here. The CC and PC corresponds to Fast switching Limit (FSL) and Slow Switching Limit Impedance (SSL) given in (Seeman, 2009). The general case considered is state 6, where the conversion ratio is $V_{in2} + 0.5V_{in1}$ for explanation through out this chapter and the same procedure can be applied for all other VCRs. The input voltage of both sources V_{in1} and V_{in2} are assumed to be both 6 V. The simulation model rigged in PSIM is run and the capacitor current waveform transition for different frequencies are observed. The flying capacitor instantaneous current waveform shown in Figure 5.10 is the anticipated current pattern when converter operates at 5 kHz, 27 kHz and 94 kHz, in CC, PC and NC modes respectively.
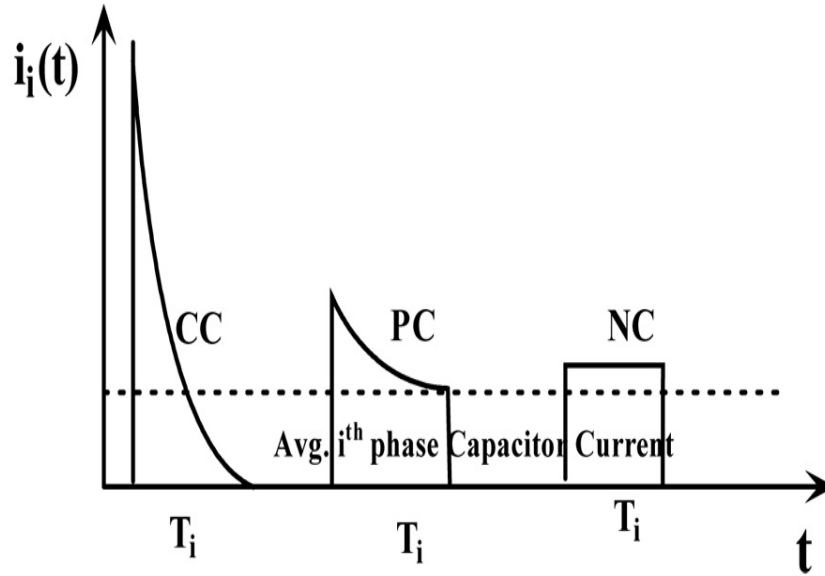
Figure 5.10: Instantaneous Flying Capacitor Current Waveform in CC, PC and NC Operating States

The value of λ_i sets the operation of the converter between CC, PC and NC modes. Figure 5.11a is the simulated waveform of flying capacitor current (I_{c1}) through C_1 corresponding to a frequency of 5 kHz. This mode corresponds to the complete charging (CC) or slow switching limit (SSL). The waveform is exponential in nature and this is because $\lambda_i \gg 1$, $T_i \gg R_{outi}C_i$. λ_i is a function of R_{outi} the switch resistance and it has no influence in this mode. This can be verified from Equation (5.11) by approximating R_{outi} to zero. In partial charge (PC) case which is an intermediate switching frequency of 27 kHz the switch resistance does influence the results, and the waveform (I_{c1}) is presented in Figure 5.11b. When $\lambda_i \ll 1$, $T_i \ll R_{outi}C_i$, the converter operation shifts to the no charging (NC) mode or fast switching limit (FSL) when the frequency is selected as 94 kHz. Here the charge pump capacitor voltage is nearly constant and the I_{c1} waveform is shown in Figure 5.11c. It can be concluded that for large values of λ_i, in CC mode, the converter equivalent resistance R_{outi} increases linearly with λ_i as $R_{outi} \propto (\frac{1}{f_S C_i})$ from Equation (5.11). This is due to the fact that the switching frequency selected is 5 kHz and therefore the switching time is greater than the time constant of the sub circuit operation phase defined as large λ_i. In PC mode the switching frequency is selected as 27 kHz and 94 kHz in NC both much higher than CC case. This corresponds to small λ_i or the switching time period is much smaller than the time constant of the sub circuit operation phase. R_{outi} is constant in this region and switch resistance does influence the losses and efficiency. Experimental verification of capacitor current waveforms in
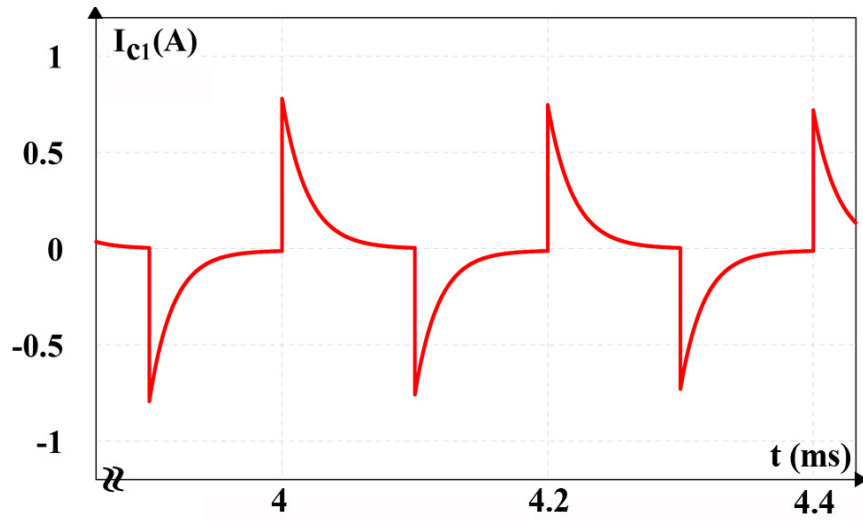
(a) Frequency 5 kHz CC Mode
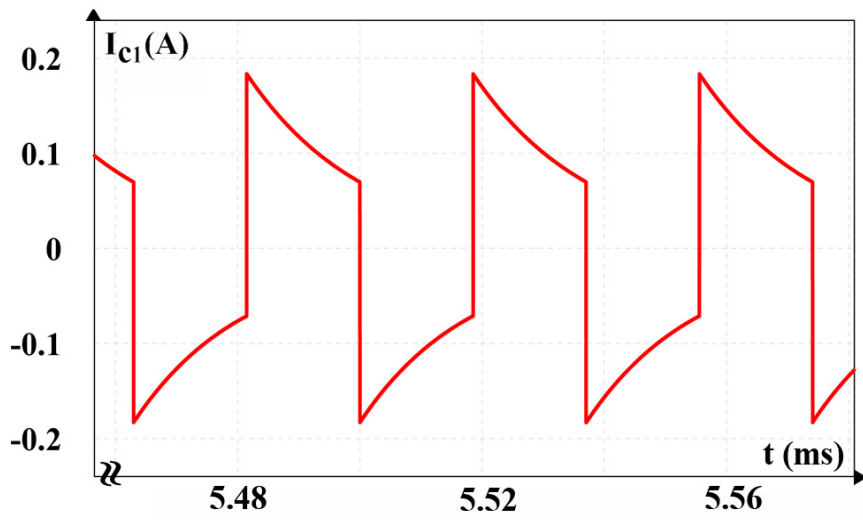
(b) Frequency 27 kHz PC Mode
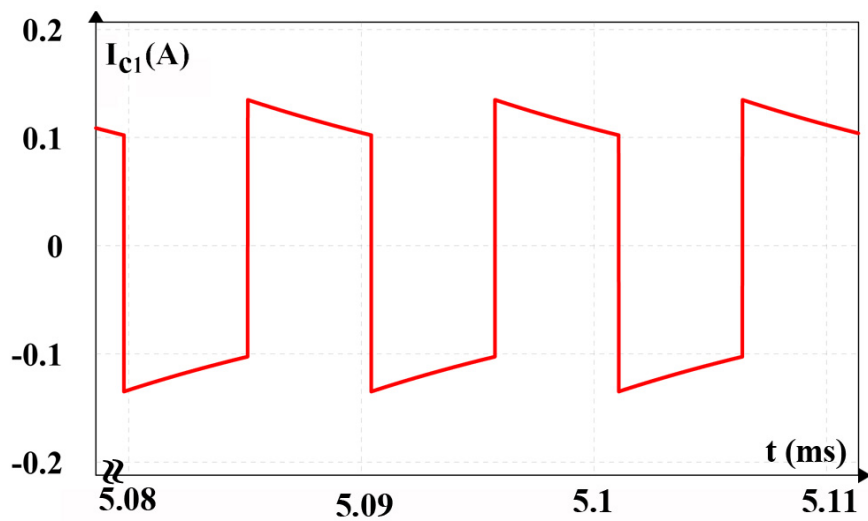
(c) Frequency 94 kHz NC Mode

Figure 5.11: Instantaneous, Expected and Simulated Flying Capacitor Current (I_{C1}) Waveform in State 6

92

CC, PC and NC modes validating simulated results are shown in Figure 5.12 and are in a good agreement. As expected from the simulated and experimental waveforms, the peak capacitor current in all the modes CC, PC and NC decrease respectively when switching frequency increases.

5.6.3   Experimental Verification and Validation of Results

The converter output voltage V_{out} and its waveform are analysed in a next step. The expected model derived R_{out} from Equation (5.31) and diode conduction loss V_{diode} from Equation(5.34) is calculated and applying KVL in Figure 5.3 and including the diode drop the equivalent circuit is developed. Selecting the values for MOSFET switch resistance, flying capacitor, filter capacitor and diodes as specified earlier, the different parameters defined in Equations (5.11) to (5.34) are calculated and are shown in Table 5.2, for the three frequency ranges.   The most significant part in modelling of the

Table 5.2: Model Derived Parameter Values For Selected Three Frequency Ranges

f_s kHz	λ_{CS}	λ_{TS}	R_{outCS} Ω	R_{outTS} Ω	R_{out} Ω	$V_{diodeCS}$ V	$V_{diodeTS}$ V	V_{diode} V	V_{out} V	η %
5	26.73	14.6	2.272	2.272	4.54	0.45	0.6	1.05	7.45	82.8
27	4.949	2.71	0.427	0.753	1.18	0.45	0.6	1.05	7.82	86.9
94	1.422	0.78	0.197	0.325	0.52	0.45	0.6	1.05	7.9	87.8

converter is to find out the equivalent converter output resistance R_{out} and the diode voltage drop V_{diode}. Once these values are calculated the actual output voltage V_{out} can be accurately determined for a particular load. Referring to, Table 5.2 and Figure 5.13a, for a switching frequency of 5 kHz, V_{out} is derived as 7.45 V. The input voltage and load resistance are 6 V and 68 Ω respectively. The model derived and simulated values with V_{out} mean and the ripple pattern are shown in Figure 5.13 for 5 kHz, 27 kHz and 94 kHz. Similarly Figure 5.14 shows the experimental mean output voltage V_{out} with its ripple. The ripple in the output voltage V_{out} in simulation of Figure 5.13 is compared with experimental results of Figure 5.14. It is seen to be in the range of 20 mV - 80 mV and lower output voltage ripple is observed as frequency increases. From Equation (5.1) model derived efficiency of the converter is 82.8% at 5 kHz, 86.9% at
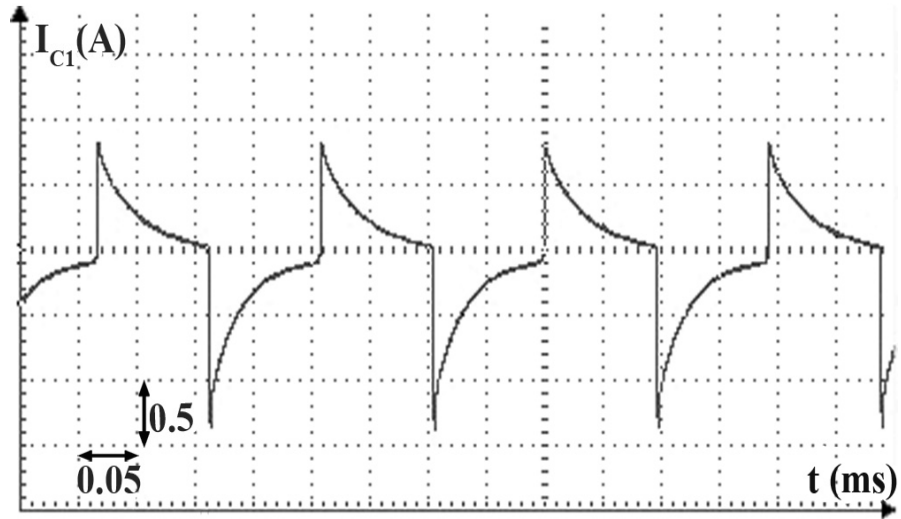
(a) Frequency 5 kHz CC Mode
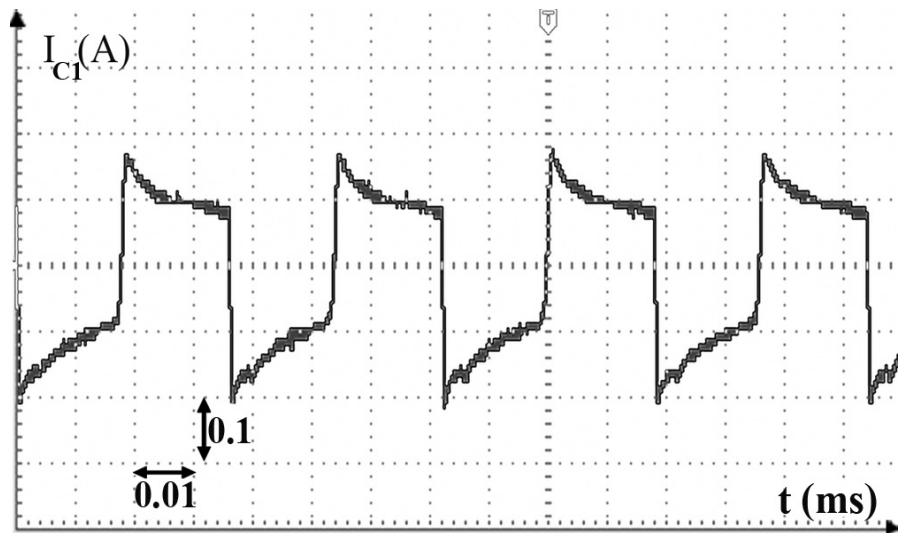
(b) Frequency 27 kHz PC Mode
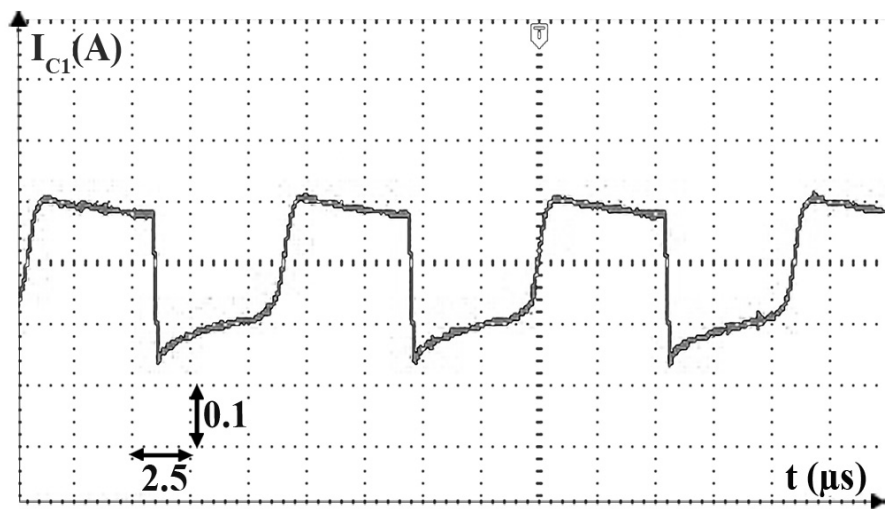
(c) Frequency 94 kHz PC Mode

Figure 5.12: Experimental Flying Capacitor Current (I_{c1}) Waveform in State 6
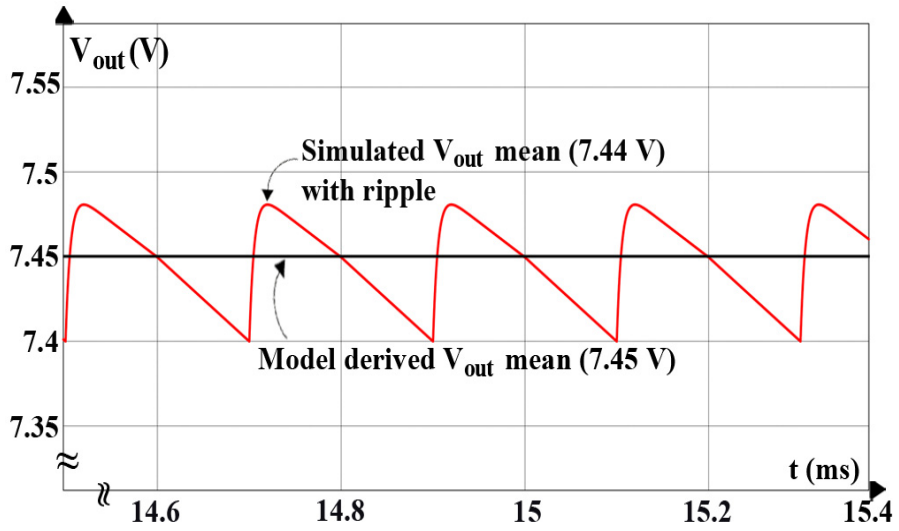
(a) Model and Simulated V_{out} at Frequency 5 kHz
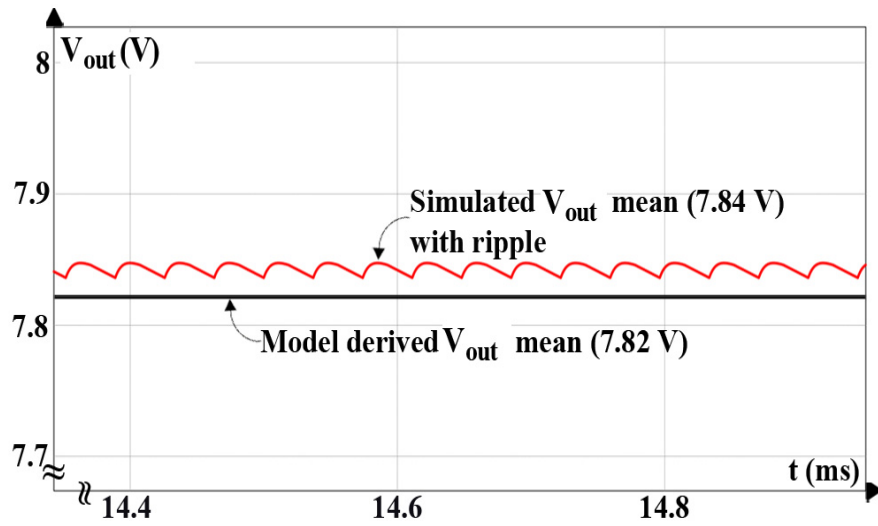
(b) Model and Simulated V_{out} at Frequency 27 kHz
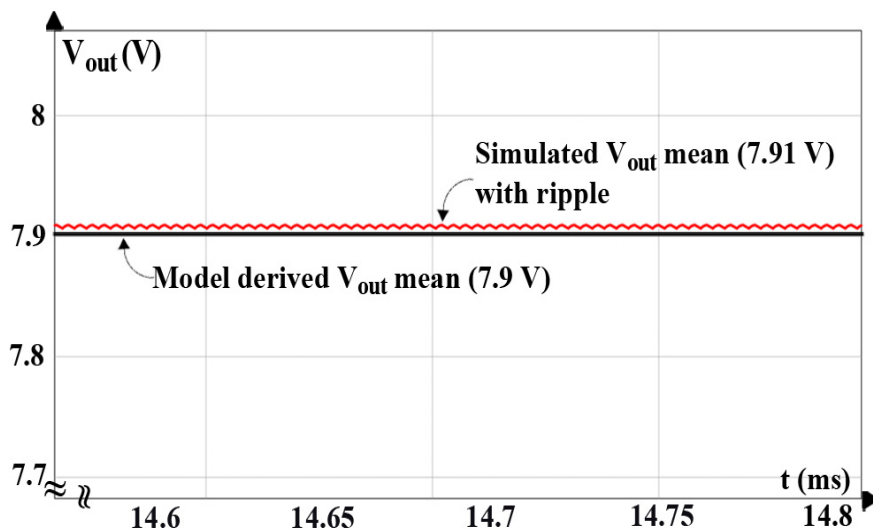
(c) Model and Simulated V_{out} at Frequency 94 kHz

Figure 5.13: Model Derived and Simulated Output Voltage (V_{out}) Waveform for State 6
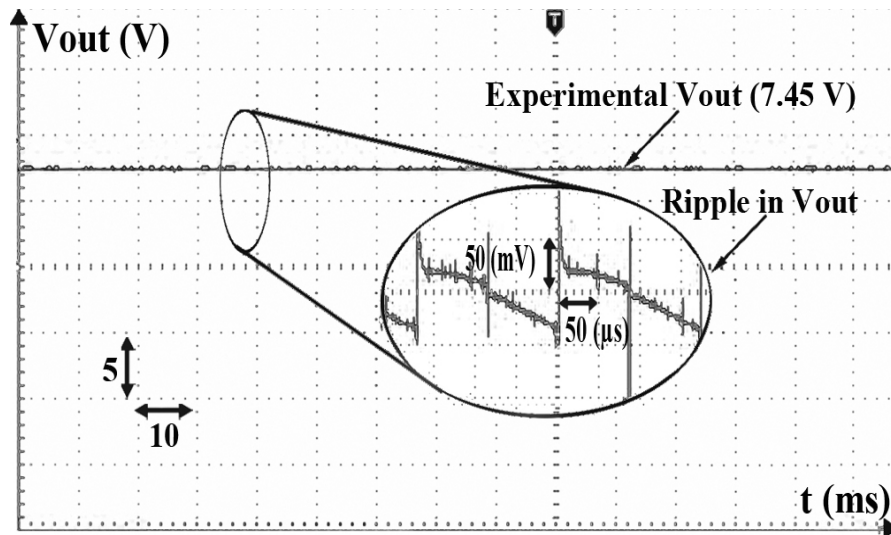
(a) Frequency 5 kHz
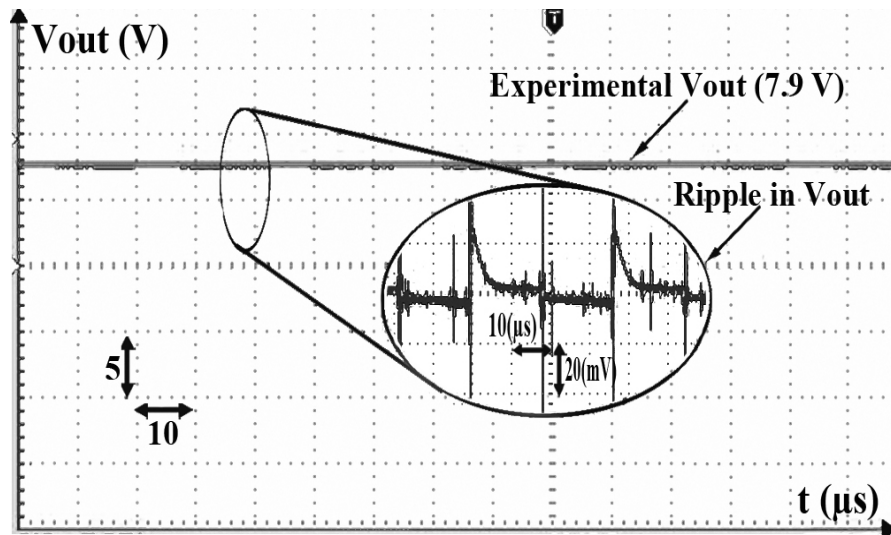
(b) Frequency 27 kHz
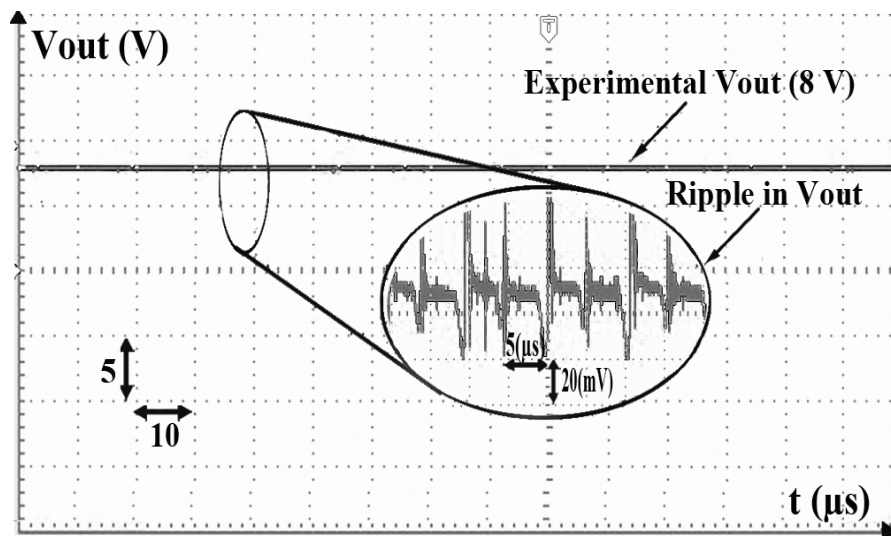
(c) Frequency 94 kHz

Figure 5.14: Experimental Mean Output Voltage Waveform for State 6 with Ripple in
         (V_{out})

27 kHz and 87.8% at 94 kHz. The model derived, simulated, experimental V_{out} values and efficiency are compiled in Table 5.3 for V_{in1} and V_{in2} of 6 V, V_S of 9 V and R_L of 68 Ω. It can be seen that there is close agreement between the modeled, simulated and experimental output voltage. Thus efficiency of the converter increases and ripple in the output voltage decreases when switching frequency is high. The losses associated with gate drives are not included in this analysis.

Table 5.3: V_{out} Comparison Between Model Derived, Simulated, Experimental and Efficiency (η) in State 6 for Different Frequencies

f_s (kHz)	V_{out} (V)			η (%)		
	Model	Simulated	Experimental	Model	Simulated	Experimental
5	7.45	7.44	7.45	82.8	82.7	82.8
27	7.82	7.84	7.9	86.9	87.1	87.8
94	7.9	7.91	8.0	87.8	88.0	88.9

The load resistance used in the experiment is 68 Ω and for an experimental measured output voltage V_{out} of 7.45 V at 5 kHz, the load current I_{out} = 109.5 mA. The ideal anticipated output voltage V_s for state 6 is 9 V. The difference between V_s and sum of measured output voltage (7.45 V) and V_{diode} (total practical average diode voltage drop of 1.05 V) divided by I_{out} results in R_{out} of 4.57 Ω. Similarly V_{out} has been obtained as 7.6 V and 7.28 V with R_L 100 Ω and 50 Ω. R_{out} has been found to be 4.6 Ω in both cases. The average experimental R_{out} is calculated as 4.59 Ω against the model derived R_{out} of 4.54 Ω. Slightly higher experimental R_{out} can be attributed to the varying practical total forward voltage drop across the diodes in experiments versus the theoretical average voltage drop taken directly from the data sheet for model derivation.

State 1 (First source only), state 3 (both the sources) and state 4 (second source only) has been simulated at 'f_s'of 100 kHz to verify the output. In this case, the two input sources are selected with V_{in1} and V_{in2} being 6 V and 9 V respectively. The average values of the output voltage in all the three states are presented in Figure 5.15. In Figure 5.15a for State 1(V_{in1}x2) the output voltage V_{out} is found to be 10.62 V. Similarly for

State 3 ($V_{in1}+V_{in2}$) and State 4 (V_{in2}x1.5) V_{out} is 13.6 V and 12.4 V respectively. The simulated results presented in Figure 5.15 are compiled in Table 5.4. It can also be

Table 5.4: Summary of Simulated V_{out} for Three Independent States

State	VCR	V_{in1} (V)	V_{in2} (V)	V_{out}(V)
1	V_{in1}x2	6	0	10.62
3	$V_{in1} + V_{in2}$	6	9	13.6
4	V_{in2}x1.5	0	9	12.4

inferred from Equation (5.31) that when a variable switching frequency control is used R_{out} changes and this technique can be applied for converter regulation and extension of output voltage range which is referred to as Pulse Frequency Modulation.

The model parameters calculated for other states and VCRs in Table 5.1 are compiled and presented in Table 5.5. The same frequencies 5 kHz, 27 kHz and 94 kHz are selected for calculation. Once the R_{out} values are known and by adding the diode drops the model can be completely developed for all VCRs.

Table 5.6 summarizes a comparison of the number of switches, flying capacitors and output VCRs used in this work with the state of the art SCC topologies. The converter presented in this work can give 11 VCRs and features the ability to operate off two sources, utilizing both simultaneously, or separately as demanded by the application. Further, the number of switches and flying capacitors used is also competitive ensuring less circuit space with flexibility of more VCRs.

5.7   Conclusion

A new two input series parallel topology switched capacitor converter is presented in this chapter. The converter has a simple topology, uses no magnetic elements, yet robust enough to deliver eleven voltage conversion ratios when two sources are used. One potential application is a simultaneous interface to both renewable energy source and energy storage component, for example solar panel and battery. The converter is analyzed and modeled to derive and predict the exact output voltage based on the
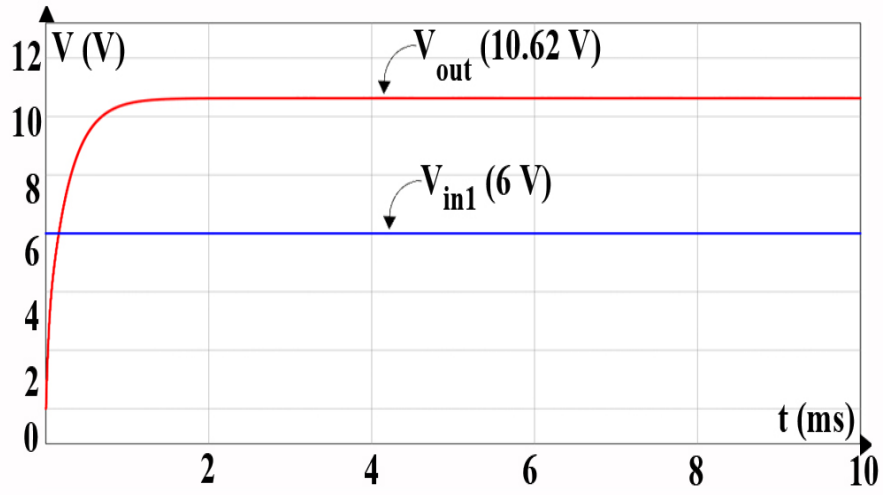
(a) State 1(V_{in1}x2)
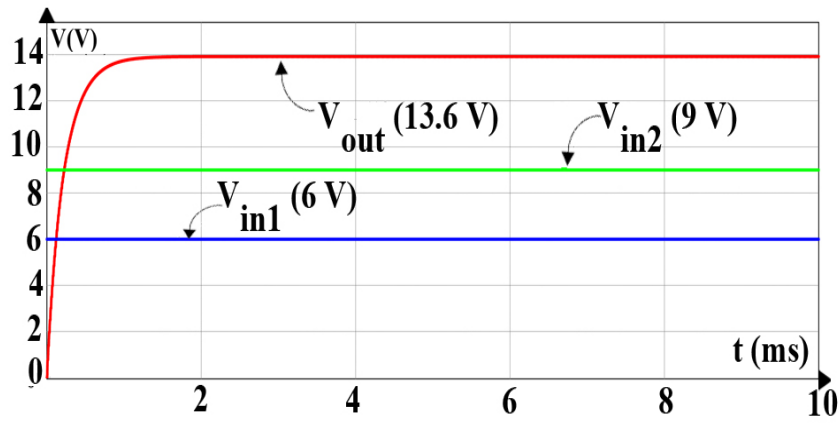
(b) State 3(V_{in1}+ V_{in2})

(c) State 4(V_{in2}x1.5)

Figure 5.15: Simulated Output Voltage and Input Voltage for State 1, 3 and 4 at 100 kHz

Table 5.5: Parameter Calculation for All VCRs

State	f_s(kHz)	λ_{CS}	λ_{TS}	$R_{outCS}\,\Omega$	$R_{outTS}\,\Omega$	$R_{out}\,\Omega$
1 or 2 $\phi_{CS} = 1, \phi_{TS} = 1$	5	44.34	26.73	1.143	2.27	3.4
	27	8.21	4.95	0.21	0.42	0.63
	94	2.35	1.42	0.07	0.19	0.27
3 $\phi_{CS} = 1, \phi_{TS} = 1$	5	37.87	44.34	4.54	4.54	9.09
	27	7.014	8.21	0.84	0.84	1.68
	94	1.95	2.28	0.31	0.28	0.59
4 or 5 $\phi_{CS} = 0.5, \phi_{TS} = 1$	5	59.6	37.8	2.27	2.27	4.5
	27	11.03	7	0.42	0.42	0.84
	94	3.17	2.01	0.13	0.15	0.28
6 or 7 $\phi_{CS} = 0.5, \phi_{TS} = 1$	5	26.7	14.6	2.2	2.2	4.54
	27	4.94	2.71	0.42	0.75	1.18
	94	1.42	0.78	0.19	0.32	0.52
8 or 9 $\phi_{CS} = 0.5, \phi_{TS} = 1$	5	53.47	37.87	2.27	2.27	4.54
	27	9.9	7.014	0.42	0.42	0.84
	94	2.75	1.95	0.13	0.15	0.28
10 or 11 $\phi_{CS} = 1, \phi_{TS} = 1$	5	37.87	44.34	1.13	4.54	5.68
	27	7.01	8.21	0.21	0.84	1.05
	94	1.95	2.28	0.07	0.28	0.36

Table 5.6: Comparison of Some Existing SCC Topologies

Converter Type	No. of switches and sources used	No. of flying capacitors	No. of output voltage states	Ratings	Efficiency @ Arbitrary VCR
(Le, 2015)	15 Single source reconfigurable	4	2	250 mA @ 1 V	> 74%
(Yuanmao and Cheng, 2012)	4 Two sources non reconfigurable	1	1	120 mA @ 36 V	> 90%
(Max1910, 2004)	7 Single source non reconfigurable	2	2	120 mA @ 5.4 V	>70%
This Work	14 Two sources reconfigurable	2	11	120 mA @ 9 V	> 85%

equivalent resistance and diode voltage drop. The simulated and experimental values are in good agreement with theoretical predictions. In the next chapter, extension of more VCRs and CMOS implementation potential is explored. An application of the proposed converter to power white LEDs is also verified.

CHAPTER 6

CMOS IMPLEMENTATION WITH EXTENDED VCRs AND AN APPLICATION TO POWER WHITE LEDs USING MOSFETS

The converter proposed in Chapter 5 was capable of generating 11 VCRs. In this chapter, possibility of obtaining additional VCRs is explored and 4 more VCRs are proposed which include an inversion mode. The circuit prototype is rigged using CMOS switches and simulation, modeled and hardware results are compiled. It can be seen that the efficiency increases considerably. Furthermore, an application of the proposed multiple input variable output buck boost based series - parallel SCC capable of powering a string of LED's is also presented in this chapter using MOSFET switches. The proposed converter offers the additive combinations of solar energy and battery source or stepped - up voltages converting either of sources to drive the LEDs. Eleven gain modes of operation are achieved by the circuit operating with only 9 switches, 5 diodes, 2 flying capacitors and one filter capacitor as discussed in Chapter 5. The power is shared between two sources depending on availability of solar source. The voltage of solar source is sensed using a voltage sensor and accordingly the required mode is automatically triggered to provide the constant voltage at output. In spite of variation in clean energy input, the proposed converter utilizes clean energy effectively and battery input plays major role in reliability. The converter efficiency has been found to be in the range of 80% to 90% with an acceptable regulation in open loop mode. The tested converter has potential for application involving LEDs for general lighting or for any applications involving dual source at the input with buck, boost or unity gain modes available at the output. Compared to conventional inductor - based converter it can achieve multiple gains, realize small hardware cost, compact in size, have light weight, and do not posses flux of magnetic induction. An experimental prototype is implemented for verification of the circuit. Simulation and experimental results concur for the converter to provide a constant output voltage of 17.5 to 18 V across the LED string for a current of 200 to 250 mA working from a battery source of 12 V and a solar source

voltage ranging from 0 to 12 V. Furthermore, the potential of line and load regulation techniques in SCC is also introduced and verified in this chapter.

6.1   Extension of VCRs in the Proposed Converter

The converter discussed in Chapter 5 was capable of delivering 11 VCRs in buck, boost and unity mode. Additional 4 more VCRs are proposed as an extension of the capability of the converter, including an inversion mode, by the addition of one more switch S_{b10} as shown in Figure 6.1. The first source is named as V_{bat} and the second source as V_s denoting battery and solar sources. Being CMOS the switches are renamed as switches $S_{b1} - S_{b10}$. The switching logic for the newly explored VCRs is shown in Table 6.1. The additional VCR states are labeled as 12 to 15 in continuation to show that it is an extended version explored in the same circuit in Chapter 5 explained in Table 5.1 and Figure 5.1. The difference between the two architecture is that state 12 and 13 can also be realized using the same architecture shown in Figure 5.1, with the help of 9 switches and 5 diodes but diodes are not needed when CMOS switches are used. In Table 6.1 "x" means diodes are not considered in these extended states. Since all the switches $S_{b1} - S_{b10}$ used are of CMOS type, as typically used in low power applications there will be considerable improvement in efficiency, battery life and chip space.
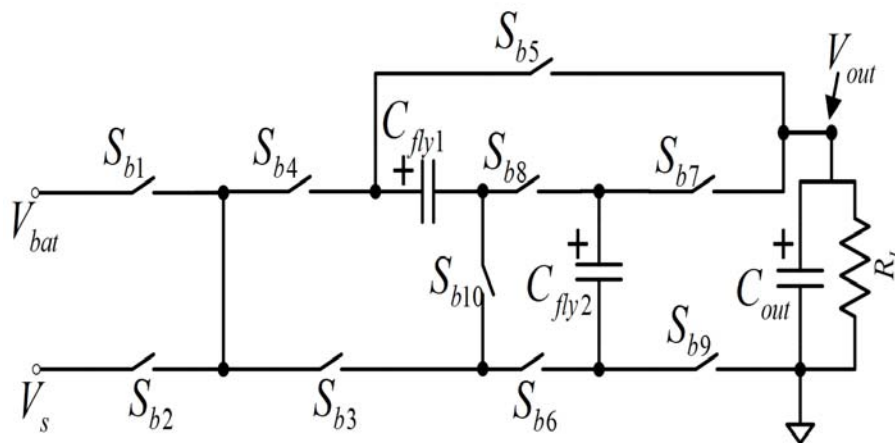
Figure 6.1: Circuit Lay out of the Proposed Converter with 10 Switches for CMOS Implementation

Table 6.1: Extended VCRs Switching Logic

State	VCR	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	D_1	D_2	D_3	D_4	D_5
12	$(V_{bat}+V_s)$ x0.5	CS	TS	TS	CS	TS	-	TS	CS	CSTS	TS	x	x	x	x	x
13	$(V_{bat}+V_s)$x0.75	CS	TS	TS	CS	TS	TS	TS	CS	CS	TS	x	x	x	x	x
14	V_{bat}x-1	CS	-	CS	-	CSTS	CSTS	TS	CS	TS	TS	x	x	x	x	x
15	V_sx-1	-	CS	CS	-	CSTS	CSTS	TS	CS	TS	TS	x	x	x	x	x

6.2 Realization of the SC Converter with CMOS Switches

The circuit diagram shown in Figure 6.1 uses MOSFET switches and to plug the unwanted conduction of the anti parallel diodes few diodes were used. The diodes though fast acting with less forward voltage still reduces the efficiency of the converter. The feasibility of the converter for low power application using CMOS switches driving μA is studied in this section. The circuit diagram redrawn for CMOS implementation with 10 switches is shown in Figure 6.1. The switching logic is the same as referred earlier in Table 5.1 and Table 6.1 for VCRs 1 to 11 and 12 to 15 respectively. The switches $S_{b1} - S_{b10}$ used are of bi - directional SPST analog switch manufactured by MAXIM INTEGRATED circuits MAX4678 (Integrated, 2016) with individual onstate resistance of $R_{on} = 0.3\ \Omega$. The flying capacitor and filter capacitor are manufactured by SANYOUNG 22 μF, 50 V with an ESR of 100 mΩ. The load current ranges between between 10 μA - 10 mA at an output voltage level of 0.55 V to 2.5 V. Figure 6.2A shows a prototype of PIC16F controller which is used to generate switching sequence for CMOS switch and LCD are used to display the particular state of proposed converter. The dead time is 10 ns. Figure 6.2B shows the MAX4678 SMD bidirectional switch and the prototype size is 5 cm x 5 cm including all components. Figure 6.2C shows the test bench of the proposed prototype where LED is used as a load which is highlighted in the circle. Experimental result shown in Figure 6.2D corresponds to an input voltage of 1.17 V and the output voltage is 1.76 V which is in good agreement of state 6. Two frequencies 100 kHz at an input voltage of 1.17 and 5 kHz with an input voltage of 2 V, both at a duty cycle of 50% are implemented with suitable dead time and is shown in Figure 6.3. We can conclude from Figures 6.3a and 6.3b that for 100 kHz and 5 kHz frequencies, simulation, modelling and experimental results are in good agreement with each other as shown in Table 6.2.

Figure 6.4 shows comparison of all the 11 VCRs using CMOS switches derived by the switching sequence referred in Table 5.1 for modelling, simulation and hardware results of the proposed circuit. The voltage regulation can be achieved by two methods discussed in Section 6.6. The efficiency increases considerably and is greater than (95%) in CMOS implementation without the diodes discussed in Chapter 5 for the same proposed topology. The size of the prototype is very much smaller than the size of existing converter when CMOS is used.
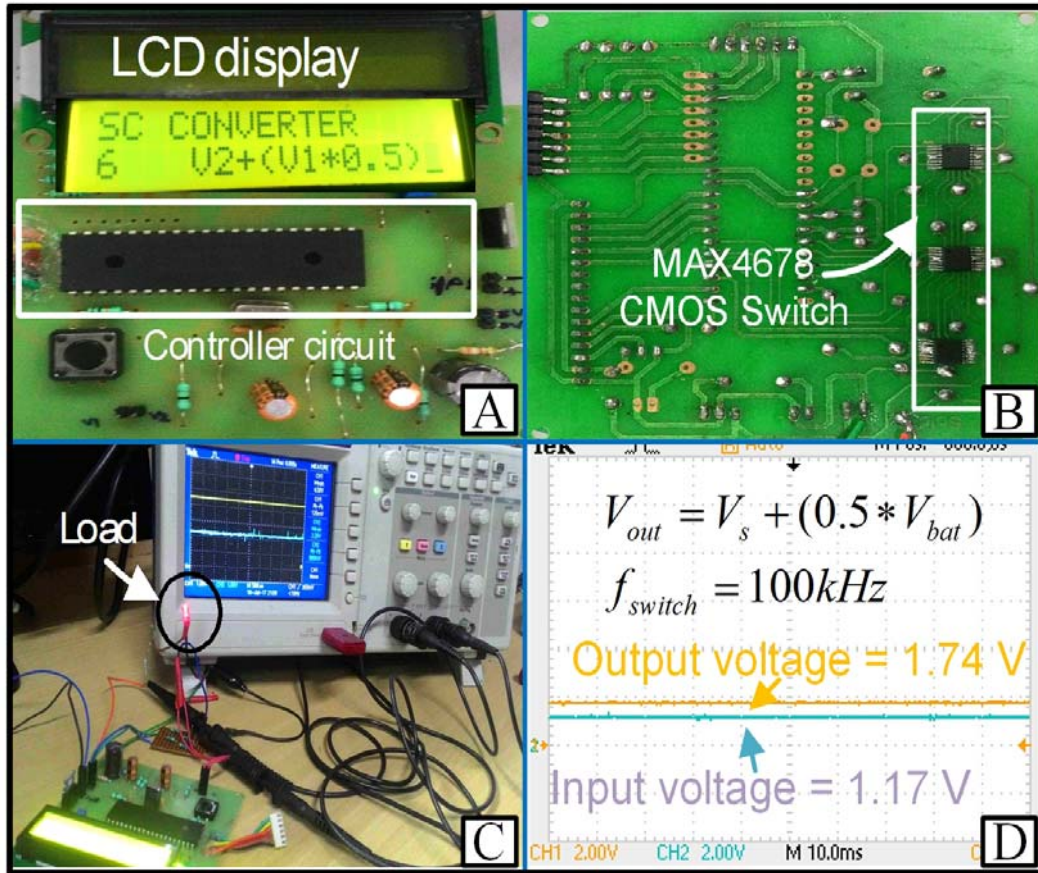
Figure 6.2: Hardware Prototype of the Converter for CMOS Implementation

Table 6.2: Modelling, Simulation and Hardware Comparison with CMOS Implementation for State 6 at 100 kHz and 5 kHz

f_{switch} (kHz)	$\lambda_{\phi c}$	$\lambda_{\phi t}$	R_{equ} (Ω)	V_{out} (V) Mode l	V_{out} (V) Simulation	V_{out} (V) Hardware	η % Hardware
100 (@ 1.17 V)	3.24	1.43	0.25	1.75	1.75	1.74	99
5 (@ 1.2 V)	1.62	7.17	5	1.76	1.78	1.74	96.5
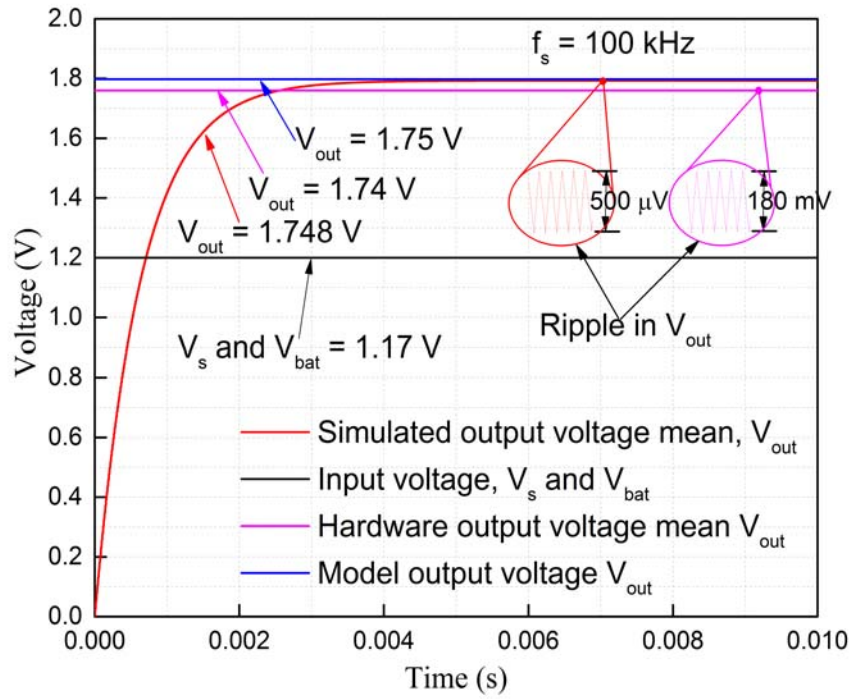
(a) Frequency 100 kHz
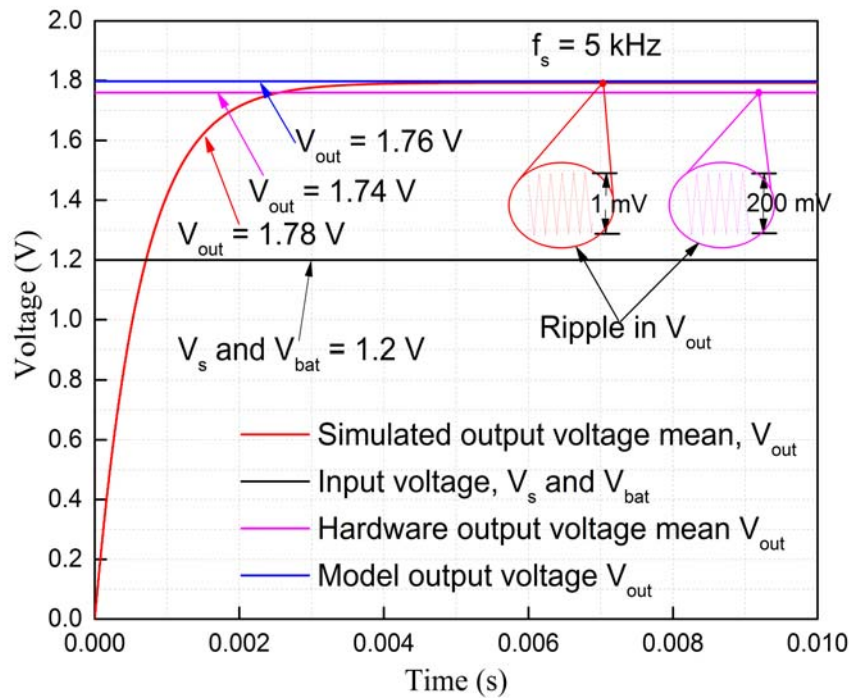
(b) Frequency 5 kHz

Figure 6.3: Simulation, Modelling and Experimental Results at 100 kHz and 5 kHz in State 6
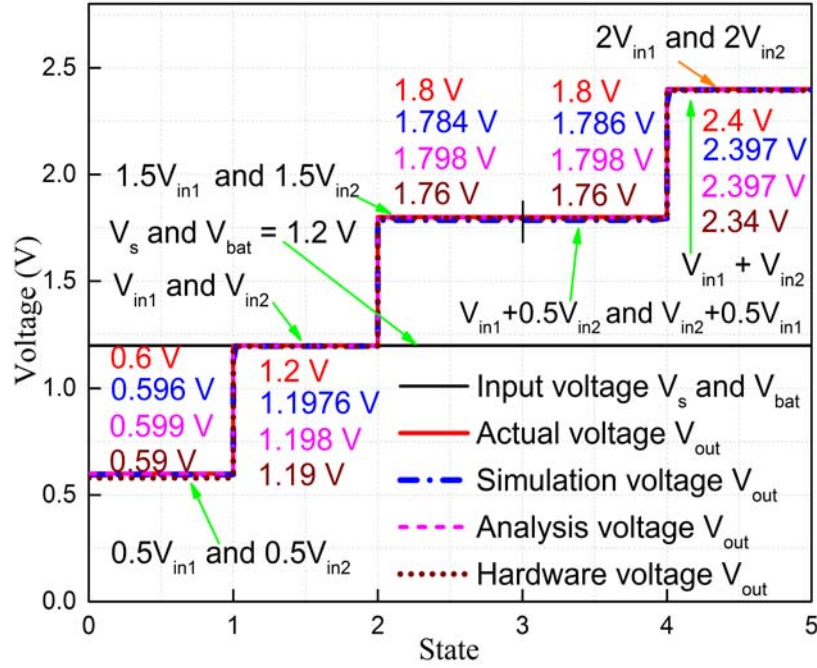
Figure 6.4: Comparison of All 11 VCRs in Modelling, Simulation and Hardware in CMOS Implementation

6.2.1 Circuit States and Comparison of Results for State 12

Referring to Figure 6.1 and Table 6.1, state 12 for a VCR of $(V_{in1} + V_{in2})$ **x0.5** is implemented. In this case, the ninth switch S_9, may completely be in the ON state shown as CSTS. The first switch S_1, the fourth switch S_4, and the eighth switch S_8 may be connected in the charging state CS. The second switch S_2, the third switch S_3, the fifth switch S_5, the seventh switch S_7 and the tenth switch S_{10} may be connected in the transfer state TS. In the charging state CS, the first source V_{bat} may be connected to the first flying capacitor C_1, the second flying capacitor C_2 and to the ground terminal through S_1, S_4, S_8 and S_9. In this case, the first flying capacitor C_1 and the second flying capacitor C_2 may be connected in series and charges to V_{bat}**x0.5**. In the transfer state TS, the second source V_s may be connected to the first flying capacitor C_1, the second flying capacitor C_2, and to the output, ground terminal respectively through S_2, S_3, S_5, S_7, S_9 and S_{10}. In this case, V_s and the first flying capacitor C_1 may be connected in series and the combination is connected in parallel to the second flying capacitor C_2 and to the load R_L. Thus, the total output voltage V_{out} may be $(V_{bat} + V_s)$ **x0.5**. The

simulation, Mode l and hardware results for the output voltage V_{out} is shown in Figure 6.5 for a frequency of 100 kHz. It can be seen that the hardware output voltage is 1.17 V when V_{bat} is selected as 1.2 V and V_s is selected as 1.2 V which is $(V_{bat} + V_s)$ **x0.5**, the desired output.

6.2.2 Circuit States and Comparison of Results for State 13

Referring to Figure 6.1 and Table 6.1, state 13 for a VCR of $(V_{bat} + V_s)$**x0.75** is implemented. In this case, as represented in Table 6.1, the first switch S_1, the fourth switch S_4, the eighth switch S_8, and the ninth switch S_9 may be connected in the charging state CS. The second switch S_2, the third switch S_3, the fifth switch S_5, the sixth switch S_6, the seventh switch S_7 and the tenth switch S_{10} may be connected in the transfer state TS. In the charging state CS, V_{in1} may get connected to the first flying capacitor C_1, the second flying capacitor C_2, and to the ground terminal through S_1, S_4, S_8 and S_9. In this case, the first flying capacitor C_1 and the second flying capacitor C_2 may be connected in series during the charging state CS and charges to V_{bat}**x0.5**. The output voltage V_{out} during the charging state CS may be supplied by filter or buffer capacitor C_{out}. In the transfer state TS, V_s may get connected to the first flying capacitor C_1 and the second flying capacitor C_2 through S_2, S_3, S_5, S_6, S_7 and S_{10}. In this case, the first flying capacitor C_1 and the second flying capacitor C_2 may be connected in parallel during the transfer state TS. Thus, in this case, the total output voltage V_{out} may be $(V_{bat} + V_s)$**x0.75**. The simulation, Mode l and hardware results for the output voltage V_{out} is shown in Figure 6.5 for a frequency of 100 kHz. It can be seen that the hardware output voltage V_{out} is 1.79 V when V_{bat} is selected as 1.2 V and V_s is selected as 1.2 V which is very near to $(V_{bat} + V_s)$ **x0.75**, the desired output.

6.2.3 Circuit States and Comparison of Results for State 14/15

Referring to Figure 6.1 and Table 6.1, state 14 for a VCR of V_{bat}**x-1** is implemented. In this case, as represented in Table 6.1, the fifth switch S_5 and the sixth switch S_6 may be in the ON state which is CSTS state. The first switch S_1, the third switch S_3, and the eighth switch S_8 may be connected in the charging state CS. The first flying capacitor C_1, the second flying capacitor C_2 is charged in series with the load R_L through the
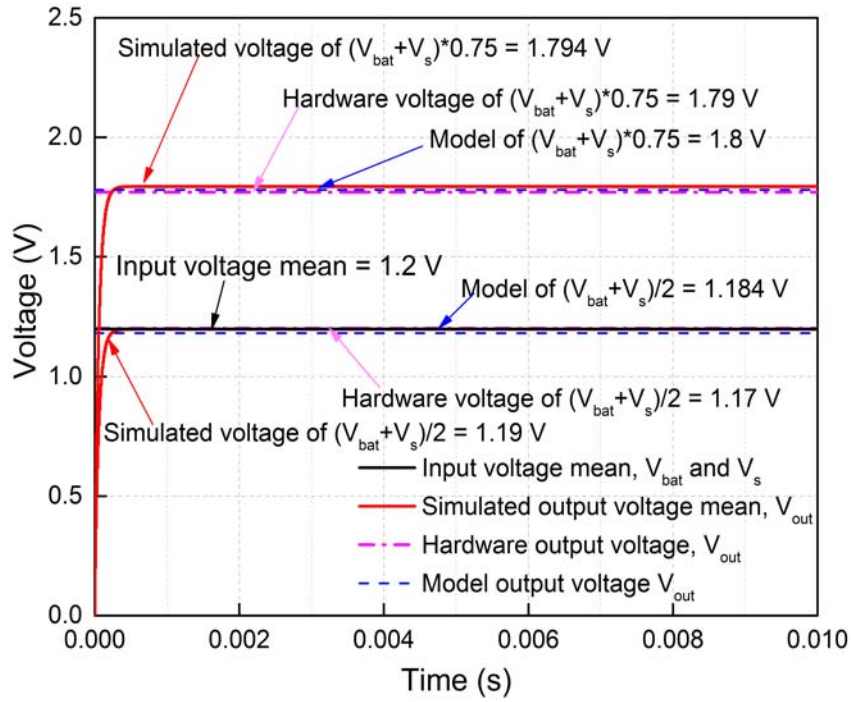
Figure 6.5: Comparison of Modelling, Simulation and Hardware Results for VCRs 12 and 13

switches S_1, S_3, S_5,S_8 and S_6 with lower plate of the flying capacitors "+" and upper plate "-". The seventh switch S_7, the ninth switch S_9, and the tenth switch S_{10} may be connected in the transfer phase TS. In this case, the first flying capacitor C_1 and the second flying capacitor C_2 may be connected in parallel through the switches S_7, S_9, S_{10},S_5 and S_6 to the load R_L in opposite polarity with respect to the reference. Thus, the total output voltage V_{out} may be V_{in1}x-1. The simulation, Mode l and hardware results for the output voltage V_{out} is shown in Figure 6.6 for a frequency of 100 kHz. It can be seen that the output voltage V_{out} is -1.18 V when V_{bat} is selected as 1.2 V, which is V_{bat}x-1, the desired output. A similar approach can be taken to analyze VCR 15.

6.3 Realization of the SC Converter to Light White LEDs Utilizing Solar Power Using MOSFET Switches

Renewable energy utilization and SCC circuits for efficient tapping is gaining popularity and has been discussed in (Das and Agarwal, 2016; Li *et al.*, 2016; Ajami *et al.*,
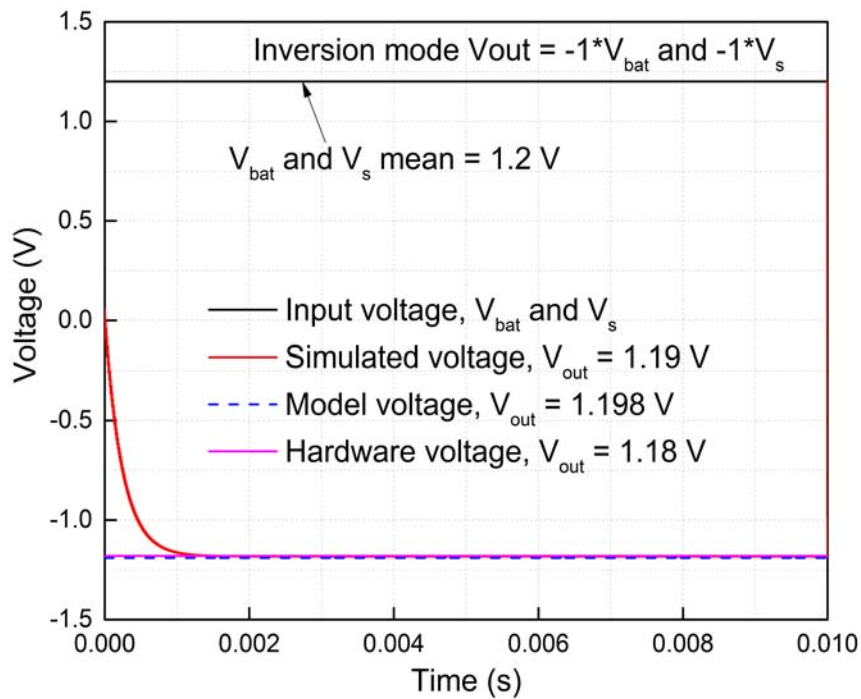
Figure 6.6: Comparison of Modelled, Simulated and Hardware V_{out} for State 14

2015). The hardware set up block diagram for experimental implementation of the new buck - boost converter to power LEDs using input as battery and solar source is shown in Figure 6.7. The two sources, battery and solar feeds the converter. The solar voltage is sensed continuously and the decision of switching sequence as to which mode is to be operated is taken by the gating circuit. This decision is realized with the help of two microcontrollers in this set up. By varying how the switches are clocked, according to particular switch configuration, different gains can be obtained by this multi - topology converter. The target application in this experiment is to power white LEDs that works at 18 V when driven by a current of around 240 mA which is shown as load in Figure 6.8. The SCC is the heart of the block diagram and its circuit diagram is shown in Figure 6.9. It consists of two flying capacitors C_1 and C_2. The flying capacitors are the one that stores and transfers energy from the selected sources. The switches S_1 to S_9 and the diodes D_1 to D_5 are switched in order to change the connection of flying capacitors so that capacitors can be charged and discharged through different paths in order to obtain desired voltage at the output of converter. The converter input consists of two input sources V_{in1} and V_{in2}. V_{in1} is the fixed battery input and V_{in2} is a variable solar source. The switches are controlled using two phase non overlapping clock

111
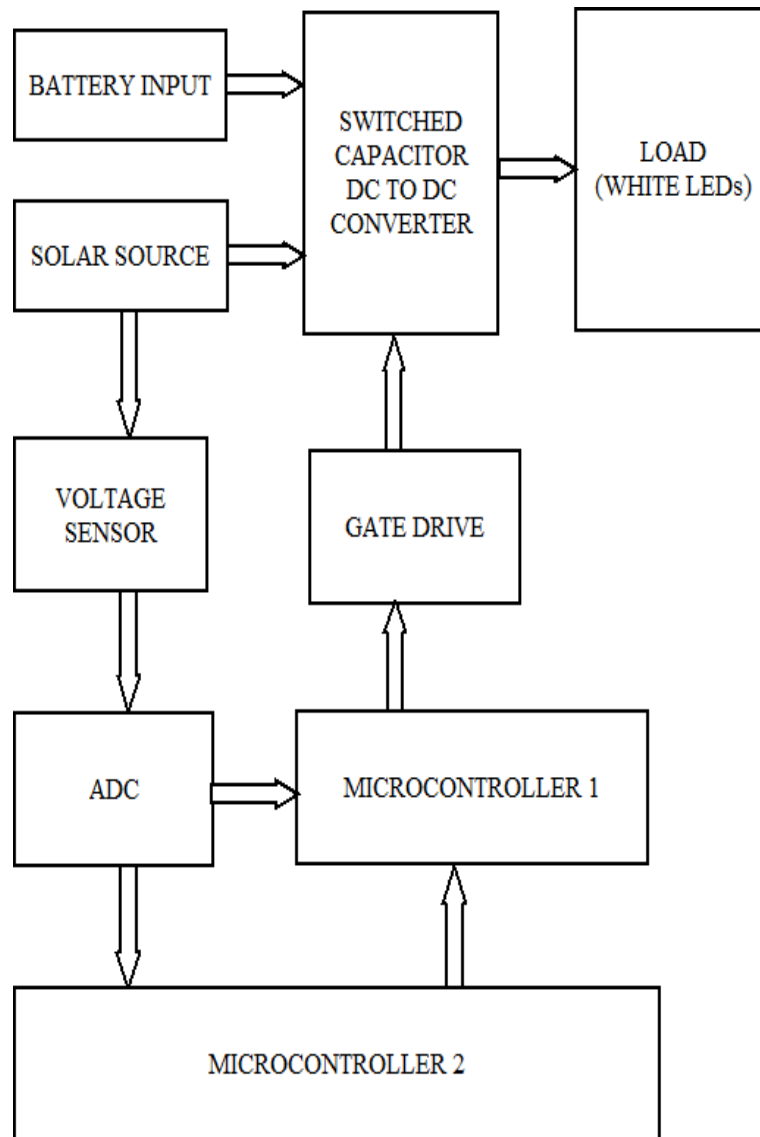
Figure 6.7: Block Diagram for Implementation of the Buck - Boost SC Converter
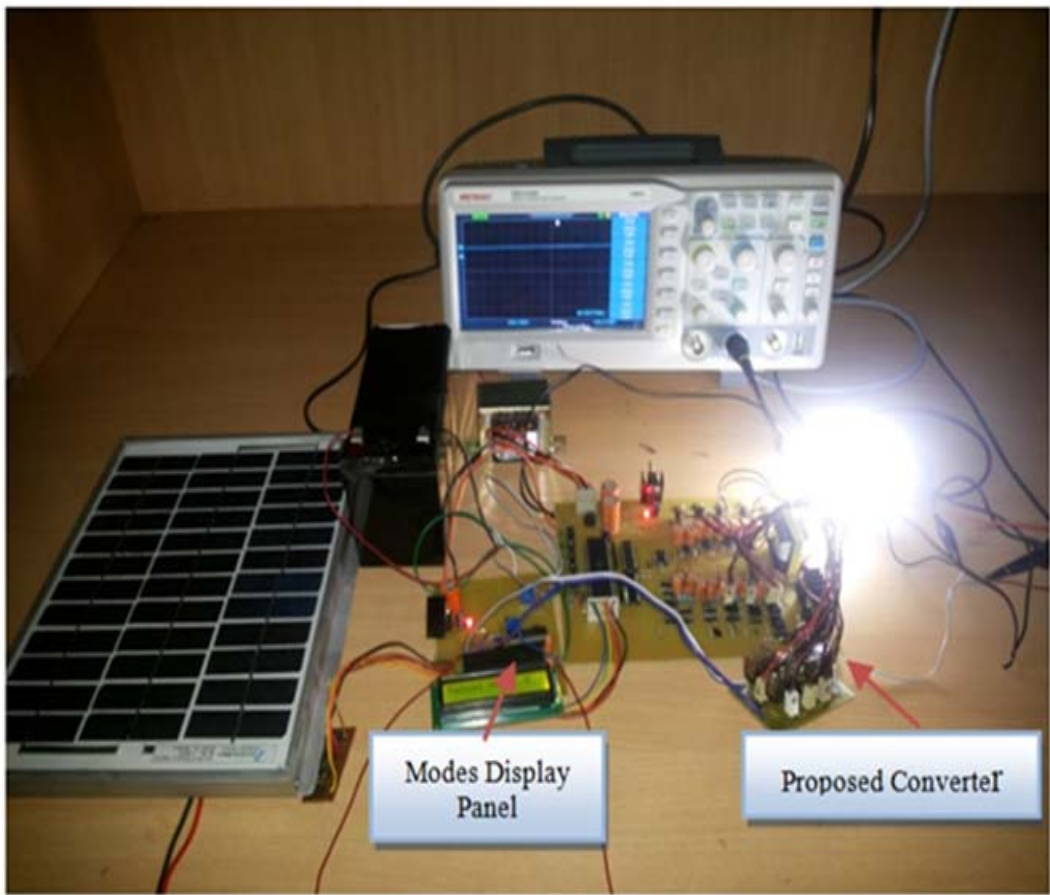
Figure 6.8: Hardware Set Up of the Proposed Converter in Laboratory

signals or complementary triggering pulses. Accordingly it has two phases: charging state (CS) and transfer state (TS). Charging phase is when the capacitors get charged from input supply. Discharging or dumping phase is when the capacitors discharge to output. By alternating in a periodical way the output corresponds to a constant voltage in accordance with the selected gain configuration to which the topology belong to. The converter switches to battery operation V_{in1} when solar voltage is absent and to a combination of both battery and solar when solar voltage is lower than that required to completely drive the load. The converter switches to solar operation if solar source is available in ample thus providing good utilization of solar energy. For this let the range of solar supply is divided into four regions. Thus there are four modes of operation that the converter has to transit through. The gain configuration or VCRs selected in different states, for accomplishing the four modes discussed above used in this experiment is shown in Table 6.3.
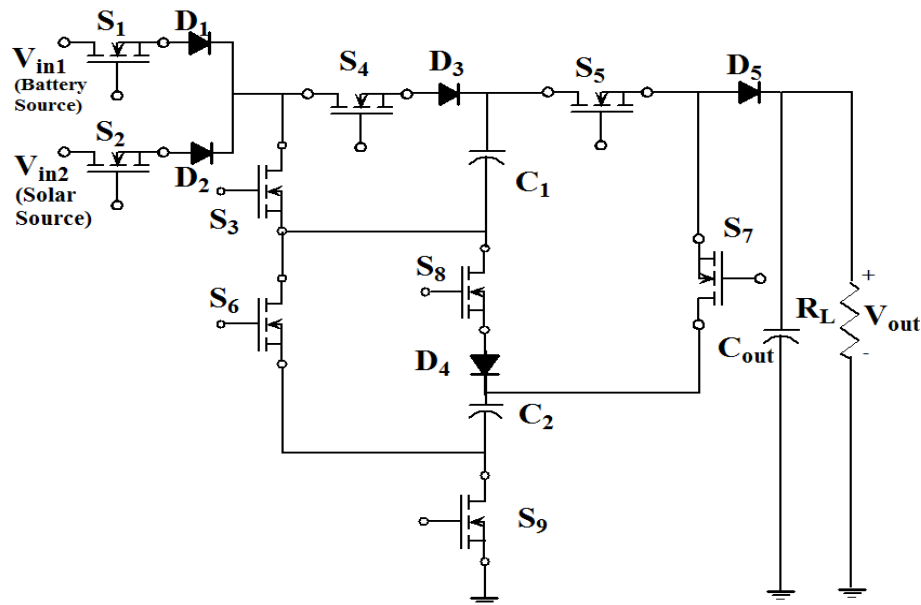
Figure 6.9: Circuit Diagram of the Proposed Multiple Input Multiple Output Buck - Boost SCC

Table 6.3: VCR for the Targeted Output Voltage in the Four States Used

Mode	VCR	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	D_1	D_2	D_3	D_4	D_5
1	V_{in1}x1.5	CSTS	-	TS	CS	TS	TS	TS	CS	CS	CSTS	-	CS	CS	TS
2	$V_{in1} + V_{in2}$	CS	TS	TS	CS	TS	CS	-	-	CS	CS	TS	CS	-	TS
3	V_{in2}x2	-	CSTS	TS	CS	TS	CS	-	-	CS	-	CSTS	CS	CS	TS
4	V_{in2}x1.5	-	CSTS	TS	CS	TS	TS	TS	CS	CS	-	CSTS	CS	CS	TS

According to the solar output the converter operation changes into corresponding modes. Thus the converter operation is set in four modes shown below. Here V_{out} is the targeted output voltage to power LEDs which is desired at 18 V.

1. Mode 1 ($V_{in2} \leq \frac{V_{out}}{3}$)

2. Mode 2 ($\frac{V_{out}}{3} \leq V_{in2} \leq \frac{V_{out}}{2}$)

3. Mode 3 ($\frac{V_{out}}{2} \leq V_{in2} \leq \frac{2V_{out}}{3}$)

4. Mode 4 ($V_{in2} \geq \frac{2V_{out}}{3}$)

Table 6.4: Four Modes and Their Conditions

MODES	Sensed Solar Input voltage (V)	Battery Conversion ratio (V_{in1})	Solar Conversion ratio (V_{in2})
Mode 1	$V_{in2} \leq \frac{V_{out}}{3}$	3/2	0
Mode 2	$\frac{V_{out}}{3} \leq V_{in2} \leq \frac{V_{out}}{2}$	1	1
Mode 3	$\frac{V_{out}}{2} \leq V_{in2} \leq \frac{2V_{out}}{3}$	0	2
Mode 4	$V_{in2} \geq \frac{2V_{out}}{3}$	0	3/2

6.3.1 Explanation of Mode 1

Consider the Mode 1. When solar output $V_{in2} \leq \frac{V_{out}}{3}$, it can be seen that the switches S_1, S_4, S_8, S_9 and diodes D_1, D_3, D_4 are on during the charging state (CS) and switches S_1, S_3, S_5, S_6, S_7 and diodes D_1, D_5 are on during transfer state (TS) as seen from Table 6.3. The circuit states can be traced in Figure 6.9 . Since the solar input is less than 6 V ($V_{in2} \leq \frac{V_{out}}{3}$) in both these phases CS and TS, the battery source supplies the load. The steady state equivalent circuits of charging and dumping phase are shown in Figure 6.10. Then by KVL following equations can be written. The flying capacitors are charged in series through switches S_1, S_4, S_8, S_9 and diodes D_1, D_3, D_4 in CS according to the equations,

$$V_{C1} = V_{C2} = \frac{V_{in1}}{2} \tag{6.1}$$
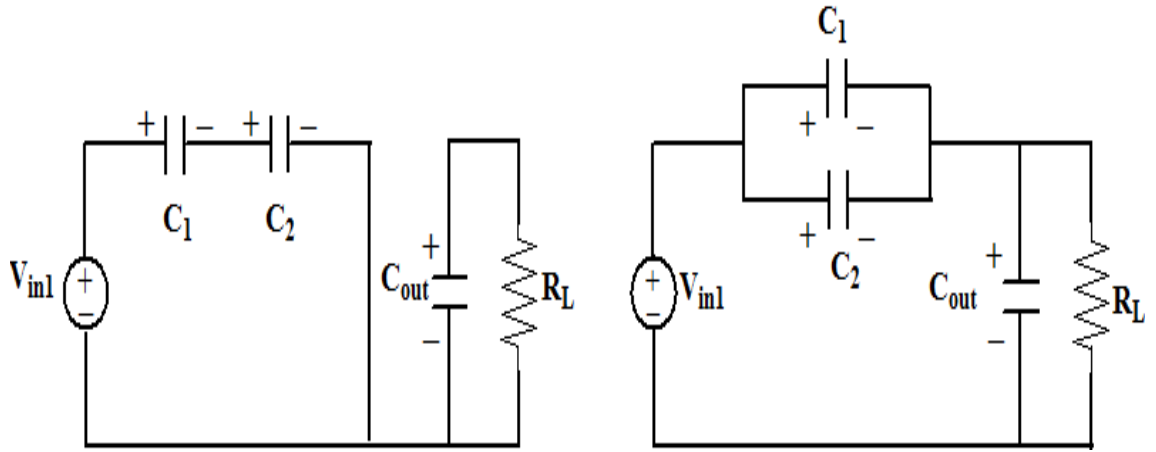
Figure 6.10: Switched Circuits for Mode 1

In TS, C_1 and C_2 are connected in parallel with the load but in series with V_{in1} through switches S_1, S_3, S_5, S_6, S_7 and diodes D_1, D_5 . The voltages of C_1 and C_2 are,

$$V_{C1} = V_{C2} = V_{in1} - V_{out} \tag{6.2}$$

In steady state both relations will hold. Combining equations result in,

$$V_{out} = \frac{3}{2} V_{in1} \tag{6.3}$$

Thus when the solar source is less in its capability to power,

$$V_{in2} \leq \frac{V_{out}}{3} \tag{6.4}$$

then battery input alone provides the output load by equation,

$$V_{out} = \frac{3}{2} V_{in1} \tag{6.5}$$

Therefore to achieve a boost mode of 1.5x the input battery as seen in Equation 6.5 the logic in Table 6.3 should switch to mode 1 configuration.

6.3.2   Explanation of Mode 2

Consider the operation of the converter in Mode 2. This condition is when solar output voltage sensed is greater than 6 V but less than 9 V as seen in the condition $\frac{V_{out}}{3} \leq V_{in2} \leq \frac{V_{out}}{2}$. It can be seen that the switches S_1, S_4, S_6, S_9 and diodes D_1, D_3 are on during the

charging state (CS) and switches S_2, S_3, S_5 and diodes D_2, D_5 are on during transfer state (TS)as seen from Table 6.3. The circuit states can be traced in Figure 6.9 . Since the solar input is targeted in between 6 V to 9 V, the battery source added to the solar supplies the load. The steady state equivalent circuits of charging and transfer phase are shown in Figure 6.11. Then by using KVL, following equations can be written. The
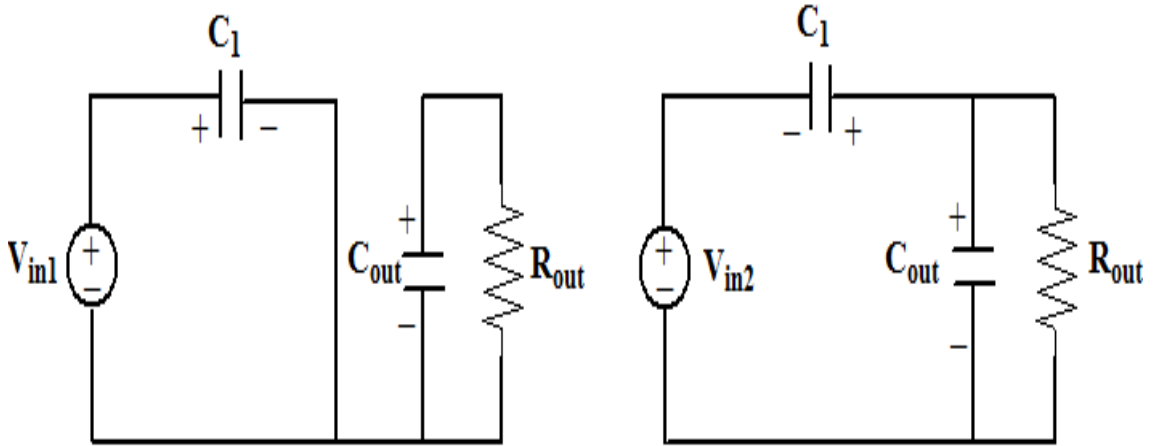
Figure 6.11: Switched Circuits for Mode 2

flying capacitor C_1 is charged in series through switches S_1, S_4, S_6, S_9 and diodes D_1, D_3 in CS from source V_{in1} according to the equations,

$$V_{C1} = V_{in1} \tag{6.6}$$

In TS, C_1 and V_{in2} are connected in series delivering the load. The voltages of C_1 and C_2 are,

$$V_{C1} = V_{out} - V_{in2} \tag{6.7}$$

In steady state, both relations will hold. Combining equations results in,

$$V_{out} = V_{in1} + V_{in2} \tag{6.8}$$

Thus when the solar source is less in its capability to power fully,

$$\frac{V_{out}}{3} \leq V_{in2} \leq \frac{V_{out}}{2} \tag{6.9}$$

then battery input added to the solar voltage provides the output load by equation,

$$V_{out} = V_{in1} + V_{in2} \tag{6.10}$$

118

Therefore to harness the available solar power and burden the battery less, the converter to satisfy Equation 6.10, logic in Table 6.3 should switch to Mode 2 configuration.

6.3.3 Explanation of Mode 3

Consider the operation of the converter in Mode 3. This condition is when solar output voltage sensed is greater than 9 V but less than 12 V as seen in the condition $\frac{V_{out}}{2} \leq V_{in2} \leq \frac{2V_{out}}{3}$. It can be seen that the switches S_2, S_4, S_6, S_9 and diodes D_2, D_3, D_4 are on during the charging state (CS) and switches S_2, S_3, S_5 and diodes D_2, D_5 are on during transfer state (TS)as seen from Table 6.3. The circuit states can be traced in Figure 6.9. Since the solar input targeted is greater than 9 V, the solar source can completely supply load if the voltage is doubled practically powering entirely from solar source. The steady state equivalent circuits of charging and dumping phases are shown in Figure 6.12. Then by
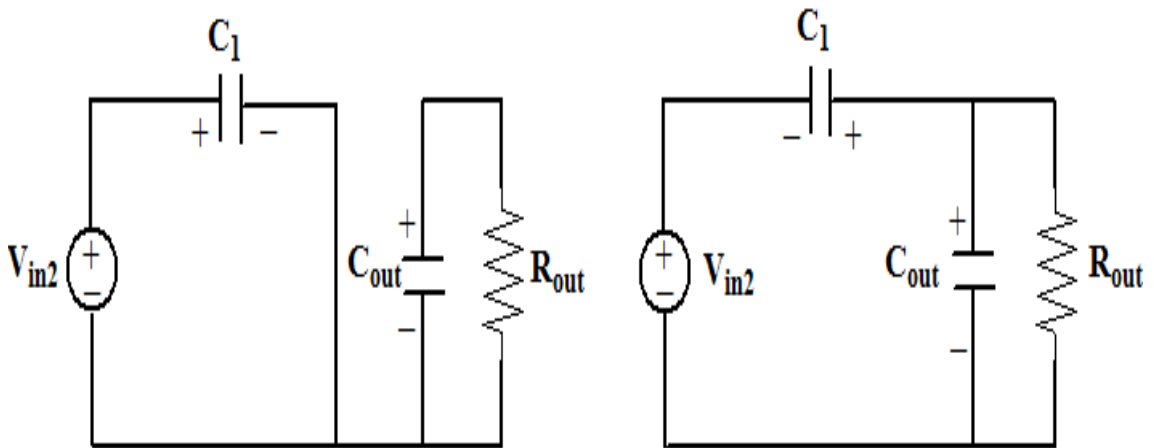
Figure 6.12: Switched Circuits for Mode 3

KVL following equations can be written. The flying capacitor C_1 is charged in series through switches S_2, S_4, S_6, S_9 and diodes D_2, D_3, D_3 in CS through solar source V_{in2} according to the equations,

$$V_{C1} = V_{in2} \tag{6.11}$$

In TS, C_1 and V_{in2} are connected in series delivering the load. The voltage across C_1 is,

$$V_{C1} = V_{out} - V_{in2} \tag{6.12}$$

In steady state both relations will hold. Combining equations result in,

$$V_{out} = V_{in2} + V_{in2} = 2V_{in2} \qquad (6.13)$$

Thus when the solar source is available partially as per Equation 6.14,

$$\frac{V_{out}}{2} \leq V_{in2} \qquad (6.14)$$

using a double boost mode the solar source provides the output load by equation,

$$V_{out} = 2V_{in2} \qquad (6.15)$$

Therefore to harness the available solar power completely, the converter to satisfy Equation 6.15, logic in Table 6.3 should switch to mode 3 configuration.

6.3.4 Explanation of Mode 4

Consider the operation of the converter in Mode 4. This condition is when solar output voltage sensed is greater than or equal to 12 V as seen in the condition $V_{in2} \geq \frac{2V_{out}}{3}$. It can be seen that the switches S_2, S_4, S_8, S_9 and diodes D_2, D_3, D_4 are on during the charging state (CS) and switches S_2, S_3, S_5, S_6, S_7 and diodes D_2, D_5 are on during transfer state (TS) as seen from Table 6.3. The circuit states can be traced in Figure 6.9. Since the solar input targeted is greater than 12 V, the solar source can completely supply load if the voltage is boosted 1.5x the input voltage. In this case also the solar source can practically power the entire load. The steady state equivalent circuits of charging and dumping phase are shown in Figure 6.13. Then by KVL, following equations can be written. The flying capacitors C_1 and C_2 are charged in series through switches S_2, S_4, S_8, S_9 and diodes D_2, D_3, D_4 in CS through solar source V_{in2} according to the equations,

$$V_{C1} = V_{C2} = \frac{V_{in2}}{2} \qquad (6.16)$$

In TS, source V_{in2} is connected in series to the parallel combination of C_1, C_2 through S_2, S_3, S_5, S_6, S_7 and diodes D_2, D_5 delivering the load. The voltages of C_1 and C_2 are,

$$V_{C1} = V_{C2} = V_{in2} - V_{out} \qquad (6.17)$$
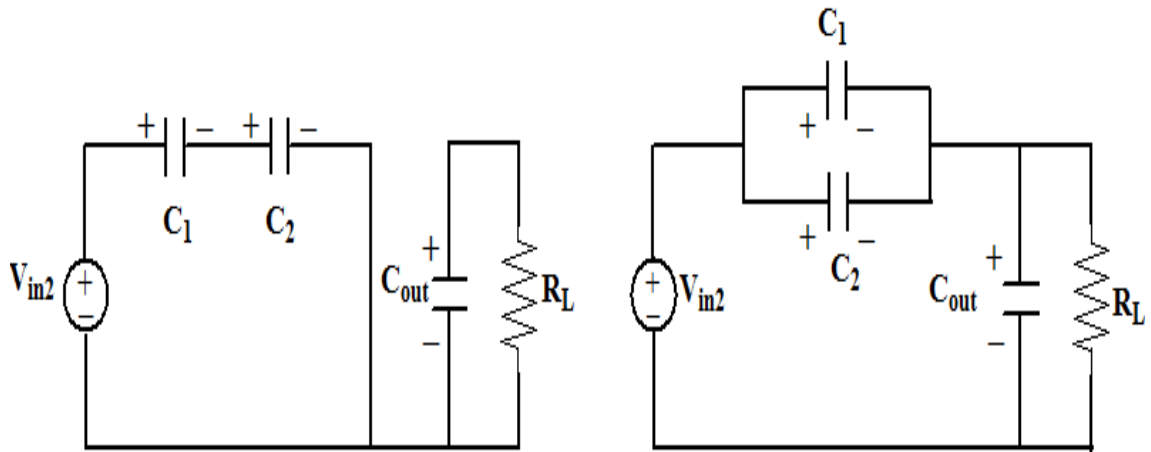
Figure 6.13: Switched Circuits for Mode 4

In steady state both relations will hold. Combining equations result in,

$$V_{out} = \frac{3}{2}V_{in2} \tag{6.18}$$

Thus when the solar source output voltage is sensed as in Equation 6.19,

$$V_{in2} \geq \frac{2V_{out}}{3} \tag{6.19}$$

then solar input alone provides the output load by equation,

$$V_{out} = \frac{3}{2}V_{in2} \tag{6.20}$$

Therefore to achieve a boost mode of 1.5x the solar power, as seen in Equation 6.20 the logic in Table 6.3 should switch to Mode 4 configuration.

6.4 Building Blocks of the Hardware Set Up

The proposed converter hardware is rigged up in laboratory facility to light white LEDs tapping the solar energy. Referring to Table 6.3 and Figure 6.7, a flow chart is prepared to automatically select the switching logic verifying the availability of solar power to select the required modes and is shown in Figure 6.14. This logic is realized using microcontrollers. According to the solar input available the converter working changes to required mode. The required gain configuration is automatically chosen by feedback provided by voltage sensor that senses the voltage of solar panel. Thus the
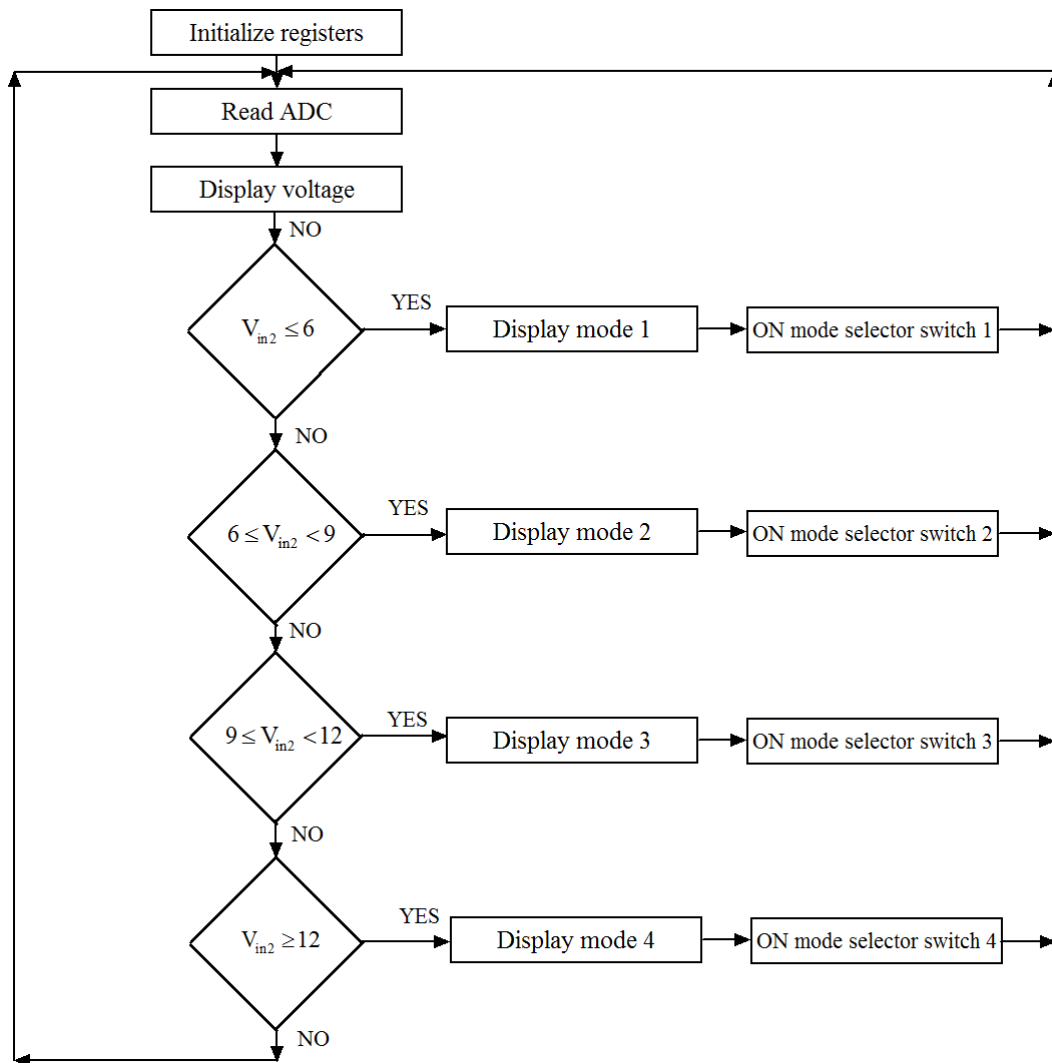
Figure 6.14: Flow Chart for the Selection of Required Mode

clocking pulses are provided accordingly and the waveforms of battery input voltage, solar source voltage and output voltage have been obtained.

6.4.1 Hardware Specifications

It can be seen that from Equations (5.31) and (5.34), the parameters involved in R_{out} and V_{diode} significantly influence the output voltage V_{out}. One way to reduce R_{out} and increase V_{out} is by selecting a higher value of flying capacitors or increasing the switching frequency. In the hardware set up discussed here switching frequency is selected as 10 kHz and flying capacitor value is fixed as 47 μF. The load is white LEDs and later for obtaining variable current load resistance is taken as 72Ω with filter capacitor value is fixed as 470 μF. The diodes D_1 to D_5 are used to check the unwanted turn on of the anti parallel diodes of the MOSFET switches. The forward voltage drop of diode reduces the output voltage V_{out} as seen from Equation (5.34). If MOSFET switches can be replaced with unidirectional other switches then the efficiency can be increased to a greater extend. Referring to Figure 6.9 the switches and diodes used are of the same type discussed in Chapter 5. From Figure 6.7 there are two sources fixed, battery source and variable source that are connected to power the SCC. The sensor senses the solar source voltage and accordingly a mode of operation is selected automatically using microcontroller 2. This input goes to microcontroller 1, which then selects the input voltage source as per the mode. Gating signals for turning on switches is produced by this microcontoller. The gate driver unit amplifies and isolates the pulses produced by microcontroller and provides it to gate of switches. The components are powered from filtered supply from the 230 V AC after conversion into the usable form. Two types of filtered supplies are required, one for the analog circuits while other for the digital circuits. The two supplies are separated so that the noise prone analog circuits do not get affected by switching of digital circuits. The power supply required for microcontrollers and gating circuit is generated using the block diagram as in Figure 6.15 and the circuit layout is shown in Figure 6.16. A 12-0-12 V step down transformer is connected to provide the necessary low voltage. The transformer also works as an isolator between the hot and cold end. The hot end refers to the 230 V supply, which is a hazardous one, and the cold one refers to the low, safe voltage. Now the hot portion appears only at the primary of the transformer. The secondary of the transformer deliver 12 V ac pulses

along with a ground. This ac supply goes to a center tapped rectifier, which converts the ac into a unidirectional voltage. The ripples in the resulting supply is filtered and smoothed by a 2200 μF/25 V capacitor. The 0.1 μF capacitor, bypasses any high frequency noises. The resulting supply has the magnitude above 17 V. This voltage is fed to the regulator IC 7805 and IC 7905 (Semiconductors, 2006). These IC's provides a regulated 5 V positive supply and negative at its 3rd pin respectively. The required input for this is more than 7.5 V. Also there is an LED in series with a 470 Ω resistor. This will act as a power ON indicator.
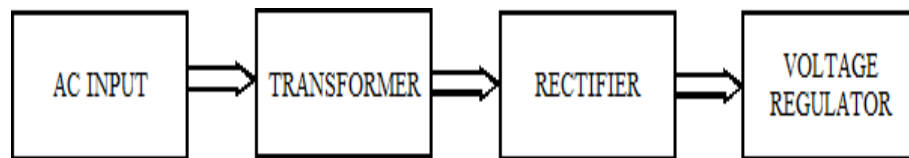
Figure 6.15: Block Diagram of Regulated Power Supply
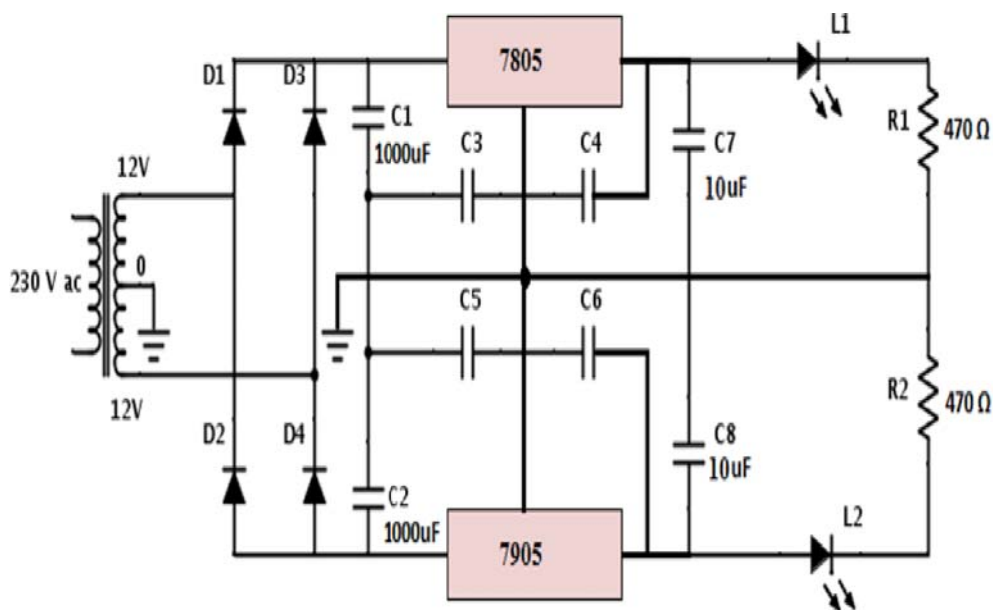
Figure 6.16: Circuit Layout of Regulated Power Supply

6.4.2 Gating Circuit

The optocoupler in the gate circuit is supplied using a Push - pull Converter circuit shown in Figure 6.17. The pulses for operation of switches in push pull converter is obtained from IC HCF40106BE (Trigger, 2014), consisting of six schmitt trigger circuits. Primary of push - pull converter is fed from 12 V. Secondary output is used to supply power to optocoupler. The optocoupler is used to isolate the voltages between

the main circuit and gating circuit. MCT2E is a 6 pin optocoupler IC. It is an NPN silicon phototransistor optically coupled to gallium arsenide infrared emitting diode. The output +10 / -10 V is required from push - pull converter to drive the phototransistor when there is an input pulse to it. For fast turn off, -10 V is required when there is no pulse to the input of the optocoupler. The resistors used are of 10 kΩ and capacitors are of 100 μF in the secondary side of the circuit. The collector of the transistor is
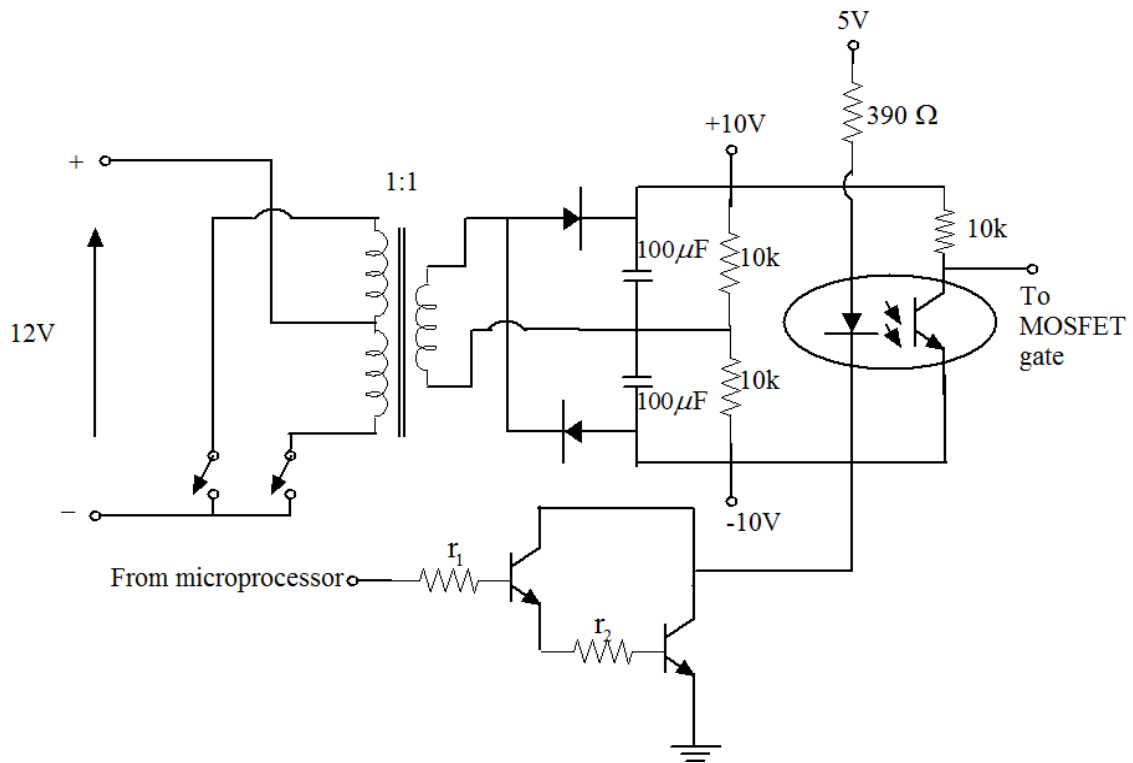
Figure 6.17: Push Pull Converter Circuit to Supply Power to Gating circuit

pulled high through a 10 kΩ resistor. The emitter grounded and the base is connected to the port pin. The collector voltage will be +10 V as far as the transistor is in cut off region. The transistor will act as an open switch in cut off region thereby blocking the collector current from entering the emitter terminal. The collector voltage drops to zero whenever the transistor goes to the saturation region. The transistor allows the collector current to flow through the transistor thereby acting like a closed switch. The collector terminal of the transistor is connected to the drain of the MOSFET. The logic high level between the base - emitter junctions generates base current in the transistor which in turn drives the transistor to the saturation region. The transistor will act like a closed switch thereby connecting the gate of the MOSFET to the source. The current flows directly to the source through the transistor, not through the gate. This will make the gate-source voltage as zero, which in turn switches off the MOSFET. The transistor

will be switched off as far as the base voltage becomes logic low level since the base current is zero. The short circuit across the gate and source will become open thereby forcing the resistor current to flow through the gate of the MOSFET. This gate current will drive the MOSFET to switch on condition, there by switching on the load. In short, a logic high level at the port pin will force the collector current of the transistor to flow through the MOSFET, which in turn switches on the load. Likewise, a logic low level on the port pin will switch on the transistor thereby shorting the gate and the source of the MOSFET. Zero gate - current will switch off the MOSFET thereby disconnecting the load from the supply.

6.4.3 Microcontroller AT89S8253

The controller used in this work is AT89S8253 (ATMEL, 2006), which is a low - power, high - performance CMOS 8 - bit microcontroller with 12 K bytes of In - System Programmable (ISP) Flash program memory and 2 K bytes of EEPROM data memory. The Atmel AT89S8253 is a powerful microcontroller which provides a highly - flexible and cost - effective solution to many embedded control applications. The microcontroller program is written in such a way, so that the microcontroller can read and can store the information received from the keyboard (mode selector). According to the received information from the keyboard, the microcontroller turns on the corresponding switches.

6.4.4 Sensor Unit

The sensor senses the solar source voltage and gives it to microcontroller 2. Microcontroller 2 then executes the process of selecting the mode of operation according to range of solar voltage. The solar voltage and mode of operation is then displayed using a line character intelligent display. The program flowchart for automatic selection and display of modes is as shown in Figure 6.14. This contains a liquid crystal display panel and an in built microcontroller. The ASCII characters can be displayed by giving the ASCII data for the required character to the data lines. The microcontroller in the LCD display contains two internal registers, one for commands and the second for the characters to be displayed.

6.4.5 Analog to Digital Converter

As we know, a part of the microcontroller is implemented in digital domain and thus an analog to digital converter is used to convert signals to digital domain. ADC0804 is used here. The IC ADC0804 has an internal clock generator. We just want to connect an RC network to the CLKR and CLKIN pins. The manufacturer data sheet instructs us to set the value of this RC network as 10 KΩ and 150 pF. The interrupt and the write control pins are shorted together for a stand - alone operation. The chip enable and the read control pins are connected together and are tied to the port of the micro controller. The chips will be activated only when the pin goes low. The converter reads the input voltage and converts it into the digital form. After completing this, it gives an interrupt signal through the INTR pin.

6.4.6 Input Sources - Battery and Solar Panel Specifications

The solar cell used in this hardware is having a rated voltage of 12V and the short circuit current is 50 mA. V_{mpp} is 16 V and I_{mpp} is 750 mA. This act as the second source V_{in2} referred in earlier sections. The short circuit current is 50 mA. A 12 V, 7 Ah Lead acid battery has been used in this work in order to provide constant voltage named as the first source V_{in1}.

6.4.7 White LED Module

A string of 10 LEDs of Lumichip LC5630 (Lumichip, 2011) has been used as the load. It consists of two parallel sets, with one set having 5 LEDs connected in series. Each LED works on forward voltage drop V_{fd} = 3.5 V, forward current I_{fd} = 100 to 120 mA, thus requiring an output voltage of 17.5 V - 18 V, at 200 - 250 mA supply for lighting the entire LED string. Each LED provides light with luminous flux of 44 lumens, amounting to a total of 440 lumens. It is well suited for general purpose lighting. The peak forward current and peak power dissipation are 150 mA and 420 mW respectively at absolute maximum ratings of 25°C and 120 mA. The maximum anticipated increase in the level of voltage is 21 V. Current limiting resistors are given in series to the string for protection.

6.5 Experimental Set up to Power White LEDs by Harnessing Solar Energy

The converter is tested in presence of solar light as shown in Figure 6.18 using 12 V battery source and 12 V solar panel as input voltage sources. The switching frequency is 10 kHz with a duty cycle of 50%. The main components include the circuit of the proposed topology for performing the fixed gain conversions, gating circuit that provides the gate signals for the switches, the sensing and display circuit for sensing the solar voltage and display it. A 12 V battery is used as constant voltage source and solar panel as variable source to power the switched capacitor converter. An LED module is used as the load for converter. The digital storage oscilloscope DSO - 5100A is used to view the input and output voltages.

Figure 6.18: Hardware Set Up of the Proposed Converter for Harnessing Solar Energy

6.5.1 Experimental Results Mode 1

The converter was tested to power white LEDs outside under sun as shown in Figure 6.18. The solar panel was mostly shaded forcefully to mimic Mode 1 since the desired solar voltage shall be less than 6 volts driving to the condition $V_{in2} \leq \frac{V_{out}}{3}$ as in Table

6.4, where V_{out} is desired as 18 V. In this case the sensed solar voltage was 5 V and the microcontroller will select Mode 1 operation of V_{in1}x1.5. The actual measured battery voltage was 12.8 V and therefore the expected theoretical output voltage V_{out} is 19.2 V. The experimental output voltage is measured as 17.6 V driving a current of 200 mA in this mode. The efficiency for this case can be calculated using Equation 5.1 and found to be 91.6%. The efficiency of the same converter from Table 5.3 was around 83% for an input of 6 V. The increase in efficiency can be due to the decrease in R_{out} by selecting the flying capacitor value as 47μF in place of 22μF for the experiments referring to Equation (5.31). The results are shown in Figure 6.19.
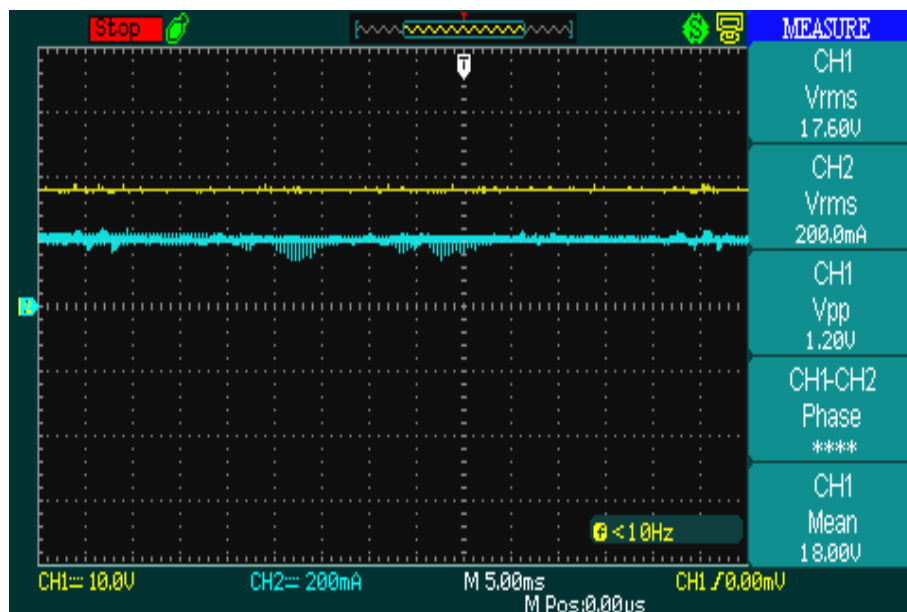
Figure 6.19: Hardware Results for Mode 1 with Battery Alone

6.5.2 Experimental Results Mode 2

When the solar input voltage sensed is in the range of 6 V to 9 V as modeled in the condition $\frac{V_{out}}{3} \leq V_{in2} \leq \frac{V_{out}}{2}$ in Table 6.4, the microcontroller forces the converter to select Mode 2 operation which is (V_{in1} + V_{in2}). The sensed solar voltage in this case is 7 V. The actual measured battery voltage was 12.8 V and therefore the expected theoretical output voltage V_{out} is 19.8 V. The experimental output voltage is measured as 18 V driving a current of around 250 mA in this mode. The efficiency of the converter in this case from Equation 5.1 is 90.9%. The results are shown in Figure 6.20.
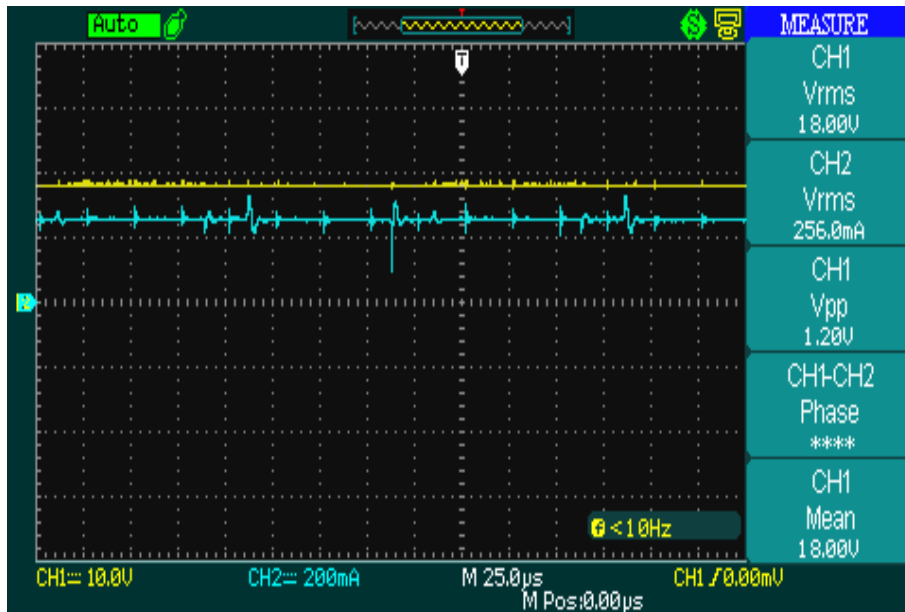
Figure 6.20: Hardware Results for Mode 2 with Battery and Solar Source

6.5.3 Experimental Results Mode 3

When the solar input voltage sensed is in the range of 9 V to 12 V as modeled in the condition $\frac{V_{out}}{2} \leq V_{in2} \leq \frac{2V_{out}}{3}$ in Table 6.4, the microcontroller forces the converter to select Mode 3 operation which is $V_{in2}\mathbf{x}2$. The sensed solar voltage in this case is 10 V and therefore the expected theoretical output voltage V_{out} is 20 V. The experimental output voltage is measured as 17.6 V driving a current of around 250 mA in this mode. The efficiency calculated from Equation 5.1 is 88%. The results are shown in Figure 6.21
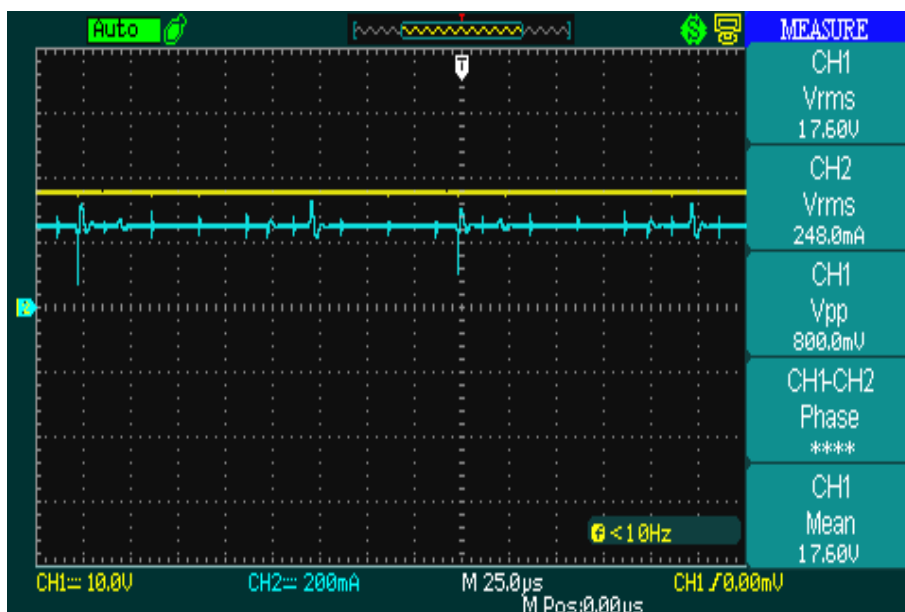
Figure 6.21: Hardware Results for Mode 3 with Battery and Solar Source

6.5.4 Experimental Results Mode 4

When the solar input voltage sensed is 12 V or greater, as modeled in the condition $V_{in2} \geq \frac{2V_{out}}{3}$ in Table 6.4, the microcontroller forces the converter to select Mode 4 operation which is V_{in2}x1.5. The actual measured solar voltage was 12.8 V and the expected theoretical output voltage V_{out} is 19.2 V. The experimental output voltage is measured as 17.6 V driving a current of 200 mA in this mode. It may be noted here that Mode 1 and Mode 4 are the same modes except that in the first case the load is powered by battery source and in the second case it is from solar source. The efficiency in this case using Equation 5.1 is found to be 91.6%. The results are shown in Figure 6.22.
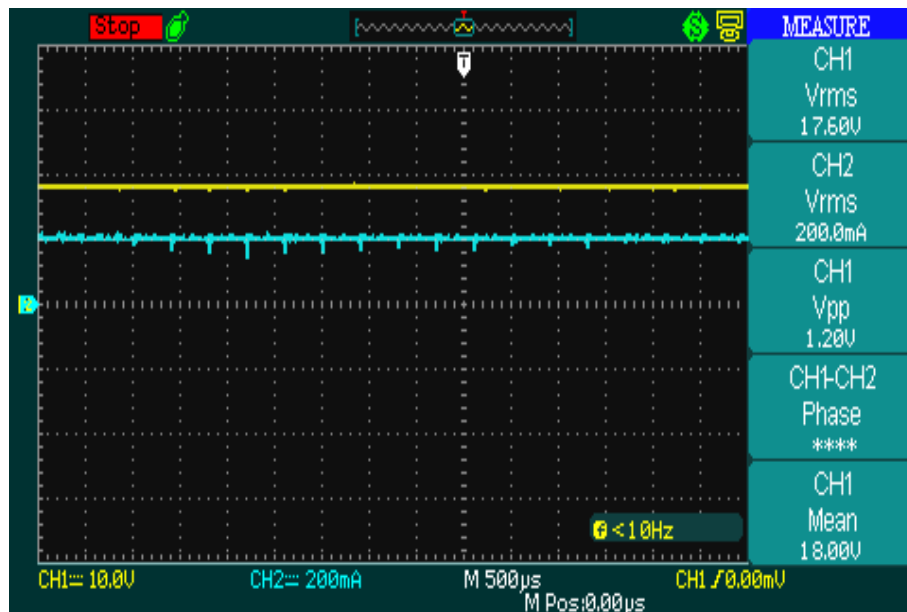
Figure 6.22: Hardware Results for Mode 4 with Battery and Solar Source

6.5.5 Efficiency and Output Voltage Comparison for the Four Modes

The efficiency and the variation of output voltages for various load current is compiled and presented in Figure 6.23. The load current is varied using rheostats in the range of 50 mA to 300 mA. Since the solar input is continuously varying it is taken as 12.8 V same as battery in Mode 1 and 4. In Mode 2, the solar voltage is fixed at 8 V and in Mode 3 it is taken as 10 V. The solar voltages of 12.8 V, 8 V and 10 V is mimicked through a laboratory dual power supply. The Figure 6.23a shows that the output voltage is maximum in Mode 2. It is true because the input voltage itself in this mode is the highest among all the modes which is the sum of 12.8 V and 8 V. Similarly, in Mode 3

the output voltage is in the range of 17 V to 18.2 V and in Mode 1 and 4 it is in the range of 16.8 V to 18 V. It can be seen that the input voltage is maximum for Mode 2 (12.8 V + 8 V) and therefore the output voltage is also maximum among all modes but not the maximum in that particular mode. Hence efficiency is less in Mode 2. This argument is applicable for Mode 3 also. However for an input voltage of 12.8 V, Mode 1, 4 gives the maximum voltage in that particular mode and hence efficiency if maximum. The drop in voltage is in the diodes of the circuit. Referring to 6.23b the efficiency is in the range of 80% to 92% from light load of 50 mA to maximum load of 300 mA. A comparison of efficiency comparing Table 5.3 when the input was 6 V shows that it has improved slightly in this case since the flying capacitor value selected is 47 μF here against 27 μF in Chapter 5 experiments. A higher value of flying capacitor reduces the converter equivalent resistance R$_{out}$ which can be verified from Equation (5.34). This in turn will increase the output voltage and efficiency.

A comparison of efficiency for various VCRs is performed. Since the ratings of the compared converters are different efficiency also may vary. However, to show a trend the comparison between earlier three converters and proposed converter is compiled in Table 6.5. Few of the earlier reported converters have compiled the overall efficiency and in the proposed converter the gating circuit efficiency is not considered.

Table 6.5: Comparison of VCR and Efficiency of few SCC Topologies

Converter Type	Voltage Conversion Ratio	Efficiency
(Le, 2015)	$\frac{1}{3}$, $\frac{2}{5}$	73%, 74.3% (overall)
(Yuanmao and Cheng, 2012)	$\frac{1}{2}$	84% (Excluding Gating Circuit)
(Max1910, 2004)	$\frac{1}{2}$, 2	70%, 75% (overall)
This Work	$\frac{3}{2}$, 2	90%, 85% (Excluding Gating Circuit)
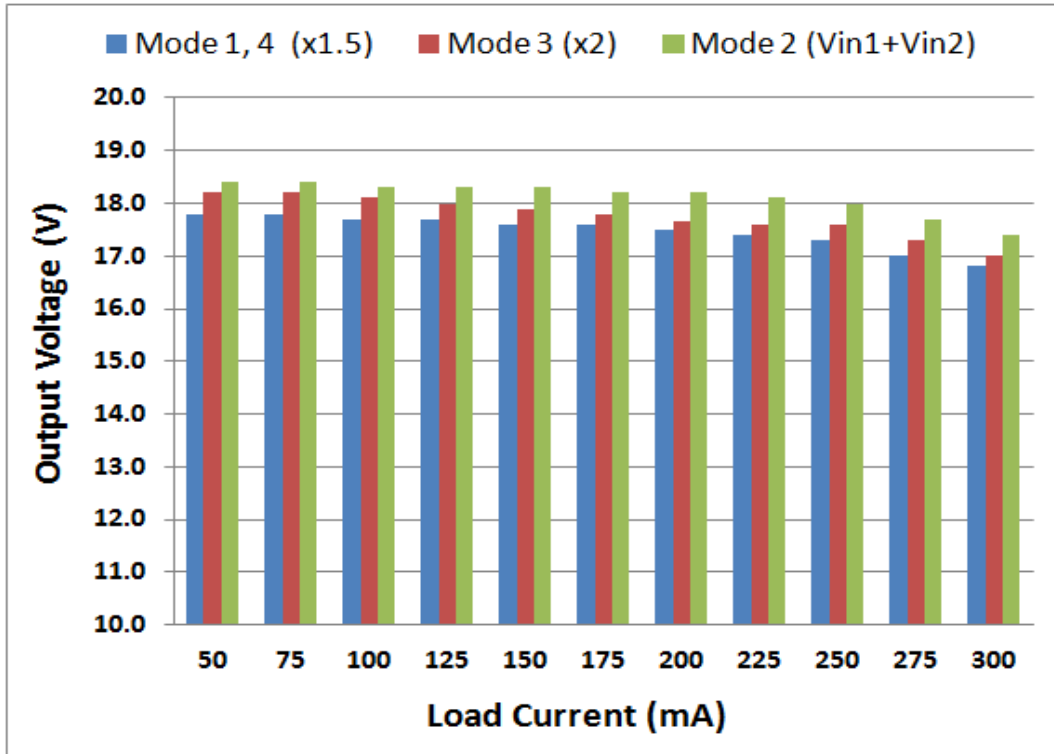
(a) Variation of Output Voltage with Load Current
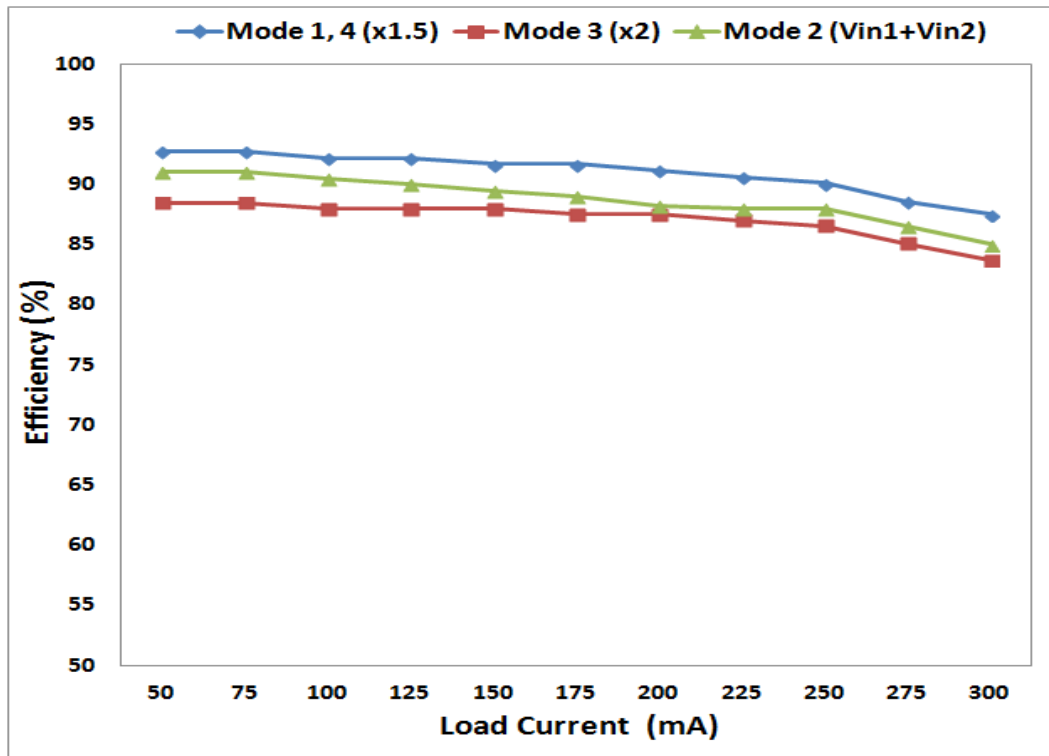
(b) Variation of Efficiency with Load Current

Figure 6.23: Efficiency and Output Voltage Comparison with Load Current

6.6 Discussion on the Regulation Capability in the Proposed SCC

Maintaining a constant voltage at the output terminals is one of the parameters which is used to measure the quality of power converters. Thus in any converter inductor or SCC based, voltage regulation capability is of significance. There are two classical regulation schemes namely,

- Load Regulation
- Line Regulation

The load regulation capability of a power converter is defined as the ability to maintain a constant voltage at the output terminals despite a change in load parameters which is the basically the resistance. The line regulation scheme is a measure of the ability of the converter to maintain a constant voltage at the output due to change in input voltage. Both the regulation capabilities can be achieved in this converter. Few other SCC control schemes for regulation are discussed in (Wu *et al.*, 2016; Yang *et al.*, 2016; Evzelman and Zane, 2016; Uno and Sugiyama, 2017).

6.6.1 Load Regulation Capability

One possible method to regulate the output voltage due to changes in the load parameters is to vary the switching frequency of the converter. Referring to Equation (5.31), it can be seen that the equivalent converter resistance "R_{out}" in Figure 5.3 is inversely dependent on switching frequency "f_s" and flying capacitor "C" values. Usually the flying capacitor values will be fixed and it is possible to vary the switching frequency f_s. This will change the values of R_{out}. The effect of this variation can be observed from Table 5.2. A plot of the variation of "R_{out}" and "f_s" is shown in Figure 6.24. It can be seen that during higher switching frequencies R_{out} decreases and the explanation for the same can be found in Chapter 5 Section 5.6.2.
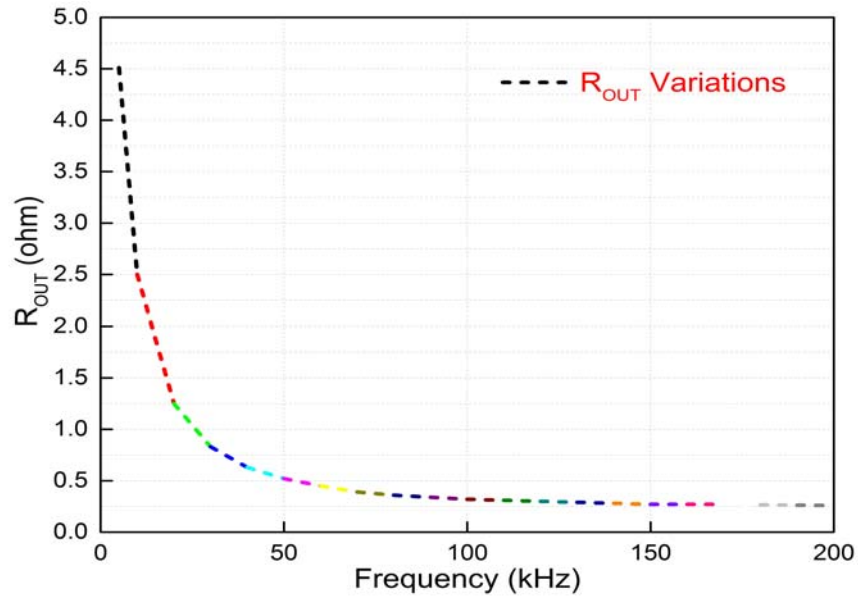
Figure 6.24: Variation of Equivalent Resistance R$_{out}$ with Switching Frequency f$_s$

6.6.2 Line Regulation Capability

The variations in input line voltage can be regulated by sensing the input voltage as discussed in Table 6.4. The converter put forward altogether 15 VCRs of operation and according to the variations of the input voltage any of these modes can be selected to keep the output voltage constant. This method is demonstrated in Section 6.5.

6.7 Conclusion

This chapter discuss the possibility of extension of VCRs of the proposed converter from 11 to 15 which includes an inversion mode if additionally one more switch is added. The implementation results shows good potential for the additional modes. Thus the converter with 10 switches and 2 flying capacitors is capable of generating 15 VCRs. The diodes used can be removed if CMOS type of switches are used. This will not only increase the efficiency but also reduce the PCB space. An application of the converter to power white LEDs by harnessing solar energy is also demonstrated. The battery and solar source is optimally used by sensing the availability of solar energy and forcing the converter to utilize it to the maximum. The regulation methods, load and line regulation capability of the converter is also discussed in this chapter.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1   Conclusions

This research has provided an insight into the exciting new areas of Switched Capacitor Converters (SCC), potential enough to replace the inductor based conventional converters. There are numerous low power applications where SCC due to its high energy density, compact size (due to absence of inductors) and easy on chip integration can be a preferred choice. The thesis is consolidated in seven chapters. A thorough review about the basic working principle, types of SC converters and accepted equivalent circuit representation has been extensively covered in the first two chapters. Few industrial SCC based regulators are also highlighted.

Different types of SCC topology which are available in the literature has been studied from the basics through simulating and prototype hardware development for verifying the feasibility of SCC when this topic was first dealt. In Chapter 3, few such converters that can work in buck or boost or inverting mode has been realized. For fixed target application where flexibility is of less concern, such converters are suited. However, the converters occupies more PCB space if multiple Voltage Conversion Ratio (VCR) has to be realized. The above limitation has opened the scope to develop new SCC topologies with the prime focus to achieve maximum VCRs with reduced switch counts or electronic components. The ability of the converter to accept and be able to be powered from multiple sources in tandem add another figure of merit to the flexibility of the converter. A step down converter (buck) that can generate 3 VCRs and a unity gain which can be operated from two sources if desired is dealt in Chapter 4. An attempt to develop a theoretical framework for establishing a converter model using the differential charge technique is presented. The framework details the procedure but better accurate model is to be realized for establishing the validation between theoretical, simulated and hardware results. Surpassing the above limitations has been the focus while developing the new converter presented in Chapter 5.

The most significant contribution in this research work has been the development of a new series parallel buck - boost based SCC that can work on simultaneously two sources providing the ability to tap renewable energy like solar if used as one of the sources as reported in Chapter 5. A detailed mathematical model of the new converter based on the average current conduction loss analysis and step to step development sequence has been detailed. The model of the converter is accurately derived and represented as an equivalent output resistance R_{out} taking into account both switch resistances and capacitors ESR. The simplicity of the converter due to its two phase switching and less switch count while delivering 11 output VCRs is the advantage. In any operating phase 'i' of the SCC corresponding to a time period T_i, if the charging and discharging process in the flying capacitor is fully completed then the converter is operating in the CC (Complete Charge) state or SSL (Slow Switching Limit). Similarly if the charging and discharging is partially completed then it is operating in the PC (Partial Charging) state. Finally, if the capacitor current is constant then it is operating in the NC (No charging) or FSL (Fast Switching Limit). The mathematical model developed for the new converter presented in Chapter 5, can be useful for analysis and prediction of various performance parameters like efficiency, effect of varying switching frequency, behavior of flying capacitor current, selection of flying capacitor values and the important aspect of regulation capability using variable switching frequency. Theoretical, simulated and experimental result concur well to propose this new converter as a potential replacement of traditional buck inductor based converters. The converter open loop efficiency is in the range of 85%. Further, in Chapter 6, a CMOS implementation of the converter along with extension of VCRs is demonstrated making the converter very much suitable in low power applications with improved efficiency of 95% above. A practical application to power LEDs using this new converter is demonstrated by developing a prototype hardware circuit using MOSFET switches. Here the regulation of output voltage is achieved by sensing the input voltage and selectively switching to the required VCR for the required boost gain to retain a constant output voltage. This work demonstrates the potential of SCC but it is only a small step in understanding the higher capabilities of these family of converters.

7.2   Future Work

This section discusses the possible future improvements on the converter that has been presented in this work along with possible extension and new application domain.

- One of the factors that favored high current applications in traditional converters is the presence of inductors. SCC eliminate the use of inductors. Hence to improve the current handling capability, one possible way is to use high current capacity controlled bidirectional switches instead of MOSFETs and better current carrying CMOS switches. This can add more power handling capability to the converter.

- Another inherent drawback of SCC is the limited voltage regulation capability compared to inductor type converters. In Inductor type converters, regulation of output voltage can be directly achieved by controlling the duty cycle ratio. One possible solution to overcome this disadvantage in SCC is to add more VCRs. Extension of furthermore VCRs can be explored in the presented converter. Similarly, development of more efficient regulation techniques can be another feature that can be explored in SC converter presented here.

- In most SCC only two phase gating is used. However, use of multiple phase gating can make the converter more efficient, selective and competent. Multiple phase gating technique has made the Fibonacci SCC to deliver more VCRs. Hence this gating technique can be incorporated in the proposed converter which may give more VCRs.

- The converter used in this work switches in the hard switch mode. This may increase the switch stress and lowers efficiency. Understanding the switch stress, using resonant concepts in switching, can further increase the reliability and life of the presented converter.

- Any attempt to reduce the components used in SCC like the number of switches, flying capacitors, but not comprising the expected features of maximum VCRs,

can further reduce the circuit board size and making the converter still compact. Thus as a future work, the optimization of the components of the converter can be studied.

- Bidirectional SCC are gaining popularity among researchers and the possibility of extending the proposed converter to transfer energy from source to load and load to source, both realized in the same SCC can be studied as a future work.

- An attempt has been made to replace the MOSFET switches with CMOS switches in Chapter 6. In Chapter 2, Section 2.3.4, few industrial regulators by reputed manufacturers has come out in IC form. As a future work IC implementation of the proposed converter can be considered.

- SCC is finding application in bio-medical domain nowadays, where there is stringent requirement of miniaturizing the gadgets. To power such sensitive and small gadgets, SCC can be an alternative. Thus the scope of SCC is tremendous due to the absence of inductors and associated magnetics. Higher power densities and ease of on chip integration can further expand the potential of these converters.

Programming Code for Microcontrollers AT89S8253 Used in Chapter 6

```
MICROCONTROLLER 1


;AT 89S8253
ORG 0000H
;  BYTE Register
P0        DATA    80H
P1        DATA    90H
P2        DATA    0A0H
P3        DATA    0B0H


RD        BIT     0B7H
WR        BIT     0B6H
T1        BIT     0B5H
T0        BIT     0B4H
INT1      BIT     0B3H
INT0      BIT     0B2H
TXD       BIT     0B1H
RXD       BIT     0B0H


PSW       DATA    0D0H
CY        BIT     0D7H
AC        BIT     0D6H
F0        BIT     0D5H
RS1       BIT     0D4H
RS0       BIT     0D3H
OV        BIT     0D2H
P         BIT     0D0H


ACC       DATA    0E0H
```

```
B        DATA    0F0H

SP       DATA    81H

DPL      DATA    82H

DPH      DATA    83H

PCON     DATA    87H

CKCON    DATA    8FH


;----------------- TIMERS registers --------------------

TCON     DATA    88H

TF1      BIT     8FH

TR1      BIT     8EH

TF0      BIT     8DH

TR0      BIT     8CH

IE10     BIT     8BH

IT1      BIT     8AH

IE00     BIT     89H

IT0      BIT     88H


TMOD     DATA    89H


T2CON    DATA    0C8H

TF2      BIT  0CFH

EXF2     BIT  0CEH

RCLK     BIT  0CDH

TCLK     BIT  0CCH

EXEN2    BIT  0CBH

TR2      BIT  0CAH

C_T2     BIT  0C9H

CP_RL2   BIT  0C8H


T2MOD    DATA 0C9H

TL0      DATA    8AH

TL1      DATA    8BH
```

```
TL2  DATA 0CCH

TH0     DATA     8CH

TH1     DATA     8DH

TH2  DATA 0CDH

RCAP2L   DATA 0CAH

RCAP2H   DATA 0CBH




;------------------ UART registers ----------------------

SCON    DATA    98H

SM0   BIT  9FH

FE    BIT 9FH

SM1   BIT 9EH

SM2   BIT 9DH

REN   BIT 9CH

TB8   BIT 9BH

RB8   BIT 9AH

TI    BIT 99H

RI    BIT 98H


SBUF    DATA    99H

SADEN   DATA 0B9H

SADDR   DATA 0A9H



;------------------- FLASH EEPROM registers ------------

AUXR   DATA 08EH



;------------------- IT registers ----------------------


IP  DATA 0B8H

IE   DATA 0A8H


;  IE
```

```
EA    BIT  0AFH

EC    BIT  0AEH

ET2   BIT  0ADH

ES    BIT  0ACH

ET1   BIT  0ABH

EX1   BIT  0AAH

ET0   BIT  0A9H

EX0   BIT  0A8H


;------------------ SPI registers ------------------------

SPCR EQU 0D5H

SPSR EQU 0AAH

SPDR EQU 86H


SPCON EQU 0D5H

SPSTA EQU 0AAH

SPDAT EQU 86H

;------------------ WATCHDOG registers ----------------------


WDTCON  DATA  0A7H  ; watchdog control register

WDTRST  DATA  0A6H  ; watchdog reset register

WDTEN  EQU  00000001B  ; watchdog timer enable bit

WSWRST  EQU  00000010B  ; watchdog timer software reset bit

HWDT  EQU  00000100B  ; watchdog timer hardware mode bit

PS0  EQU  00100000B  ; watchdog timer period select bits

PS1  EQU  01000000B  ;

PS2  EQU  10000000B  ;


;.................................................


SW1 EQU P1.3

SW2 EQU P1.4
```

```
SW3 EQU P1.5
SW4 EQU P1.6
SW5 EQU P1.7


SW6 EQU P3.0
SW7 EQU P3.1
SW8 EQU P3.2
SW9 EQU P3.3
SW10 EQU P3.4
SW11 EQU P3.5


S1A EQU P0.0
S1B EQU P0.1
S2A EQU P0.2
S2B EQU P0.3
S3A EQU P0.4
S3B EQU P0.5
S4A EQU P0.6
S4B EQU P0.7


S5A EQU P2.7
S5B EQU P2.6
S6A EQU P2.5
S6B EQU P2.4
S7A EQU P2.3
S7B EQU P2.2
S8A EQU P2.1
S8B EQU P2.0


S9A EQU P3.4
S9B EQU P3.5
S10A EQU P3.6
S10B EQU P3.7
```

```
DLH EQU 08H
DLM EQU 09H
DLL EQU 0AH


ST1ON EQU 0BH
ST2ON EQU 0CH
ST1OF EQU 0DH
ST2OF EQU 0EH
ST3ON EQU 0FH
ST3OF EQU 10H


BOOST EQU 00H
;................................................................
ORG 0000H
MOV P0,#0FFH
MOV P2,#0FFH
MOV P1,#0FFH
MOV P3,#0FFH
AJMP BOOT
;................................................................
ORG 001BH


MOV P0,#0FFH
MOV P2,#0FFH
MOV P3,#0FFH
NOP
NOP


JBC F0,DIS


SETB F0 ; CHG
```

```
        MOV P0,ST1ON

        MOV P2,ST2ON

        MOV P3,ST3ON

        RETI


DIS:    MOV P0,ST1OF

        MOV P2,ST2OF

        MOV P3,ST3OF

        RETI
;..............................................................
        ORG 0050H

BOOT:   MOV SP,#0A0H ; SYS INIT
;..............................................................
; TIMERS AND INTERRUPT

        CLR C_T2 ; T2 CLK OUT

        MOV T2MOD,#02H

        MOV RCAP2H,#0FFH ; f = FXTL / 4 * (65536-[TH2 TL2])

        MOV RCAP2L,#6AH ; FF6A = 20kHz @ 12MHz IN X1 MODE

        SETB TR2


;..............................................................


        MOV TMOD,#20H

        MOV TH1,#156

        MOV TL1,#156

        CLR TR1

        MOV IE,#88H


;..............................................................


        MOV P0,#0FFH ; 2V1 MODE

        MOV P2,#0FFH ; ALL SW OFF

        SETB F0 ; STATUS FLG
```

```
MOV ST1ON,#0FFH ;

MOV ST2ON,#0FFH ;

MOV ST3ON,#0FFH

MOV ST1OF,#0FFH ;

MOV ST2OF,#0FFH ;

MOV ST3OF,#0FFH


ACALL DLY
;.........................................................................


KEY: JNB SW1,MOD1

JNB SW2,MOD2

JNB SW3,MOD3

JNB SW4,MOD4

JNB SW5,MOD5

SJMP KEY


DBNCE: ACALL DLY

SJMP KEY
;.........................................................................
; V2 < VOUT/3
; 1.5V1 + 0V2
MOD1: MOV ST1ON,#0CH

MOV ST2ON,#0FFH

MOV ST3ON,#0FH


MOV ST1OF,#0FCH

MOV ST2OF,#00H

MOV ST3OF,#0CFH


SETB TR1

AJMP DBNCE
```

```
;..............................................................

; VOUT/3 < V2 < VOUT/2
; V1+V2
MOD2: MOV ST1ON,#0CCH
MOV ST2ON,#0FCH
MOV ST3ON,#3FH


MOV ST1OF,#0F3H
MOV ST2OF,#30H
MOV ST3OF,#0FFH


SETB TR1
AJMP DBNCE
;..............................................................
; V2 = VOUT/2
; 2 V2
MOD3: MOV ST1ON,#0C3H
MOV ST2ON,#0FCH
MOV ST3ON,#3FH


MOV ST1OF,#0F3H
MOV ST2OF,#30H
MOV ST3OF,#0FFH
SETB TR1
AJMP DBNCE
;..............................................................
; VOUT/2 <V2 < 2VOUT /3
; V1 + 0.5V2
MOD4: MOV ST1ON,#03H
MOV ST2ON,#0FFH
MOV ST3ON,#0FH
```

```
MOV ST1OF,#0FCH

MOV ST2OF,#00H

MOV ST3OF,#0CFH


SETB TR1

AJMP DBNCE

;.................................................................
; V2 > 2VOUT /3
; 1.5 V2
MOD5: MOV ST1ON,#03H

MOV ST2ON,#0FFH

MOV ST3ON,#0FH


MOV ST1OF,#0F3H

MOV ST2OF,#00H

MOV ST3OF,#0CFH


SETB TR1

AJMP DBNCE

;.................................................................


DLY: MOV DLH,#100

DL1: MOV DLM,#100

DL2: MOV DLL,#100

DL3: DJNZ DLL,DL3

DJNZ DLM,DL2

DJNZ DLH,DL1

RET


;.................................................................


END
```

```
MICROCONTROLLER 2


; AT 89S8253

; LCD 8-bit

; ADC 4-ch Mux

; PWM T0, UP P3.7, DN,P3.6


ORG 0000H

;   BYTE Register

P0        DATA    80H

P1        DATA    90H

P2        DATA    0A0H

P3        DATA    0B0H


RD        BIT     0B7H

WR        BIT     0B6H

T1        BIT     0B5H

T0        BIT     0B4H

INT1      BIT     0B3H

INT0      BIT     0B2H

TXD       BIT     0B1H

RXD       BIT     0B0H


PSW       DATA    0D0H

CY        BIT     0D7H

AC        BIT     0D6H

F0        BIT     0D5H

RS1       BIT     0D4H

RS0       BIT     0D3H

OV        BIT     0D2H

P         BIT     0D0H


ACC       DATA    0E0H
```

```
B        DATA    0F0H

SP       DATA    81H

DPL      DATA    82H

DPH      DATA    83H

PCON     DATA    87H

CKCON    DATA    8FH


;------------TIMERS registers ------------

TCON     DATA    88H

TF1      BIT     8FH

TR1      BIT     8EH

TF0      BIT     8DH

TR0      BIT     8CH

IE10     BIT     8BH

IT1      BIT     8AH

IE00     BIT     89H

IT0      BIT     88H


TMOD     DATA    89H


T2CON    DATA    0C8H

TF2      BIT  0CFH

EXF2     BIT  0CEH

RCLK     BIT  0CDH

TCLK     BIT  0CCH

EXEN2    BIT  0CBH

TR2      BIT  0CAH

C_T2     BIT  0C9H

CP_RL2   BIT  0C8H


T2MOD    DATA 0C9H

TL0      DATA    8AH

TL1      DATA    8BH
```

```
TL2  DATA 0CCH

TH0     DATA    8CH

TH1     DATA    8DH

TH2  DATA 0CDH

RCAP2L  DATA 0CAH

RCAP2H  DATA 0CBH



;------------ UART registers ------------

SCON    DATA    98H

SM0  BIT  9FH

FE    BIT 9FH

SM1  BIT 9EH

SM2  BIT 9DH

REN  BIT 9CH

TB8  BIT 9BH

RB8  BIT 9AH

TI   BIT 99H

RI   BIT 98H


SBUF    DATA    99H

SADEN  DATA 0B9H

SADDR  DATA 0A9H

------- FLASH EEPROM registers ------------

AUXR   DATA 08EH


;------- IT registers -------------------


IP  DATA 0B8H

IE   DATA 0A8H


;  IE

EA    BIT  0AFH
```

```
EC    BIT  0AEH

ET2   BIT  0ADH

ES    BIT  0ACH

ET1   BIT  0ABH

EX1   BIT  0AAH

ET0   BIT  0A9H

EX0   BIT  0A8H


;----------- SPI registers ----------
SPCR EQU 0D5H

SPSR EQU 0AAH

SPDR EQU 86H


SPCON EQU 0D5H

SPSTA EQU 0AAH

SPDAT EQU 86H
;----- WATCHDOG registers -------------


WDTCON  DATA  0A7H  ; watchdog control register

WDTRST  DATA  0A6H  ; watchdog reset register

WDTEN  EQU  00000001B  ; watchdog timer enable bit

WSWRST  EQU  00000010B  ; watchdog timer software reset bit

HWDT  EQU  00000100B  ; watchdog timer hardware mode bit

PS0  EQU  00100000B  ; watchdog timer period select bits

PS1  EQU  01000000B  ;

PS2  EQU  10000000B  ;


CLKREG EQU 8FH
;...........................................
ADC EQU P1 ; *****
INTR EQU P0.1 ; *****


; SW1 EQU P1.3 ; M1
```

```
; SW2 EQU P1.4 ; M2
; SW3 EQU P1.5 ; M3
; SW4 EQU P1.6 ; M4
; SW5 EQU P1.7 ; M5


MOD1 EQU P0.0
MOD2 EQU P0.5
MOD3 EQU P0.2
MOD4 EQU P0.3
MOD5 EQU P0.4



LCD     EQU  P2 ; LCD
EN EQU P2.3
RW EQU P2.2
RS EQU P2.1
LCDR EQU 08H
LCDTMP EQU 09H


;...............................................................

DLL EQU 0AH
DLM EQU 0BH
DLH EQU 0CH


VTG EQU 0DH


;...........................................................

ORG  0000H
BOOT: CLR INTR
MOV SP,#40H ; SP = 0A0H
ACALL LINI
```

```asm
MOV P0,#0FFH

;........................................
START: ACALL LN1
MOV A,ADC
MOV VTG,A
ACALL BCDV
MOV DPTR,#MSG1
ACALL MSG

MOV A,VTG
SUBB A,#60 ; IS V2 < 6
JC MODE1

MOV A,VTG
SUBB A,#90 ; IS V2 < 9
JC MODE2

MOV A,VTG
SUBB A,#119 ; IS V2 < 11.9
JC MODE3

MOV A,#'5'
ACALL DSP

MOV P0,#0FFH
CLR MOD5

PROS: ACALL DLY
AJMP START

;........................................
```

```
MODE1: MOV A,#'1'
ACALL DSP

MOV P0,#0FFH
CLR MOD1
SJMP PROS


MODE2: MOV A,#'2'
ACALL DSP

MOV P0,#0FFH
CLR MOD2
SJMP PROS


MODE3: MOV A,#'3'
ACALL DSP

MOV P0,#0FFH
CLR MOD3
SJMP PROS


MODE4: MOV A,#'4'
ACALL DSP

MOV P0,#0FFH
CLR MOD4
SJMP PROS


;.......................................................

LINI: MOV A,#20H ; DL=0, 4BIT, 1 LINE,5X7
```

```
        ACALL CMD

        MOV A,#20H ; DL=0, 4BIT, 1 LINE,5X7

        ACALL CMD

        MOV A,#20H ; DL=0, 4BIT, 1 LINE,5X7

        ACALL CMD

        MOV A,#28H ; DL=0, 4BIT, 2 LINE,5X7

        ACALL CMD

        MOV A,#06H ; INC DSP SHIFT

        ACALL CMD

        MOV A,#0CH ; DSP ON, CRSR OFF BLNK OFF

        ACALL CMD


        ;.............................................


DLR:    MOV  A,#01H ; LCD CLEAR SBR

CMD:    MOV LCDR,A ; PUSH ACC

ACALL  RDY  ; LCD COMMAND SBR

              CLR  RW

              CLR  RS


MOV A,LCDR

ANL A,#0F0H

MOV LCD,A

              SETB  EN

              CLR  EN


MOV A,LCDR ; POP A

SWAP A

ANL A,#0F0H

MOV LCD,A

              SETB  EN

              CLR  EN

              RET
```

```
SPACE: MOV A,#' '
DSP:   MOV LCDR,A ; PUSH ACC
ACALL  RDY  ; LCD COMMAND SBR
         CLR  RW
         SETB RS


      MOV A,LCDR
ANL A,#0F0H
MOV LCD,A
CLR  RW
         SETB RS
         SETB  EN
         CLR  EN


MOV A,LCDR ; POP A
SWAP A
ANL A,#0F0H
MOV LCD,A
         CLR  RW
         SETB RS
         SETB  EN
         CLR  EN
RET


RDY:     CLR  EN         ; LCD READY CHK SBR
         MOV  LCD,#0F0H
         CLR  RS
         SETB  RW


WAT:     SETB  EN
MOV A,LCD
CLR  EN          ; LCD WAIT SBR
```

```
        ANL A,#0F0H ; [A] X0
MOV LCDTMP,A


ORL LCD,#0F0H
SETB  EN
MOV A,LCD
CLR  EN        ; LCD WAIT SBR
ANL A,#0F0H ; [A] X0
SWAP A
ORL A,LCDTMP
        JB  ACC.7,WAT
        RET


;...............................................
LN1:    MOV  A,#80H       ; SELECT LINE 1 OF THE LCD
ACALL  CMD
        RET


LN2:    MOV  A,#0C0H      ; SELCTS THE LINE OF THE LCD
ACALL  CMD
        RET


LN3: MOV  A,#90H
ACALL  CMD
        RET


LN4: MOV  A,#0D0H
ACALL  CMD
        RET


RO1:    MOV  A,#80H       ; SELECT ROW 1
        SJMP  ROMSG
```

```
RO3:    MOV  A,#90H     ; SELECT ROW 1
        SJMP  ROMSG


RO4:    MOV  A,#0D0H    ; SELECT ROW 1
        SJMP  ROMSG


RO2:    MOV  A,#0C0H   ; SELECT ROW 2
ROMSG: ACALL  CMD
;.....................................................


MSG:    ACALL  RDY     ; STRING WRITE SBR
        CLR  A
        MOVC  A,@A+DPTR
        CJNE  A,#0FFH,ST2
        RET


ST2:    ACALL  DSP
        INC  DPTR
        AJMP  MSG
;...............................................


BCDV: MOV B,#100
DIV AB
ADD A,#30H
ACALL DSP


MOV A,B
MOV B,#10
DIV AB
ADD A,#30H
ACALL DSP


MOV A,#'.'
```

```
        ACALL DSP

        MOV A,B
        ADD A,#30H
        ACALL DSP

        RET
;..............................................................
DLY: MOV DLH,#10
DL1: MOV DLM,#100
DL2: MOV DLL,#100
DL3: DJNZ DLL,DL3
        DJNZ DLM,DL2
        DJNZ DLH,DL1
        RET
;..............................................................
        MOV R7,A
ASC: DB '0123456789ABCDEF'
        MOV R7,A
MSG1: DB ' Mode - '
        MOV R7,A
;..............................................................

        END
```

REFERENCES

1. **Abutbul, O.**, **A. Gherlitz**, **Y. Berkovich**, and **A. Ioinovici** (2003). Step - up switching-mode converter with high voltage gain using a switched-capacitor circuit. *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, **50**(8), 1098 – 1102.

2. **Ajami, A.**, **H. Ardi**, and **A. Farakhor** (2015). A novel high step-up dc/dc converter based on integrating coupled inductor and switched-capacitor techniques for renewable energy applications. *IEEE Transactions on Power Electronics*, **30**(8), 4255 – 4263.

3. **Amjadi, Z.** and **S. S. Williamson** (2010). A novel control technique for a switched - capacitor - converter - based hybrid electric vehicle energy storage system. *IEEE Transactions on Industrial Electronics*, **57**(3), 926 – 934.

4. **ATMEL** (2006). 8 bit microcontroller. URL `http://www.atmel.com/images/doc3286.pdf`.

5. **Baughman, A. C.** and **M. Ferdowsi** (2008). Double - tiered switched - capacitor battery charge equalization technique. *IEEE Transactions on Industrial Electronics*, **55**(6), 2277 – 2285.

6. **Ben-Yaakov, S.** (2012). On the influence of switch resistances on switched - capacitor converter losses. *IEEE Transactions on Industrial Electronics*, **59**(1), 638 – 640.

7. **Ben-Yaakov, S.** and **M. Evzelman**, Generic and unified model of switched capacitor converters. *In Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE*. IEEE, 2009.

8. **Ben-Yaakov, S.** and **M. Evzelman**, Generic average modeling and simulation of the static and dynamic behavior of switched capacitor converters. *In Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE*. IEEE, 2012.

9. **Cervera, A.**, **S. S. Ben-Yaakov**, and **M. M. Peretz**, Single - stage switched-resonator converter topology with wide conversion ratio for volume - sensitive applications. *In Applied Power Electronics Conference and Exposition (APEC), 2017 IEEE*. IEEE, 2017*a*.

10. **Cervera, A.**, **M. M. Peretz**, and **S. Ben-Yaakov** (2017*b*). A generic and unified global - gyrator model of switched - resonator converters. *IEEE Transactions on Power Electronics*.

11. **Chandrakasan, A. P.**, **N. Verma**, and **D. C. Daly** (2008). Ultralow - power electronics for biomedical applications. *Annual Review of Biomedical Engineering*, **10**.

12. **Chang, L.**, **R. K. Montoye**, **B. L. Ji**, **A. J. Weger**, **K. G. Stawiasz**, and **R. H. Dennard**, A fully-integrated switched-capacitor 2 : 1 voltage converter with regulation capability and 90% efficiency. *In VLSI Circuits (VLSIC), 2010 IEEE Symposium on*. IEEE, 2010.

13. **Chau, K.** and **C. Chan** (2007). Emerging energy - efficient technologies for hybrid electric vehicles. *Proceedings of the IEEE*, **95**(4), 821 – 835.

14. **Chen, R.** and **H. Hashemi**, Analysis and synthesis of passive coupled - switched - capacitor - resonator - based rf filters. *In Circuits and Systems (ISCAS), 2016 IEEE International Symposium on*. IEEE, 2016.

15. **Cheung, C.-K.**, **S.-C. Tan**, **Y.-M. Lai**, and **K. T. Chi**, A new visit to an old problem in switched - capacitor converters. *In Circuits and Systems (ISCAS), Proceedings of 2010 IEEE International Symposium on*. IEEE, 2010.

16. **Choi, H.**, **M. Jang**, and **V. G. Agelidis** (2016). Zero current switching bidirectional interleaved switched capacitor dc - dc converter: analysis, design and implementation. *IET Power Electronics*, **9**(5), 1074 – 1082.

17. **Dagan, H.**, **A. Shapira**, **A. Teman**, **A. Mordakhay**, **S. Jameson**, **E. Pikhay**, **V. Dayan**, **Y. Roizin**, **E. Socher**, and **A. Fish** (2014). A low - power low - cost 24 ghz rfid tag with a c-flash based embedded memory. *IEEE Journal of Solid - State Circuits*, **49**(9), 1942 – 1957.

18. **Das, M.** and **V. Agarwal** (2016). Design and analysis of a high-efficiency dc - dc converter with soft switching capability for renewable energy applications requiring high voltage gain. *IEEE Transactions on Industrial Electronics*, **63**(5), 2936 – 2944.

19. **Dias, J. C.** and **T. B. Lazzarin**, Steady state analysis of voltage multiplier ladder switched - capacitor cell. *In Industry Applications (INDUSCON), 2016 12th IEEE International Conference on*. IEEE, 2016.

20. **Dickson, J. F.** (1976). On - chip high - voltage generation in mnos integrated circuits using an improved voltage multiplier technique. *IEEE Journal of Solid State Circuits*, **11**(3), 374 – 378.

21. **Dickson, J. F.** (1980). Voltage multiplier employing clock gated transistor chain. US Patent 4,214,174.

22. **Eguchi, K.**, **S. Pongswatd**, **K. Tirasesth**, **H. Sasaki**, **I. Oota**, and **T. Inoue** (2011). A switched - capacitor - based serial dc - dc converter using clean energy power supplies. *International Journal of Innovative Computing, Information and Control*, **7**(6), 3485 – 3498.

23. **Evzelman, M.** and **S. Ben-Yaakov** (2013). Average - current - based conduction losses model of switched capacitor converters. *IEEE Transactions on Power Electronics*, **28**(7), 3341 – 3352.

24. **Evzelman, M.** and **R. Zane**, Burst mode control and switched - capacitor converters losses. *In Applied Power Electronics Conference and Exposition (APEC), 2016 IEEE*. IEEE, 2016.

25. **FAN8301** (2008). *Non Synchronous Buck Regulator*. Fairchild. Online:http://mouser.com/ds/2/149/FAN8301-1006946.pdf.

26. **Forbes, L.** and **K. Y. Ahn** (2002). Efficient cmos dc - dc converters based on switched capacitor power supplies with inductive current limiters. US Patent 6,429,632.

27. **Gregoire, B. R.** (2006). A compact switched - capacitor regulated charge pump power supply. *IEEE Journal of Solid - State Circuits*, **41**(8), 1944 – 1953.

28. **Guo, F.**, **L. Fu**, **X. Zhang**, **C. Yao**, **H. Li**, and **J. Wang**, A family of dual - input dc - dc converters based on quasi-switched-capacitor circuit. *In Energy Conversion Congress and Exposition (ECCE), 2014 IEEE*. IEEE, 2014.

29. **Hamo, E.**, **A. Cervera**, and **M. M. Peretz** (2015*a*). Multiple conversion ratio resonant switched - capacitor converter with active zero current detection. *IEEE Transactions on Power Electronics*, **30**(4), 2073 – 2083.

30. **Hamo, E.**, **M. Evzelman**, and **M. M. Peretz** (2015*b*). Modeling and analysis of resonant switched - capacitor converters with free-wheeling zcs. *IEEE Transactions on Power Electronics*, **30**(9), 4952 – 4959.

31. **Hamo, E.**, **M. M. Peretz**, and **S. Ben-Yaakov**, Resonant binary and fibonacci switched - capacitor bidirectional dc - dc converter. *In Electrical and Electronics Engineers in Israel (IEEEI), 2012 IEEE 27th Convention of*. IEEE, 2012.

32. **Han, J.**, **A. von Jouanne**, and **G. C. Temes** (2006). A new approach to reducing output ripple in switched - capacitor - based step-down dc - dc converters. *IEEE Transactions on power electronics*, **21**(6), 1548 – 1555.

33. **HARADA, I.**, **F. UENO**, **T. INOUE**, and **I. OOTA** (1992). Characteristics analysis of fibonacci type sc transformer. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **75**(6), 655 – 662.

34. **He, L.**, **J. Zhang**, **T. Li**, *et al.* (2016). A bidirectional bridge modular switched - capacitor - based power electronics transformer. *IEEE Transactions on Industrial Electronics*.

35. **Henry, J. M.** and **J. W. Kimball** (2011). Practical performance analysis of complex switched - capacitor converters. *IEEE Transactions on Power Electronics*, **26**(1), 127 – 136.

36. **Hsieh, Y.-P.**, **J.-F. Chen**, **T.-J. Liang**, and **L.-S. Yang** (2012). Novel high step - up dc - dc converter with coupled-inductor and switched-capacitor techniques. *IEEE Transactions on Industrial Electronics*, **59**(2), 998 – 1007.

37. **Huang, Q.** and **M. Oberle** (1998). A 0.5 - mw passive telemetry ic for biomedical applications. *IEEE Journal Of Solid - State Circuits*, **33**(7), 937 – 946.

38. **Integrated, M.** (2016). Max4678. URL `https://datasheets.maximintegrated.com/en/ds/MAX4677-MAX4679.pdf`.

39. **Ioinovici, A.** (2001). Switched-capacitor power electronics circuits. *IEEE Circuits and Systems Magazine*, **1**(3), 37 – 42.

40. **Ioinovici, A.**, **H. S. Chung**, **M. S. Makowski**, and **K. T. Chi** (2007). Comments on unified analysis of switched - capacitor resonant converters. *IEEE Transactions on Industrial Electronics*, **54**(1), 684 – 685.

41. **Ioinovici, A.**, **C. K. Tse**, and **H.-H. Chung** (2006). Comments on" design and analysis of switched - capacitor - based step - up resonant converters". *IEEE Transactions on Circuits and Systems I: Regular Papers*, **53**(6), 1403.

42. **ITRS2.0** (2015). International technology road map for semiconductors 2.0. URL `http://www.itrs2.net//`.

43. **Jung, W.**, **S. Oh**, **S. Bang**, **Y. Lee**, **Z. Foo**, **G. Kim**, **Y. Zhang**, **D. Sylvester**, and **D. Blaauw** (2014*a*). An ultra - low power fully integrated energy harvester based on self - oscillating switched-capacitor voltage doubler. *IEEE Journal of Solid-State Circuits*, **49**(12), 2800 – 2811.

44. **Jung, W.**, **S. Oh**, **S. Bang**, **Y. Lee**, **D. Sylvester**, and **D. Blaauw**, 23.3 a 3nw fully integrated energy harvester based on self - oscillating switched-capacitor dc - dc converter. *In Solid - State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International*. IEEE, 2014*b*.

45. **Kesarwani, K.** and **J. T. Stauth**, A comparative theoretical analysis of distributed ladder converters for sub - module pv energy optimization. *In Control and Modeling for Power Electronics (COMPEL), 2012 IEEE 13th Workshop on*. IEEE, 2012.

46. **Kilani, D.**, **M. Alhawari**, **B. Mohammad**, **H. Saleh**, and **M. Ismail** (2016). An efficient switched - capacitor dc - dc buck converter for self - powered wearable electronics. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **63**(10), 1557 – 1566.

47. **Kim, M.-Y.**, **C.-H. Kim**, **J.-H. Kim**, and **G.-W. Moon** (2014). A chain structure of switched capacitor for improved cell balancing speed of lithium-ion batteries. *IEEE Transactions on Industrial Electronics*, **61**(8), 3989 – 3999.

48. **Kushnerov, A.** (2014). Multiphase fibonacci switched capacitor converters. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, **2**(3), 460 – 465.

49. **Kushnerov, A.** and **S. S. Ben-Yaakov** (2013). Unified algebraic synthesis of generalised fibonacci switched capacitor converters. *IET Power Electronics*, **7**(3), 540 – 544.

50. **Law, K.**, **K. E. Cheng**, and **Y. B. Yeung** (2005). Design and analysis of switched - capacitor - based step - up resonant converters. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **52**(5), 943 – 948.

51. **Le, H. P.** (2015). *Design Techniques for Fully Integrated Switched - Capacitor Voltage Regulators*. Ph.D. thesis, EECS Department, University of California, Berkeley. URL `http://www2.eecs.berkeley.edu/Pubs/TechRpts/2015/EECS-2015-21.html`.

52. **Le, H.-P.**, **M. Seeman**, **S. R. Sanders**, **V. Sathe**, **S. Naffziger**, and **E. Alon**, A 32 nm fully integrated reconfigurable switched - capacitor dc - dc converter delivering 0.55 w/mm2 at 81% efficiency. *In Solid - State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International*. IEEE, 2010.

53. **Lee, E. S.**, **B. H. Choi**, **D. T. Nguyen**, **G. C. Jang**, and **C. T. Rim** (2016). Versatile led drivers for various electronic ballasts by variable switched capacitor. *IEEE Transactions on Power Electronics*, **31**(2), 1489 – 1502.

54. **Lee, Y.-S.**, **Y.-Y. Chiu**, and **M.-W. Cheng**, Zcs switched - capacitor bi-directional quasi - resonant converters. *In Power Electronics and Drives Systems, 2005. PEDS 2005. International Conference on*, volume 2. IEEE, 2005.

55. **Lei, K.-M.**, **H. Heidari**, **P.-I. Mak**, **M.-K. Law**, **F. Maloberti**, and **R. P. Martins**, 28.1 a handheld 50pm - sensitivity micro - nmr cmos platform with b-field stabilization for multi - type biological/chemical assays. *In Solid - State Circuits Conference (ISSCC), 2016 IEEE International*. IEEE, 2016*a*.

56. **Lei, K. M.**, **H. Heidari**, **P.-I. Mak**, **M.-K. Law**, **F. Maloberti**, and **R. P. Martins** (2017). A handheld high-sensitivity micro-nmr cmos platform with b - field stabilization for multi - type biological/chemical assays. *IEEE Journal of Solid-State Circuits*, **52**(1), 284 – 297.

57. **Lei, Y.**, **R. May**, and **R. Pilawa-Podgurski** (2016*b*). Split - phase control: Achieving complete soft-charging operation of a dickson switched-capacitor converter. *IEEE Transactions on Power Electronics*, **31**(1), 770 – 782.

58. **Li, K.**, **M. Chen**, **J. Hu**, and **A. Ioinovici**, Mixed switched-capacitor based high conversion ratio converter and generalization for renewable energy applications. *In Energy Conversion Congress and Exposition (ECCE), 2016 IEEE*. IEEE, 2016.

59. **Liang, T.-J.**, **S.-M. Chen**, **L.-S. Yang**, **J.-F. Chen**, and **A. Ioinovici** (2012). Ultra - large gain step-up switched - capacitor dc - dc converter with coupled inductor for alternative sources of energy. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **59**(4), 864 – 874.

60. **LM2788** (2013). *120 mA High Efficiency Step-Down Switched Capacitor Voltage Converter*. Texas Instruments. Online:http://ti.com/lit/ds/symlink/lm2788.pdf.

61. **LMZ12001** (2010). *Switched Power Module*. Texas Instruments. Online:http://ti.com/lit/ds/snvs651f/snvs651f.pdf.

62. **Lopez, A.**, **R. Diez**, **G. Perilla**, and **D. Patino** (2012). Analysis and comparison of three topologies of the ladder multilevel dc - dc converter. *IEEE Transactions on Power Electronics*, **27**(7), 3119 – 3127.

63. **LT1054** (2015). *Switched Capacitor Voltage Converters with Regulators*. Texas Instruments. Online:http://ti.com/lit/ds/symlink/lt1054.pdf.

64. **LTC1044** (2011). *Switched Capacitor Voltage Converter*. Linear Technologies. Online:http://cds.linear.com/docs/en/datasheet/lt1044.pdf.

65. **LTC3115-1** (2012). *Synchronous Buck Boost Converter*. Linear Technology. Online:http://analog.com/media/en/technical-documentation/data-sheets/31151fb.pdf.

66. **Lumichip** (2011). White leds. URL `http://www.lumichip.com/Lumichip/Photon_modulation_files/LC_5630XXPN_G1X.pdf`.

67. **Mak, O. C.**, **Y.-C. Wong**, and **A. Ioinovici** (1995). Step - up dc power supply based on a switched - capacitor circuit. *IEEE Transactions on Industrial Electronics*, **42**(1), 90 – 97.

68. **Makowski, M. S.** and **D. Maksimovic**, Performance limits of switched - capacitor dc - dc converters. *In Power Electronics Specialists Conference, 1995. PESC'95 Record., 26th Annual IEEE*, volume 2. IEEE, 1995.

69. **Max1910** (2004). *1.5x/2x High-Efficiency White LED Charge Pumps*. Maxim Integrated. Online:http://datasheets.maximintegrated.com/en/ds/MAX1910-MAX1912.pdf.

70. **Microchip** (2010). Dspic30f3011. URL `http://ww1.microchip.com/downloads/en/DeviceDoc/70141F.pdf`.

71. **Miller, I. G.**, **D. A. Garrity**, and **T. Cassagnes** (2002). Dual input switched capacitor gain stage. US Patent 6,362,770.

72. **Milliken, R. J.**, **J. Silva-Martínez**, and **E. Sánchez-Sinencio** (2007). Full on - chip cmos low-dropout voltage regulator. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **54**(9), 1879 – 1890.

73. **Mohan, N.**, **T. M. Undeland**, and **W. P. Robbins**, *Power Electronics. Converters, Applications and Design*. John Wiley and Sons, Inc, 2003, third edition.

74. **Myono, T.** (2004). Multi - stage switched capacitor dc - dc converter. US Patent 6,834,001.

75. **Narayanasamy, R.**, **M. K. N. Swamy**, **D. G. Wright**, and **S. Kolokowsky** (2017). Capacitive sensing button on chip. US Patent 9,588,626.

76. **Ngo, K.** and **R. Webster** (1994). Steady state analysis and design of a switched - capacitor dc - dc converter. *IEEE Transactions on Aerospace and Electronic Systems*, **30**(1), 92 – 101.

77. **Nguyen, M.-K.**, **T.-D. Duong**, and **Y. C. Lim** (2017). Switched - capacitor - based dual - switch high - boost dc - dc converter. *IEEE Transactions on Power Electronics*.

78. **Oraw, B. S.** and **P. Kumar** (2010). Switched capacitor converters. US Patent 7,696,735.

79. **Pandey, A.**, **M. J. Khan**, **D. Prasad**, **V. Nath**, **S. Solanki**, and **L. Singh**, Switched capacitor circuit realization of sigma - delta adc for temperature sensor. *In Proceeding of International Conference on Intelligent Communication, Control and Devices*. Springer, 2017.

80. **Pascual, C.** and **P. T. Krein**, Switched capacitor system for automatic series battery equalization. *In Applied Power Electronics Conference and Exposition, 1997. APEC'97 Conference Proceedings 1997., Twelfth Annual*, volume 2. IEEE, 1997.

81. **Psychalinos, C.**, **G. Tsirimokou**, and **A. S. Elwakil** (2016). Switched - capacitor fractional - step butterworth filter design. *Circuits, Systems, and Signal Processing*, **35**(4), 1377 – 1393.

82. **REG71027** (2015). *Switched Capacitor Converter*. Texas Instruments. Online:http://ti.com/product/REG710-27.

83. **Rosas Caro, J. C.**, **J. C. Mayo Maldonado**, **F. Mancilla-David**, **A. Valderrabano Gonzalez**, and **F. B. Carbajal** (2015). Single - inductor resonant switched capacitor voltage multiplier with safe commutation. *IET Power Electronics*, **8**(4), 507 – 516.

84. **Sako, M.**, **Y. Watanabe**, **T. Nakajima**, **J. Sato**, **K. Muraoka**, **M. Fujiu**, **F. Kono**, **M. Nakagawa**, **M. Masuda**, **K. Kato**, *et al.* (2016). A low power 64 gb mlc nand-flash memory in 15 nm cmos technology. *IEEE Journal of Solid-State Circuits*, **51**(1), 196 – 203.

85. **Sanders, S. R.**, **E. Alon**, **H. P. Le**, **M. D. Seeman**, **M. John**, and **V. W. Ng** (2013). The road to fully integrated dc - dc conversion via the switched - capacitor approach. *IEEE Transactions on Power Electronics*, **28**(9), 4146 – 4155.

86. **Sanders, S. R.** and **M. Kline** (2016). Switched-capacitor isolated led driver. US Patent 9,295,116.

87. **Sano, K.** and **H. Fujita** (2008). Voltage - balancing circuit based on a resonant switched - capacitor converter for multilevel inverters. *IEEE Transactions on Industry Applications*, **44**(6), 1768 – 1776.

88. **Seeman, M. D.** (2009). *A Design Methodology for Switched - Capacitor DC - DC Converters*. Ph.D. thesis, EECS Department, University of California, Berkeley. URL `http://www2.eecs.berkeley.edu/Pubs/TechRpts/2009/EECS-2009-78.html`.

89. **Seeman, M. D.**, **V. W. Ng**, **H.-P. Le**, **M. John**, **E. Alon**, and **S. R. Sanders**, A comparative analysis of switched - capacitor and inductor - based dc - dc conversion technologies. *In Control and Modeling for Power Electronics (COMPEL), 2010 IEEE 12th Workshop on*. IEEE, 2010.

90. **Seeman, M. D.** and **S. R. Sanders** (2008). Analysis and optimization of switched - capacitor dc - dc converters. *IEEE Transactions on Power Electronics*, **23**(2), 841 – 851.

91. **Semiconductors, O.** (2006). Voltage regulators. URL `https://www.fairchildsemi.com/pf/Lm/LM7805.html`.

92. **Serra, H.**, **R. Santos-Tavares**, and **N. Paulino** (2017). A numerical methodology for the analysis of switched - capacitor filters taking into account non - ideal effects of switches and amplifiers. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **64**(1), 61 – 71.

93. **Shoyama, M.**, **T. Naka**, and **T. Ninomiya**, Resonant switched capacitor converter with high efficiency. *In Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, volume 5. IEEE, 2004.

94. **Stauth, J. T.**, **M. D. Seeman**, and **K. Kesarwani** (2013). Resonant switched-capacitor converters for sub - module distributed photovoltaic power management. *IEEE Transactions on Power Electronics*, **28**(3), 1189 – 1198.

95. **Trigger, S.** (2014). Hex schmitt trigger circuits. URL `http://www.st.com`.

96. **Tse, C.**, **S. Wong**, and **M. Chow** (1995). On lossless switched - capacitor power converters. *IEEE Transactions on Power Electronics*, **10**(3), 286 – 291.

97. **Uno, M.** and **K. Sugiyama**, Pwm and pfm controlled switched capacitor converter - based multiport converter integrating voltage equalizer for photovoltaic systems. *In Future Energy Electronics Conference and ECCE Asia (IFEEC 2017-ECCE Asia), 2017 IEEE 3rd International*. IEEE, 2017.

98. **Van Breussegem, T.** and **M. Steyaert**, *CMOS integrated capacitive DC - DC converters*. Springer Science & Business Media, 2012.

99. **Wang, H.**, **G. Mora-Puchalt**, **C. Lyden**, **R. Maurino**, and **C. Birk** (2017). A 19 nv, 2-μv offset 75-μa capacitive-gain amplifier with switched-capacitor adc driving capability. *IEEE Journal of Solid-State Circuits*.

100. **Wong, C. S.**, **K. Loo**, **H. H.-C. Iu**, **Y. Lai**, **M. Chow**, and **K. T. Chi** (2017). Independent control of multicolour - multistring led lighting systems with fully switched-capacitor-controlled lcc resonant network. *IEEE Transactions on Power Electronics*.

101. **Wong, L. S.**, **S. Hossain**, **A. Ta**, **J. Edvinsson**, **D. H. Rivas**, and **H. Naas** (2004). A very low - power cmos mixed-signal ic for implantable pacemaker applications. *IEEE Journal of Solid-State Circuits*, **39**(12), 2446 – 2456.

102. **Wu, B.**, **S. Li**, **K. M. Smedley**, and **S. Singer** (2016). Analysis of high - power switched-capacitor converter regulation based on charge-balance transient - calculation method. *IEEE Transactions on Power Electronics*, **31**(5), 3482 – 3494.

103. **Yang, L.**, **X. Zhang**, **B. Wu**, **K. Smedley**, and **G. Li**, A nonlinear control for switched - capacitor converter based on one-cycle control technique. *In Transportation Electrification Conference and Expo (ITEC), 2016 IEEE*. IEEE, 2016.

104. **Ye, Y.** and **K. Cheng** (2017*a*). Analysis and design of zero-current switching switched - capacitor cell balancing circuit for series - connected battery/supercapacitor. *IEEE Transactions on Vehicular Technology*.

105. **Ye, Y.** and **K. W. E. Cheng** (2017*b*). Analysis and optimization of switched capacitor power conversion circuits with parasitic resistances and inductances. *IEEE Transactions on Power Electronics*, **32**(3), 2018 – 2028.

106. **Yeung, Y. B.**, **K. E. Cheng**, **S. Ho**, **K. Law**, and **D. Sutanto** (2004). Unified analysis of switched - capacitor resonant converters. *IEEE Transactions on Industrial Electronics*, **51**(4), 864 – 873.

107. **Yuan-mao, Y.** and **K. W. E. Cheng** (2013). Multi - input voltage-summation converter based on switched - capacitor. *IET Power Electronics*, **6**(9), 1909 – 1916.

108. **Yuanmao, Y.** and **K. Cheng** (2012). Level - shifting multiple - input switched - capacitor voltage copier. *IEEE Transactions on Power Electronics*, **27**(2), 828 – 837.

109. **Yuanmao, Y.**, **K. Cheng**, and **Y. Yeung** (2012). Zero - current switching switched-capacitor zero - voltage - gap automatic equalization system for series battery string. *IEEE Transactions on Power Electronics*, **27**(7), 3234 – 3242.

110. **Zhu, G.** and **A. Ioinovici**, Switched - capacitor power supplies: Dc voltage ratio, efficiency, ripple, regulation. *In Circuits and Systems, 1996. ISCAS'96., Connecting the World., 1996 IEEE International Symposium on*, volume 1. IEEE, 1996.

PATENT FILED AND LIST OF PAPERS PUBLISHED
BASED ON THE THESIS

PATENT FILED

Chikku Abraham, Babita Roslind Jose, Jimson Mathew, Vivekanandhan Subburaj, "A Dual Input Buck, Boost and Inverter Mode SC Based Voltage Converter", *Indian Patent Application No.* **201741031722**, filed on 07/09/2017.

REFEREED JOURNALS

1. **Chikku Abraham**, Babita Roslind Jose, J. Mathew and M. Evzelman, "Modelling, Simulation and Experimental Investigation of a Novel Two Input Series Parallel Switched Capacitor Converter", *IET Power Electronics*, Issue 3, Vol. 10, pp. 368-376, March 2017, SCIE indexed, Impact Factor : 3.547, DOI : 10.1049/iet-pel.2015.1000

2. **Chikku Abraham**, V. Subburaj, D. Jena, P. Perumal, B. R. Jose, and J. Mathew. "Reconfigurable highly efficient CMOS-based dual input variable output switched capacitor converter for low power applications." *IET Electronic Letters*, Issue 2, Vol. 54, pp. 89-91, January 2018, SCI indexed, Impact Factor : 1.155, DOI : 10.1049/el.2017.3576

3. **Chikku Abraham**, Babita Roslind Jose and J. Mathew, "A Dual Source Variable Output Switched Capacitor (SC) DC-DC Converter with Renewable Energy Integration Capability", *International Journal of Energy Technology and Policy (IJETP)*, Inderscience publishers, Vol. 13, Nos. 1/2, 2017, Scopus Indexed, DOI: 10.1504/IJETP.2017.0610

4. **Chikku Abraham**, Babita Roslind Jose and J. Mathew , "A Multiple Input Variable Output Switched Capacitor DC-DC Converter for Harnessing Renewable Energy and Powering LEDs", *Journal of Low Power Electronics*, Vol. 11, 2015, ESCI and Scopus Indexed, Impact Factor:0.84, DOI:10.1166/jolpe.2015.1392

PRESENTATIONS IN INTERNATIONAL CONFERENCES

1. **Chikku Abraham**, Poornima, M.S. and Jose, B.R., "A Novel Multiple Gain Inductorless Buck-Boost DC-DC Converter", Fourth International Conference on Advances in Computing and Communications (ICACC), August 2014, (pp. 356-361). IEEE.

2. **Chikku Abraham**, Preetha G, Susan Ninan and Babita Roslind Jose, "Charge Pump Driven High Step-up Converter for Renewable Energy Harvesting", Proceedings of the Int. Conference on Emerging Trends in Electrical Engineering (ICETREE-14), July, 2014, Elsevier.

3. **Chikku Abraham**, Rakhee R, Jose B.R., "A Multiple Input Multiple Output Switched Capacitor DC-DC Converter with Reduced Switch Count", In Electronic System Design (ISED), 2014 Fifth International Symposium on 2014 Dec 15 (pp. 104-108). IEEE.

<div align="center">**CURRICULUM VITAE**</div>

1.　**NAME**　　　　　　：　Chikku Abraham

2.　**DATE OF BIRTH**　　：　16th May, 1975

3.　**EDUCATIONAL QUALIFICATIONS**

1997 Bachelor of Technology (B.Tech.)

Institution　　　：　Mahatma Gandhi University, Kerala

Specialization　：　Electrical & Electronics Engineering

2008 Master of Technology (M.Tech.)

Institution　　　：　Indian Institute of Technology, Bombay

Specialization　：　Energy Systems Engineering

Doctor of Philosophy (Ph.D)

Institution　　　：　Cochin University of Science and Technology

Registration Date　：　25 - 11 - 2011