EFFICIENT ΣΔ MODULATOR ARCHITECTURES FOR NEXT GENERATION WIRELESS TRANSCEIVERS

A THESIS

submitted by

JOS PRAKASH A V

for the award of the degree

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DOCTOR OF PHILOSOPHY

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THESIS CERTIFICATE

This is to certify that the thesis entitled "**EFFICIENT ΣΔ MODULATOR ARCHITECTURES FOR NEXT GENERATION WIRELESS TRANSCEIVERS**" submitted by **Mr. Jos Prakash A V** to the Cochin University of Science and Technology, Kochi for the award of the degree of Doctor of Philosophy is a bonafide record of research work carried out by him under my supervision and guidance at the Division of Electronics Engineering, School of Engineering, Cochin University of Science and Technology. The contents of this thesis, in full or in parts, have not been submitted to any other University or Institute for the award of any degree or diploma.

I further certify that the corrections and modifications suggested by the audience during the pre-synopsis seminar and recommended by the Doctoral Committee of **Mr. Jos Prakash A V** are incorporated in the thesis.

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Dedicated to my Family

DECLARATION

I hereby declare that the work presented in the thesis entitled "**EFFICIENT ΣΔ MODULATOR ARCHITECTURES FOR NEXT GENERATION WIRELESS TRANSCEIVERS** " is based on the original research work carried out by me under the supervision and guidance of **Dr. Babita Roslind Jose**, Assistant Professor, for the award of degree of Doctor of Philosophy with Cochin University of Science and Technology. I further declare that the contents of this thesis, in full or in parts, have not been submitted to any other University or Institute for the award of any degree or diploma.

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Date: 11/04/2017

Jos Prakash A. V

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ABSTRACT

Analog-to-digital interfaces are evolving into something which is beyond our imagination while we come across mobile telecommunication systems and advanced signal processing architectures. Historical aspects and literatures reinforce the fact that analog and digital domains can never side-step each other to their complete extent. With the utmost demand for next generation massive multiple-input multiple-output (MIMO) based 5G wireless systems, expecting data bandwidth of several GHz and carrier frequencies in the millimetre wave range (tens of GHz to 100 GHz), require an analog-to-digital converter (ADC) for each receiver antenna. Future wireless applications have driven high-speed and high performance complementary metal oxide semiconductor (CMOS) ADC designs, realized by time-interleaved (TI) multi-path architectures, and there arise a necessity to explore efficient techniques and architectural perspectives. Software defined radio (SDR) is another challenging technology for future wireless systems, which is comprised of both software and hardware systems that can be dynamically reconfigured to enable communication between wide varieties of changing communication standards and protocols within radio links.

Sigma delta ($\Sigma\Delta$) modulator based ADC offers a promising role to overcome conversion resolution and noise free bandwidth limitations. Modern wireless telecommunications systems are benefited extensively with the usage of $\Sigma\Delta$ ADCs because of its remarkable linearity, cost effectiveness, robustness to circuit imperfections, implicit bandwidth-resolution trade-offs and improved programmability in the digital realm. The thesis discusses on the potential of $\Sigma\Delta$ modulator based ADC architectures for implementing high-resolution/bandwidth next generation digitization applications, utilizing multi-path signal processing, TI operation and noise-coupling concepts.

The thesis initially presents a detailed review of literatures and background information. Then a low-cost time division multiplexing (TDM) based 3^{rd} order continuous-time (CT) incremental sigma delta (I$\Sigma\Delta$) modulator for analog-to-digital conversion of time-multiplexed low frequency signal channels is proposed. Different signal types to be digitized have led to a diverse selection of data converters in terms of architectures,

resolution and sampling rates. In the context of high-resolution multi-channel digital signal processing and applications like SDRs the role of I$\Sigma\Delta$ modulators are inevitable. A 3^{rd} order CT design is investigated here because of its inherent low-power and implicit anti-aliasing characteristics. The high-resolution characteristics of the proposed modulator make it suitable for time-multiplexed audio applications. A method to compensate the excess loop delay (ELD) to improve the performance of the modulator is adopted here.

Secondly, a novel TI extended noise shaping based cross-coupled multi-path sturdy multi-stage noise shaping (SMASH) architecture that compensates the excess SMASH loop delay (ESLD) is presented. The idea of SMASH logic in a multi-path TI scenario is modelled and demonstrated by using an extended noise shaping based TI cross-coupled 2-path 3^{rd} order structure as the first stage of the SMASH architecture. The second stage of the modulator was obtained by using either a shaped high-resolution quantizer or a combination of first order $\Sigma\Delta$ modulator with a shaped high-resolution quantizer. The finite delay associated with the SMASH loop deteriorates its ability to completely cancel the first stage quantization error. This finite delay was compensated by the proposed ESLD compensation mechanism and thus the input referred stability was greatly enhanced.

Targeting more efficient and enhanced noise shaping structures, a dual extended (DE) noise shaping based TI symmetric cross-coupled $\Sigma\Delta$ modulator, which enhances the performance of conventional unextended and extended noise shaping based TI cross-coupled $\Sigma\Delta$ modulator architecture, is proposed. The N-path first order cross-coupled $\Sigma\Delta$ modulator can attain only N^{th}-order noise shaping for unextended case and $(2N-1)^{th}$-order noise shaping in the extended case. By dual extended noise shaping characteristics, the proposed architecture was able to achieve $2N^{th}$-order noise shaping out of an N-path cross-coupled first order $\Sigma\Delta$ modulator, without sacrificing its high conversion rate and bandwidth.

One of the most important aspects for ADCs in next generation wireless systems is the ability to support multiple standards without significant increase in power and area. The thesis describes an efficient triple-mode hexa-standard TI reconfigurable cross-coupled $\Sigma\Delta$ modulator designed for six different wireless communication standards such as GSM, Bluetooth, GPS, WCDMA, WLAN and WiMAX. Enhanced noise shap-

ing characteristics, obtained by TI cross-coupling of $\Sigma\Delta$ paths, have been utilized for the modulator design. Power and hardware efficiency is achieved by using the new dual extended noise shaping technique. The cross-coupled paths and the building blocks are reconfigured to adapt the requirements of wide hexa-standard specifications. The modulator adopts time-interleaving technique targeting a reduced operating speed or equivalently an increased conversion bandwidth.

Finally, a differential quantizer based error feedback modulator (DQEFM) architecture intended for digitizing analog signals and its comparison to the traditional interpolative $\Sigma\Delta$ analog-to-digital conversion is presented. The DQEFM also falls under the class of noise shaping data converters. This newly introduced technique replaces the integrator with a differential quantizer to achieve noise shaping characteristics. Thus, integrator associated non-idealities, loop-stability issues and optimization of the integrator scaling coefficients is no more a concern. DQEFM technique can perform well in high-precision and low-power applications. Furthermore, the thesis also describes the design, analysis and implementation of a novel differentially quantized bandpass analog-to-digital conversion technique for digital radio application. Behavioural-level simulation results demonstrate the mathematical equivalence of the differential quantizer based error feedback modulator technique with interpolative $\Sigma\Delta$ modulator technique, and confirms its novelty, theoretical stability and scalability to higher order.

KEYWORDS: Analog-to-digital converters; Sigma delta modulators; Incremental sigma delta modulators; Oversampling; Noise shaping; Time division multiplexing; Excess loop delay; Cross-coupled; Multi-path; Multi-standard; Multi-mode; Multi-stage, Time interleaving; Reconfigurable; Differential Quantizer; Error feedback modulator.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ABBREVIATIONS

2G	Second Generation
3G	Third Generation
4G	Fourth Generation
5G	Fifth Generation
3GPP	Third Generation Partnership Project
ADC	Analog-to-Digital Converter
ASIC	Application Specific Integrated Circuit
BOM	Bill of Material
BW	Bandwidth
CIFF	Cascade of Integrators in Feedforward
CMOS	Complementary Metal Oxide Semicondcutor
CT	Continuous Time
DAC	Digital to Analog Converter
DE	Dual Extended
DEM	Dynamic Element Matching
DNC	Delay based Noise Cancellation
DNL	Differential Nonlinearity
DSP	Digital Signal Processing
DT	Discrete Time
DQ	Differential Quantizer
ECG	Electrocardiogram
EEG	Electroencephalogram
EFM	Error Feedback Modulator
ELD	Excess Loop Delay
ENOB	Effective Number of Bits
ERBW	Effective Resolution BandWidth
ESLD	Excess Sturdy MASH Loop Delay
FFT	Fast Fourier Transform

FPGA	Field Programmable Gate Array
GaAs	Gallium Arsenide
GBW	Gain Bandwidth Product
GSM	Global System for Mobile communications
GSPS	Giga Samples Per Second
HDR	Hardware Defined Radio
HDS	Harmonic Distortion
IC	Integrated Circuits
IIP3	Input-referred Third-order Intercept Point
InP	Indium Phosphide
INL	Integral Nonlinearity
ITRS	International Technology Roadmap for Semiconductors
LSB	Least Significant Bit
MASH	Multi-Stage Noise Shaping
MSPS	Million Samples per Second
MIMO	Multi-Input Multi-Output
MUX	Multiplexer
NPR	Noise Power Ratio
NRZ	Non Return to Zero
NTF	Noise Transfer Function
OFDM	Orthogonal Frequency Division Multiplexing
OL	Overloading Point
opamp	Operational Amplifier
OSR	Oversampling Ratio
OTA	Operational Transconductance Amplifier
PSD	Power Spectral Density
RF	Radio Frequency
SC	Switched Capacitor
SDR	Software Defined Ratio
SFDR	Spurious Free Dynamic Range
SI	Switched Current
SMASH	Sturdy Multistage Noise Shaping
SNDR	Signal to Noise-plus-Distortion Ratio

SNR	Signal to Noise Ratio
SNRp	Peak Signal to Noise Ratio
SQNR	Signal to Quantization Noise Ratio
SR	Slew Rate
STF	Signal Transfer Function
TDM	Time Division Multiple Access
TI	Time Interleaved
UWB	Ultra Wide Band
VLSI	Very Large Scale Integration
WLAN	Wireless Local Area Network
WCDMA	Wideband Code Division Multiple Access

NOTATION

C	Capacitance
C_f	Feedback capacitance
dB	Decibel
dBc	Decibels relative to the carrier
$dBFS$	Decibels relative to full scale
Δ	Quantization step size
ε	Quantization error
FoM_w	Walden figure of merit
F_s	Sampling frequency
g_m	Transconductance
k	Boltzmann's constant
k_i'	Feed-forward coefficients
N	Number of paths of the modulator
n	Nano
Nc	Number of cycles per conversion
p	Pico
P_{diss}	Power Dissipated
ϕ	Clock rate
S/H	Sample and hold
$\Sigma\Delta$	Sigma delta
T	Temperature
T_s	Sampling time
μ	Micro (10^{-6})
τ_d	Excess loop delay
V	Volts

CHAPTER 1

INTRODUCTION

1.1 Motivation

The exponential growth in the very large scale integration (VLSI) technologies and the development of broadband wireless telecommunication systems has propelled the advancement of sophisticated digital transceiver architectures. ADC functions as a platform between the analog and digital worlds that encodes natural continuous quantities to logical codes. Numerous types of ADCs are available in market, each with its own strengths and shortcomings. These ADCs has to deal with a wide variety of signal categories for digitization and has forced the evolution of diversified choice of data converters in terms of power/area efficiency, accuracy and sampling frequency.

A number of parameters exist to evaluate the performance of ADCs which includes resolution (number of bits per sample), signal-to-noise ratio (SNR), spurious free dynamic range (SFDR), and power dissipation (P_{dss}) (Walden, 1994). An increment in the sampling frequency limits the resolution of the ADC. The potential of the comparator(s) for unambiguous decision making while digitizing the analog voltage and the ADC fabrication technology constraints limits the sampling rate or speed of operation. The maximum Nyquist sampling rate attained so far is around 8 giga samples per second (GSPS) (Oppenheim and Schafer, 2009).

The huge demand for power efficient electronic devices is a well known fact in the age of modern telecommunication systems, advanced networking computers/ laptops and high-speed portable systems. Battery life, which is a serious concern in portable/ wearable electronic devices, can be enhanced by making the hardware more power efficient and allows us to integrate new robust and sophisticated functional capabilities within the same allocated resources. In this context the size and weight of portable electronic equipments are also significant concern and can be minimized by the same power efficiency principle without degrading the functionalities and battery life. The

total power consumption of multi-path parallel structures, like phased-array systems, is also an important concern in modern electronic systems.

Ultra high speed, of the order of thousands of GSPS, and ultra high bandwidth with excellent SNR performance and power efficiency, compatible with the evolving electronic, wireless multi-standard and photonic technologies is the future research scope of ADCs. Technological advances in the electronic hardware industry have also contributed much into the growth of present high-precision, low-power ADC architectures. Photonic analog-to-digital conversion architectures have long been recognized as having the potential to provide significant advantages in bandwidth, timing precision, and timing stability (Shoop, 2012). We may possibly have ADCs by 2020 that are implemented in 10-11 nm CMOS and are operating from 40 mV supplies. 1 GSPS ADCs with high effective number of bits (ENOB) will be reported, but ADCs from 100 MSPS and below will not have much better resolution than today.

Different approaches have been developed for addressing the ADC bottleneck in realizing mostly digital multi-gigabit transceiver architectures. For communication systems using low-precision ADC, algorithms for timing and carrier synchronization, along with transmit precoding strategies, need to be devised and evaluated. Aperture uncertainty, matching between the transistors and drain-bulk capacitance improvement (Lundberg, 2005) remain major problems in the evolving high-speed, low-power ADCs. Despite of these adversities, a substantial betterment has been made in terms of operating speed and power consumption recently.

Hardware defined radio (HDR) based multi-path structures demands highly sophisticated signal processing for each path and necessitates broader area, higher complexity, improved flexibility and tolerance to interference. High-speed ADCs makes possible flexible and re-configurable ultra-wideband systems, incorporating several narrowband and wideband paths, and its realizations in digital signal processors, field programmable gate arrays (FPGAs) or application specific integrated circuits (ASICs). The evolution of wideband radio systems like ultra-wideband (UWB) and orthogonal frequency division multiplexing (OFDM) brings a growing need to provide faster sampling rates and higher resolutions with better power efficiency. With the innovations in communication techniques like MIMO and multi-standard mobile systems, the demand is growing to provide multi-channel programmable data conversion, both of which are pushing the

performance of ADCs further in the coming years.

ADCs play an important role in almost all application fields, which makes it important to review the technology trends every few years. The communication industry has consistently pushed the boundaries of ADCs, and current advances in UWB and SDRs continue the trend. Today, sensor technologies are becoming increasingly popular and is another area where ADCs play a major part.

The demand for higher sampling speed keeps increasing, while the requirement for greater resolution has ceased since 1995. It is because such ADC resolution is enough for most modern applications such as 3G, 4G and wireless local area network (WLAN). Although there are other applications pushing ADC performance extremities, such as UWB, OFDM, and radar systems, the major challenge in ADC design has changed from the performance expansion to power reduction, especially for mobile communications and SDRs. During recent years, we have witnessed a rapid increase of multi-channel ADCs with nearly the same power as single channel counterparts. ADCs with multiple channels are ideal solutions for diversity-based wireless applications and SDR platforms. More importantly, power dissipation and cost are greatly reduced for each signal channel, especially for mobile communications

The use of oversampling $\Sigma\Delta$ modulators in the integration of high-resolution analog-to-digital converters have shown promise for overcoming the analog component limitations inherent in modern VLSI technologies. $\Sigma\Delta$ modulators employ coarse quantization enclosed in one or more feedback loops. Among different ADC topologies, the $\Sigma\Delta$ ADC efficiently trades speed for accuracy, providing an effective way to implement high-resolution ADCs without stringent matching requirement or calibration in a low-voltage environment. Through oversampling and noise shaping, the $\Sigma\Delta$ ADC transfers most of the signal processing tasks to the digital domain where the power consumption can be drastically reduced by the technology and supply voltage scaling-down.

1.1.1 Research Focus

This research work is concentrated on the design, analysis, modelling and implementation of efficient $\Sigma\Delta$ modulator architectures, particularly TI multi-path and noise coupled structures, intended for future wireless telecommunication systems. TI multi-path

structures has the capability to realize high-speed, high-precision ADCs using parallel low-speed, high-precision ADCs and noise coupling modulators helps to achieve higher order noise shaping with relaxed hardware requirements.

1.2 Author's Contributions

The thesis commences with an overview of the related research in the field of $\Sigma\Delta$ based analog-to-digital conversion for wireless transceivers and discusses the relevance of this research in the light of the cited previous research works. The thesis initially proposes an incremental $\Sigma\Delta$ modulator intended for processing time-division multiplexed multi-channel applications. The primary technical contribution of the thesis is in developing and implementing a multi-standard cross-coupled $\Sigma\Delta$ modulator architecture suitable for six different mobile communication standards. The research also focuses on the architectural exploration of cross-coupled $\Sigma\Delta$ modulators. A novel differential quantizer based error feedback modulator is also proposed and analyzed. This is followed by a few suggestions for future works. The thesis is based on the following papers. [**C** represents International Conferences and **J** represents International Journals]

C1. Jos Prakash A.V, Babita R Jose, "ADC Bottleneck - Past, Present and Future" IEEE International Workshop on Recent Advances in Computing and Communications (ACCW-2013), Workshop Proceedings, pp. 48-62, August 2013, ISBN: 978-93-83083-25-1.

Author's Contribution: This paper presents a survey of the state-of-the-art of ADCs that are presented in research papers from 1997 to 2013, including some commercially available parts, its architectures detailing resolution and sampling rate and provides insight into ADC performance limitations. The sampling rates of the order of million samples per second (MSPS) and GSPS limits the resolution of the ADC because of the thermal noise, aperture jitter and speed of the device technology. The power dissipation in ADCs is addressed by several architectural variants and system-on-chip concepts. The basic ADC performance parameters such as the signal-to-noise ratio, spurious free dynamic range, quantization energy, figure of merit, resolution, speed and future research scopes are also discussed in detail.

C2. Jos Prakash A.V, Babita R Jose, J. Mathew, "TDM Based 3^{rd} Order CT Incremental $\Sigma\Delta$ Modulator for Low Frequency ADC Application" International Conference on Next Generation Computing and Communication Technologies (ICNGCCT) held at Dubai, Conference Proceedings, pp. 220-225, April 2014, ISBN 978-93-83303-42-7. (Got the Outstanding Paper Presentation Award during the event). The paper also got nomination for best paper award in the 26^{th} Kerala Science Congress, held at wayanad, published by KSCSTE, Shastha Bhavan, Pattom, Trivandrum - 695004.
An extended version of **C2** has been published as

J1. Jos Prakash A.V, Babita R Jose, "A Low Cost Design of Time Division Multiplexing Based 3^{rd} Order Continuous-Time Incremental $\Sigma\Delta$ Modulator with Excess Loop Delay", Journal of Low Power Electronics, Vol. 10, no. 3, pp. 495-505(11), September 2014.

Author's Contribution: A low-cost TDM based 3^{rd} order CT I$\Sigma\Delta$ modulator for analog-to-digital conversion of time-multiplexed low frequency signal channels is proposed in this paper. Different signal types to be digitized have led to a diverse selection of data converters in terms of architectures, resolution and sampling rates. The demand for new telecommunication services requiring higher bandwidth, higher capacities, higher data rates, low-power and different operating modes have motivated the development of new generation multi-standard wireless transceivers. The power dissipation in ADCs is addressed by several architectural variants and system-on-chip concepts. In the context of high-resolution multi-channel digital signal processing and applications like software defined radios, the role of I$\Sigma\Delta$ modulators are inevitable. A 3^{rd} order CT design is investigated here because of its inherent low-power and implicit anti-aliasing characteristics. The high-resolution characteristics of the proposed modulator make it suitable for time-multiplexed audio applications. A method to compensate the excess loop delay to improve the performance of the modulator is adopted in this paper. A circuit-level behavioural simulation of the CT I$\Sigma\Delta$ modulator for high frequency applications has been done using the embedded behavioural simulator, SIMSIDES.

C3. Jos Prakash A.V, Babita R Jose, J. Mathew, "Dual Extended Noise Shaping for High Performance Cross-Coupled Sigma-Delta Modulators" 8^{th} International Conference on Next Generation Mobile Applications, Services and Technologies (NGMAST 2014), held in University of Oxford, United Kingdom, published by IEEE Computer Society's CPS, pp. 209 - 214, 10-12 September 2014, ISBN 978-1-4799-5072-0.

Author's Contribution: A dual extended (DE) noise shaping based TI symmetric cross-coupled $\Sigma\Delta$ modulator, which enhances the performance of conventional unextended and extended noise shaping based TI cross-coupled $\Sigma\Delta$ modulator architecture, is proposed in this paper. The N-path first order cross-coupled $\Sigma\Delta$ modulator can attain only $2N^{th}$-order noise shaping for unextended case and $(2N-1)^{th}$-order noise shaping in the extended case. By DE noise shaping characteristics, the proposed architecture can achieve $2N^{th}$ order noise shaping out of an N-path cross-coupled first order $\Sigma\Delta$ modulator without sacrificing its high conversion rate and bandwidth. The higher order noise shaping is achieved by analytically obtaining the optimum coupling matrices. Compared to other alternatives, the DE noise shaping based TI cross-coupled $\Sigma\Delta$ modulator exhibits a better in-band noise rejection with less overhead and relaxed circuit specifications.

C4. Paul Ansel V, **Jos Prakash A.V**, Babita Roslind Jose, J. Mathew, "Enhanced Noise Shaping based Band-Pass Cross-Coupled $\Sigma\Delta$ Modulators for Advanced Wireless Transceivers", International Conference on Information and Communication Technologies (ICICT) 2014, 3 - 5 December, 2014, Elsevier Procedia Computer Science, Vol. 46, 2015, pp. 1254-1260, ISSN 1877-0509, http://dx.doi.org/10.1016/j.procs.2015.01.044. (http://www.sciencedirect.com/science/article/pii/S1877050915000459)

Author's Contribution: A bandpass $\Sigma\Delta$ modulator using three different noise shaping based cross coupling techniques is proposed here. The effective use of time interleaving technique along with noise cross-coupling improves the performance of the modulator. Three variations of the conventional architecture are proposed - simple cross-coupling, extended cross-coupling and dual extended (DE) cross-coupling, which enhances effective order of noise shaping for a bandpass modulator without significant overhead. By using extended cross-coupling and DE cross coupling architectures, the order of noise transfer function (NTF) is improved and it is evident that the proposed architectures shows a better in-band noise rejection with relaxed circuit specifications.

C5. Jos Prakash A.V, Babita R Jose, "A Low-Power Reconfigurable Cross-Coupled $\Sigma\Delta$ Modulator for Multi-Standard Wireless Applications", 4^{th} International Conference on Advances in Computing and Communications (ACC-2014), 27-30 August 2014, IEEE Computer Society's CPS, pp. 130 - 133, 27-29 Aug. 2014,
DOI 10.1109/ICACC.2014.37. ISBN 978-1-4799-4364-7. The paper also won The

Best Paper Award in 27^{th} Kerala Science Congress held at Alleppey during 27 to 29 January 2015. It was organized by Kerala State Council for Science, Technology & Environment (KSCSTE) jointly with National Transportation Planning and Research Centre (NATPAC). The Best Paper Award carries a Certificate of merit, a cash prize of Rs. 10,000/- and a contingency grant of Rs. 100,000/- (Rupees One lakh only) for two years for pursuing further research.

An extended version of **C5** has been published as

J2. Jos Prakash A.V, Babita R Jose, J. Mathew, "A Triple-mode Hexa-standard Reconfigurable TI Cross-Coupled $\Sigma\Delta$ Modulator" International Journal of Electronics - Taylor & Francis, (January 2017).
https://doi.org/10.1080/00207217.2017.1285441.

Author's Contribution: This paper describes an efficient triple-mode hexa-standard time-interleaved (TI) re-configurable cross-coupled $\Sigma\Delta$ modulator designed for six different wireless communication standards such as global system for mobile communication (GSM), bluetooth, global positioning system (GPS), wideband code division multiple access (WCDMA), wireless local area network (WLAN) and worldwide interoperability for microwave access (WiMAX). Enhanced noise shaping characteristics, obtained by TI cross-coupling of N paths, have been utilized for the modulator design. Power and hardware efficiency is achieved by introducing a new dual extended (DE) noise shaping technique. The cross-coupled paths and the building blocks are reconfigured to adapt the requirements of wide hexa-standard specifications. The modulator adopts time-interleaving technique targeting a reduced operating speed or equivalently an increased conversion bandwidth. The proposed architecture is implemented in a 45 nm CMOS process. Simulation results, both architectural and transistor-level, proves the effectiveness and feasibility of this architecture to meet the performance requirements of the mobile communication standards.

C6. Jos Prakash A.V, Babita R Jose, J. Mathew "A Novel Excess Sturdy-MASH-Loop-Delay Compensated Cross-Coupled Multipath Time-Interleaved $\Sigma\Delta$ Modulator" IEEE 29th International Conference on VLSI Design (VLSID) held at Kolkata, IEEE Xplore, pp. 246 - 251, 4-8 January 2016, DOI:10.1109/VLSID.2016.59, INSPEC Accession Number:15855990.

Author's Contribution: A novel TI extended noise shaping based cross-coupled multi-path SMASH architecture that compensates the ESLD is presented in this paper. The idea of SMASH logic in a multi-path TI scenario is modelled and demonstrated by using an extended noise shaping based TI cross-coupled 2-path 3^{rd} order structure as the first stage of the SMASH architecture. The second stage of the modulator is obtained by using either a shaped high-resolution quantizer or a combination of first order $\Sigma\Delta$ modulator with a shaped high-resolution quantizer. The finite delay associated with the SMASH loop deteriorates its ability to completely cancel the first stage quantization error. This finite delay is modelled using a unit delay in the main path and is compensated by the proposed ESLD compensation mechanism and thus the input referred stability is greatly enhanced. The switched capacitor (SC) circuit based implementation of the proposed model is done in Hspice. It is implemented in a 45 nm CMOS process. Simulation results, both behavioural and transistor-level, proves the effectiveness of this architecture.

J3. Jos Prakash A.V, Babita R Jose, J. Mathew, "A Differential Quantizer based Error Feedback Modulator for Analog to Digital Converters" IEEE Transactions on Circuits and Systems II, vol.PP, no.99, pp.1-1, February 2017.
doi:10.1109/TCSII.2017.2666822.

Author's Contribution: A differential quantizer based error feedback modulator intended for digitizing analog signals and its comparison to the traditional interpolative $\Sigma\Delta$ analog-to-digital conversion is presented in this paper. The differential quantizer based error feedback modulator also falls under the class of noise shaping data converters. This newly introduced technique replaces the integrator with a differential quantizer to achieve noise shaping characteristics. Thus, integrator associated nonidealities, loop-stability issues and optimization of the integrator scaling coefficients is no more a concern. Differential quantizer based error feedback modulator technique can perform well in high-precision and low-power applications. Behavioural-level simulation results demonstrate the mathematical equivalence of the differential quantizer based error feedback modulator technique with interpolative $\Sigma\Delta$ modulator technique, and confirms its novelty, theoretical stability and scalability to higher order. The circuit-level feasibility and effectiveness of the proposed architecture is verified in a 45 nm CMOS process.

J4. Jos Prakash A.V, Babita R Jose, J. Mathew, "A Differentially Quantized Bandpass Error Feedback Modulator for ADCs in Digital Radio" Submitted to Springer Circuits Systems and Signal Processing.

Author's Contribution: Bandpass $\Sigma\Delta$ modulators are highly desirable in precision analog-to-digital conversion applications for narrow band intermediate frequency signals. This paper describes the design, analysis and implementation of a novel differentially quantized bandpass analog-to-digital conversion technique for digital radio application. A new class of noise shaping data converter, i.e. the differential quantizer based error feedback modulator is introduced, which replaces the integrator/resonator with a differential quantizer to achieve noise shaping characteristics. Thus, integrator associated non-idealities, loop-stability issues and optimization of the integrator scaling coefficients is no more a concern. Furthermore, a comparison to the traditional interpolative bandpass $\Sigma\Delta$ analog-to-digital conversion has also been presented here. Behavioural-level simulation results demonstrate the mathematical equivalence of the differential quantizer based bandpass error feedback modulator technique with interpolative bandpass $\Sigma\Delta$ modulator technique, and confirms its novelty, theoretical stability and scalability to higher order. The circuit-level feasibility and effectiveness of the proposed architecture is verified in a 45nm CMOS process.

1.2.1 Contributions not Included in the Thesis

C7. Sabarinath, **Jos Prakash A.V**, Babita Roslind Jose, J. Mathew, "Overloading Prediction in Symmetric Cross Coupled Low-Pass Sigma Delta Modulators", International Conference on Information and Communication Technologies (ICICT) 2014, 3 - 5 December, 2014, Elsevier Procedia Computer Science, vol. 46, 2015, pp. 1223-1229, ISSN 1877-0509.
http://dx.doi.org/10.1016/j.procs.2015.01.037.
(http://www.sciencedirect.com/science/article/pii/S1877050915000381)

C8. Rijo Sebastian, **Jos Prakash A.V**, Babita R Jose, Shahana T K, "A Multi-mode MASH $\Sigma\Delta$ Modulator for Low Power Wideband Applications", Sixth International Symposium on Electronics Design (ISED 2016), held in IIT Patna, December 2016.

1.3 Thesis Outline

Chapter 2 illustrates the background concepts and literature review related to the thesis.

In **Chapter 3**, a time division multiplexing based 3^{rd} order CT incremental $\Sigma\Delta$ modulator with ELD compensation is proposed. The high-resolution characteristics of the proposed modulator make it suitable for time-multiplexed audio applications. Behavioural simulation demonstrates that the ELD compensated modulator with modified coefficients and an extra direct path restores the NTF. A circuit-level behavioural simulation of the proposed modulator for high frequency application has been done using the behavioural simulator SIMSIDES (José and del Río, 2013).

Wide band analog-to-digital conversion necessitates higher order noise shaping based $\Sigma\Delta$ modulator architectures. Due to the instability associated with single loop higher order $\Sigma\Delta$ modulators, SMASH architecture is preferred. With a mission of achieving enhanced noise shaping characteristics, a novel TI extended (Hamidi and Miar-Naimi, 2014) cross-coupled multi-path SMASH architecture that compensates the ESLD, is proposed in **Chapter 4**. The ESLD compensation ensures perfect TI cross-coupled SMASH $\Sigma\Delta$ modulator operation. The chapter also offers more architectural-level exploration of enhanced noise shaping based TI cross-coupled $\Sigma\Delta$ modulator. A new $\Sigma\Delta$ modulator architecture, called the dual extended (DE) noise shaping architecture is proposed for high performance analog-to-digital conversion. The technique enables the realization of higher order NTF with greatly relaxed circuit specifications and without significant increase in power and area. Dual extended noise shaping based bandpass cross-coupled $\Sigma\Delta$ modulators for advanced wireless transceivers has also been presented in this chapter.

Chapter 5 proposes a triple-mode hexa-standard reconfigurable TI cross-coupled $\Sigma\Delta$ modulator. Enhanced noise shaping characteristics, obtained by TI cross-coupling of $\Sigma\Delta$ paths, have been utilized for the modulator design. The cross-coupled paths and the building blocks are reconfigured to adapt the requirements of wide hexa-standard specifications. Using MATLAB and sigma-delta toolbox (Schreier, 2004) the behavioural-level simulation of the proposed reconfigurable architecture is performed, verifying its performance and flexibility to hexa-standard scenarios. Circuit-level realization of the architecture is verified in 45 nm CMOS technology using Hspice and implementa-

tion is done in Cadence tools.

In **Chapter 6** a novel differential quantizer based error feedback modulator for analog-to-digital conversion is proposed. The major challenges associated with the design of higher order $\Sigma\Delta$ modulators are loop stability issues due to its inherent non-linearity, integrator associated non-idealities, optimization of the integrator scaling co-efficients (Maloberti, 2007) and low operating bandwidth due to the accumulation of samples. An excellent alternative in the class of oversampling and noise shaping converters, that can mitigate these problems associated with $\Sigma\Delta$ modulator, is the newly introduced DQEFM. The switched capacitor (SC) model of the architecture is done in Hspice. A bandpass version of the differentially quantized error feedback modulator, intended for digital radio applications, is also proposed and presented in this chapter. The differential quantizer based replacement to integrator/resonator and $\Sigma\Delta$ loop itself makes the DQEFM technique less sensitive to circuit non-idealities, hardware efficient and power efficient, and is very likely to be useful for high-speed, wide-band, high-precision and low-power data conversion applications.

Chapter 7 summarizes the work presented in the thesis.

CHAPTER 2

BACKGROUND AND LITERATURE REVIEW

ADCs are inevitable modules in the context of digital signal processing and software defined radios. By using conventional receiver architectures, simultaneous operation at different frequencies can only be achieved by building multiple independent signal paths which may eventually increase the cost and power dissipation. Therefore, multi-standard receivers often re-use circuit blocks, or multiple radio frequency (RF) front-ends. To achieve higher data rates in emerging wireless generations, (for example WCDMA, IEEE 802.11b, GSM), the analog front-end must be able to handle wider bandwidths at lower noise and power levels. This research is to explore efficient techniques for the design of $\Sigma\Delta$ ADC, specifically for next generation of multi-channel wireless transceivers. In particular, the aim is to develop novel models and techniques which are able to assist the designer's decisions in the system-level exploration phase.

The chapter offers a detailed literature review and background to the thesis. A brief introduction to ADC architectures, efficient $\Sigma\Delta$ modulator structures and major domain of applications are explained. The major challenges involved in the implementation of such efficient architectures have also been analyzed throughout the thesis.

2.1 ADC Fundamentals and Characterization

For every ADC, there must be a sampler and a quantizer. Mathematically, an n-bit analog-to-digital conversion can be expressed as in Equation 2.1 (Schreier *et al.*, 2005).

$$V_{in} = \sum_{i=1}^{n} 2^{-i} b_i V_{ref} + e_q. \tag{2.1}$$

where V_{in}, V_{ref}, b_i and e_q represents input signal amplitude, reference signal amplitude, value of i^{th} bit (0 or 1) and quantization error, respectively. For an ADC, there is always an error, Equation 2.2, associated with the ADC. This error is called quantization

error. Higher the resolution of ADC, smaller will be its quantization error.

$$\frac{-\Delta}{2} \leq e_q \leq \frac{+\Delta}{2}. \tag{2.2}$$

The quantization step Δ, with a value of $V_{ref}/2^n$, is called the least significant bit (LSB) of an ADC. Assuming that the quantization error is uniformly distributed, the quantization error power is related to the quantization step as given in Equation 2.3,

$$e_q^2 = \frac{\Delta^2}{12} \tag{2.3}$$

The quantization error is dependent on the resolution of the ADC and it is often referred to as the quantization noise of an ADC. The peak SNR of an ideal n bit ADC for a sinusoidal input signal can be calculated as in Equation 2.4.

$$SNR_p = 6.02n + 1.76dB. \tag{2.4}$$

It is assumed that the quantization noise is independent from the input signal. Moreover, the quantization noise power spectral density is uniformly distributed in the sampling frequency band, i.e. the white noise interpretation of quantization noise. Shown in Figure 2.1, the power spectral density of the quantization noise, $S_e(f)$, is white and all its power is within $\pm F_s/2$, where F_s is the sampling frequency. The total quantization power is the amplitude of power spectral density as given in Equation 2.5.

$$h_e = \frac{\Delta^2}{12}\frac{1}{F_s} \tag{2.5}$$

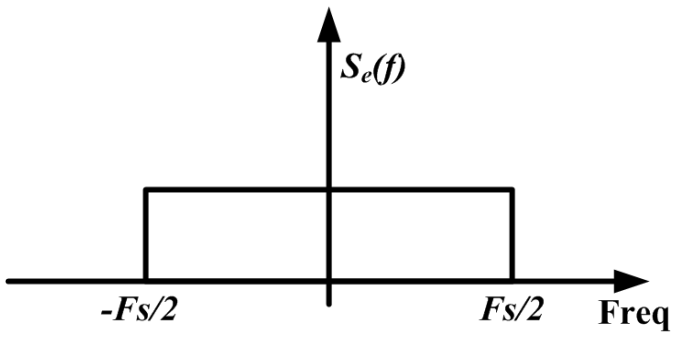


Figure 2.1: The power spectral density of quantization noise

The total power of the quantization noise is evenly distributed in the range $\pm F_s/2$. The common white noise approximation helps to assume that the probabilities of quantization errors are equal. As the sampling frequency increases, the amplitude of the spectral density decreases, but the total quantization noise power remains the same. This property is utilized in oversampling converters.

Resolution of an ADC can be determined both quasi-statically and dynamically. Quasi-static measurement includes differential nonlinearity (DNL) and integral nonlinearity (INL). Dynamic measures include SNR, SFDR, and noise power ratio (NPR). These quantities are determined from spectral analysis, usually in the form of a fast fourier transform (FFT) of a sequence of ADC output samples. The only error mechanism present in an ideal ADC is quantization. This error arises because the analog input signal may assume any value within the input range of the ADC while the output data is a sequence of finite precision samples (Lundberg, 2005).

In physical ADC devices, additional error mechanisms are present which includes circuit noise, aperture uncertainty, transistor non-linearity and comparator ambiguity. It can be characterized by a parameter called the ENOB or SNR bits. It is given by,

$$ENOB = \frac{SNR_{dB} - 1.76}{6.02} \tag{2.6}$$

The difference between stated resolution and ENOB for a given ADC indicates the degradation in SNR due to all other error sources. The SNR performance of an ADC depends on the signal frequency f with F_s as a parameter. SNR decreases as signal frequency increases. The value of f at which the SNR decreases to 3 dB below the low frequency value is the effective resolution bandwidth (ERBW). ERBW implies the range of frequencies over which the converter may be used.

P a universal measure of ADC performance, is the product of the effective number of quantization levels and the sampling rate (Lundberg, 2005).

$$P = 2^{ENOB}.F_s \tag{2.7}$$

The figure of merit (FoM) of an ADC is given by,

$$FoM = \frac{2^{ENOB}.F_s}{P_{diss}} \tag{2.8}$$

where P_{diss} is the power dissipation. Since many A/D converters exhibit severe degradation of SNDR at frequencies well below the Nyquist frequency, ERBW is chosen instead of the sampling rate in the equation for figure of merit. Then the new FoM is given by (Lundberg, 2005),

$$FoM_Q = \frac{(2^{ENOB}).(2ERBW)}{P_{diss}} \tag{2.9}$$

and the quantization energy (E_Q - figure of merit proposed by Walden, also denoted as FoM_w) is given by,

$$FoM_w (or) E_Q = \frac{P_{diss}}{(2^{ENOB}).(2ERBW)} \tag{2.10}$$

The effective number of bits associated with SFDR is

$$SFDR\ bits = \frac{SFDR(dBc)}{6.02} \tag{2.11}$$

This figure of merit emphasizes efficiency with respect to P_{diss}, SNR, $SFDR$, P, FoM and E_Q are used subsequently to quantify ADC performance (Walden, 1999). Figure 2.2 exhibits this difference with a degradation of approximately 1.4 bits for a given sampling rate, with scatter in the data. Figure 2.3 shows the difference between stated resolution and SFDR-bits.

The difference between stated resolution and SNR bits for a given ADC indicates the degradation in SNR due to all other error sources. SFDR is the ratio of the single-tone signal amplitude to the largest non-signal component within the spectrum of interest.

Figure 2.4 shows ADC resolution, as stated by various research papers from 1997 to 2013, versus sampling rate. Figure 2.5 shows the analysis of spurious free dynamic range (SFDR) expressed as effective number of bits, of the wide range of ADCs in the research papers from 1997 to 2013, according to Equation 2.11. Comparing Figures

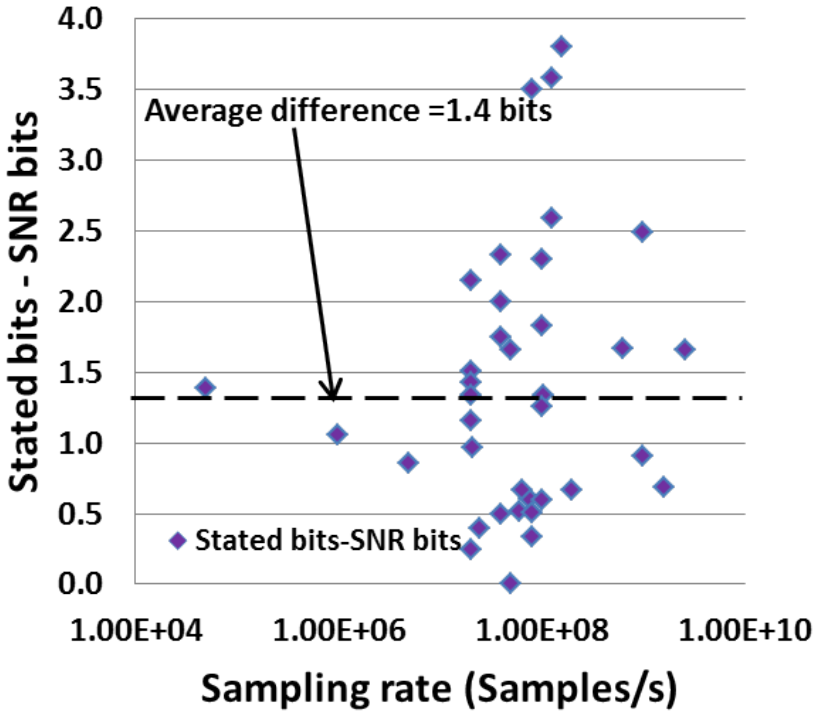


Figure 2.2: Stated bits-SNR bits versus sampling rate of wide range of ADCs in research papers from 1997 to 2013

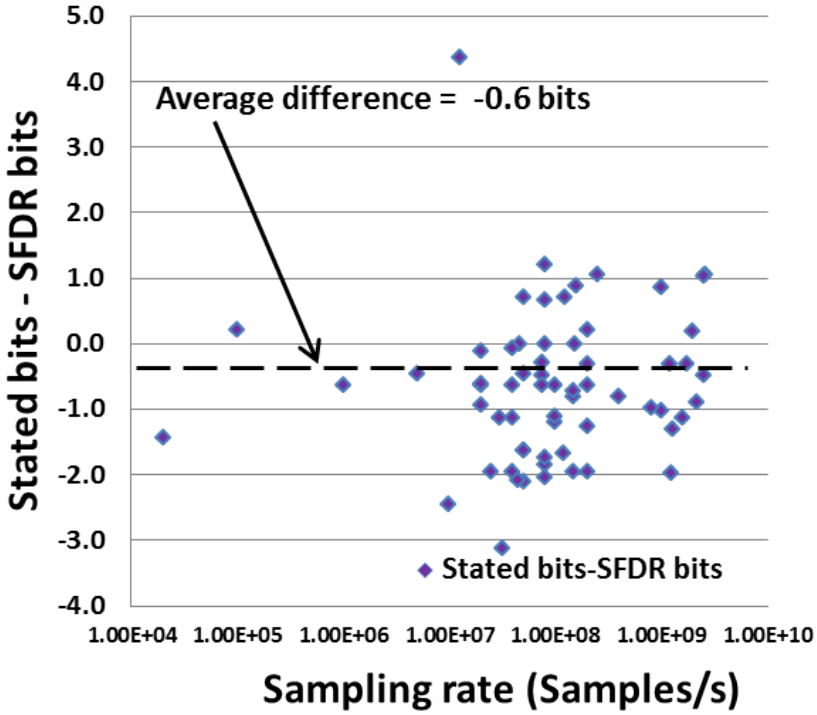


Figure 2.3: Stated bits-SFDR bits versus sampling rate of wide range of ADCs in research papers from 1997 to 2013

2.4 and 2.5 indicates that the effective resolution expressed as SFDR-bits seems to be similar to stated resolution, but from Figure 2.5 we can see that they differ by $\approx \pm 2$ bits. On comparing with the ADCs available from 1988 to 1997 (Walden, 1999) the SFDR bit variation was around $\approx \pm 3$ bits. So the variation in SFDR bits from the actual stated resolution reduced by $\approx \pm 1$ bit.

A similar graph of SNR-bits versus sample rate of the wide range of ADCs in the research papers from 1997 to 2013 is shown in Figure 2.6. Comparing with Figure 2.4 shows that the distribution of ADC's in the SNR-bits plane is approximately 1.5 to 2 bits lower than the distribution of stated resolutions. This conclusion is consistent with Figure 2.5.

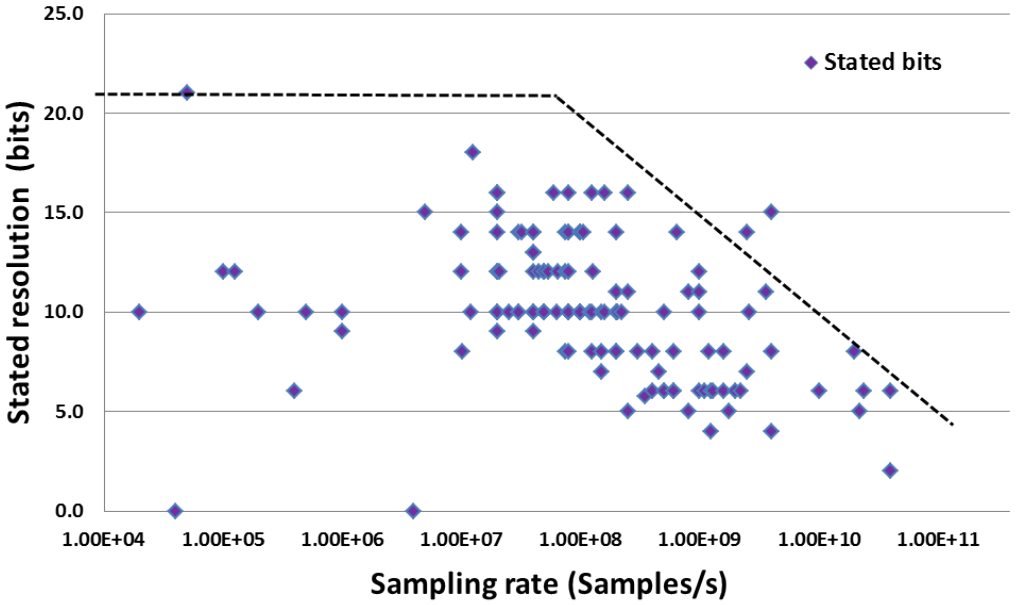


Figure 2.4: Stated resolution versus sampling rate of wide range of ADCs in research papers from 1997 to 2013.

2.2 High-Performance ADC Architectures

Integrated circuit design and fabrication technology has evolved to the point where a variety of converter architectures are available to address the high speed segment of the market. The largest market for high-speed converters is in wireless infrastructure equipment, specifically wireless radio base stations. In systems using OFDM air interfaces, including LTE and LTE-Advanced, which employ amplitude and phase modulation, the signals, are frequency modulated on RF carriers. Deciding on the correct ADC requires

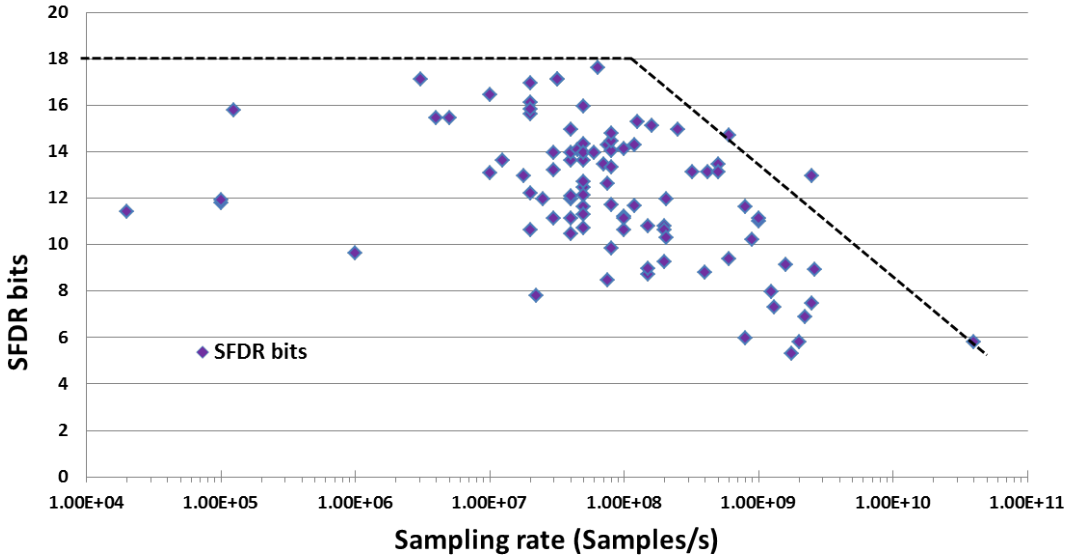


Figure 2.5: SFDR bits versus sampling rate of wide range of ADCs in research papers from 1997 to 2013.

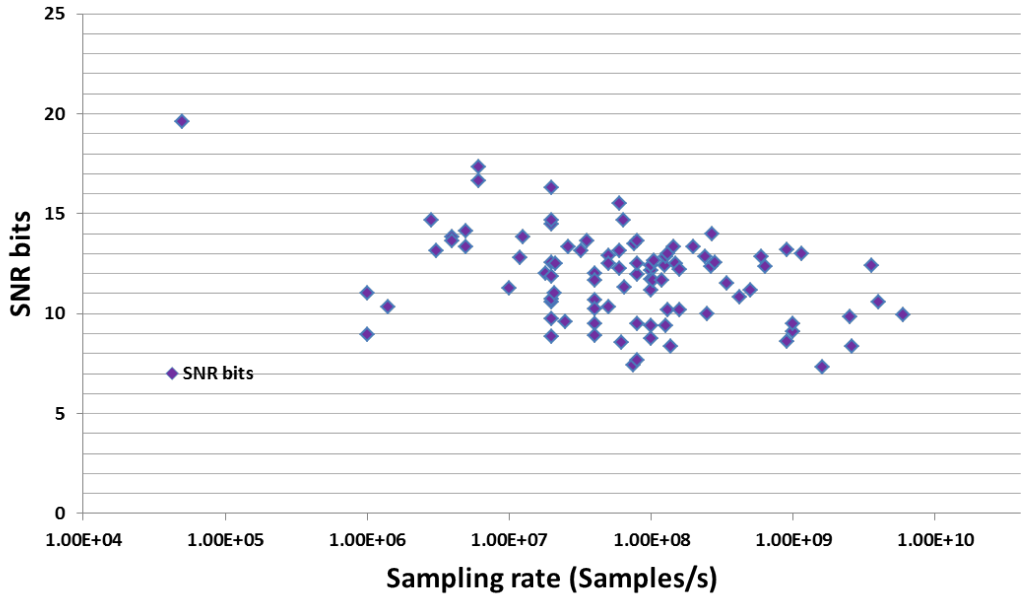


Figure 2.6: SNR bits versus sampling rate of wide range of ADCs in research papers from 1997 to 2013.

tradeoffs between resolution, channel count, power consumption, size, conversion time, static performance, dynamic performance, and price.

In present day technology of multi-standard, multi-carrier, multi-band base station systems, the bandwidth of these signals reaches 100 MHz or 125 MHz (Maury Wood and Bolatkale, 2012). In this application, a dual-channel 14-bit or 16-bit converter is suitable for synchronized I/Q sampling. In a "high IF" radio receiver configuration, the ADC should offer more than 85 dBc SFDR, and more than 77 dBFS SNR performance. Power dissipation should be minimal as a general rule. The current technology, 65 nm or 45 nm RF CMOS, offers usable transistor switching frequencies of about 8 GHz, which makes an oversampling frequency of 4 GHz feasible. The converter needs an equivalent Nyquist sample rate of 250 MHz to capture the 100 MHz of input signal bandwidth. 250 MHz x 16 = 4 GHz, so an oversampling ratio of 16 is realistic, but suggests that the modulator should be multi-bit, to provide adequate headroom to retain the system merit of simplified anti-alias filtering. In this digital radio communication application, adjacent channel rejection is critically important, so a high-order modulator is appropriate, with a bandpass response being the ideal.

Most of the data converters have been fabricated in silicon, while a few have been realized in gallium arsenide (GaAs) and indium phosphide (InP). The flash architecture uses $2^N - 1$ comparators, where N is the stated resolution. Flash converters often include one or two additional comparators to measure overflow conditions. All comparators sample the analog input voltage simultaneously. This ADC is thus inherently fast. The fastest ADC reported is the 40 GSPS 6b ADC in 65nm CMOS used for optical communication in 2010 (Greshishchev *et al.*, 2010).

Table 2.1 provides a brief description about the variety of ADCs currently used in market along with their commercial applications. The parallelism of the flash architecture has drawbacks for high-resolution applications. The number of comparators grows exponentially with resolution. In addition, the separation of adjacent reference voltages grows smaller exponentially. Consequently, this architecture requires very large IC's. It has high power dissipation. It is difficult to match components in the parallel comparator channels. Finally, increasingly large input capacitance reduces analog input bandwidth. Most flash converters available today have $\leq$ 8bit resolution, which is clear from Table 2.1. Folded flash and pipeline architectures are other alternatives which can

operate at high speed with better resolution.

A promising architecture for next generation high-speed ADC is the $\Sigma\Delta$ converter architecture. Sigma delta converters offer high-resolution, high integration and low-cost, making them a good ADC choice for applications such as process control and weighing scales. During the last decade, the bandwidth and resolution of $\Sigma\Delta$ modulators have increased more than an order of magnitude, significantly enlarging the application domain of $\Sigma\Delta$ converters which traditionally was used for primarily in digital audio and instrumentation products. The analog side of a $\Sigma\Delta$ converter (a 1-bit ADC) is very simple. The digital side, which is what makes the $\Sigma\Delta$ ADC inexpensive to produce, is more complex. It performs filtering and decimation (Maury Wood and Bolatkale, 2012).

The first commercial $\Sigma\Delta$ (or $\Delta\Sigma$) data converters were introduced to the market in the early to mid-1990s. They almost entirely eliminated the external analog anti-aliasing and anti-image filters required by legacy Nyquist converters. This significantly reduced the bill of materials (BOM) costs, and improved system phase linearity. And unlike their predecessors, the new $\Sigma\Delta$ converters did not require the laser trimming of resistor ladders, thereby significantly reducing both die and test manufacturing costs. Because $\Sigma\Delta$ converters generally use high frequency pulse density or pulse proportion modulation to encode continuous time/continuous amplitude analog signals, they can be fabricated in fine-line CMOS processes. This helps to reduce die manufacturing cost, and enables $\Sigma\Delta$ converters to be easily integrated with other CMOS digital circuit functions. These converters were initially targeted at digital voice and audio applications, including voice-band analog modems, CD players and Mini-Disc recorders. They have found broad commercial application. Mixed-signal semiconductor design and fabrication technology has now evolved to the point where $\Sigma\Delta$ converters are an attractive alternative to traditional high-speed ADC architectures.

The various parameters that impact the performance of high-speed $\Sigma\Delta$ converters are order of the modulator loop filter, number of quantizer bits in the modulator and oversampling ratio. Each parameter plays an important role in determining the performance characteristics of the converter. Therefore, the right balance has to be found to achieve the targeted performance.

Sigma-delta ADCs have been in commercial use for about 20 years. Innovations

Table 2.1: ADC categories with commercial applications

	ADC Categories	Architectures	Speeds Available	Resolution Available	Power Consumption	Channels Available	Applications
1	**High speed ADCs-1 (>10 MSPS)**	**Continuous time ΣΔ, Flash,** Folding+ interpolating, Pipeline, Two step.	**(>10 MSPS) 10 MSPS to 5 GSPS**	**16, 14, 12, 10, 8, 6**	**33mW to 4400mW**	**single, dual, quad, octal**	Telecommunications Receivers Low Power Instrumentation Multi-Channel- Data Acquisition Cellular Base Stations Spectrum Analysis Imaging Systems Software defined radios Portable Medical Imaging Multi-Channel- Data Acquisition Nondestructive Testing Broadband Communication Ultrasound Power Amplifier- Linearization
		Continuous time ΣΔ	50 MSPS	12	385mW	8	
		Flash time ΣΔ	20 MSPS to 40 MSPS	8	85mW to 150mW	1	
		Folding+ interpolating,	500 MSPS to 5 GSPS	8, 10, 12	800mW to 4400mW	1,2	
		Pipeline	80 MSPS to 900 MSPS	8,9,10,11, 12,13,14,16	49mW to 2500mW	1, 2, 4, 8	
		Two step	15 MSPS to 50 MSPS	8, 10	33mW to 267mW	1, 2	
2	**High speed ADCs-2 (≥1 GSPS)**	**Folding+ interpolating, Pipeline**	**(≥1GSPS) 1 GSPS to 25 GSPS**	**7,8,10,12,**	**1200mW** to **4400mW**	**single, dual**	Software defined radios Portable Medical Imaging Broadband Communication ATE Systems Digital Oscilloscopes Digital RF/IF- Signal Processing Electronic Warfare- (EW) Systems High-Energy Physics Instrumentation High-Speed Data- Acquisition Systems Light Detection and - Ranging (LIDAR) Radar Warning- Receivers (RWR)
		Folding+ interpolating	1 GSPS to 3.6 GSPS	7,8,10,12,	1200mW to 4400mW	single, dual	
		Pipeline	1 GSPS	12	2200mW	single	
3	**Precision ADCs**	ΣΔ **Dual slope, Pipeline**	**(≤12MSPS) 3 SPS** to **12 MSPS**	**31,24,20,18, 16,15,14,12, 10,8,4.5**	**0.21mW to 960mW**	**1,2,4,5,6, 8,10,12,16**	Avionics Data-Acquisition Systems Industrial Control Systems Robotics Automated Test Equipment (ATE) Medical Instruments Weigh Scales Portable Battery- Powered Equipment Multiple Transducer- Measurements Vibration Analysis Patient Monitoring Multiphase Power Systems Power-Protection- Relay Equipment
		SAR Hybrid Pipeline-SAR					
		ΣΔ	10 SPS to 10 MSPS	31,24,20,18, 16,14,12,10	0.21mW to 960mW	1,2,3,4,6, 7, 16	
		Dual slope	3 SPS to 3 kSPS	14, 4.5	5mW	1,4	
		Pipeline	1 MSPS to 12.5 MSPS	10,12,14	15mW to 270mW	1,2,4	
		SAR Hybrid pipeline-SAR	4.6 MSPS	12	42.9mW	1	

in $\Sigma\Delta$ ADC architecture combined with advanced RF CMOS process technology have now made these converters suitable for use in wireless digital communications applications, with associated cost and performance advantages. As the inexorable progress of "nano scale" CMOS continues, the bandwidth of CT $\Sigma\Delta$ ADCs are also expected to scale with improvements in transistor switching speed.

The performance analysis of ADCs based on the Walden's figure of merit (FoM_w) (Equation 2.10) is analyzed here. Actually Robert Walden suggested a figure of merit for A/D converters that takes into account power dissipation, resolution in terms of ENOB, and sampling rate. It has units of energy, and represents the energy used per conversion step. In practice, many A/D converters exhibit severe degradation of SNDR at frequencies well below the Nyquist frequency. For this reason, effective resolution bandwidth (ERBW) instead of the sampling rate as pointed out in Equation 2.9.

Figure 2.7 shows the figure of merit versus speed (in terms of Nyquist sampling rate) of wide range of ADCs in research papers from 1997 to 2013. The idea here is to evaluate energy efficiency against absolute speed. Lower the FoM, better the performance of the ADC with respect to energy efficiency. Figure 2.7 also shows a comparison of ADCs reported in the year 2013 with the past ADCs reported over the years 1997 to 2012. It is clear that the latest ADCs shows better FoM-Speed performance compared to the previous ones. However, the performance degrades above a speed of $\approx$ 1 GSPS.

2.3 ADC Performance Over Time

It is revealing to examine the trends in ADC performances during recent years. Excellent progress has been made recently in developing power-efficient designs. However, the same is not true for the advancement of the resolution-speed product. To show this, the SNR data were sorted according to the year in which the ADC's were reported. The results are given in Figure 2.8, and it is evident that relatively little improvement has been made over the last 10 years or so. From the scatter in the data it is also evident that the improvement is quite sporadic. Over the past 10 years (from 2003 to 2013) an SNR performance improvement of 3 SNR-bits is achieved.

It is interesting to look at the development of ADCs over the years (Lee *et al.*, 2005). The historical trends of ADCs provide some insight into their progress and de-

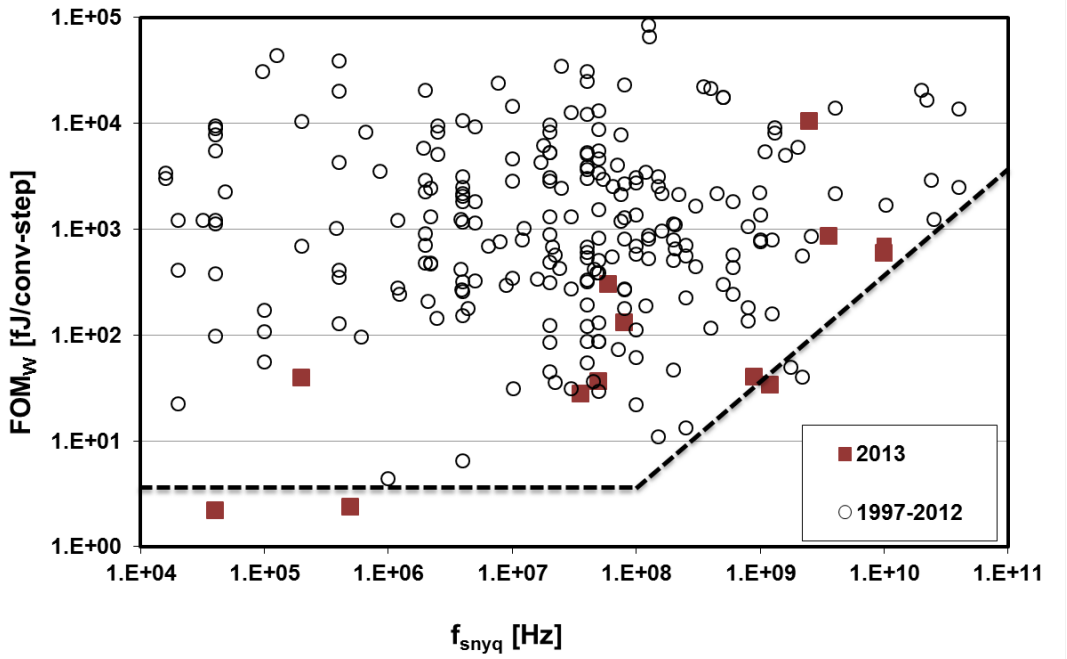


Figure 2.7: Walden's FoM versus Nyquist sampling rate (speed) of wide range of ADCs in research papers from 1997 to 2013.

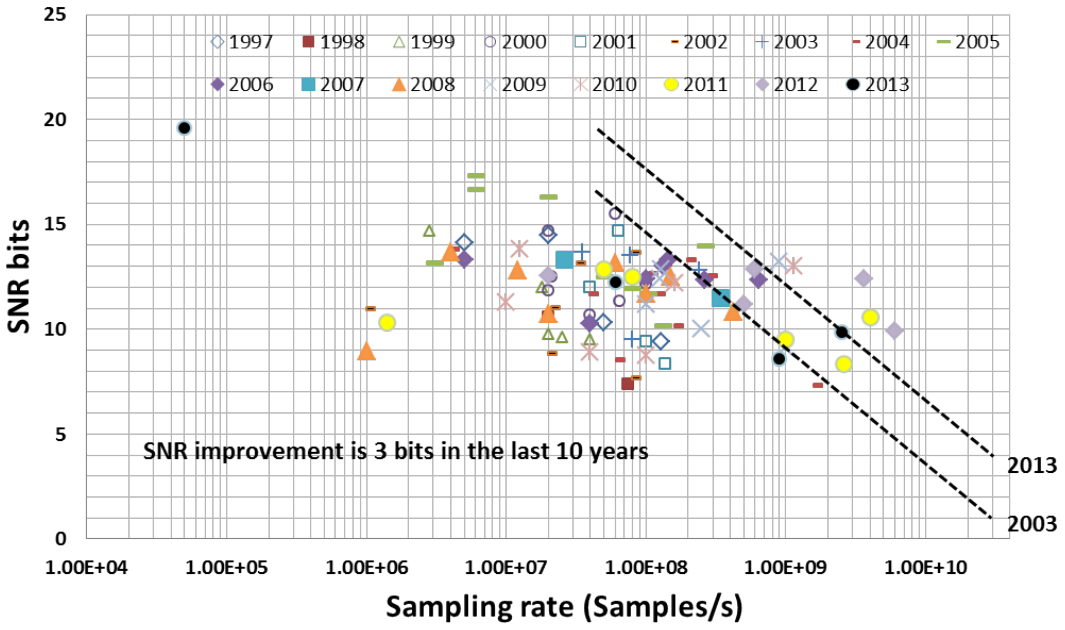


Figure 2.8: Trend in SNR bits over time

velopment, which can then compare with Walden's publication that discusses the ADC trends up to 1997 with future projections into 2015. The latest trends in ADC research over the last 16 years is discussed in Figure 2.9. Each and every year the FoM_w continue to reduce and hence shows performance enhancement in terms of power consumption, resolution and bandwidth. Over the last 3 years researches are more concentrated on Sigma Delta, Flash and SAR ADCs.

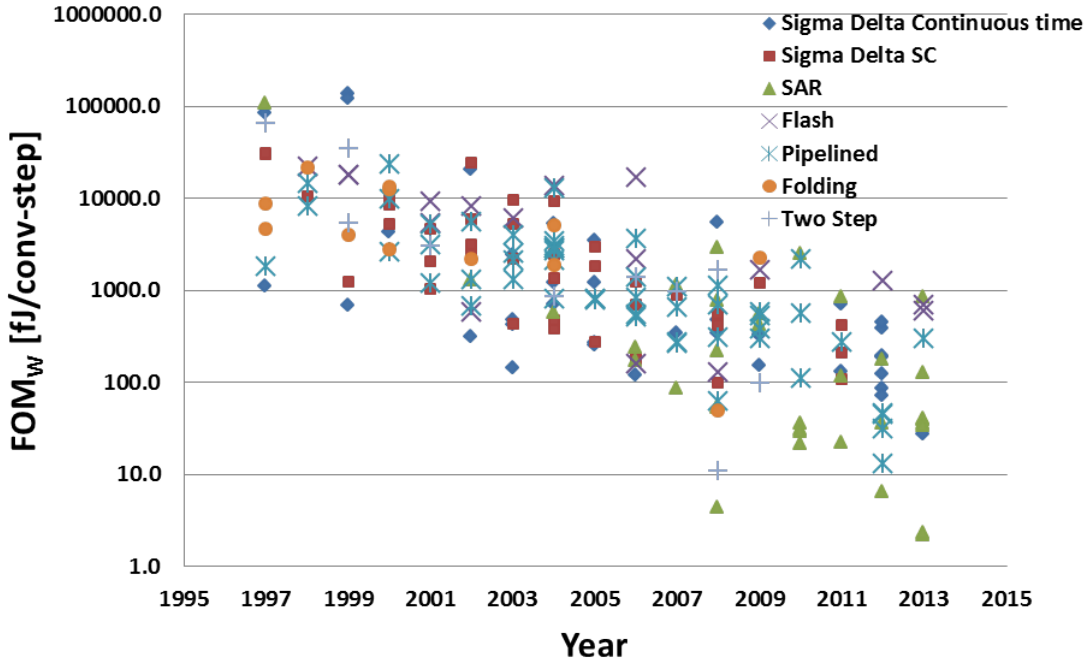


Figure 2.9: Historical trend in Walden's FoM of a wide range of ADCs in research papers from 1997 to 2013

2.4 Relevance of the Work

Mobile telecommunication has experienced tremendous growth since the progressive development of wireless communication systems. Several mobile telecommunications standards are used worldwide in the transition from the second generation (2G) digital system into the third generation (3G) system. The most popular standard for 3G systems is WCDMA, supported by the third generation partnership project (3GPP). 4G mobile systems will be further integrated with WLAN. A user will employ the WLAN mode whenever the mobile terminal is within range of a WLAN access point. WLAN-enabled cell phones are expected to contain multi-mode cellular capability. A suggestion is to encompass GSM and WCDMA operation, in addition to WLAN.

Sigma-delta modulator is the most promising candidate to achieve high-resolution over a wide variety of bandwidth requirements in multi-mode receivers. The advantage of $\Sigma\Delta$ ADCs in providing high-resolution with low-precision components lies on the use of over-sampling and noise shaping. As bandwidth requirement increases, the over-sampling ratio decreases which results in a decrease in the resolution. Designing $\Sigma\Delta$ modulators that can achieve high-resolution and wide bandwidth remains challenging.

Technologies are available for various wireless transceiver design and technology is keep changing based on the scaled implementation technique. However, researchers are still pursuing extensive research for improving the design for better features. Also there are new problems with latest technologies. As fabrication technology scales, chips are becoming less reliable, thereby increasing the power and performance costs for reliable wireless designs. There exist scopes for improvement of technology for new wireless standard design. Programmable and configurable chips are rapidly replacing function specific devices. Processing systems increasingly need to consider the actual content that is being processed and adapt their processing to the content. The amount of reconfigurability present in a system-on-chip is increasingly steadily and is expected to reach 68% by 2022 according to the International Technology Roadmap for Semiconductors (ITRS) 2007. These future devices will integrate billions of transistors with feature sizes in the order of nanometers. New approaches will be required to cope with high expected process variation and to obtain energy efficient and reliable designs with good yields.

Most of the research to date (Lim, 2002; Horn and Demian, 2002; Burger and Huang, 2001; Gomez and Haroun, 2002; Miller and Petrie, 2003; Dezzani and Andre, 2003; Xotta *et al.*, 2005) has been focused on ADC, which do not have as tight constraints on area and power as handsets. However, the ultimate aim of $\Sigma\Delta$ converter designs are targeted to mobile transceivers where their true potential can be realized. Significant progress has been made in $\Sigma\Delta$ ADC research by various research institutes through different programmes. But these radios have yet to reach the compact form factors that characterize mobile handsets. The additional area and power constraints placed by handsets with limited resources pose a major design challenge. The main objective of this research is to develop novel models and techniques to address state of the art design issues.

Future wireless multimedia computing devices will have to be flexible enough to accommodate various multimedia services and communication capabilities while meeting the high-performance computational demand. At the same time, low-power consumption will continue to be the predominant design challenge of wireless systems The diverse but complementary research issues addressed will lead to a new horizon of knowledge in future research on wireless circuits and systems. The findings reported in the thesis could trigger future research in other wireless devices where low-power consumption and reconfigurability are important design concerns. The research problems in this project could also find application in wireless sensor networks, which is an interdisciplinary area involving distributed computing, networking, wireless communications, and ultra-low-power design.

2.5 Literature Review

2.5.1 TDM based Incremental $\Sigma\Delta$ Modulators

Many multi-channel applications require low-power ADCs covering bandwidths from kilo-hertz to mega-hertz and resolutions in the range of 9 to 20 bits. With the advancements in DSP field, $\Sigma\Delta$ modulator was ready to tackle industry problems and to be applied for real applications. The first application was in the audio field which requires high-accuracy with small signal bandwidth and has been difficult for traditional Nyquist-rate data converters to deliver the required performance. By utilizing the potential of highly sophisticated digital processing and the advantages of oversampling and noise shaping techniques $\Sigma\Delta$ modulator achieves high-resolution, absolute accuracy and relaxes the matching required between analog components, when compared to Nyquist counterparts. Unfortunately, traditional ADCs are dynamic systems with memory and thus, they cannot be directly used in time-multiplexed environments. In some biomedical sensor systems such as electroencephalogram (EEG) and electrocardiogram (ECG) systems incremental ADCs are well suited due to their ability to be multiplexed among several channels.

In traditional I$\Sigma\Delta$ modulators, the associated integrators, memory elements and the entire modulator itself is re-setted periodically between each input sample. The corre-

sponding digital stream is generated between successive resets. By the process of channel switching during each successive resets enables the modulator to access samples from multiple channels. Thus a single I$\Sigma\Delta$ modulator can be easily time-multiplexed between several channels. In contrast to traditional incremental models, the proposed TDM based I$\Sigma\Delta$ operates with respect to TDM frames rather than samples. The process of periodic resetting of the modulator and channel switching between multiplexed channels takes place in between successive TDM frames, thereby, enhancing the operating speed of the modulator.

For high-resolution multi-channel applications, the role of I$\Sigma\Delta$ ADCs are inevitable (Robert *et al.*, 1987), (Chi and Cauwenberghs, 2010), (Guo *et al.*, 2011), (Liang and Johns, 2010), (Márkus *et al.*, 2004), (Mollazadeh *et al.*, 2009), (Uhlig *et al.*, 2009), (Yu *et al.*, 2010). From a power consumption perspective, high-order architectures are especially attractive, as they reduce the number of cycles per conversion (Nc). High-order loop-filter topologies have been used in discrete-time (DT) I$\Sigma\Delta$ ADC implementations (Liang and Johns, 2010; Quiquempoix *et al.*, 2006; Yu *et al.*, 2010). First-order topologies have been proposed for continuous time (CT) I$\Sigma\Delta$ ADC implementations (Chi and Cauwenberghs, 2010), (Mollazadeh *et al.*, 2009). In order to exploit their advantage in terms of power dissipation, high-order CT topologies have been employed in several traditional ADCs (Pavan and Sankar, 2010), (Zhang *et al.*, 2011). This advantage of having reduced power consumption originates from the absence of switches in a CT loop filter which relaxes the settling and bandwidth requirements of the active blocks. Third order I$\Sigma\Delta$ CT topologies have been employed for time-multiplexed biosensor applications (Garcia *et al.*, 2013). The input of the modulator is the form of samples, as sampling occurs at the output of the multiplexer (MUX) preceding a multi-channel ADC. The CT I$\Sigma\Delta$ modulators would still be able to benefit from the CT advantages like implicit anti-aliasing and low-power implementation, as the loop filter processes each sampled input in a CT fashion by making use of oversampling. Higher-order CT I$\Sigma\Delta$ ADCs have been investigated in Garcia and Rusu (2011) for single-loop architectures and in Guo *et al.* (2011) for cascaded counterparts. A CT implementation would benefit from the aforementioned advantages, compared to high-order DT I$\Sigma\Delta$ ADCs (Liang and Johns, 2010), (Quiquempoix *et al.*, 2006), (Yu *et al.*, 2010). Certain possible issues such as wider integrators' coefficients spread and increased sensitivity to ELD and jitter would impose difficulties in CT implementations which are not

present in a DT alternatives. High-order CT architecture would benefit from a lower number of cycles per conversion, Nc, at the expense of increasing the complexity in the CT loop filter, when compared to first order CT I$\Sigma\Delta$ ADCs (Chi and Cauwenberghs, 2010), (Mollazadeh *et al.*, 2009). The required sampling frequency can be reduced considerably by reducing Nc as it possibly relaxes the integrators' bandwidth as well as the sensitivity to jitter. In chapter 3, a TDM based 3^{rd} order CT I$\Sigma\Delta$ modulator for analog-to-digital conversion of time-multiplexed low frequency channels is presented. The proposed scheme has the potential to evaluate the benefits of combining a high-order topology with a CT approach and to realize a high-resolution modulator for high-precision applications like TDM based audio channels and biomedical sensor channels.

Excess loop delay (ELD) is a severe problem that degrades the performance of the $\Sigma\Delta$ loop and that too much delay can result in an unstable modulator (Pavan, 2008). Several techniques for mitigating the effect of loop delay have been proposed. In Benabes *et al.* (1997), the authors propose the use of a direct path around the quantizer. Additional feedback paths and tuning of the loop filter coefficients are proposed in Gao *et al.* (1997) to restore the noise transfer function (NTF) to the one without excess loop delay. Cherry and Snelgrove (1999*b*) suggests a feedback DAC with a different pulse shape (while also tuning the loop filter coefficients) to accomplish the same objective. All of the delay compensation methods in the papers cited above are essentially equivalent to adding a direct path around the quantizer and tuning the filter coefficients. The modified coefficients and the gain of the direct path around the quantizer needed to restore the NTF to the desired one are computed and illustrated using a second-order example (Cherry and Snelgrove, 1999*b*) in chapter 3.

2.5.2 Enhanced Noise Shaping based Cross-Coupled $\Sigma\Delta$ Modulators

The most popular choice of ADC for low-to-medium bandwidth high-resolution applications is the $\Sigma\Delta$ ADC due to its inherent noise shaping and oversampling characteristics. It is well known that $\Sigma\Delta$ modulators are extensively used in instrumentation, audio and broadband applications. The traditional trade-off between resolution and bandwidth in ADCs forms an all time barrier in any mixed signal design. The sampling frequency

of the converter, a critical parameter, is always limited by the technology constraints.

In order to accomplish realizable $\Sigma\Delta$ modulators for high-bandwidth applications, a lower OSR is preferred. Resolution of ADCs depends directly on OSR, quantizer resolution and in-band noise rejection. TI modulators are an attractive solution for high-speed applications to achieve high SNR at low OSR using low-order modulators (Lee and Maloberti, 2004). Several ADCs operate in parallel, using different clock phases, in an N-path $\Sigma\Delta$ modulator. Each of the path runs at $1/N$ times the overall sampling frequency (i.e.F_s/N), where N is the number of paths used (Bernardinis *et al.*, 2006). N-path architecture achieves the same SNR of single-path architecture with a lower order loop filter with benefits in terms of stability and complexity (Gharbiya and Johns, 2008). A wideband cross-coupled $\Sigma\Delta$ modulator that uses this method to increase SNR and signal bandwidth is analyzed in Bilhan and Maloberti (2008). In addition, the effect of cross-coupling the noise on TI $\Sigma\Delta$ ADCs is investigated in Pamarti (2008). Hamidi et al. proposed an unextended and extended noise-coupling techniques in TI cross-coupled $\Sigma\Delta$ modulators to improve the effective order to $(2N-1)$ (Hamidi and Miar-Naimi, 2014).

A wide-band ADC necessitates the requirement of higher sampling rate, which drastically degrades the performance in terms of power dissipation. An alternative approach is to employ higher-order noise shaping. Unfortunately the single-loop high-order $\Sigma\Delta$ modulators are highly sensitive to loop instability issues. Multi-stage noise shaping (MASH) architecture is the best candidate for achieving a stable higher-order modulator, but the analog-digital filter mismatches (Schreier *et al.*, 2005) and resulting quantization-error leakage in the MASH structure degrades its performance. A solution to alleviate this problem was the SMASH (Maghari *et al.*, 2006) structure that makes the modulator purely analog and perfectly cancels the first stage (stage-I) quantization error. Chapter 4 proposes a novel TI extended (Hamidi and Miar-Naimi, 2014) cross-coupled multi-path SMASH architecture that compensates the ESLD. The TI architecture makes the hardware run at half the clock rate (Hamidi and Miar-Naimi, 2014), which drastically reduces the power consumption. A 2-path extended noise shaping based TI cross-coupled $\Sigma\Delta$ modulator is used as stage-I of the proposed SMASH modulator. The quantization error (ε_1 and ε_2) of stage-I is extracted and processed by the second stage (stage-II) loop filter and a quantizer with error (ε_{11} and ε_{22}) is injected back to stage-I. The finite delay caused by the extraction and processing of ε_1 and ε_2

performed by stage-II, called ESLD, is modelled in the proposed multi-path TI architecture. The mechanism realized to compensate the effect of ESLD perfectly cancels stage-I quantization error by the modified SMASH logic and also improves the overall stability. An enhanced noise shaping technique, called the Dual Extended noise shaping, to improve the effective order of the modulator is also proposed in chapter 4.

2.5.3 Multi-standard Reconfigurable Time Interleaved Cross-Coupled $\Sigma\Delta$ Modulator

The demand for efficient and portable broadband wireless devices have made them to be of small volume, light weight, low-power, low-cost and support all radio technologies in a common platform, thanks to the rapid advances in VLSI. A fully reconfigurable low-power ADC is needed for having to handle diverse wireless standards in 4G radios. The multi-standard cellular capability covering GSM/ Bluetooth/ GPS/ WCDMA/ WLAN/ WiMAX for wide range of applications created the necessity to develop multi-mode, portable, power and area efficient ADC architectures.The increasing demand of $\Sigma\Delta$ ADC for state-of-the-art multi-standard wireless receivers is due to its high degree of robustness to physical level effects, inherent resolution-bandwidth tradeoff and increased digital programmability (Rusu *et al.*, 2006*b*; Silva *et al.*, 2009; Gerosa *et al.*, 2006; Morgado *et al.*, 2012). Sigma delta ADC suitable for multi-mode receivers has already been published in many literatures. These solutions of switched capacitor (SC) $\Sigma\Delta$ modulators that cover mainly GSM/ Bluetooth/ GPS/ WCDMA/ WLAN/ WiMAX standards are presented in Table 2.2.

Chapter 5 describes an efficient triple-mode hexa-standard reconfigurable TI cross-coupled $\Sigma\Delta$ modulator, utilizing the flexible switching between unextended (Bilhan and Maloberti, 2009), (Hamidi and Miar-Naimi, 2014), extended (Hamidi and Miar-Naimi, 2014) and dual extended (DE) (proposed scheme) (Prakash *et al.*, 2014) noise shaping characteristics, targeting required performance specifications for a wide variety of mobile communication standards mentioned above. The DE noise shaping (Prakash *et al.*, 2014) technique provides $2N^{th}$-order noise shaping out of an N-path cross-coupled $\Sigma\Delta$ modulator without degrading its high conversion rate and bandwidth. A low oversampling ratio (OSR) is the preferred choice to accomplish stable and realizable $\Sigma\Delta$ modulators for high-bandwidth applications. In the case of wide-band

Table 2.2: Performance summary of the published multi-standard $\Sigma\Delta$ ADCs

Work	Modes	Bandwidth (MHz)	Sampling Freq.(MHz)	Architecture	CMOS Process	Power (mW)
(Burger and Huang, 2001)	2	0.2/3.84	104/184.32	3^{rd} order $\Sigma\Delta$	0.25µm	11.5/13.5
(Gomez and Haroun, 2002)	2	0.2/2	26/46	2^{nd} order $\Sigma\Delta$	0.13µm	2.4/2.9
(Miller and Petrie, 2003)	2	2/1.92	23/46	2^{nd} order $\Sigma\Delta$	0.18µm	30/50
(Dezzani and Andre, 2003)	2	0.1/1.92	39/38.4	Cascaded 2-1	0.13µm	2.4/4.3
(Zhang *et al.*, 2004)	3	0.2/5/20	51.2/100/100	Cascaded 2-1-1-1	0.18µm	–
(Farahani and Ismail, 2004)	3	0.2/1.5/1.92	23/46	Cascaded 2-2	0.18µm	5.8/5/11
(Gerosa *et al.*, 2006)	3	0.271/3.84/20	138/245/320	Cascaded 2-1-1	0.35µm	58/82/128
(Rusu *et al.*, 2006*a*)	3	0.1/2/10	32/64/160	3^{rd} order FF $\Sigma\Delta$	0.18µm	1.75/0.99/4.76
(Du and Tiew, 2007)	3	0.5/2/8	64/64/64	Cascaded 2-2-2	0.18µm	1.22/0.95/7.9
(Bos *et al.*, 2009)	4	0.1-2	50-90	Cascaded 2-1	90nm	0.72 - 2.97
(Jose *et al.*, 2011)	3	0.1/1/10	64/64/200	Cascaded 2-2-2	0.18µm	5.35/4.87/4.27
(Morgado *et al.*, 2012)	6	0.1-10	40-240	Cascaded 2-2-2	90nm	7.6 - 23.5
(Seyedhosseinzadeh and Yavari, 2012)	5	0.25-12.5	62.5-200	Cascaded 2-2	90nm	5 - 37

applications, to achieve high SNR at low OSR and using low-order modulator, time-interleaving technique is the best solution (Lee and Maloberti, 2004). Power dissipation of battery operated hand held electronic devices is a critical parameter, which drastically increases with sampling frequency, F_s (Jinfeng *et al.*, 2011). By the introduction of time interleaving technique the proposed architecture operates at half the sampling rate, which significantly brings down the power consumption (Bernardinis *et al.*, 2006). Compared to other alternatives, a low OSR is sufficient to attain the expected performance for all the six wireless standards using the proposed reconfigurable $\Sigma\Delta$ architecture, of which a basic model has been presented in (AV and Jose, 2014).

The major challenge in the design of reconfigurable low-power structures is the wide variations in bandwidth and ENOB, power and chip area optimization for different operation modes, immunity towards circuit non-idealities and capability to reconfigure in worst case situations. Chapter 5 contributes to the novel design of a cross-coupling based efficient method for implementing higher order hexa-standard reconfigurable ADCs and to the best of the authors' knowledge none of the reported multi-standard $\Sigma\Delta$ modulators can be reconfigured with this level of hardware and power efficiency.

2.5.4 Differential Quantizer based Error Feedback Modulator for Analog-to-Digital Conversion

The idea of oversampling and noise shaping data conversion, specifically $\Sigma\Delta$ analog-to-digital conversion technique (Inose *et al.*, 1962), has emerged as a promising candidate in the field of high-precision data conversion applications, like digital radio, hifi audio, micro-sensors, telecommunications and wireless IF applications (Galton, 2002). $\Sigma\Delta$ ADCs are inevitable in a wide range of electronic devices in professional and consumer markets, due to its inherent simplicity. The spectral separation of the noise and input signal and the benefits like linearity, tolerance to analog component imperfections and simple antialiasing filtering achieved by oversampling and noise shaping phenomena makes it far superior to other ADC methodologies. The rigorous search for efficient digitization techniques has resulted in the invention of delta modulator (Deloraine and Reeves, 1951) and its successor $\Sigma\Delta$ modulator. The analog-to-digital converter (ADC) design can be optimized for a specific application and context, because of the availability of wide variety of $\Sigma\Delta$ modulators and associated signal processing tools. Nowadays,

oversampled ADCs are inevitable in the broad domain of electronic equipment markets.

Until now the only choice of an ADC technique, which we have in the domain of oversampling and noise shaping converters, were the $\Sigma\Delta$Ms. The major challenges associated with the design of higher order $\Sigma\Delta$M are loop stability issues due to its inherent non-linearity, integrator associated non-idealities, optimization of the integrator scaling coefficients (Maloberti, 2007) and low operating bandwidth due to the accumulation of samples. An excellent alternative in the class of oversampling and noise shaping converters, that can mitigate these problems associated with $\Sigma\Delta$M, is the newly introduced DQEFM. Like the interpolative $\Sigma\Delta$ ADC technique, DQEFM also works on the basis of negative feedback system, but the feedback signal is the quantization error rather than the modulator's output. The error feedback modulators (EFMs) (Norsworthy *et al.*, 1997) has been widely utilized for the implementation of highly efficient digital-to-analog converters (DACs). In EFMs the error signal is generated by extracting the LSBs of the output signal, whereas, in DQEFM ADC the error signal is obtained by the analog subtraction performed by the differential quantizer, discussed later. The imperfections associated with the analog subtraction and analog loop filter can be compensated by simple tuning mechanism.

Bandpass $\Sigma\Delta$ modulators (BP-$\Sigma\Delta$Ms) are used to suppress quantization noise for narrow band signals that are concentrated at an intermediate frequency (IF) rather than DC. Digitizing such narrow band IF signals of superheterodyne radios, like digital radio, are of great industrial significance because, it allows digital channel-select filtering, digital gain control, digitally coded communication with multiple standards and also manufacturing advantages in terms of robustness of the digital hardware (Singor and Snelgrove, 1995; Schreier and Snelgrove, 1989; Jantzi *et al.*, 1991, 1993; Longo and Horng, 1993).

The SC based implementation, which is the most popular approach for sampled-data systems, is used to realize the proposed DQEFM architecture. The implementation of differential quantization normally uses switched capacitors and a quantizer (He *et al.*, 2014). The new DQEFM uses this differential quantizer as a replacement to the integrators and the $\Sigma\Delta$ loop itself, and thus obviates the requirement of power hungry op-amps. The mathematically synonymous characteristic makes all the existing topologies and robust techniques, which are developed for $\Sigma\Delta$M, are very well applicable

for DQEFM. The noise shaping characteristics and the dynamic range of interpolative $\Sigma\Delta$M can be enhanced by quantization noise-coupling techniques (He *et al.*, 2014), (Lee *et al.*, 2006). The quantization noise self-coupling used for ADC performance enhancement and EFM technique for efficient DAC implementation, have been employed in the DQEFM based analog-to-digital conversion.

CHAPTER 3

A TDM BASED CONTINUOUS TIME INCREMENTAL $\Sigma\Delta$ MODULATOR

A low-cost time division multiplexing (TDM) based 3^{rd} order continuous time (CT) I$\Sigma\Delta$ modulator for analog-to-digital conversion of time-multiplexed low frequency signal channels is proposed in this chapter. A 3^{rd} order CT design is investigated here because of its inherent low-power and implicit anti-aliasing characteristics. The high-resolution characteristics of the proposed modulator make it suitable for time-multiplexed audio applications. A method to compensate the excess loop delay (ELD) to improve the performance of the modulator is also adopted in this chapter. A circuit-level behavioural simulation of the CT incremental sigma delta (I$\Sigma\Delta$) modulator for high-frequency applications has been done using the embedded behavioural simulator, SIMSIDES, and the effect of thermal noise, fixed loop delay and signal-dependent loop delay on the performance is analyzed thoroughly.

The chapter is organized as follows. Section 3.1 provides the system-level overview and describes the operation and design methodology of the proposed I$\Sigma\Delta$ ADC. Section 3.2 describes the measurement setup to enable the incremental mode of operation and measurement results highlighting the performance of the proposed modulator and comparison with state-of-the-art counterparts. Section 3.3 adopts a method to mitigate the effect of ELD in the proposed CT modulator. Circuit-level simulation using Simulink based time-domain behavioural simulator - SIMSIDES is presented in section 3.4. Finally, Section 3.5 portrays the inferences from this chapter.

3.1 System Architecture

3.1.1 System overview

A block diagram of a TDM based CT I$\Sigma\Delta$ modulator for a multi-channel environment, together with the input channel multiplexer and the necessary sample and hold circuit

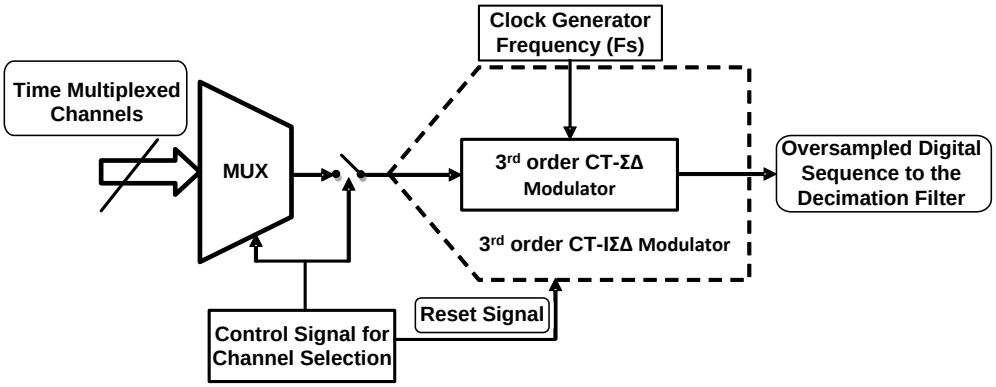


Figure 3.1: Multi-channel TDM based CT IΣΔ modulator block diagram

is shown in Figure 3.1. IΣΔ ADC reset their memory elements before each conversion and hence they can offer sample-by-sample conversion as Nyquist-rate ADCs. The feature of one-to-one mapping between input and output makes them suitable for processing multiplexed input signals (Tao *et al.*, 2013). From a system-level perspective, the main difference that distinguishes IΣΔ ADCs from traditional ADC counter parts is that they can be used in a multi-channel environment, processing time-multiplexed signals. The proposed model specifically targets a time division multiplexed communication scenario and processes such multiplexed signal channels on a TDM-frame-by-frame basis rather than handling them in a sample-by-sample topology. Since the signal channels are processed on TDM-frame-by-frame topology, one-to-one mapping between input and output is strictly maintained which makes them suitable for processing multiplexed input signals.

At the beginning of every conversion, the input signal of the selected channel is sampled and the modulator's states are reset. A TDM frame of the selected channel is then fed to the CT IΣΔ modulator which performs the conversion at frequency F_s. The number of cycles, N, the modulator runs per TDM frame is proportional to the number of samples per TDM frame which in turn depends on the oversampling ratio and signal bandwidth. As a rule of thumb at least 16k samples are needed per frame for obtaining sufficient SNR. After N clock cycles have passed, an oversampled digital sequence corresponding to the TDM frame of the selected channel is obtained from the output of the modulator, then the modulator states are reset and new conversion of the next TDM frame of another channel can take place.

Besides the advantage of being suitable for multi-channel environments, IΣΔ ADCs have some limitations compared to traditional ΣΔ counterparts (Garcia *et al.*, 2013).

The main limitation is that, as shown in (Caldwell and Johns, 2010), traditional $\Sigma\Delta$ ADCs have improved signal-to-quantization-noise ratio ($SQNR$) performance with respect to equivalent I$\Sigma\Delta$ ADCs in all situations but at very low OSRs. The proposed TDM based I$\Sigma\Delta$ modulator topology overcomes this limitations by achieving excellent SQNR performance equivalent to that of traditional $\Sigma\Delta$ topology.

3.1.2 Design Methodology

The block diagram of the proposed CT I$\Sigma\Delta$ modulator is shown in Figure 3.2.

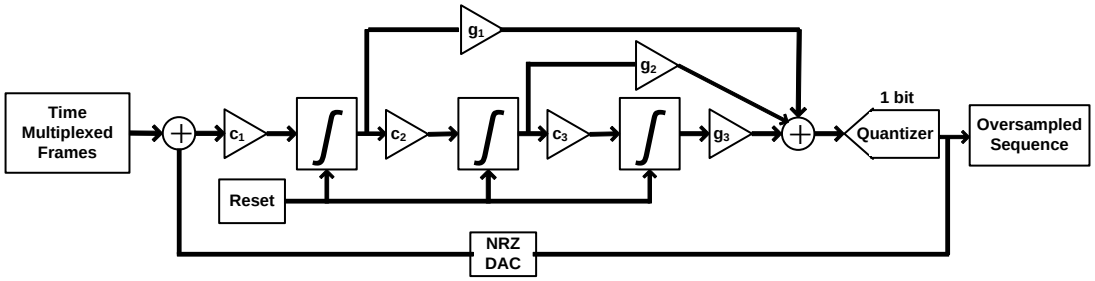


Figure 3.2: Block diagram of the proposed CT I$\Sigma\Delta$ modulator

With respect to previous CT I$\Sigma\Delta$ ADCs, 3^{rd} order architectures have been implemented using CT loop filters (Garcia *et al.*, 2013) with the limitation of poor SNR performance. Cascade-of-integrators in feed-forward (CIFF) configuration with input signal feed-forward has been used to relax the signal swing in the integrators path and minimize the performance degradation due to coefficient variations. The CIFF structure eliminates the reliance of integrators on the input signal leaving quantization and circuit noise only, so the output swing of integrators is significantly reduced and the power consumption is largely saved (Lei *et al.*, 2011). All previous incremental implementations, but (Yu *et al.*, 2010), have used a single bit implementation. At a cost of less aggressive noise transfer function (NTF), a single-bit implementation has been chosen in this work as it minimizes the digital filter complexity and avoids the use of linearization techniques in the feedback DAC. In CT implementations, however, the use of a single-bit DAC will increase the sensitivity to jitter and ELD, unless properly assessed. The effect of ELD is analyzed in this chapter.

A 3^{rd} order DT NTF is synthesized using the Sigma-Delta Toolbox (Schreier, 2004)

for an out of band gain (OBG) of 1.5 and all zeros at DC.

$$NTF(z) = \frac{(z-1)^3}{D(z)} = \frac{(z-1)(z^2-2z+1)}{(z-0.6694)(z^2-1.531z+0.6639)} \tag{3.1}$$

where $D(z) = (z-0.6694)(z^2-1.531z+0.6639)$ The CT NTF is derived from the DT NTF using impulse invariance transformation. The discrete time loop transfer function L(z) is obtained from the NTF(z) using the expression,

$$NTF(z) = \frac{1}{1+L(z)} \tag{3.2}$$

Using impulse invariance transformation the discrete time loop transfer function L(z) is converted to CT loop transfer function L(s) as

$$L(s) = \frac{k_1}{s} + \frac{k_2}{s^2} + \frac{k_3}{s^3} \tag{3.3}$$

where, $k_1 = c_1 \times g_1 = 0.6703, k_2 = c_1 \times c_2 \times g_2 = 0.2442, k_3 = c_1 \times c_2 \times c_3 \times g_3 = 0.0440$. Thus synthesis of the CT $\Sigma\Delta$ modulator is done by discretizing its loop filter and equating it with the loop filter of a discrete time (DT) using impulse invariance transformation. A sampling rate of 1Hz is adopted here to get generality. For higher sampling rates, $s \rightarrow s\,T_s$ transformation can be used. The effect of ELD on the proposed modulator and the technique adopted to compensate it by modifying the coefficients and an extra direct path is illustrated in Section 3.3.

3.2 Simulation Setup and Results

A Matlab Simulink model was developed to simulate the proposed TDM based CT I$\Sigma\Delta$ modulator for a two channel time division multiplexed low frequency signals of bandwidth 22 kHz. Two successive TDM frames of both the channels, considered for the analysis, are shown in Figure 3.3.

In the two channel time multiplexed scenario two successive frames are processed by the CT I$\Sigma\Delta$ modulator. The time multiplexed signals are sampled at an oversampling ratio of 256 and each TDM frame is composed of 16k samples of the TDM signals. The modulator runs at a speed of 11.3 MHz. The incremental processing is achieved

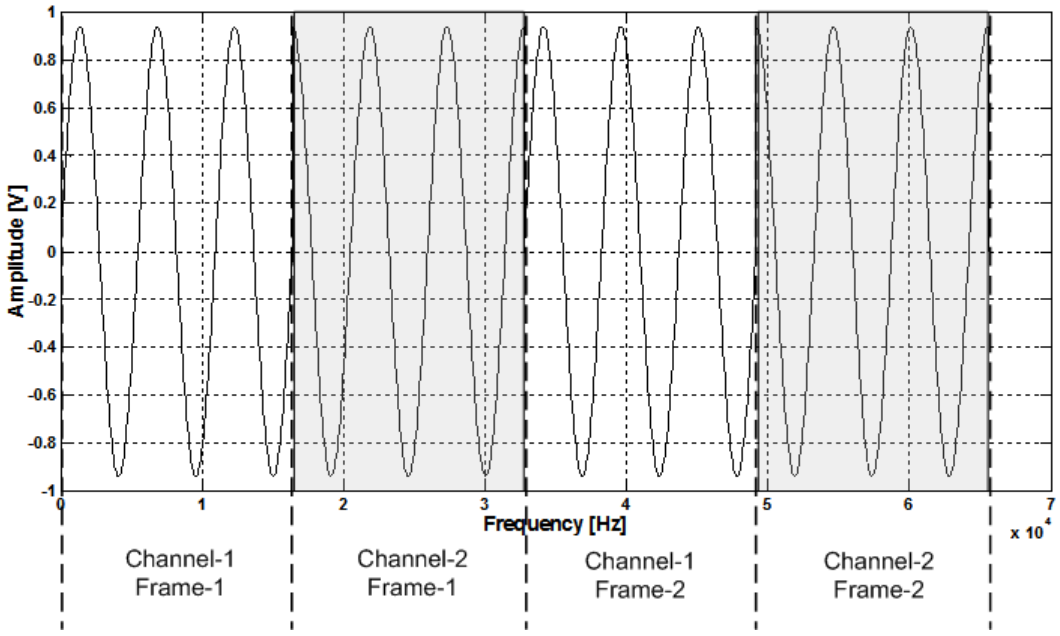


Figure 3.3: Time division multiplexed channels

by the time multiplexing of the channels and resetting of the modulator states (or integrators) during the instant of channel switching. The resetting of the modulator states during each channel switching helps to avoid inter-channel interference and cross talks, thus enables it to perform efficiently in a multi-channel environment. In contrast to traditional CT IΣΔ modulator, TDM frame-by-frame processing is done rather than sample-by-sample processing, thereby reducing the overall design complexity of the modulator and also maintains the one-to-one mapping between the input and output which is necessary for handling multiplexed signals. The proposed CT IΣΔ modulator with feed-forward architecture was tested for its monotonicity by plotting the amplitude of the input signal versus SNR curve as shown in Figure 3.4.

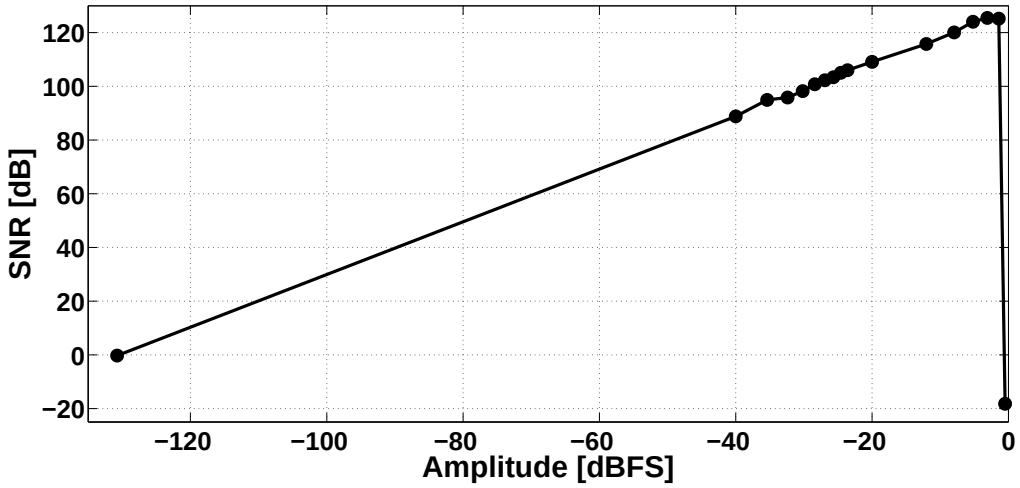


Figure 3.4: SNR vs amplitude (dB) - monotonicity characteristics

As illustrated in the figure, simulations were performed in Matlab Simulink and the modulator shows excellent monotonicity and achieves a dynamic range of 130 dB.

The most important aspect of the proposed CT IΣΔ modulator is its excellent SNR performance and monotonicity. Two TDM signals, each of 2 kHz, were fed as the input to the modulator and the oversampled digital data stream at the output of the modulator were taken to analyze the SNR performance. The obtained results for both the channels under ideal conditions are shown in Figure 3.5-3.10.

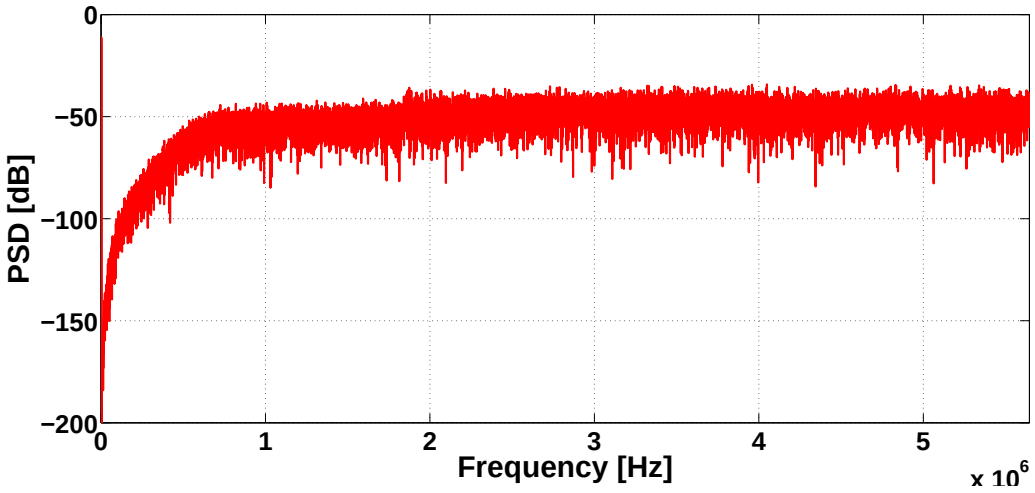


Figure 3.5: Output power spectral density of channel-1

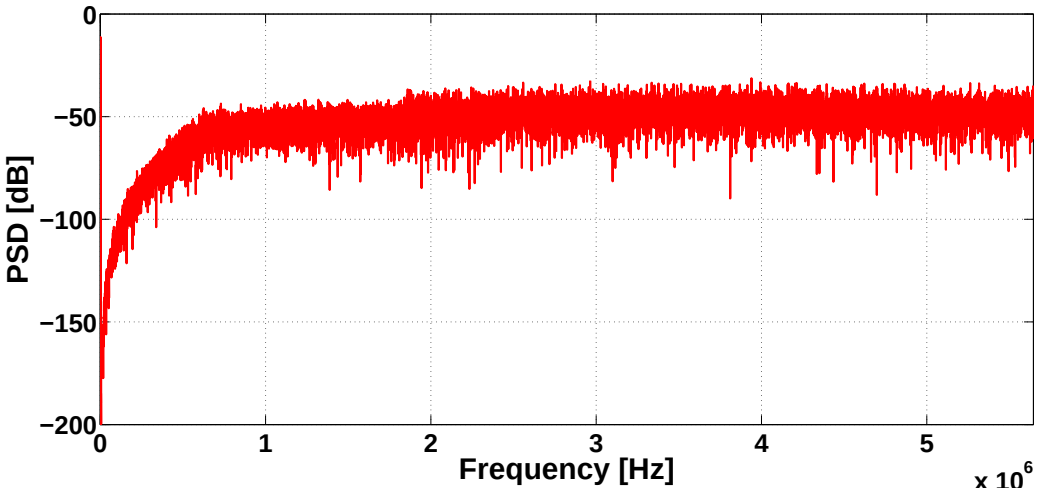


Figure 3.6: Output power spectral density of channel-2

An SNR of 117dB with effective number of bits (ENOB) of 19.15 bits were achieved for channel-1 and an SNR of 123dB with ENOB of 20.17 bits were achieved for channel-2. A 3^{rd} order noise shaping and SNR performance equivalent to that of a traditional CT ΣΔ modulator (without incremental operation) can be verified from the results.

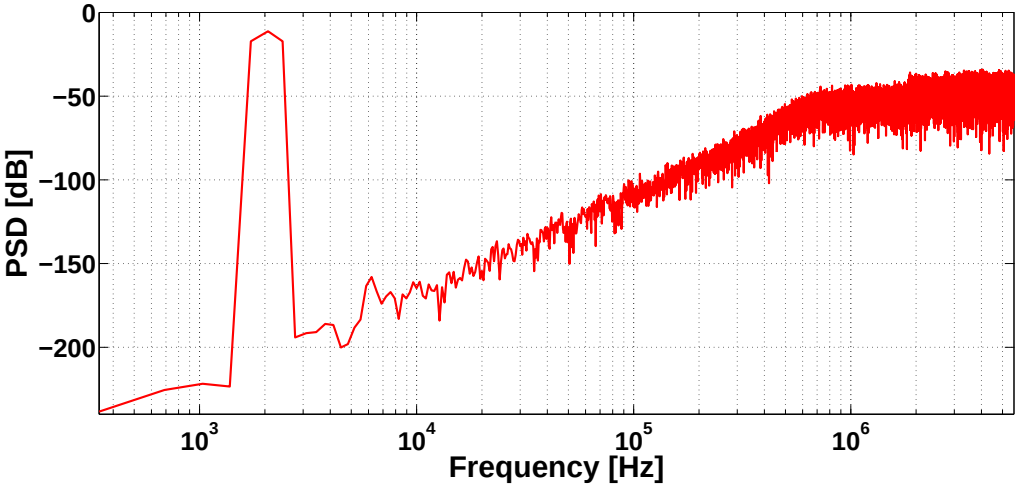


Figure 3.7: Output power spectral density of channel-1 (log scale)

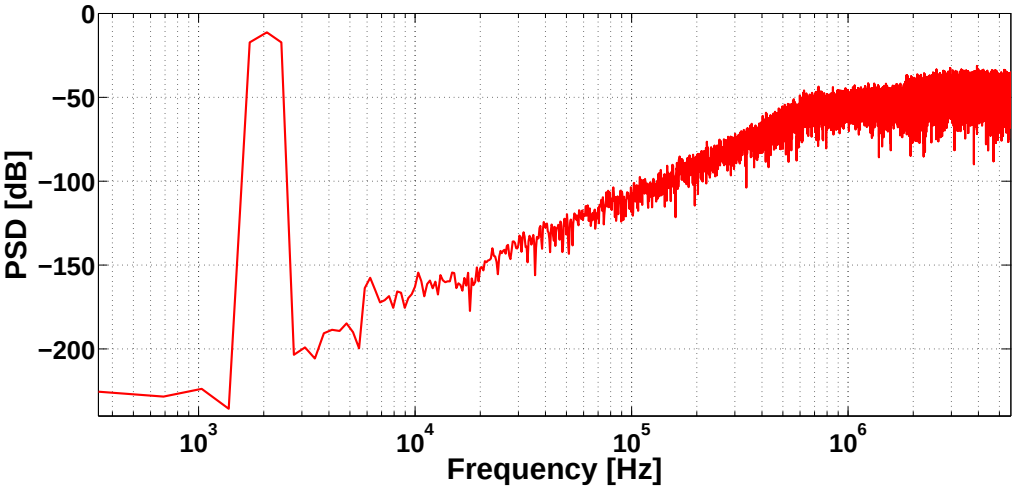


Figure 3.8: Output power spectral density of channel-2 (log scale)

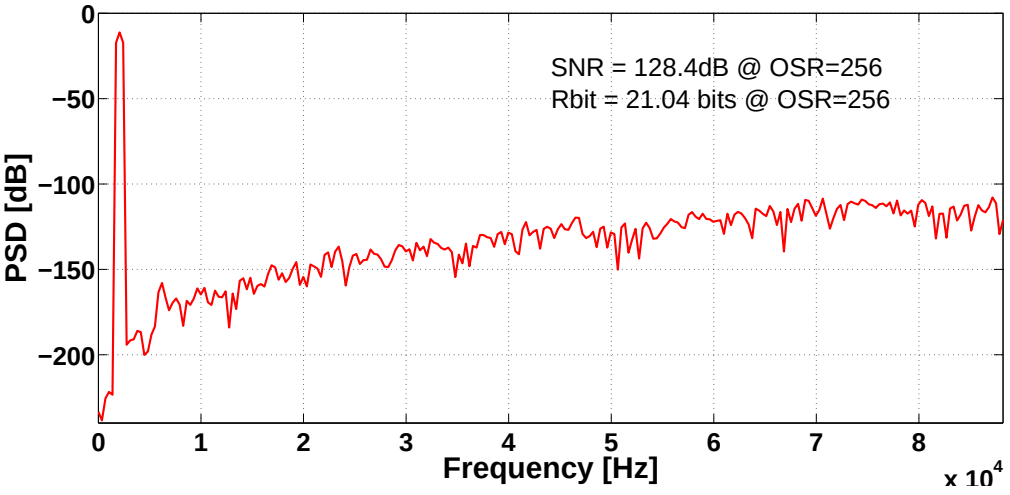


Figure 3.9: Output power spectral density of channel-1(detailed)

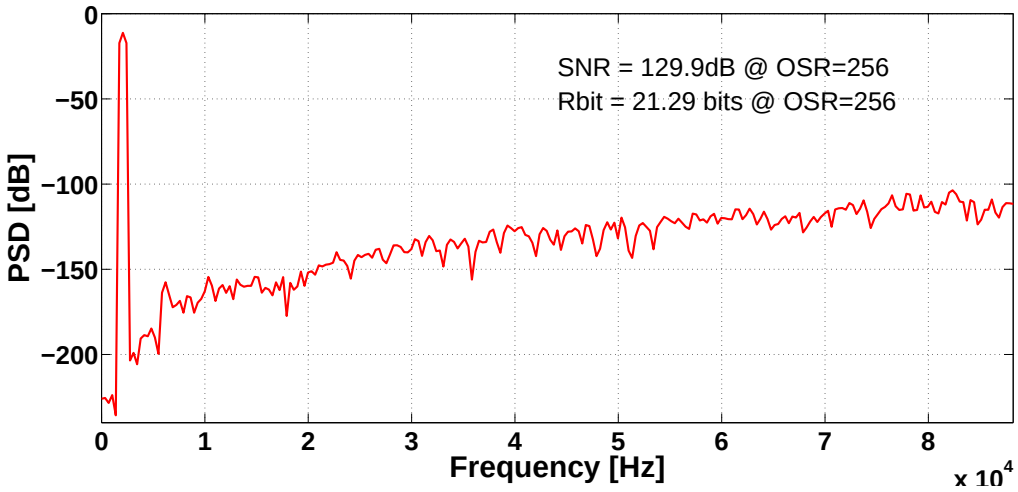


Figure 3.10: Output power spectral density of channel-2(detailed)

3.3 Excess Loop Delay (ELD) Analysis

Excess loop delay (τ_d) is defined as the delay time between the quantizer output signal and the D/A converter output signal, i.e. it refers to the non-zero delay between the quantizer clock edge and the edge of the DAC pulse. It is more severe in CT $\Sigma\Delta$ modulator because the timing errors are continuously accumulated at the integrator through the feedback DAC. The value of the delay time, τ_d, is dependent on the switching speed of the transistors, the quantizer clock frequency F_s, and the number of switched transistors in the feedback path (Cherry and Snelgrove, 1999*b*). This delay decreases the performance of CT-$\Sigma\Delta$ modulators due to the fact that the noise transfer function (NTF) of the CT modulator is altered with respect to the equivalent DT case. The phenomenon of ELD is depicted in Figure 3.11.

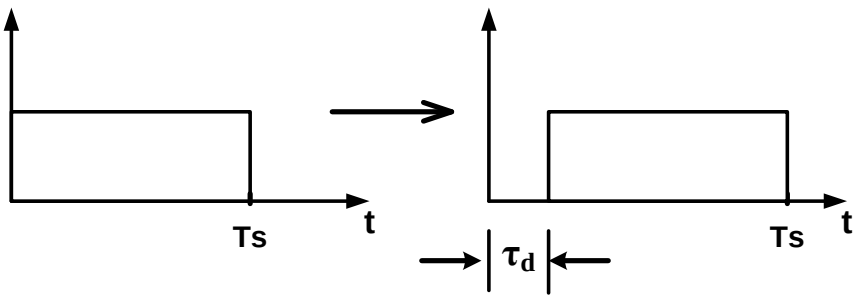


Figure 3.11: Illustration of ELD on non return to zero (NRZ) DAC pulse.

A simple intuitive ELD compensation technique to find how the loop filter coefficients need to be modified in a CT modulator is proposed in (Pavan, 2008). The same coefficient tuning approach is adopted here to re-compute the coefficients for compen-

sating ELD. A maximum ELD of 50% of T_s (i.e. τ_d = 0.5T_s), which drives the modulator to instability, is considered for compensation. As per the method proposed in (Pavan, 2008), for a 3^{rd} order CT modulator with feed-forward architecture, the feed-forward coefficients k_1', k_2' and k_3', and the new direct path coefficient k_0' can be obtained using the closed form equations as follows:

$$\begin{aligned} k_3' &= k_3 = c_1' c_2' c_3' g_3' = 0.0440 \\ k_2' &= k_2 + k_3 \tau_d = c_1' c_2' g_2' = 0.2662 \\ k_1' &= k_1 + k_2 \tau_d + k_3 \frac{\tau_d^2}{2} = c_1' g_1' = 0.7979 \\ k_0' &= k_1 \tau_d + k_2 \frac{\tau_d^2}{2} + k_3 \frac{\tau_d^3}{6} = g_0' = 0.3666 \end{aligned} \tag{3.4}$$

The modified structure with compensated coefficients is shown in Figure 3.12. The

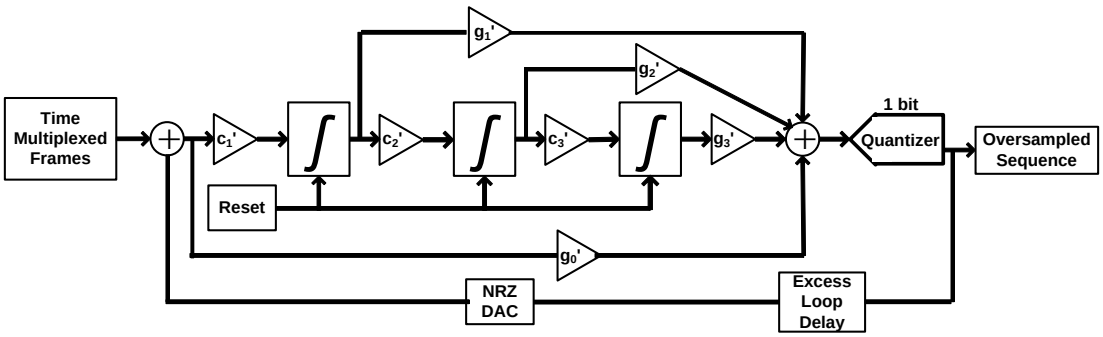


Figure 3.12: Modified structure with ELD compensation

proposed TDM based CT I$\Sigma\Delta$ modulator is again simulated for a two channel time division multiplexed low frequency signals of bandwidth 22kHz.

Behavioural-level simulations reveal that the presence of ELD drives the modulator to instability. The output spectrum of the ELD compensated modulator is shown in Figure 3.13.

The effective SNR of the modulator drops from 128 dB to 108 dB for the compensated case and thus restores the desired NTF. Compared to other alternatives, the ELD compensated 3^{rd} order CT I$\Sigma\Delta$ modulator does not require an extra DAC to perform compensation and thereby further reduces the power consumption.

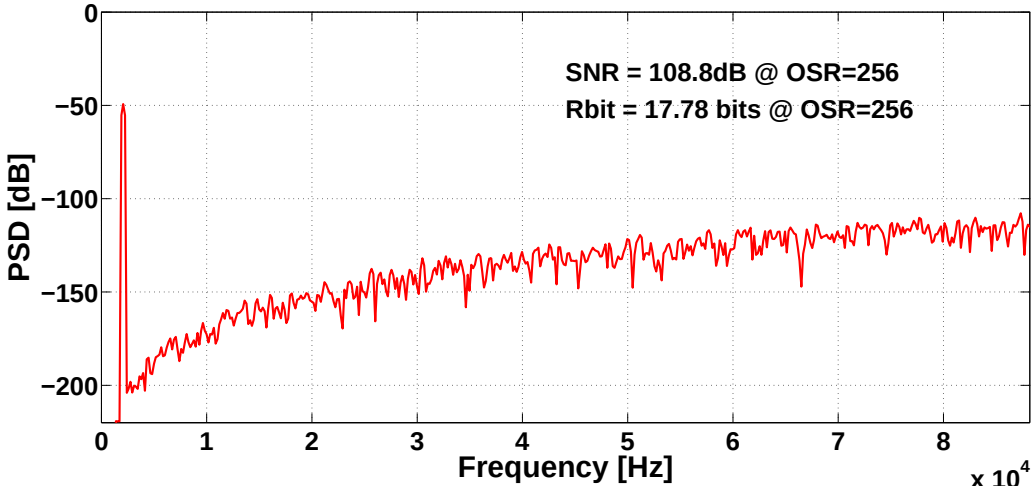


Figure 3.13: Output spectrum of the modified structure with ELD compensation

3.4 Circuit-Level Simulation using Simulink based Behavioural Simulator - SIMSIDES

SIMSIDES is an embedded behavioural simulator which is able to efficiently evaluate the performances of lowpass (LP) or bandpass (BP) $\Sigma\Delta$Ms implemented using either switched capacitor (SC), switched current (SI) or continuous-time (CT-g_mC) circuit techniques (José and del Río, 2013). A complete list of non-idealities of the building blocks for all circuit techniques (SC, CT and SI) have been considered in SIMSIDES (José and del Río, 2013). The simulator is suitable for simulation as well as synthesis of $\Sigma\Delta$ modulators.

One of the major advantages of CT $\Sigma\Delta$ modulators lies in that they can achieve higher sampling frequencies. However, the performance of CT $\Sigma\Delta$ modulators degrades drastically as a result of two important errors: clock jitter noise and delay time between the quantizer clock edge and DAC response. A circuit-level model, implemented based on SIMSIDES, was developed to simulate the proposed TDM based CT I$\Sigma\Delta$ modulator for a two channel time division multiplexed low frequency signals and high-frequency signals. A circuit-level conceptual diagram of the proposed modulator and its SIMSIDES based simulation model is shown in Figure 3.14 and Figure 3.15, respectively.

A single bit quantizer with 1V full scale range is assumed in the analysis. The s-domain transfer functions have been replaced by $g_m - C$ integrators and the feed-forward coefficients are implemented using transconductors. The modulator has been

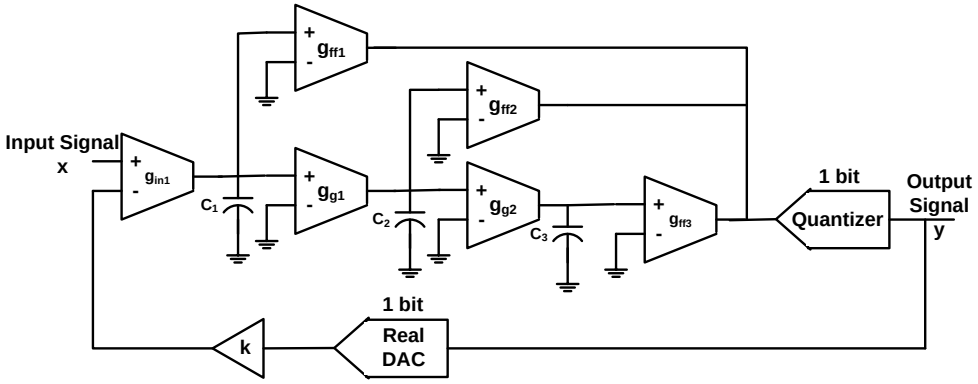


Figure 3.14: Conceptual circuit-level diagram of the 3^{rd} order CT IΣΔ modulator

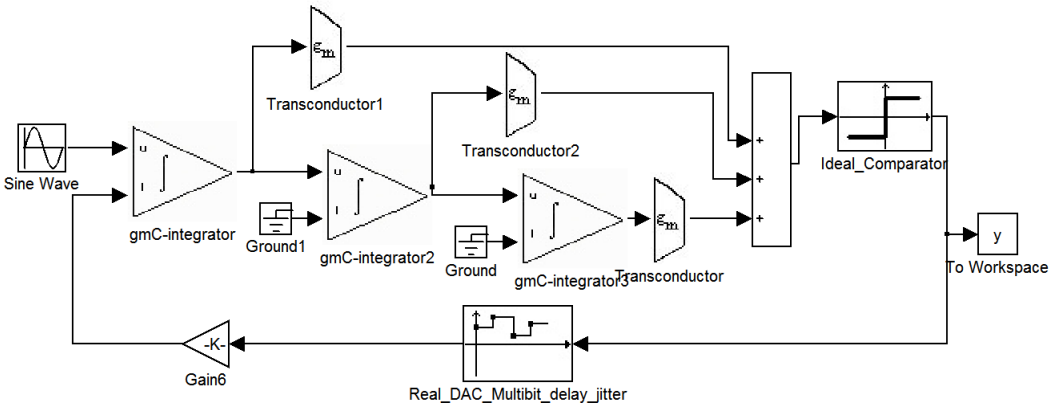


Figure 3.15: SIMSIDE implementation of the 3^{rd} order CT IΣΔ modulator

modelled based on the procedure discussed in section 3.1. The values of loop-filter transconductances gi, as well as the capacitances Ci, used in the modulator, are depicted in Table 3.1.

Table 3.1: Loop filter coefficients of the 3^{rd} Order CT IΣΔ modulator of Figure 3.14

Capacitors	C_1 = 1 pF, C_2 = 0.2 pF, C_3 = 0.2 pF
Feed-Forward Transconductances	g_{in1} = 500 µA V^{-1}, g_{g1} = 100 µA V^{-1}, g_{g2} = 100 µA V^{-1}, g_{ff1} = 670 µA V^{-1}, g_{ff2} = 244 µA V^{-1}, g_{ff3} = 44 µA V^{-1}, K = $-g_{in1}$

In order to evaluate the performance of the proposed modulator four different cases have been considered: ideal modulator; modulator with thermal noise; modulator with thermal noise and fixed loop delay; and modulator with thermal noise and signal-dependent loop delay. The behavioural model used for the transconductors in SIMSIDES takes into account several non-ideal circuit effects, including finite DC gain, output saturation voltage, and the input-referred 3^{rd} order intercept point $IIP3$. In the case of ideal modulator, thermal noise and all kinds of circuit non-idealities are ne-

glected. The ideal output power spectral density of the modulator, for a -6dBFS input tone at 156.25 kHz when clocked at sampling frequency at F_s = 500 MHz, is plotted in Figure 3.16.

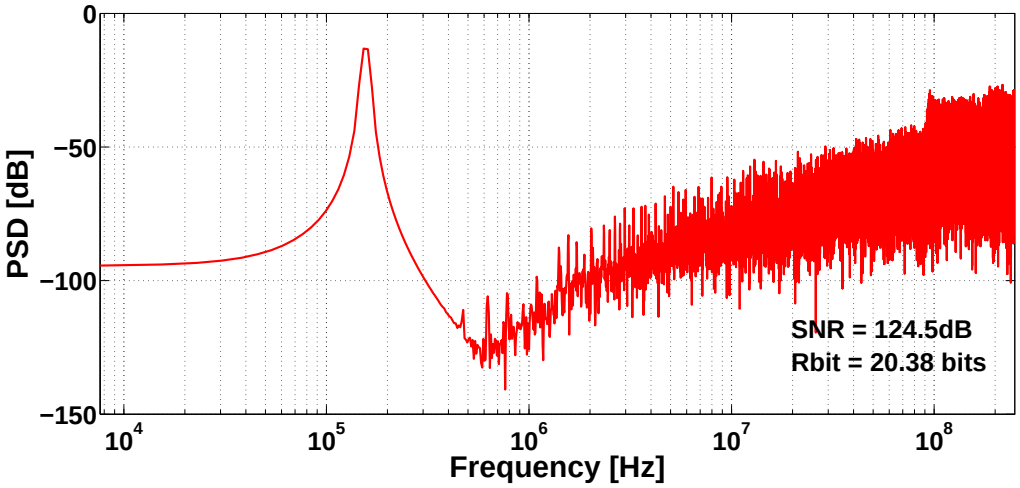


Figure 3.16: SIMSIDE based output power spectral density of the ideal model of the 3^{rd} order CT I$\Sigma\Delta$ modulator

The ideal SNR and the ideal effective resolution for the ideal case are 124.5 dB and 20.38 bits, respectively, which can be verified from Figure 3.16. However, in practice, the performance is degraded by the action of circuit non-idealities. The thermal (circuit) noise associated with the circuit components is incorporated into the model and the resulting output power spectral density of the modulator is depicted in Figure 3.17.

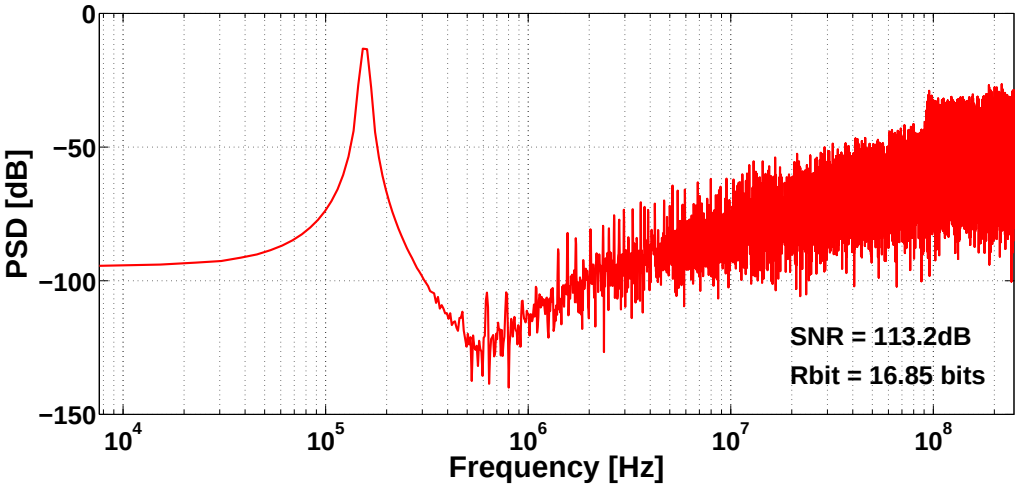


Figure 3.17: SIMSIDE based output power spectral density of the 3^{rd} order CT I$\Sigma\Delta$ modulator with thermal noise

The input-referred noise of the opamp and kT/C noise are considered for the analysis. The degradation in the SNR to 113dB can be easily verified. The fixed ELD is a constant delay between quantizer sampling edge and the corresponding edge of the

feedback DAC pulse. It arises from the nonzero switching time of transistors in the quantizer and DAC circuitry (Cherry and Snelgrove, 1999*b*). Quantizer metastability can also introduce a statistical variation in the charge that is fed back. Real quantizers contain a regenerative stage with a finite regeneration gain, quantizer inputs with a magnitude near zero will take longer time to resolve than inputs with a large magnitude (Cherry and Snelgrove, 1999*a*). This non-ideal effect is often referred to as signal-dependent loop delay (José and del Río, 2013). The degradation in the SNR due to the effect of fixed loop delay and signal-dependent loop delay are shown in Figure 3.18 and Figure 3.19, respectively.

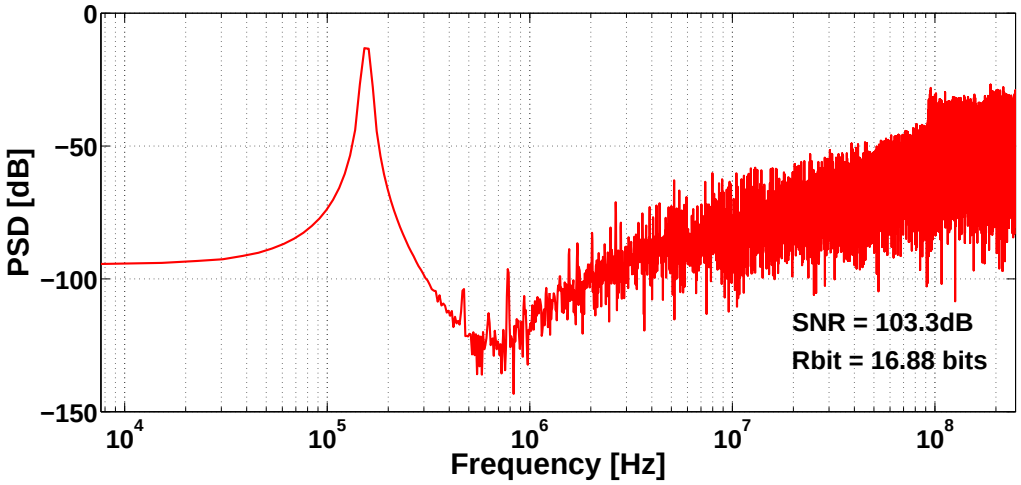


Figure 3.18: SIMSIDE based output power spectral density of the 3^{rd} order CT IΣΔ modulator with thermal noise and fixed loop delay

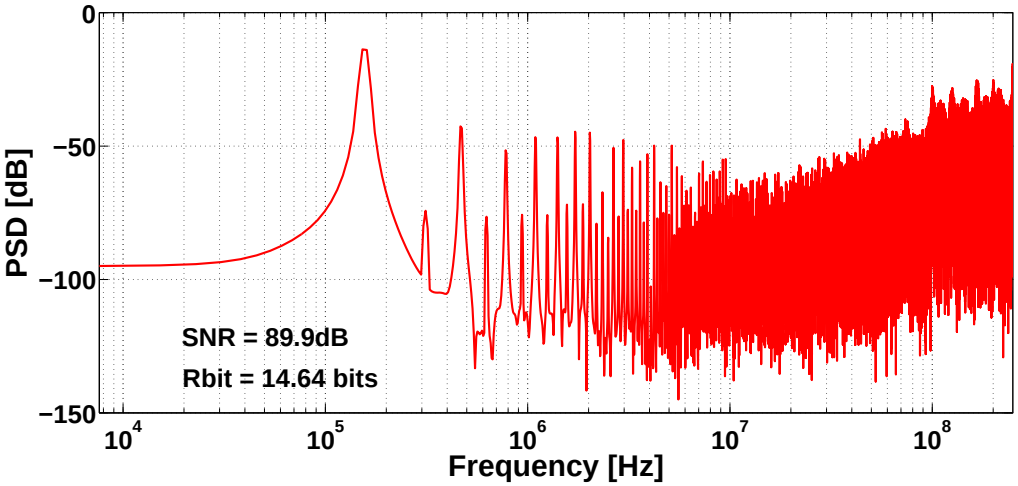


Figure 3.19: SIMSIDE based output power spectral density of the 3^{rd} order CT IΣΔ modulator with thermal noise and signal dependent loop delay

A maximum delay of $0.1T_s$ is considered for the analysis. The thermal noise is incorporated in the delay analysis so as to maintain the clinical significance and va-

lidity of the measurements. There is an 11.5 dB performance drop between the ideal performance of the ADC (124.5dB), that is only limited by quantization noise, and the measured 113 dB SNR in presence of thermal noise. The introduction of fixed noise and signal-dependent noise translates into a significant degradation of SNR to approximately 103dB and 90dB, respectively.

A performance comparison of recently published I$\Sigma\Delta$ modulators is given in Table 3.2. In order to obtain a fair comparison, only the modulator's performance parameters have been taken into account in all cases.

In this chapter, the SIMSIDES based circuit-level simulation results are presented and it is being compared with circuit-level results of other papers in Table 3.2. It is worth to mention that only I$\Sigma\Delta$ modulators have been included in this comparison, thereby, excluding both traditional $\Sigma\Delta$ modulators and possible expansions applied to I$\Sigma\Delta$ modulators. In order to maintain the realness of the modulator the model with thermal noise has been considered for the comparison. The proposed I$\Sigma\Delta$ modulators stands well ahead in its SNR performance, because of the TDM based frame-by-frame processing in contrast to sample-by-sample processing, and can be a feasible solution to low/high-frequency, low-power, low-cost multi-channel applications. Further improvements in the proposed scheme could be done by extending the modulator's resolution and varying the DAC coding scheme to obtain better jitter immunity performance.

3.5 Chapter Summary

A TDM based incremental CT feed-forward $\Sigma\Delta$ modulator for low frequency ADC applications has been simulated using Matlab Simulink. A 3^{rd} order CT modulator has been employed to take advantage of less number of cycles per conversion and relaxed bandwidth requirements of the active blocks, thus, making it suitable for low-power multi-channel applications. The CT architecture helps to relax the amplifiers' GBW requirement. The proposed TDM based CT I$\Sigma\Delta$ modulator running at 11.3 MHz achieves a peak signal-to-noise ratio of 128dB and dynamic range of 130dB over a bandwidth of 22 kHz and can be very effectively used in a TDMA based communication system. The high-resolution characteristics of the proposed modulator make it suitable for time-multiplexed audio applications. The complexity of decimation filter, a future

Table 3.2: Performance comparison with recently published IΣΔ ADCs

	This work	Garcia *et al.* (2013)	Garcia *et al.* (2013)	Quiquempoix *et al.* (2006)	Yu *et al.* (2010)	Liang and Johns (2010)	Liang and Johns (2010)	Mollazadeh *et al.* (2009)	Chi and Cauwen-berghs (2010)
		For 2kHz	For 4kHz			For 1670Hz	For 1.67Hz		
Year	2014	2013	2013	2006	2010	2010	2010	2009	2010
Implementation	CT	CT	CT	DT	DT	DT	DT	CT	CT
Bandwidth	1MHz	2kHz	4kHz	7.5Hz	21739Hz	1670Hz	1.67Hz	1kHz	250Hz
F_s (Hz)	500M	320k	320k	7.68k	10000k	-	-	2048k	512k
SNR(dB)	113	65.3	61.7	-	83.7	89.9	86.5	-	-

scope of this work, will be drastically reduced because a simple de-multiplexer, LPF, down-sampler can reconstruct the input signal associated with multiple channels independently from the output oversampled digital data stream of a single $\Sigma\Delta$ modulator. The model also offers high-accuracy, absence of idle tones, low-power dissipation, and ease of multiplexing. The effect of ELD and an intuitive method to compensate it, is illustrated in this chapter. An ELD of 50% of sampling frequency drives the modulator to instability. Behavioural simulations demonstrates that the compensated modulator with modified coefficients and an extra direct path restores the NTF and the modulator achieves an SNR of 108 dB. A circuit-level behavioural simulation of the proposed modulator for high frequency application has been done using the behavioural simulator SIMSIDES. The degradation in SNR performance due to thermal noise, fixed noise and signal dependent noise is verified from the results. The SIMSIDES based simulation results of the real model, i.e. with thermal noise SNR = 113 dB, is compared with the existing I$\Sigma\Delta$ modulator architectures to show the dominance of the proposed architecture. The most important aspect of this work is that an excellent SNR performance, low-cost and a high-bandwidth equivalent to that of a traditional CT $\Sigma\Delta$ modulator (without incremental operation) is achieved with proposed CT I$\Sigma\Delta$ modulator.

CHAPTER 4

ARCHITECTURAL EXPLORATION OF CROSS-COUPLED $\Sigma\Delta$ MODULATORS

A novel time interleaved (TI) extended noise shaping based cross-coupled multi-path sturdy multi-stage noise shaping (SMASH) architecture that compensates the excess sturdy MASH loop delay (ESLD) is presented in this chapter. The idea of SMASH logic in a multi-path TI scenario is modeled and demonstrated by using an extended noise shaping based TI cross-coupled 2-path 3^{rd} order structure as the first stage of the SMASH architecture. A dual extended (DE) noise shaping based TI symmetric cross-coupled $\Sigma\Delta$ modulator, which enhances the performance of conventional unextended and extended noise shaping based TI cross-coupled $\Sigma\Delta$ modulator architecture, is also proposed in this chapter. By dual extended noise shaping characteristics, the proposed architecture can achieve $2N^{th}$-order noise shaping out of an N-path cross-coupled first order $\Sigma\Delta$ modulator without sacrificing its high conversion rate and bandwidth. The higher order noise shaping is achieved by analytically obtaining the optimum coupling matrices.

The chapter is organized as follows. Section 4.1 reviews the extended noise shaping based cross-coupled $\Sigma\Delta$ modulator. Section 4.2 presents the proposed ESLD compensated architecture. Two architectures based on the proposed model are demonstrated in section 4.3. Section 4.4 and Section 4.5 illustrates the Matlab and Hspice simulation results. Section 4.6 describes proposed dual extended noise shaping based TI cross-coupled $\Sigma\Delta$ modulator. Section 4.7 is an analysis using the behavioural-level simulations of the proposed architecture and verifying the validity of the proposed modulator. Cross-Coupling Architecture for $\Sigma\Delta$ bandpass modulator is illustrated in Section 4.8. Finally, Section 4.9 portrays the inferences from this chapter.

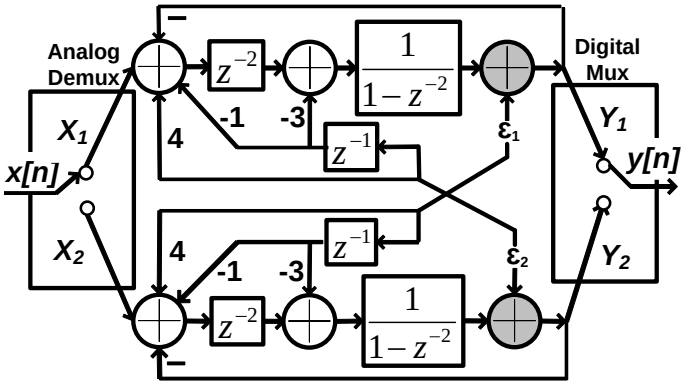


Figure 4.1: Block diagram of the two-path TI extended noise shaping based cross-coupled $\Sigma\Delta$ modulator

4.1 Two-Path TI Extended Cross-Coupled $\Sigma\Delta$ Modulator

A two-path TI extended (Hamidi and Miar-Naimi, 2014) modulator with cross-coupled paths, which enhances the performance of conventional unextended (Hamidi and Miar-Naimi, 2014), (Bilhan and Maloberti, 2008) noise shaping based TI architecture, is shown in Figure 4.1. Each path represents a first order $\Sigma\Delta$ modulator. An auxiliary input is created by separating delay block from the integrator, where the noise is coupled. The mux provides interpolation by 2. This is used to obtain the output at the sampling rate (F_s), thereby, reduces the noise power of each path by two (Han and Maghari, 2014). The noise transfer function (NTF) and signal transfer function (STF) for the 2-path TI extended cross-coupled $\Sigma\Delta$ modulator is obtained by applying transformation $z \rightarrow z^2$. This architecture has the advantage of achieving $(2N-1)^{th}$ order noise shaping, where N is the number of cross-coupled paths. So here the terms in the binomial expansion of a 3^{rd} order NTF evolve from the cross-coupled paths and loop feedback.

The practical implementation of extra coupling branches typically uses added switched-capacitors and does not require an extra opamp and hence capable of greatly relaxing the circuit specifications. The overall NTF and STF is obtained as follows:

$$Y_1 = z^{-2} * X_1 + (-z^{-3} + 4z^{-2} - 3z^{-1})\varepsilon_2 + (1 - z^{-2})\varepsilon_1$$

$$Y_2 = z^{-2} * X_2 + (-z^{-3} + 4z^{-2} - 3z^{-1})\varepsilon_1 + (1 - z^{-2})\varepsilon_2$$

$$STF(z) = z^{-2}, \quad NTF_z = (1 - z^{-1})^3$$

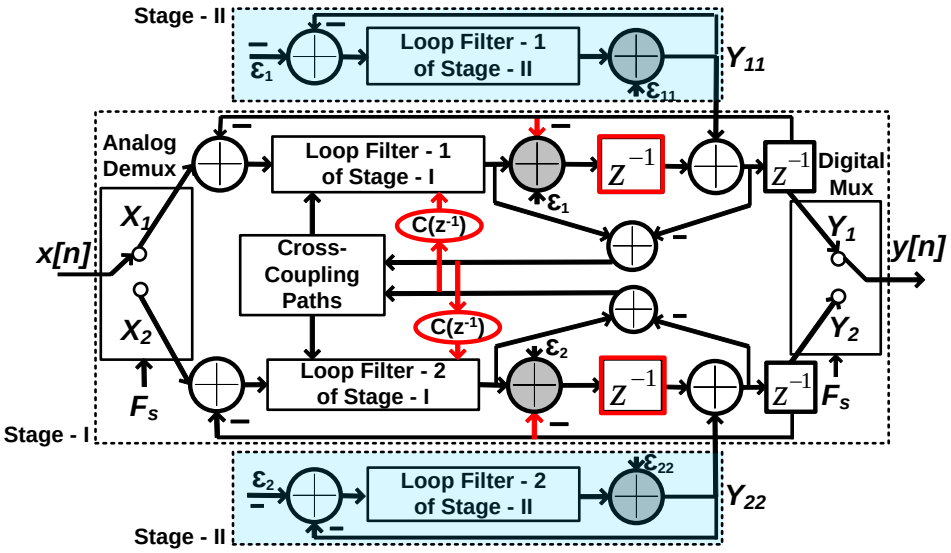


Figure 4.2: Block diagram of the the proposed modulator

The overall output is given by,

$$Y(z) = z^{-2}X(z) + (1 - z^{-1})^3\varepsilon(z) \tag{4.1}$$

where $X(z)$ and $Y(z)$ denote the z-transform of $x[n]$ and $y[n]$, respectively, and $\varepsilon(z)$ represents the z-transform of the overall quantization noise sequence.

4.2 Proposed SMASH TI Cross-Coupled $\Sigma\Delta$ Modulator with ESLD Compensation

A general block diagram of the proposed structure is shown in Figure 4.2. The 2-path extended noise shaping based TI cross-coupled $\Sigma\Delta$ modulator, discussed in the previous section, is used as stage-I. Theoretically, the quantization noise of the first stage (ε_1 and ε_2) can be cancelled completely. But, to process ε_1 and ε_2 using the stage-II loop filter and quantizer and generate its output, Y_{11} and Y_{22}, without any delay is impossible (Han and Maghari, 2014). A unit delay is intentionally introduced (Cherry and Snelgrove, 1999*b*) between the stage-I quantizer of both the paths and the point of coupling of the stage II output (Y_{11} and Y_{22}). This finite delay in stage-I alters the STF and NTF of the modulator and hence it is necessary to compensate it. The compensation is performed by a fast path around the stage-I quantizer and an additional cross-coupled

path through a polynomial,

$$C(z^{-1}) = -z^{-3} + 5z^{-2} - 7z^{-1} + 3 \tag{4.2}$$

The overall output is given by,

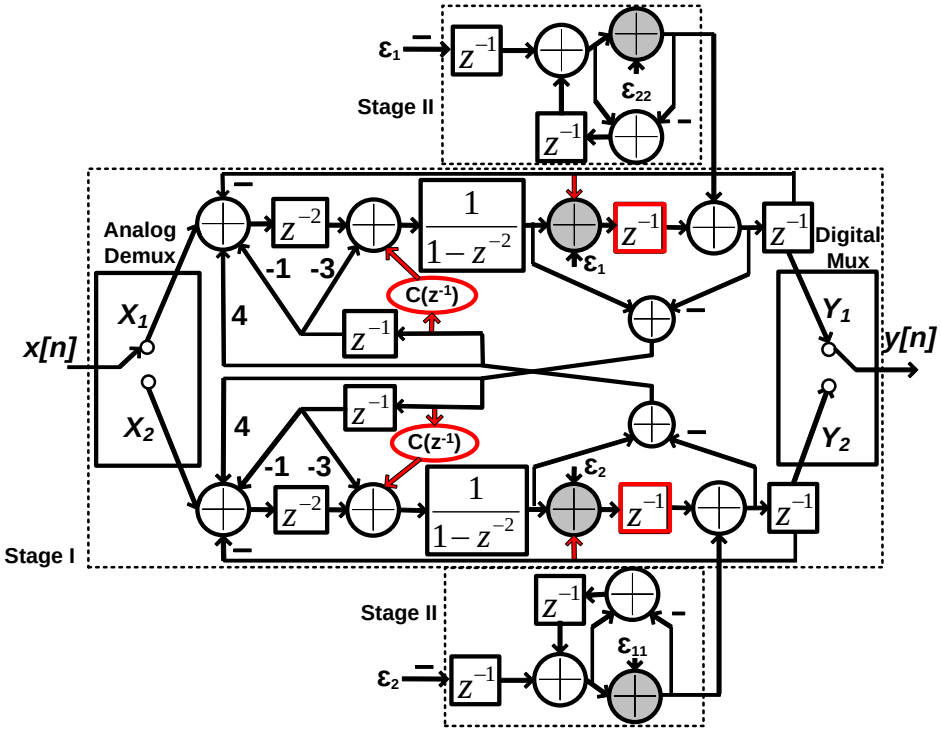
$$Y(z) = z^{-2}STF_1X(z) + z^{-1}NTF_1 \times NTF_2 \times \varepsilon_{stageII}(z) \tag{4.3}$$

where $\varepsilon_{stageII}$ is the overall quantization error of stage-II. Thus the SMASH logic makes the modulator solely analog and thereby alleviates the analog-digital filter mismatch issues and resulting quantization-error leakage.

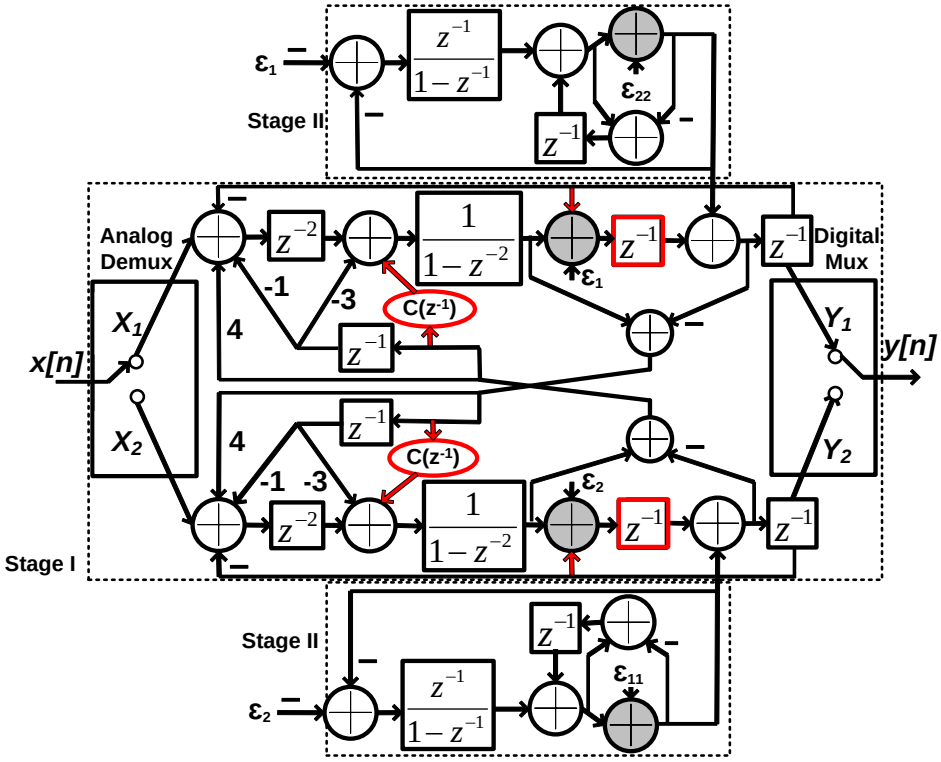
The ESLD is perfectly compensated by the proposed feedback mechanism. The stage-I quantization error of the ESLD compensated model is perfectly cancelled and the output of the modulator benefit from the 3 bit quantizer of stage-II. Since stage-I use only a 1-bit quantizer; the dynamic element matching is greatly relaxed. A $(3+1)^{th}$ order modulator and a $(3+2)^{th}$ order modulator based on the proposed model is demonstrated in the following sections.

4.3 Proposed SMASH $(3+1)^{th}$ and $(3+2)^{th}$ Order TI Cross-Coupled $\Sigma\Delta$ Modulator with ESLD Compensation

Figure 4.3(a) and Figure 4.3(b) shows the proposed SMASH $(3+1)^{th}$ order and $(3+2)^{th}$ order TI cross-coupled $\Sigma\Delta$ modulator with ESLD compensation. The 2-path 3^{rd}-order extended noise shaping based TI cross-coupled $\Sigma\Delta$ modulator with a 1-bit quantizer is used as stage-I in both the cases. A shaped quantizer (He *et al.*, 2014) is used as stage-II of the modulator for $(3+1)^{th}$ order SMASH architecture (shown in Figure 4.3(a)) and a first order $\Sigma\Delta$ with a shaped quantizer (He *et al.*, 2014) is used as stage-II of the modulator for $(3+2)^{th}$ order SMASH architecture (shown in Figure 4.3(b)). A 3-bit quantizer is used for stage-II. A unit delay is intentionally introduced between the stage-I quantizer of both the paths and the point of insertion of the stage-II output (Y_{11} and Y_{22}). The method of compensation is discussed in the following subsections.



(a)



(b)

Figure 4.3: Block diagram of (a) SMASH $(3+1)^{th}$ order and (b) SMASH $(3+2)^{th}$ order TI cross-coupled $\Sigma\Delta$ modulator with ESLD compensation

4.3.1 SMASH $(3+1)^{th}$ order

The output of stage-II for SMASH $(3+1)^{th}$ order modulator is given by,

$$Y_{11} = -\varepsilon_1 \times z^{-1} + \varepsilon_{11}(1 - z^{-1})$$
$$Y_{22} = -\varepsilon_2 \times z^{-1} + \varepsilon_{22}(1 - z^{-1})$$

The output of stage-I is given by,

$$\begin{aligned} Y_1 &= z^{-4}X_1 + \varepsilon_{11}(1 - z^{-1})[4z^{-4} - z^{-5} - 4z^{-3} - C(z^{-1})z^{-2}] \\ &+(Y_{11}z^{-1} + \varepsilon_1 z^{-2})(1 - z^{-2}) = z^{-4}X_1 + z^{-1}(1 - z^{-1})^4\varepsilon_{11} \\ Y_2 &= z^{-4}X_2 + \varepsilon_{22}(1 - z^{-1})[4z^{-4} - z^{-5} - 4z^{-3} - C(z^{-1})z^{-2}] \\ &+(Y_{22}z^{-1} + \varepsilon_2 z^{-2})(1 - z^{-2}) = z^{-4}X_2 + z^{-1}(1 - z^{-1})^4\varepsilon_{22} \end{aligned}$$

The overall output is given by,

$$Y(z) = z^{-4}X(z) + z^{-1}(1 - z^{-1})^4 \times \varepsilon_{StageII}(z) \tag{4.4}$$

4.3.2 SMASH $(3+2)^{th}$ order

The output of stage-II for SMASH $(3+2)^{th}$ order modulator is given by,

$$Y_{11} = -\varepsilon_1 \times z^{-1} + \varepsilon_{11}(1 - z^{-1})^2$$
$$Y_{22} = -\varepsilon_2 \times z^{-1} + \varepsilon_{22}(1 - z^{-1})^2$$

The output of stage I is given by,

$$\begin{aligned} Y_1 &= z^{-4}X_1 + \varepsilon_{11}(1 - z^{-1})[4z^{-4} - z^{-5} - 4z^{-3} - C(z^{-1})z^{-2}] \\ &+(Y_{11}z^{-1} + \varepsilon_1 z^{-2})(1 - z^{-2}) = z^{-4}X_1 + z^{-1}(1 - z^{-1})^5\varepsilon_{11} \\ Y_2 &= z^{-4}X_2 + \varepsilon_{22}(1 - z^{-1})[4z^{-4} - z^{-5} - 4z^{-3} - C(z^{-1})z^{-2}] \\ &+(Y_{22}z^{-1} + \varepsilon_2 z^{-2})(1 - z^{-2}) = z^{-4}X_2 + z^{-1}(1 - z^{-1})^5\varepsilon_{22} \end{aligned}$$

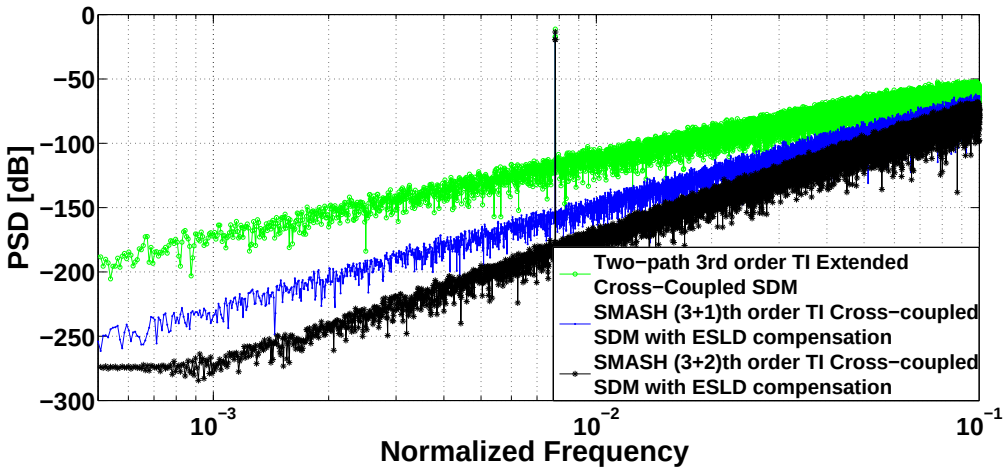


Figure 4.4: Comparison of output power spectral density of the two proposed architectures with extended cross-coupled architecture.(SDM represents sigma delta modulator)

The overall output is given by,

$$Y(z) = z^{-4}X(z) + z^{-1}(1 - z^{-1})^5 \times \varepsilon_{StageII}(z) \tag{4.5}$$

The quantization error of the first stage is completely cancelled. The ESLD is perfectly compensated by the proposed feedback mechanisms.

4.4 Behavioural Simulation of the Proposed SMASH TI Cross-Coupled $\Sigma\Delta$ Modulator

The proposed ESLD compensated $(3+1)^{th}$ order modulator and $(3+2)^{th}$ order modulator along with the simple 2-path 3^{rd} order extended noise shaping based TI cross-coupled $\Sigma\Delta$ modulator was simulated under ideal conditions and infinite opamp gain using Matlab and Simulink. An OSR of 15 is considered in all the three cases. A comparison of the power spectral densities of all the cases with -6 dBFS input level is shown in Figure 4.4. Here, Sigma Delta Modulator is represented as SDM. The results obtained are summarized in Table 4.1.

The SNR, effective order of noise shaping and number of integrators are shown in Table 4.1. As expected, a slope of 60 dB/dec, 80 dB/dec and 100 dB/dec are obtained for the simple extended architecture, proposed ESLD compensated $(3+1)^{th}$ order architecture and proposed ESLD compensated $(3+2)^{th}$ order architecture, respectively. The

Table 4.1: Performance summary of architectures

Parameters	3^{rd} order TI cross-coupled $\Sigma\Delta$ modulator	Proposed $(3+1)^{th}$ order $\Sigma\Delta$ modulator	Proposed $(3+2)^{th}$ order $\Sigma\Delta$ modulator
Order	3	4	5
No. of integrators	2	2	4
OSR	15	15	15
SNR (dB)	75	93	115
Slope (dB/dec)	60	80	100

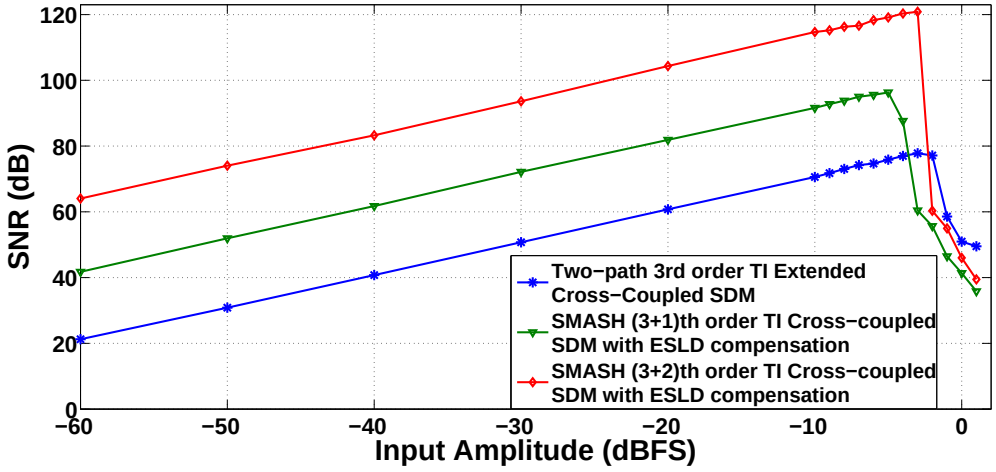
Table 4.2: Comparison with DNC-SMASH $\Sigma\Delta$ modulator

Parameters	Proposed $(3+1)^{th}$ order $\Sigma\Delta$ modulator	$(2+2)^{th}$ order DNC-SMASH (Han and Maghari, 2014)
Order	4	5
No. of integrators	2	4
OSR	15	15
Quantizer	two 9-level and two 1-bit	one 16-level and one 4-level
SNR (dB)	80	100

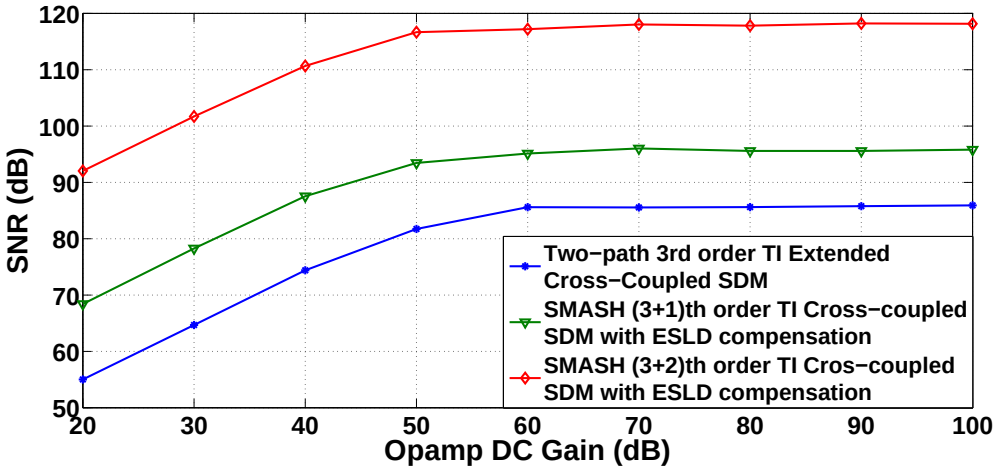
presence of ESLD leads to quantization noise leakage between individual stages and hence limits the performance of the simple SMASH architecture. The ESLD compensation mechanisms introduced perfectly cancels the stage-I quantization error, enhances the order of noise shaping and benefits from 3-bit stage-II quantizer.

A comparison of the proposed ESLD compensated $(3+1)^{th}$ order cross-coupled $\Sigma\Delta$ modulator with the $(2+2)^{th}$ order delay based noise cancelling sturdy MASH (DNC-SMASH) modulator (Han and Maghari, 2014) is shown in Table 4.2. The proposed ESLD compensated $(3+1)^{th}$ order modulator requires just two integrators to meet the performance of $(2+2)^{th}$ order DNC-SMASH, which requires four integrators. The proposed structure outperforms DNC-SMASH, in terms of hardware, which can be verified from the results reported in Table 4.2.

A comparison of the variation of SNR with input signal amplitude of the extended



(a)



(b)

Figure 4.5: Comparison of (a) variation of SNR with input signal amplitude and (b) variation of SNR with opamp DC gain of the proposed architectures with extended cross-coupled architecture. (SDM represents sigma delta modulator)

cross-coupled architecture with the proposed architectures is shown in Figure 4.5(a). The monotonicity and the input referred stability of the proposed schemes can be verified from the figure. Figure 4.5(b) shows the opamp gain requirement for the three structures under consideration. For all the three structures an opamp gain of 60dB is necessary to achieve highest SNR.

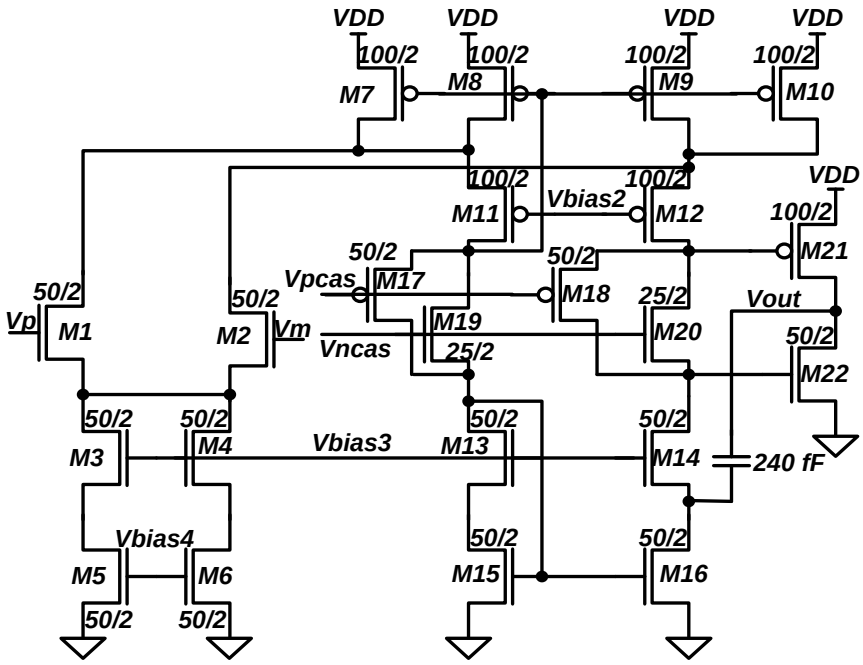


Figure 4.6: The folded cascode OTA of high output resistance

4.5 Circuit-Level Simulation of the Proposed SMASH TI Cross-Coupled $\Sigma\Delta$ Modulator

The proposed modulator is implemented in a 45 nm CMOS process, with a supply of 1V and input signal range of 0.7 V. The design of the integrator is very critical as the modulator output is highly sensitive to integrator non-idealities. The ideal OTA is characterised by an infinite output resistance. Hence, a folded-cascade opamp configuration with a class AB output buffer, shown in Figure 4.6, is used as the OTA (Baker, 2008). Increase in the load capacitance, decreases the gain-bandwidth product, and increases the stability of the OTA. So in most of the on-chip applications OTA is the most suitable opamp. The open loop gain and phase response of the OTA are shown in Figure 4.7.

Table 4.3 gives the performance summary of the OTA. Simulation results show that OTA has a gain of 75 dB, unity gain-bandwidth of 144 MHz and a phase margin of 60 degree.

The single-ended switched capacitor (SC) circuit-level implementation for one of the two paths of the proposed ESLD compensated $(3+1)^{th}$ order extended noise shaping based TI cross-coupled $\Sigma\Delta$ modulator is shown in Figure 4.8. Clock signals of 4 different phases, Φ_1, Φ_2, Φ_3 and Φ_4, were used to simulate the SC model.

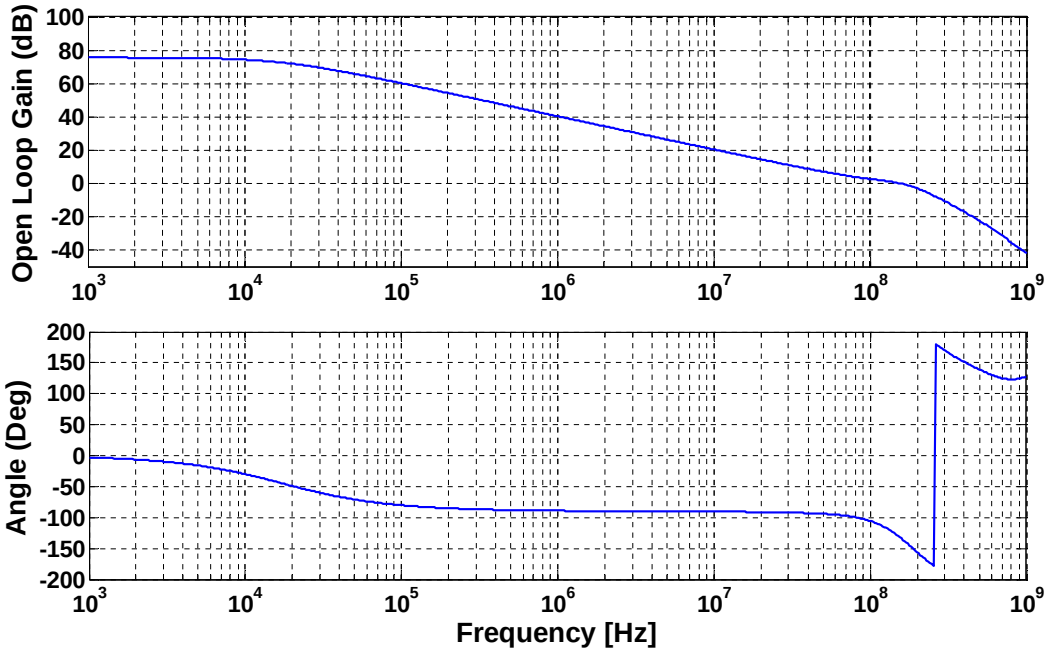


Figure 4.7: The open loop gain and phase response of the folded cascode OTA of Figure 4.6

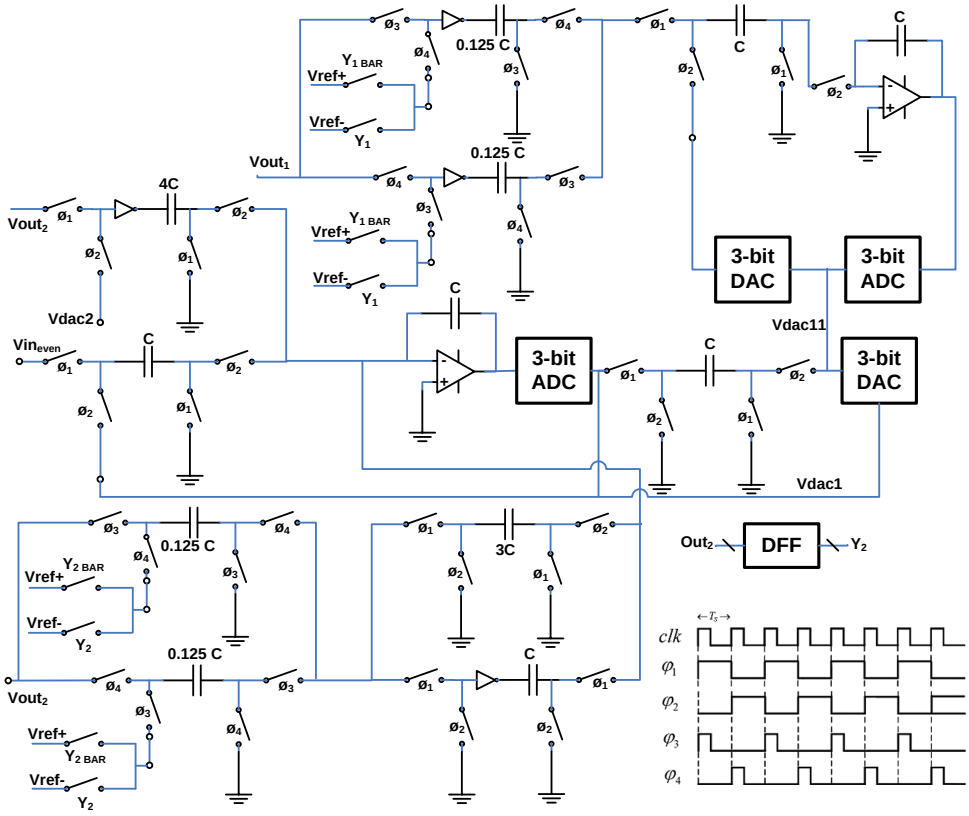


Figure 4.8: Switched-capacitor circuit-level implementation of one of the path of the proposed SMASH TI cross-coupled $\Sigma\Delta$ modulator.

They are depicted in the same figure. Each of the paths operates at half the clock rate and this decimation is achieved by making use of the clock phases Φ_1 and Φ_2. The cross coupled coefficients and the individual stage gains are realized by the ratios of

Table 4.3: Performance summary of folded-cascode OTA with output buffer

Opamp Specifications	Value
DC Gain	75dB
GBW (CL=1pF)	144 MHz
SR (CL=1pF)	200 V/μs
Phase Margin	60
Output Swing	1V
Maximum Current	135.6 μA
Power Dissipation	135.6 μW
Technology	45 nm

capacitors around the amplifier (San *et al.*, 2009). The outputs of the stage-I integrators are denoted by $Vout_1$ and $Vout_2$, and the stage-I DAC outputs as $Vdac_1$ and $Vdac_2$. The outputs of the stage-II integrators are denoted by $Vout_{11}$ and $Vout_{22}$, and the stage-II DAC outputs as $Vdac_{11}$ and $Vdac_{22}$. The error signals are generated by analog subtraction of $Vout$ and $Vdac$ using the SC logic. The simulation of the complete TI SMASH cross-coupled $\Sigma\Delta$ modulator has been carried out in Hspice circuit simulator. The switches are modelled using transmission gates. The folded-cascode OTA opamp of Figure 4.6 with an open loop gain of 75 dB and slew rate 200 V/μs were used to model the integrator. The clock frequency used is 100 MHz and the TI operation enables each path to operate at 50 MHz. Oversampling ratio is set to 16. The input signal is a sinusoid of frequency 500 kHz and bandwidth 3.125 MHz. The power consumption of the modulator is 385 μW from a 1V power supply.

Figure 4.9 shows the power spectral density from the Hspice based circuit-level simulation of the proposed modulator and its comparison with MATLAB results. A fourth order noise shaping and an SNR of 70 dB are obtained from Hspice simulations.

4.6 Proposed Dual Extended Noise Shaping Based TI Cross-Coupled $\Sigma\Delta$ Modulator

An N-path dual extended (DE) modulator with cross-coupled paths is investigated and its coupling matrices are derived in this section. Figure 4.10 depicts the generic sym-

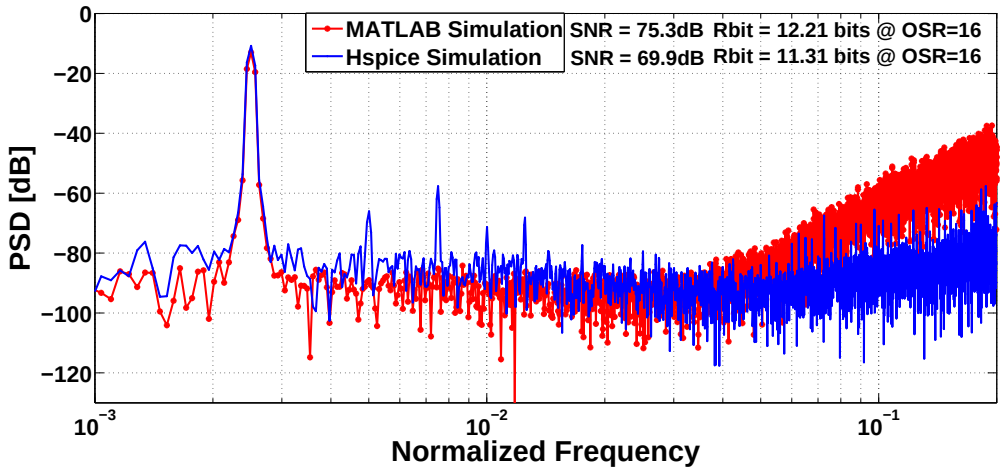


Figure 4.9: Output PSD of the switched-capacitor circuit and system-level simulations of the proposed SMASH TI cross-coupled $\Sigma\Delta$ modulator.

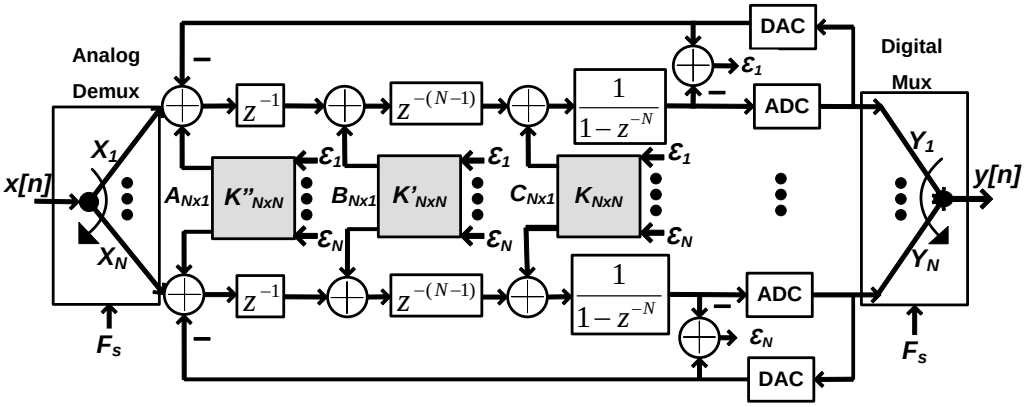


Figure 4.10: Generalized architecture of the proposed method

metric N-path architecture of the proposed modulator.

Each path represents a first order $\Sigma\Delta$ modulator. Two auxiliary inputs are created by separating delay block from the integral operator and splitting the delay block itself, where the noise coupled matrices are injected. The mux provides interpolation by N. This is used to obtain the output at F_s, thereby, reduces the noise power of each path by N. Therefore, the total noise power of the N uncorrelated noise terms equals the noise power of a single path (Hamidi and Miar-Naimi, 2014). The quantization error (ε) is computed by subtracting the input of ADC from the output of the DAC for each path. Quantization errors of paths are injected separately into three N-input, N-output bank of coupling matrices K, K' and K'', respectively. Figure 4.10 shows the way in which outputs of these banks are coupled.

The NTF for the N-path modulator is obtained by applying transformation $z \rightarrow z^N$.

As illustrated in Figure 4.10, the inherent feedback of the $\Sigma\Delta$ loop generates the term $(1-z^{-N})$ for each path. The additional terms in the binomial expansion of a $2N^{th}$ order NTF should evolve from the other cross-coupled paths so as to get the complete NTF of an equivalent non-cross-coupled modulator. The paths are using N non-overlapping phases of the main clock frequency (F_s) and the output vectors $Y_i(z)$ are multiplexed (i.e., added) to produce the overall output sequence as

$$\begin{aligned} Y(z) =& \sum_{i=1}^{N} Y_i(z) = STF(z) \sum_{i=1}^{N} X_i(z) + NTF(z) \sum_{i=1}^{N} E_i(z) \\ =& STF(z)X(z) + NTF(z)E(z). \end{aligned} \tag{4.6}$$

where $X(z)$ and $Y(z)$ denote the z-transform of $x[n]$ and $y[n]$, respectively, and $E(z)$ represents the z-transform of the overall quantization noise sequence. Like the extended one, the transformation used is $z \rightarrow z^N$ for both even and odd number of paths which leads to negative feedback sign and operator $1/(1 - z^N)$ as integrator block. The N-resultant quantization noise sequences,$[E]_{N\times1}$, are filtered by the coupling matrices,$[K'']_{N\times N}$,$[K']_{N\times N}$ and $[K]_{N\times N}$ resulting in the matrices $[A]_{N\times1}$, $[B]_{N\times1}$ and $[C]_{N\times1}$, respectively, which are injected as shown in Figure 4.10. The output column matrix $[Y]$ can be expressed as follows:

$$[Y]_{N\times1} = [STF]_{N\times N}[X]_{N\times1} + [NTF]_{N\times N}[E]_{N\times1} \tag{4.7}$$

$$\begin{aligned} [Y]_{N\times1} =& z^{-N}[X]_{N\times1} + z^{-N}[A]_{N\times1} + z^{-(N-1)}[B]_{N\times1} + \\ & [C]_{N\times1} + (1 - z^{-N})[E_I]_{N\times1} \end{aligned} \tag{4.8}$$

where,

$$[A]_{N\times1} = [K'']_{N\times N}[E]_{N\times1} \tag{4.9}$$

$$[B]_{N\times1} = [K']_{N\times N}[E]_{N\times1} \tag{4.10}$$

$$[C]_{N\times1} = [K]_{N\times N}[E]_{N\times1} \tag{4.11}$$

$$[E_I]_{N\times1} = [I]_{N\times N}[E]_{N\times1} \tag{4.12}$$

By substituting Equations (4.9), (4.10), (4.11) and (4.12) into (4.8) the output matrix $[Y]$ can be expressed as

$$\begin{aligned}[Y]_{N\times 1} =& z^{-N}[X]_{N\times 1} + \{z^{-N}[K'']_{N\times N} + z^{-(N-1)}[K']_{N\times N} + \\ & [K]_{N\times N} + (1 - z^{-N})\}[E_I]_{N\times 1}\end{aligned} \tag{4.13}$$

$$[NTF]_{N\times 1} = \{z^{-N}[K'']_{N\times N} + z^{-(N-1)}[K']_{N\times N} + [K]_{N\times N} + (1 - z^{-N})\}[E_I]_{N\times 1} \tag{4.14}$$

On comparing Equation (4.13) with Equation (4.6), $[NTF]_{N\times 1}$ can be expressed as

$$\begin{aligned}[NTF]_{N\times 1} = & z^{-N} \times \begin{bmatrix} k''_{11} & \dots & k''_{1N} \\ \vdots & \ddots & \vdots \\ k''_{i1} & \dots & k''_{iN} \\ \vdots & \ddots & \vdots \\ k''_{N1} & \dots & k''_{NN} \end{bmatrix} \times \begin{bmatrix} \varepsilon_1 \\ \vdots \\ \varepsilon_i \\ \vdots \\ \varepsilon_N \end{bmatrix} \\ & + z^{-(N-1)} \times \begin{bmatrix} k'_{11} & \dots & k'_{1N} \\ \vdots & \ddots & \vdots \\ k'_{i1} & \dots & k'_{iN} \\ \vdots & \ddots & \vdots \\ k'_{N1} & \dots & k'_{NN} \end{bmatrix} \times \begin{bmatrix} \varepsilon_1 \\ \vdots \\ \varepsilon_i \\ \vdots \\ \varepsilon_N \end{bmatrix} + \begin{bmatrix} k_{11} & \dots & k_{1N} \\ \vdots & \ddots & \vdots \\ k_{i1} & \dots & k_{iN} \\ \vdots & \ddots & \vdots \\ k_{N1} & \dots & k_{NN} \end{bmatrix} \times \begin{bmatrix} \varepsilon_1 \\ \vdots \\ \varepsilon_i \\ \vdots \\ \varepsilon_N \end{bmatrix} \\ & + \begin{bmatrix} (1 - z^{-N}) & 0 & \dots & 0 \\ 0 & (1 - z^{-N}) & \vdots & 0 \\ \vdots & \dots & \ddots & \vdots \\ 0 & \dots & \vdots & (1 - z^{-N}) \end{bmatrix} \times \begin{bmatrix} \varepsilon_1 \\ \vdots \\ \varepsilon_i \\ \vdots \\ \varepsilon_N \end{bmatrix}\end{aligned} \tag{4.15}$$

The NTF of the proposed architecture can be obtained by adding all N entries of matrix $[NTF]_{N1}$ to yield

$$NTF(z) = (1 - z^{-N}) + \sum_{j=1}^{N} (k_{ij} + z^{-(N-1)}k'_{ij} + z^{-N}k''_{ij}) \tag{4.16}$$

where

$$k_{ij} = \begin{cases} (-1)^{-(N+i-j)}\binom{2N}{N+i-j}(z)^{-(N+i-j)}, & \text{for } i < j \\ 0, & \text{for } i = j \\ (-1)^{-(i-j)}\binom{2N}{i-j}(z)^{-(i-j)}, & \text{for } i > j \end{cases} \tag{4.17}$$

$$k'_{ij} = \left\{ \begin{cases} (-1)^{-(N+i-j+1)}\binom{2N}{2N+i-j}(z)^{-(N+i-j+1)}, & \text{for } i < j \\ 0, & \text{for } i = j \\ (-1)^{-(i-j+1)}\binom{2N}{N+i-j}(z)^{-(i-j+1)}, & \text{for } i > j \end{cases} \right\} \binom{For}{Nodd} \tag{4.18}$$

$$k'_{ij} = \left\{ \begin{cases} (-1)^{-(N+i-j)}\binom{2N}{2N+i-j}(z)^{-(N+i-j+1)}, & \text{for } i < j \\ 0, & \text{for } i = j \\ (-1)^{-(i-j)}\binom{2N}{N+i-j}(z)^{-(i-j+1)}, & \text{for } i > j \end{cases} \right\} \binom{For}{Neven} \tag{4.19}$$

$$k''_{ij} = \left\{ \begin{cases} (-1)^{-N}\binom{2N}{N} + 1, & \text{for } i = j \\ (z)^{-N}, & \text{for } i = 1, j = 2 \\ 0, & \text{for } i = 1, 3 \leq j \leq N \end{cases} \right\} \binom{Toeplitz}{Circulant} \tag{4.20}$$

The coupling matrix $[K]_{NN}$ is different from the matrix mentioned for unextended and extended architecture proposed in (Hamidi and Miar-Naimi, 2014). As the quantization errors of each path is not cross-coupled to itself, the diagonal element of $[K]_{NN}$ and $[K']_{NN}$ are equal to zero. The diagonal elements of $[K'']_{NN}$ are constants.

Notice that the proposed dual extended architecture always has an even order and the sign of the highest order term is always positive. As a result, the proposed architecture does not require the $z \rightarrow -z$ transformation and the square wave modulation as in the case of extended architecture.

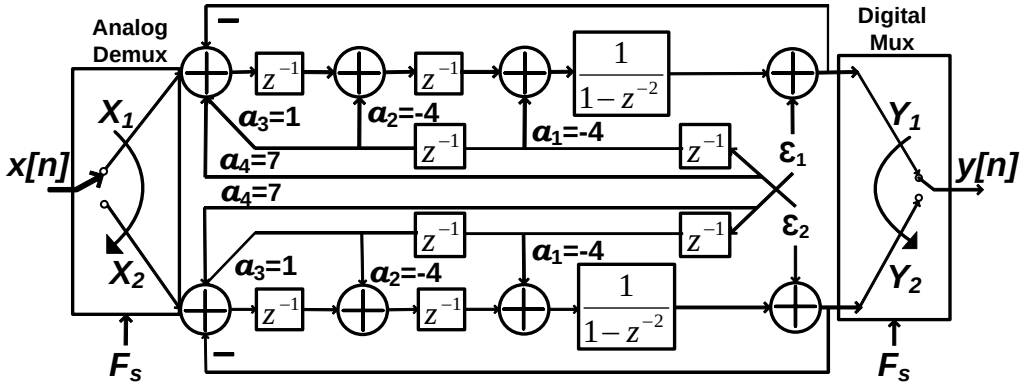


Figure 4.11: Proposed dual extended noise shaping based TI cross-coupled $\Sigma\Delta$ modulator for $N = 2$. Effective order = 4

4.7 Behavioural Simulation of the Dual Extended Architecture

A two path symmetric dual extended cross-coupled TI $\Sigma\Delta$ modulator was simulated using Matlab Simulink environment. Figure 4.11 shows the two path scheme of the proposed modulator.

Among the two paths, constants a_1, a_2, a_3 and a_4 are the noise coupled coefficients. The overall NTF can be derived as follows:

$$Y_1 = z^{-2}(X_1 + a_3 z^{-2} + a_4 \varepsilon_2) + a_1 z^{-1}\varepsilon_2 + a_2 z^{-3}\varepsilon_2 + (1 - z^{-2})\varepsilon_1 \tag{4.21}$$

$$Y_2 = z^{-2}(X_2 + a_3 z^{-2} + a_4 \varepsilon_1) + a_1 z^{-1}\varepsilon_1 + a_2 z^{-3}\varepsilon_1 + (1 - z^{-2})\varepsilon_2 \tag{4.22}$$

By combining Equations (4.21) and (4.22), NTF can be expressed by

$$NTF = 1 + a_1 z^{-1} + (a_4 - 1)z^{-2} + a_2 z^{-3} + a_3 z^{-4} \tag{4.23}$$

The n^{th}-order noise shaping determines a NTF given by $NTF = (1 - z^{-1})^n$ where, for $n = 4$, we have

$$NTF = (1 - z^{-1})^4 = 1 - 4z^{-1} + 6z^{-2} - 4z^{-3} + z^{-4} \tag{4.24}$$

Comparing Equations (4.23) and (4.24) yields the optimized coefficients of the archi-

tecture as $a_1 = -4$, $a_2 = -4$, $a_3 = 1$ and $a_4 = 7$. Coupling matrices for two path architecture can be obtained using Equations (4.17), (4.18), (4.19) and (4.20) as

$$K = \begin{bmatrix} 0 & -4z^{-1} \\ -4z^{-1} & 0 \end{bmatrix}, \; K' = \begin{bmatrix} 0 & -4z^{-2} \\ -4z^{-2} & 0 \end{bmatrix}, \; K'' = \begin{bmatrix} 7 & z^{-2} \\ z^{-2} & 7 \end{bmatrix}$$

Performance comparison of the proposed two path $(N = 2)$ modulator with unextended and extended noise shaping based TI symmetric cross-coupled $\Sigma\Delta$ modulator is performed using behavioural simulations. Figure 4.12 illustrates the comparison of output power spectra of unextended, extended and dual extended structures for $N = 2$.

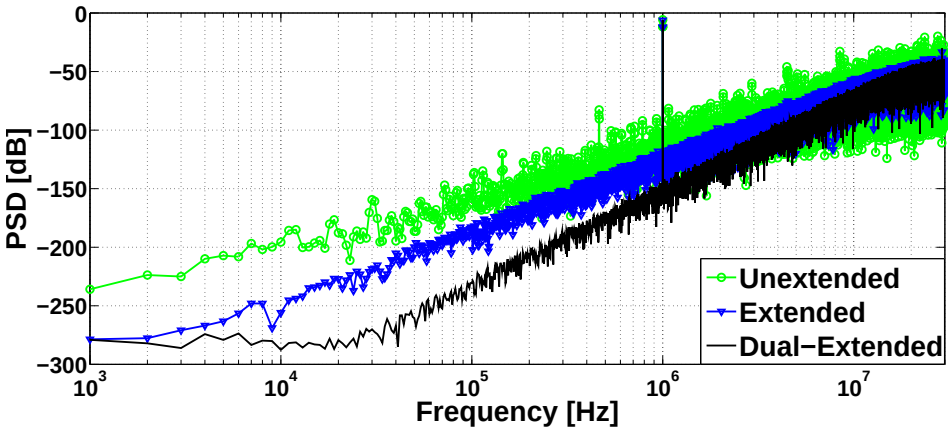


Figure 4.12: Output spectra of the unextended, extended and dual extended (proposed) architecture for $N = 2$.

A three path symmetric dual extended cross-coupled TI $\Sigma\Delta$ modulator was simulated using Matlab and Simulink environment. Figure 4.13 shows the three path scheme of the proposed modulator.

By similar analysis the coupling matrices for a three path architecture can be obtained using Equations (4.17), (4.18), (4.19) and (4.20) as

$$K = \begin{bmatrix} 0 & 15z^{-2} & -6z^{-1} \\ -6z^{-1} & 0 & 15z^{-2} \\ 15z^{-2} & -6z^{-1} & 0 \end{bmatrix}, \quad K' = \begin{bmatrix} 0 & -6z^{-3} & 15z^{-2} \\ 15z^{-2} & 0 & -6z^{-3} \\ -6z^{-3} & 15z^{-2} & 0 \end{bmatrix}, \; K'' = \begin{bmatrix} -19 & z^{-3} & 0 \\ 0 & -19 & z^{-3} \\ z^{-3} & 0 & -19 \end{bmatrix}$$

Performance comparison of the proposed three path $(N = 3)$ modulator with unextended and extended noise shaping based TI symmetric cross-coupled $\Sigma\Delta$ modulator

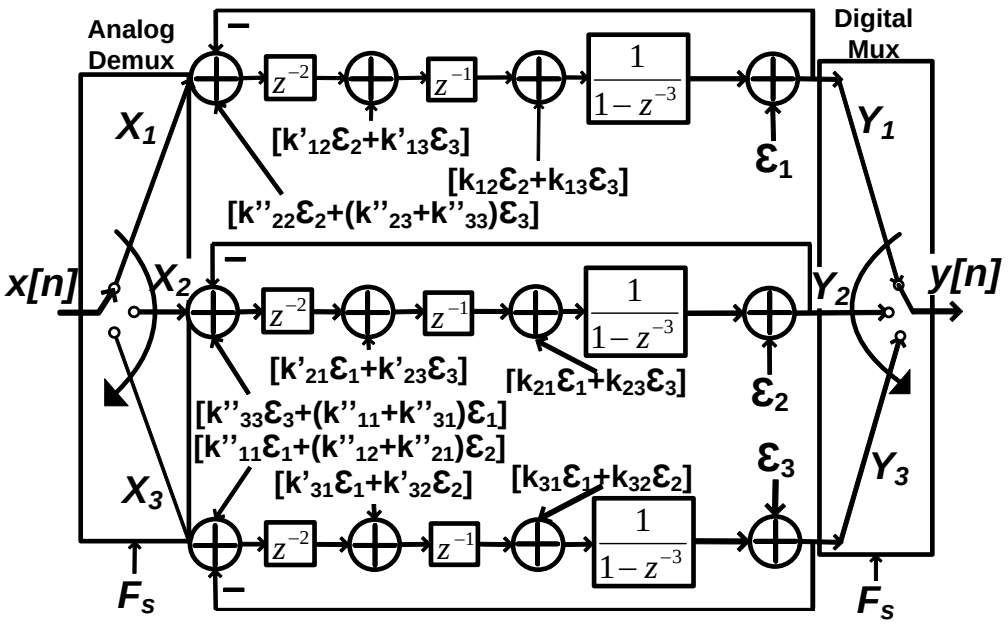


Figure 4.13: Proposed dual extended noise shaping based TI cross-coupled $\Sigma\Delta$ modulator for N = 3. Effective order = 6.

is performed using behavioural simulations. Figure 4.14 illustrates the comparison of output power spectra of unextended, extended and dual extended structures for $N = 3$.

For the analysis of two path architecture of Figure 4.11, an input sinusoidal waveform with frequency of 1 MHz is applied with -6 dBV amplitude. For the analysis of three path architecture of Figure 4.13, an input sinusoidal waveform with the same frequency of 1 MHz is applied with -12 dBV amplitude. The sampling frequency (F_s) is 60 MHz with an OSR of 15. Each path operates at a rate F_s/N. The signal bandwidth is 2 MHz. With the two path architecture, the slopes obtained are 40 dB/dec, 60 dB/dec and

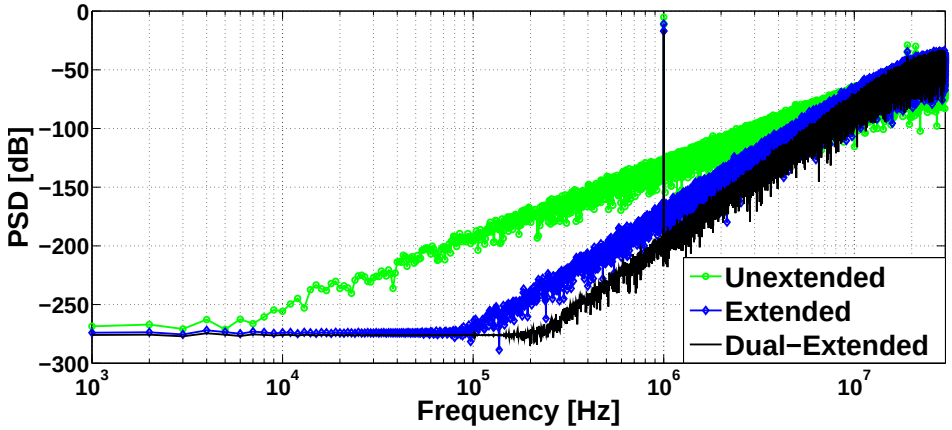


Figure 4.14: Output spectra of the unextended, extended and dual extended (proposed) architecture for $N = 3$.

Table 4.4: Comparison of architectures

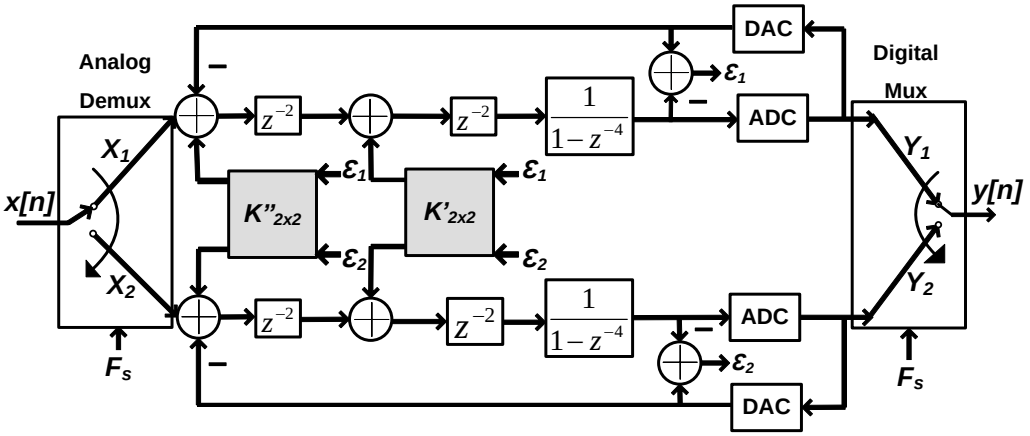
N	Parameters	Unextended (Hamidi and Miar-Naimi, 2014) (Bilhan and Maloberti, 2008)	Extended (Hamidi and Miar-Naimi, 2014)	Proposed Dual Extended
2	Effective order	2	3	4
	SNR (dB)	66.2	79.3	90.6
	Slope (dB/dec)	40	60	80
3	Effective order	3	5	6
	SNR (dB)	85.1	102.8	123.2
	Slope (dB/dec)	60	100	120

80 dB/dec for unextended, extended and dual extended architectures, respectively. With three path architecture of Figure 4.13, the slopes obtained are 60 dB/dec, 100 dB/dec and 120 dB/dec for unextended, extended and dual extended architectures, respectively. The results obtained for all the three structures are shown in Table 4.4.

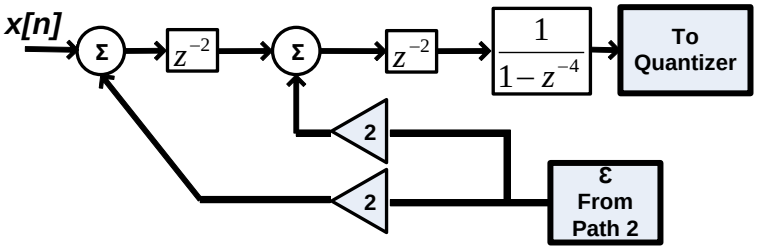
The SNR and the effective order of the proposed dual extended $\Sigma\Delta$ modulator architecture with respect to the unextended and extended $\Sigma\Delta$ modulator architectures for $N = 2$ and $N = 3$ are shown in Table 4.4. The effective order of the proposed scheme, obtained as $2N$, can be verified.

4.8 Cross-Coupling Architecture for $\Sigma\Delta$ Bandpass Modulator

Figure 4.15(a) shows the block diagram of the two path architecture of the proposed modulator. Each path forms a first order $\Sigma\Delta$ bandpass modulator. Two auxiliary inputs are created by separating delay block from the integral operator and splitting the delay block itself, where the noise coupled matrices are injected. The interpolation by 2, used to obtain the output at F_s, reduces the noise power of each path by 2. Therefore, the total noise power equals the noise power of a single path (Hamidi and Miar-Naimi,



(a)



(b)

Figure 4.15: Block diagram of the proposed cross coupled (a)$\Sigma\Delta$ bandpass modulator and (b) block diagram of the first path of the proposed simple cross-coupled bandpass model

2014). The quantization error, ε, is computed by subtracting the input of ADC from the output of the DAC for each path. Quantization errors of paths are injected separately into two 2-input, 2-output bank of coupling matrices K', and K'', respectively and the outputs of this bank are coupled as shown in Figure 4.15(a). The single path of the simple cross-coupled model is shown in Figure 4.15(b).

The paths are using two non-overlapping phases of the main clock frequency F_s and the output vectors $Y_i(z)$ are multiplexed (i.e., added) to generate the overall output sequence as

$$\begin{aligned} Y(z) &= \sum_{i=1}^{2} Y_i(z) = STF(z) \sum_{i=1}^{2} X_i(z) + NTF(z) \sum_{i=1}^{2} E_i(z) \\ &= STF(z)X(z) + NTF(z)E(z). \end{aligned} \tag{4.25}$$

where $X(z)$ and $Y(z)$ denote the z-transform of $x(n)$ and $y(n)$, respectively, and $E(z)$ represents the z-transform of the combined quantization noise sequence.

4.8.1 NTF Synthesis for Simple Cross-Coupled Bandpass $\Sigma\Delta$ Modulator

The NTF for the two-path cross coupled bandpass modulator is obtained by applying transformation to lowpass transfer function $\frac{z^{-1}}{1-z^{-1}}$.Two transformations were brought in. The first transformation is to make it bandpass by applying $z^{-1} \rightarrow -z^{-2}$ and the second transformation to make it an N path structure by applying $z^{-1} \rightarrow -z^{-N}$, following the first transformation. Since here we concentrate on the two-path architecture, the second transformation applied is $z^{-1} \rightarrow -z^{-2}$. Therefore the transfer function becomes:

$$\frac{z^{-1}}{1-z^{-1}} \rightarrow \frac{-z^{-2}}{1+z^{-2}} \rightarrow \frac{z^{-4}}{1-z^{-4}} \tag{4.26}$$

For a second order bandpass modulator NTF is given by,

$$NTF = (1+z^{-2})^2 = 1 + z^{-4} + 2z^{-2} \tag{4.27}$$

As illustrated in Figure 4.15, the inherent feedback of the $\Sigma\Delta$ loop generates the term $(1 - z^{-4})$ for each path. The additional terms $(2z^{-4} + 2z^{-2})$ evolve from the other cross-coupled path in order to complete the NTF. The coupling matrices K' and K'' are

$$K' = \begin{bmatrix} 0 & 2 \\ 2 & 0 \end{bmatrix}, \; K'' = \begin{bmatrix} 0 & 2 \\ 2 & 0 \end{bmatrix}$$

4.8.2 NTF Synthesis for Extended Cross-Coupled Bandpass $\Sigma\Delta$ Modulator

Extended cross-coupling architecture gives an effective NTF order of three with modified coupling matrices K' and K''. The single path of the extended cross-coupling model is shown in Figure 4.16.

For a third order modulator

$$NTF = (1+z^{-2})^3 = 1 + 3z^{-2} + 3z^{-4} + z^{-6} \tag{4.28}$$

The inherent feedback of the $\Sigma\Delta$ loop generates the term $(1 - z^{-4})$ for each path. The

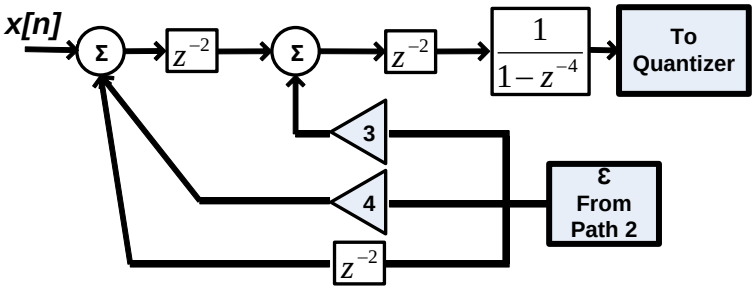


Figure 4.16: Block diagram of the first path of the proposed extended cross-coupled bandpass model.

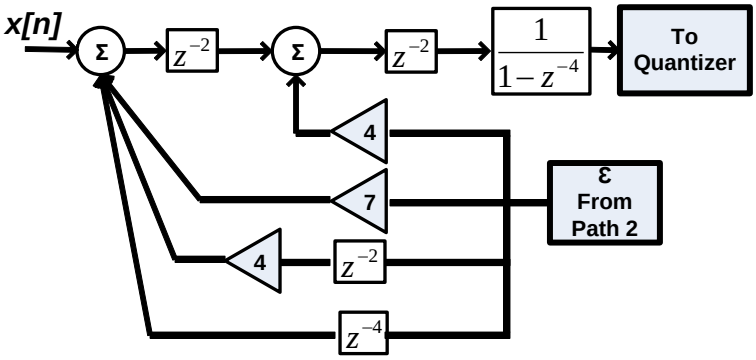


Figure 4.17: Block diagram of the first path of the proposed dual extended cross-coupled bandpass model.

additional terms $(z^{-6} + 4z^{-4} + 3z^{-2})$ evolve from the other cross-coupled path in order to complete the NTF.

The coupling matrices K' and K'' are

$$K' = \begin{bmatrix} 0 & 3 \\ 3 & 0 \end{bmatrix}, \; K'' = \begin{bmatrix} 0 & 4 + z^{-2} \\ 4 + z^{-2} & 0 \end{bmatrix}$$

4.8.3 NTF Synthesis for Dual Extended Cross-Coupled Bandpass $\Sigma\Delta$ Modulator

Dual Extended cross-coupling architecture gives an effective NTF order of 4 with modified coupling matrices K' and K''. The single path of the dual extended cross-coupling model is shown in Figure 4.17.

Table 4.5: Comparison of cross-coupled bandpass architectures

Model	Bandwidth [MHz]	OSR	Quantizer bits	SNR [dB]
Simple cross-coupled	4	107	2	62.0
Extended cross-coupled	4	107	3	72.5
Dual Extended cross-coupled	4	107	4	77.9

For a fourth order modulator

$$NTF = (1 + z^{-2})^4 = 1 + 4z^{-2} + 6z^{-4} + 4z^{-6} + z^{-8} \tag{4.29}$$

The inherent feedback of the $\Sigma\Delta$ loop generates the term $(1 - z^{-4})$ for each path. The additional terms $(z^{-8} + 4z^{-6} + 7z^{-4} + 4z^{-2})$ evolve from the other cross-coupled path in order to complete the NTF. Here the coupling matrices K' and K'' are

$$K' = \begin{bmatrix} 0 & 4 \\ 4 & 0 \end{bmatrix}, \; K'' = \begin{bmatrix} 0 & 7 + 4z^{-2} + z^{-4} \\ 7 + 4z^{-2} + z^{-4} & 0 \end{bmatrix}$$

4.8.4 Comparison of the Proposed Models with the Conventional Bandpass $\Sigma\Delta$ Modulator

Simulations of the proposed models were carried out using MATLAB with a bandwidth of 4 MHz and an OSR of 107. Table 4.5 depicts the results of simulations done for the proposed models which confirm improvement in the SNR. The performance comparison of the proposed bandpass $\Sigma\Delta$ modulator architectures with conventional bandpass feedback architecture is shown in Figure 4.18. The comparison is performed using the results obtained in the behavioural simulations carried out. The improvements in SNR with each of the proposed architectures are evident from the figure. The effective NTF order obtained for simple cross-coupled bandpass architecture is 2, and that of extended cross-coupled bandpass architecture is 3. NTF order of the dual extended cross-coupled bandpass architecture is 4 and it is evident that the noise shaping improves with the three architectures when compared to the conventional bandpass feedback architecture.

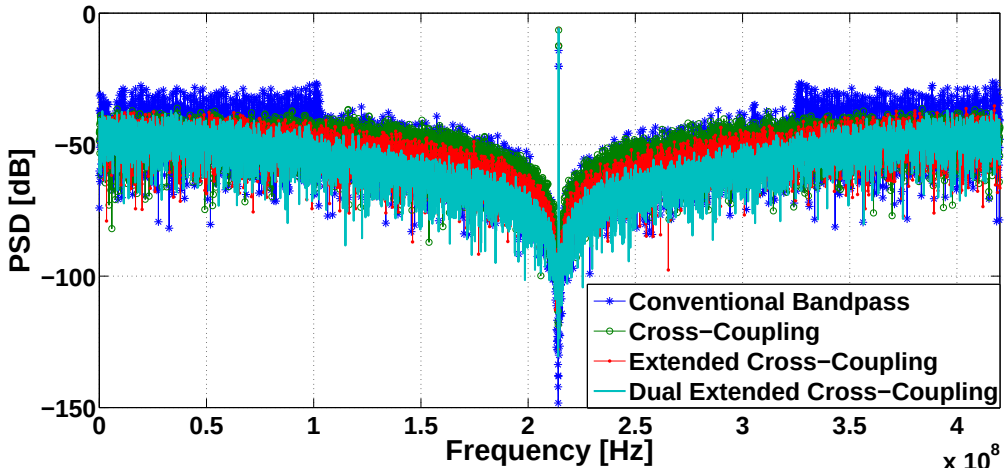


Figure 4.18: Comparison of the proposed cross-coupled bandpass architectures with conventional bandpass feedback architecture

4.9 Chapter Summary

The first part of the chapter deals with a novel ESLD compensated TI extended noise shaping based cross-coupled multi-path SMASH $\Sigma\Delta$ modulator. The excess delay associated with the SMASH loop (ESLD) of stage-II, which leads to quantization noise leakage between individual stages, is modelled in stage-I and the ESLD compensation and cancellation of the stage-I quantization error is perfectly achieved by feedback compensation mechanisms, which has been demonstrated analytically and through behavioural and circuit-level simulations. The ESLD compensation mechanisms introduced perfectly cancels the stage-I quantization error and enhances the order of noise shaping. Thus the modulator benefits from the 3-bit stage-II quantizer. The intentionally incorporated full clock cycle delay makes the circuit-level realization much easier. One bit quantizer used in stage-I and less number of integrators to achieve higher order makes the model hardware efficient. Time interleaving enables each path to operate at a lower rate which makes the model power efficient. The low hardware requirement of the proposed architecture compared to DNC-SMASH model has been illustrated in this chapter. Moreover, the input referred stability is also enhanced by the newly proposed architecture. Hspice simulations validate the proposed architecture in 45 nm CMOS technology. It consumes only 385 μW from a 1V power supply and provides 11-bit performance for -6dB input level.

A dual extended noise shaping based time interleaved symmetric cross-coupled $\Sigma\Delta$ modulator is proposed in the latter section of the chapter. This architecture showcases

the advantage of achieving an NTF order twice the number of cross-coupled paths, which has been demonstrated by using both analytical analysis and behavioural simulations. The dual extended cross-coupling technique enables the realization of additional terms of higher order NTF without significant increase in power and area. The practical implementation of extra coupling branches typically uses added switched-capacitors and does not require an extra opamp and hence capable of greatly relaxing the circuit specifications. By incorporating the TI concepts the proposed modulator demonstrates it's potential for low-power, high-bandwidth and high performance wireless applications.

CHAPTER 5

A MULTI-STANDARD RECONFIGURABLE TI CROSS-COUPLED $\Sigma\Delta$ MODULATOR

This chapter describes an efficient triple-mode hexa-standard TI reconfigurable cross-coupled $\Sigma\Delta$ modulator designed for six different wireless communication standards such as GSM, Bluetooth, GPS, WCDMA, WLAN and WiMAX. Enhanced noise shaping characteristics, obtained by TI cross-coupling of $\Sigma\Delta$ paths, have been utilized for the modulator design. Power and hardware efficiency is achieved by using the new dual extended (DE) noise shaping technique.

This chapter is structured as follows. Section 5.1 presents the proposed multi-standard architecture, and its analysis at the behavioural-level. Section 5.2 describes the effects of opamp non idealities on the multi-standard architecture. Effects of channel mismatch and cross-coupling coefficient mismatch are discussed in section 5.3. The circuit-level simulation results are presented in Section 5.4. Finally, Section 5.5 portrays the inferences from this chapter.

5.1 Proposed Hexa-standard Reconfigurable Architecture

The most attractive candidate for the implementation of multi-standard ADCs are the $\Sigma\Delta$ converters (Gerosa *et al.*, 2006),(Rusu *et al.*, 2006*a*). The capability of an ADC to handle variety of performance requirements necessitates a reconfigurable solution with different architectural modes of operation. The behavioural model of the designed hexa-standard architecture is shown in Figure 5.1 (AV and Jose, 2014). The fully reconfigurable structure works with just two integrators in order to meet the specifications of multiple standards. The hardware reconfiguration is achieved by flexible switching between the three different noise cross-coupling stages, that is, stage-1, stage-2 and stage-3, which corresponds to unextended (Bilhan and Maloberti, 2009),(Hamidi and

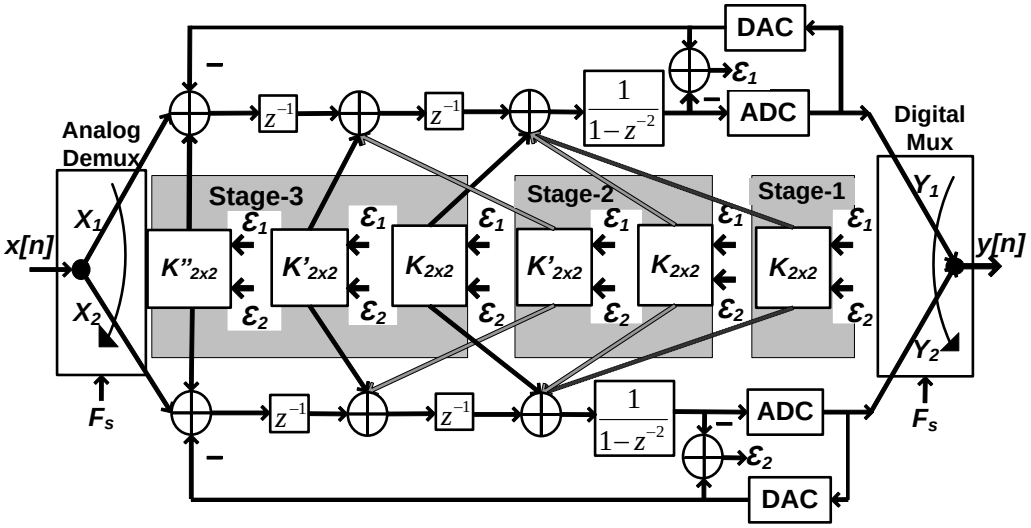


Figure 5.1: Block diagram of proposed multi-standard architecture

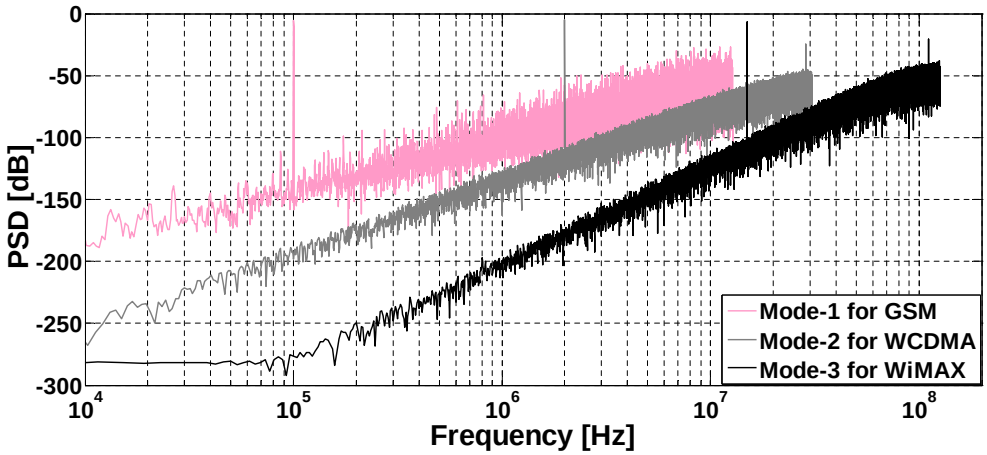


Figure 5.2: Power spectral density of three modes for different standards

Miar-Naimi, 2014), extended (Hamidi and Miar-Naimi, 2014) and dual extended noise cross-coupling architectures, respectively. The time interleaving technique enables the proposed architecture to operate at half the sampling rate ($F_s/2$), which reduces the power consumption. A reconfigurable 2+1 bit pipelined quantizer is used in each path of the modulator. The proposed architecture is able to support hexa-standard specifications and attains desired triple-mode performance by switching between its stages.

5.1.1 Mode-1 - Unextended Noise Cross-Coupling

In this mode, the proposed hexa-standard architecture is configured to operate in unextended noise cross-coupling scheme (Bilhan and Maloberti, 2009), (Hamidi and Miar-Naimi, 2014), with an effective noise transfer function (NTF) order of 2. Only stage-1

is powered on during this operating mode, where as stage-2 and stage-3 are turned off to save power. The quantizer is configured to operate in 2-bit. GSM and Bluetooth standards operate in Mode-1 configuration. The cross-coupling-matrix and the output vector is given by

$$K = \begin{bmatrix} 0 & -2z^{-1} \\ -2z^{-1} & 0 \end{bmatrix}$$

$$[Y]_{2\times1} = z^{-2}[X]_{2\times1} + [K]_{2\times2}[E]_{2\times1} + (1 - z^{-2})[I]_{2\times2}[E]_{2\times1} \tag{5.1}$$

5.1.2 Mode-2 - Extended Noise Cross-Coupling

In this mode, the proposed hexa-standard architecture is configured to operate in extended noise cross-coupling scheme (Hamidi and Miar-Naimi, 2014), with an effective NTF order of 3. Only stage-2 is powered on during this operating mode, where as stage-1 and stage-3 are turned off to save power. The quantizer is configured to operate in 2+1 bit. GPS and WCDMA standards operate in Mode-2 configuration. The coupling-matrices and the output function is given by

$$K = \begin{bmatrix} 0 & -3z^{-1} \\ -3z^{-1} & 0 \end{bmatrix} \; K' = \begin{bmatrix} 4 & -z^{-1} \\ -z^{-1} & 4 \end{bmatrix}$$

$$[Y]_{2\times1} = z^{-2}[X]_{2\times1} + z^{-1}[K']_{2\times2}[E]_{2\times1} + [K]_{2\times2}[E]_{2\times1} + (1 - z^{-2})[I]_{2\times2}[E]_{2\times1} \tag{5.2}$$

5.1.3 Mode-3 - Dual Extended Noise Cross-Coupling (proposed)

In this mode, the proposed hexa-standard architecture is configured to operate in dual extended noise cross-coupling scheme, with an effective NTF order of 4. Only stage-3 is powered on during this operating mode, where as stage-1 and stage-2 are turned off to save power. The quantizer is configured to operate in 2+1 bit. WLAN and WiMAX standards operate in Mode-3 configuration. The coupling-matrices and the output function is obtained by using (4.13), (4.17), (4.18), (4.19) and (4.20) as

$$K = \begin{bmatrix} 0 & -4z^{-1} \\ -4z^{-1} & 0 \end{bmatrix} \; K' = \begin{bmatrix} 0 & -4z^{-2} \\ -4z^{-2} & 0 \end{bmatrix} \; K'' = \begin{bmatrix} 7 & z^{-2} \\ z^{-2} & 7 \end{bmatrix}$$

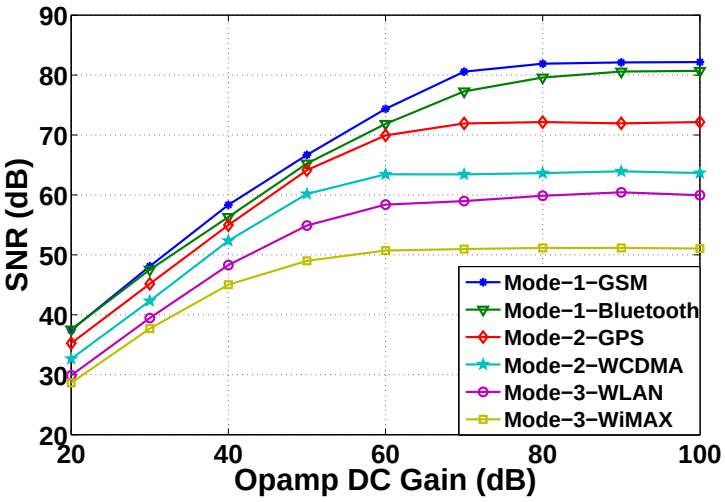
$$[Y]_{2\times1} = z^{-2}[X]_{2\times1} + \{z^{-2}[K'']_{2\times2} + z^{-1}[K']_{2\times2} + [K]_{2\times2} + (1 - z^{-2})[I]_{2\times2}\}[E]_{2\times1} \tag{5.3}$$

The three modes, respectively, for GSM, WCDMA and WiMAX, has been simulated and their power spectral density (PSD) comparison is shown in Figure 5.2. The order of noise shaping and the enhancement in performance for the three modes can be verified from the figure. Using MATLAB and Sigma-Delta Toolbox (Schreier, 2004) the behavioural-level simulation of the proposed reconfigurable architecture is performed, verifying its performance and flexibility to hexa-standard scenarios. The output spectra are obtained from the behavioural-level simulations using a 65536-point FFT.

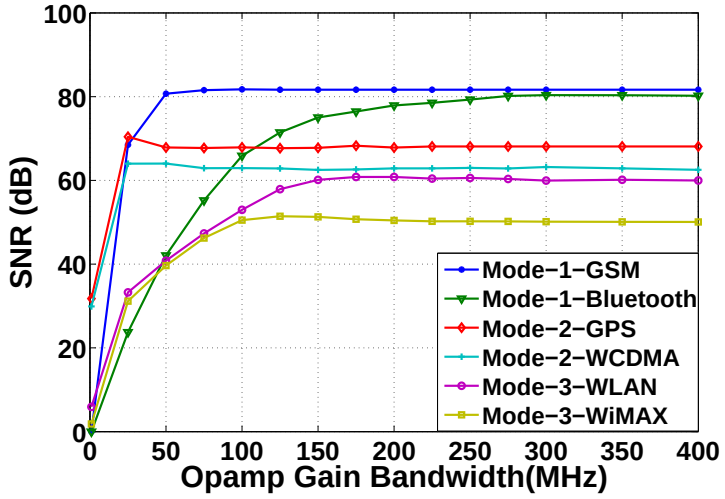
5.2 Effects of Opamp Non-Idealities on the Hexa-Standard Architecture

The low frequency gain of an integrator is limited by the finite dc gain of the opamp. The zeros of the NTF gets shifted from $z = 1$ to complex conjugate positions inside the unity circle. This degrades the in-band noise shaping performance. The opamp non-idealities like gain bandwidth product (GBW) and the finite slew rate (SR) are also important performance determining parameters (Maloberti, 2007), (Koe and Zhang, 2002).

In order to evaluate the effects of opamp non-idealities, the proposed triple-mode reconfigurable TI symmetric cross-coupled $\Sigma\Delta$ modulator was simulated for six different wireless standards, with an input sinusoidal signal of -3 dBV amplitude. The simulations were carried out in time domain using the opamp model described in (Malcovati *et al.*, 2003) and the results are depicted in Figure 5.3(a) to Figure 5.4(c). OSR and bandwidth were selected according to the standard's specifications. In Figure 5.3(a)



(a)



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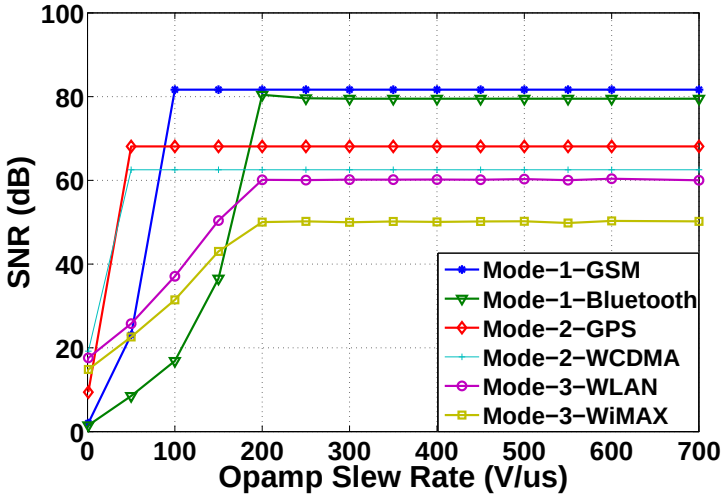
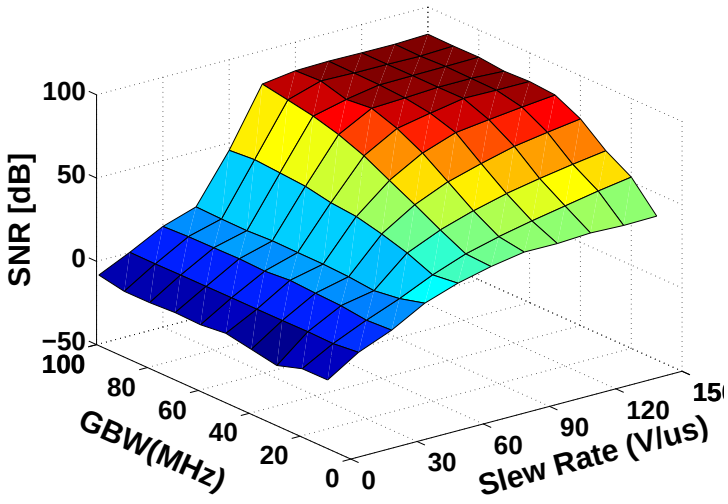
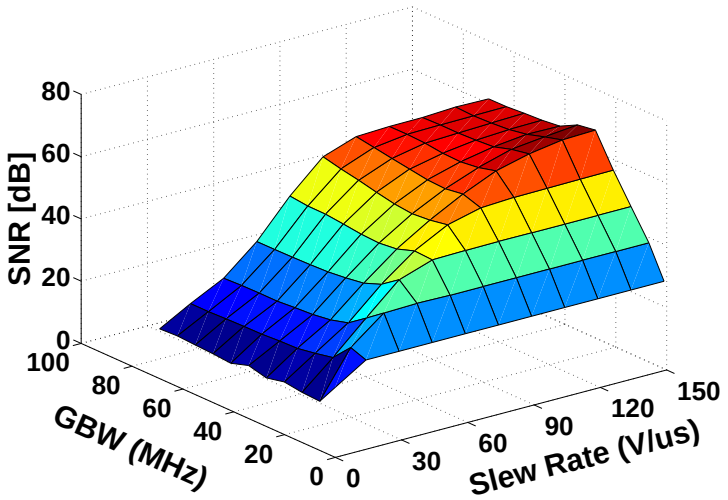


(c)

Figure 5.3: Effect of opamp non-idealities on the proposed reconfigurable cross-coupled multi-standard architecture (a) opamp DC Gain; (b) opamp gain bandwidth; (c) opamp slew rate



(a)



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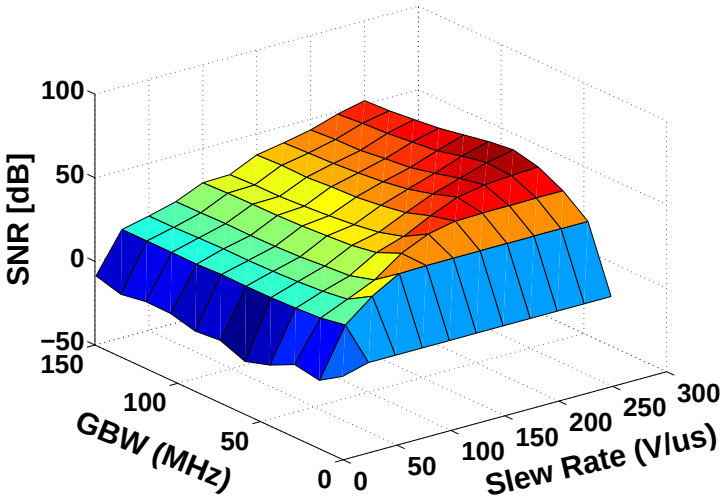


(c)

Figure 5.4: SNR variation of the proposed architecture as a function of (a) GBW and slew rate for GSM using Mode-1; (b) GBW and slew rate for WCDMA using Mode-2 ; (c) GBW and slew rate for WiMAX using Mode-3

SNR is plotted against DC gain swept from 20 dB to 100 dB. It is clear that the SNR performance of the proposed architecture is very sensitive for low opamp DC gain. Similarly, SNR is also plotted against GBW and slew rate swept from 0 to 400 MHz and 0 to 700 V/μs, respectively, as shown in Figure 5.3(b) and Figure 5.3(c). Since the same opamp is being used for all the standards an opamp DC gain of 70 dB and bandwidth of 200 MHz are necessary for the modulator to achieve the performance requirements. The slew rate requirement is also not stringent. A 200 V/μs is sufficient for all the standards.

Likewise, 3D plots are also obtained to understand the variation in SNR of the proposed multi-mode modulator architecture with opamp GBW for various values of slew rate. The plots are obtained for all the 3 modes of the modulator as depicted in Figure 5.4(a) to Figure 5.4(c). Simulations of Mode-1, Mode-2 and Mode-3 operation were done for GSM, WCDMA and WiMAX, respectively. The optimum values of the opamp GBW and slew rate can be easily obtained from the 3D plots.

5.3 Effects of Cross-Coupling Coefficient Mismatch and Channel Mismatch

The reduction in the modulator performance due to correlative coefficient mismatch in cross-coupled coefficients (a_1, a_2, a_3, a_4 described earlier in Figure 4.11) is depicted in Figure 5.5. This performance degradation is due to the leakage of quantization noises injected at various arbitrary nodes on the main paths. The amount of degradation in SNR value with -1 $\%$ to +1$\%$ mismatch error in the cross-coupled coefficients can be obtained from the 3D-plots. A worst case SNR degradation of 18 dB can be observed.

Channel mismatch is an inevitable problem in any multi-path architecture, due to the variations in layout and silicon fabrication. The architecture proposed in this chapter is a multi-path TI modulator, which is not immune to the adverse effects of channel mismatch. This can lead to an increase of the noise floor within the band of interest, degrading the effective SNR. The degradation in SNR performance of the proposed triple-mode architecture, for the six wireless standards, with -5$\%$ to +5$\%$ variation of the channel mismatch is presented in Figure 5.6(a). Monte Carlo analysis of 1000 runs were

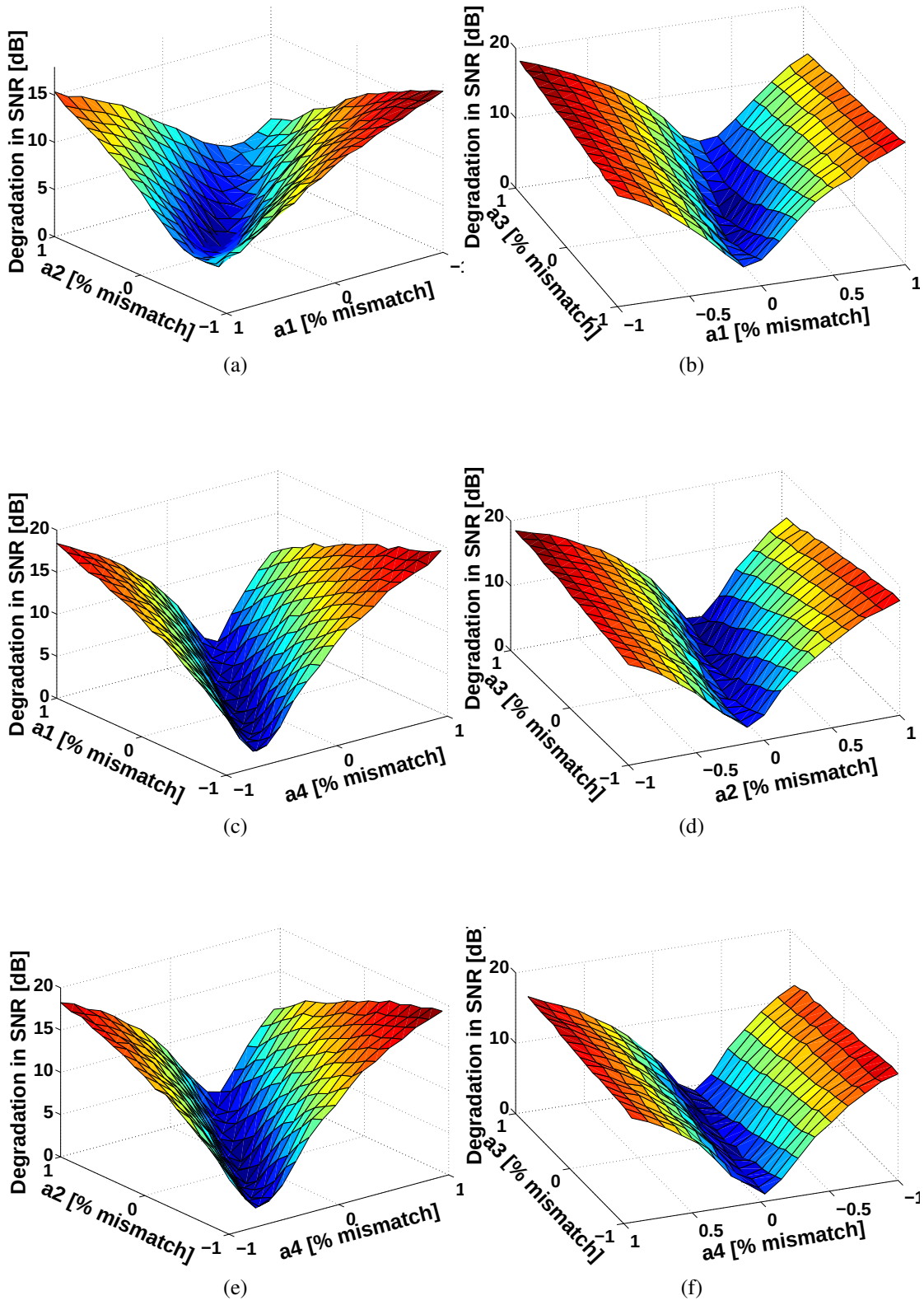
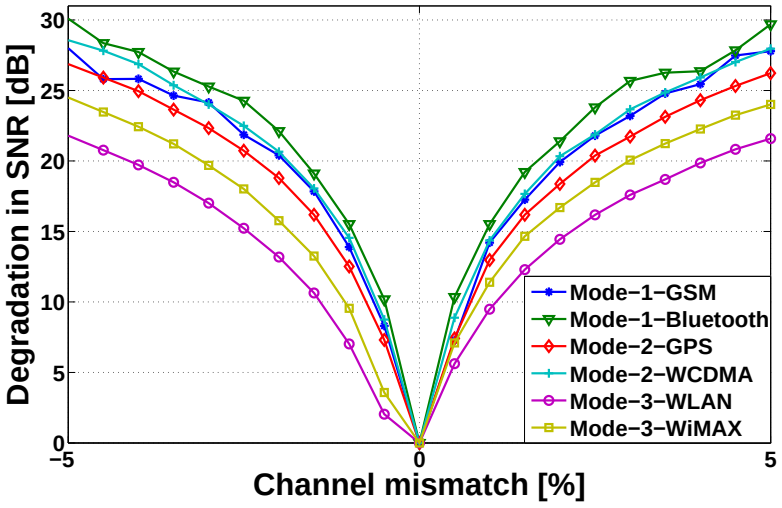
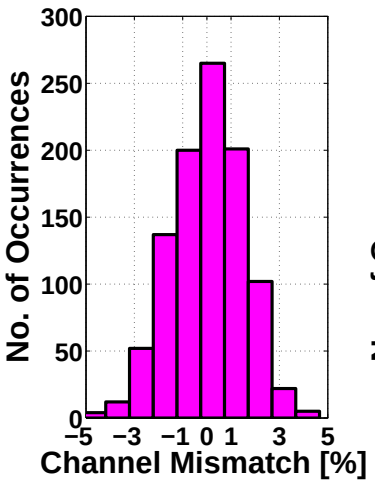


Figure 5.5: Degradation in SNR due to cross-coupled coefficients mismatches. (a) a1 and a2; (b) a1 and a3; (c) a1 and a4; (d) a2 and a3; (e) a2 and a4; (f) a3 and a4



(a)



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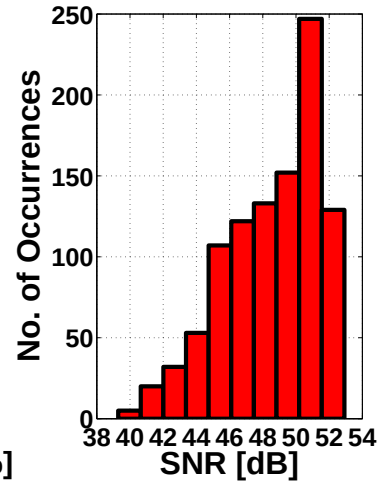


(c)

Figure 5.6: Channel mismatch analysis (a) SNR variation as a function of Channel Mismatch, (b) Monte Carlo simulation of channel mismatch for the worst case (WiMAX using Mode-3), (c) corresponding variation in SNR of the proposed reconfigurable cross-coupled multi-standard architecture

performed for which the channel mismatch with randomly selected values around the nominal value and its corresponding variation in SNR of the proposed reconfigurable cross-coupled multi-standard architecture are shown in Figure 5.6(b) and Figure 5.6(c), respectively. SNR degradation of 22 dB to 30 dB can be observed from the figure.

5.4 Circuit-Level Implementation

The proposed modulator is implemented in a 45 nm CMOS process, with a supply of 1V and input signal range of 0.7V. The design of the integrator is very critical as the modulator output is highly sensitive to integrator non-idealities. The ideal OTA is char-

acterised by an infinite output resistance. Hence, a folded-cascode opamp configuration with a class AB output buffer, is used as the OTA, shown earlier in Figure 4.6 (Baker, 2008)]. The folded-cascode amplifier is commonly used in low-voltage high-speed applications because of its large output swing and low input common-mode voltage.

As we know that, a multi-bit quantizer reduces the total quantization noise and improves the stability of the modulator while we go for higher order noise shaping. The proposed architecture employs a 3-bit quantizer, which lowers the quantization noise floor and improves the maximum stable amplitude of the modulator.

Another significant component in the design of the modulator is the wide-swing clocked comparator (Baker, 2008). The 3-bit quantizer in each path of the modulator uses eight such clocked comparators. When the positive input (+) gets above negative input (-), the output of the comparator becomes high on the rising edge of the clock. It works very well even for signal differences that are tens of millivolts. It has better sensitivity, wider input signal swing and better immunity to kickback noise.

The single-ended switched capacitor (SC) circuit-level implementation for one of the two paths of the proposed multi-mode reconfigurable TI symmetric cross-coupled $\Sigma\Delta$ modulator is depicted in Figure 5.7, with an integrating capacitor 'C' of value 10 μF. The entire multi-mode modulator architecture contains only two OTA integrators, targeting an optimum low-power multi-standard solution. Since the modulator is a symmetric TI structure, the OTAs are biased identically to meet the targeted standard's requirements.

Generally, the direct realization of six different ADCs, each targeting six wireless standards, needs 22 amplifiers; five for WiFi, five for WiMAX, four for WCDMA, four for GPS, two for Bluetooth and two for GSM (Seyedhosseinzadeh and Yavari, 2012), while only four amplifiers are sufficient to implement the proposed cross-coupled multi-standard modulator. The area requirement of the multi-standard modulator is approximately equal to that of a second-order multi-bit modulator, which makes the modulator area efficient as well.

Clock signals with four different phases, $\Phi1$, $\Phi2$, $\Phi3$ and $\Phi4$, were used to simulate the SC model. They are depicted in Figure 5.7. Each of the paths operates at half the clock rate and this decimation is achieved by making use of the clock phases $\Phi1$ and $\Phi2$.

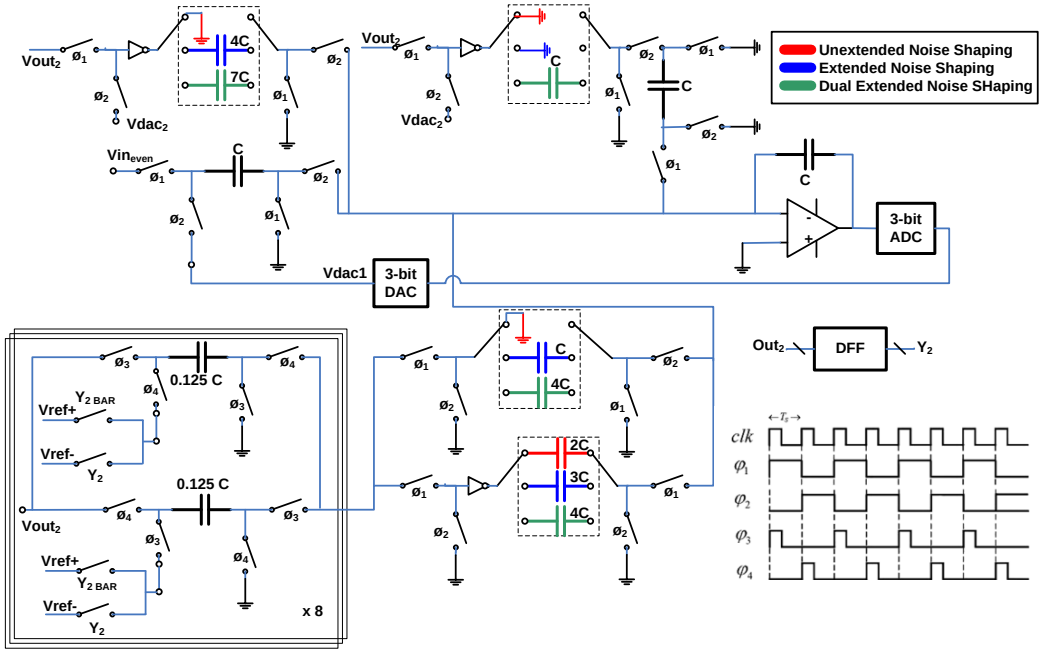


Figure 5.7: Switched-capacitor circuit implementation of a single path of the proposed multi-mode reconfigurable TI symmetric cross-coupled $\Sigma\Delta$ modulator

The cross coupled coefficients and the individual stage gains are realized by the ratios of capacitors around the amplifier (San *et al.*, 2009). The commutator switches, shown in dotted line boxes, help to select the three different modes for facilitating hexa-standard operation. The outputs of the OTA based integrators are denoted by $Vout_1$ and $Vout_2$, and the DAC outputs as $Vdac_1$ and $Vdac_2$. The error signals are generated by analog subtraction of $Vout$ and $Vdac$ using the switched capacitor logic. The circuit-level simulation of the complete triple-mode reconfigurable TI cross-coupled $\Sigma\Delta$ modulator, implemented in a 45 nm CMOS technology, were performed using HSPICE circuit simulator. The switches are modelled using transmission gates. The folded-cascode OTA opamp with an open loop gain of 75 dB and slew rate 200 V/µs were used to model the integrator. A single path of the proposed multi-mode reconfigurable TI symmetric cross-coupled $\Sigma\Delta$ modulator has been implemented in 45 nm CMOS technology using Cadence tools and the obtained layout is shown in Figure 5.8.

The circuit-level simulated dynamic range (DR) of the proposed hexa-standard architecture, ie. the variation of SNR against input amplitude, for all the six wireless standards are plotted in Figure 5.9. The data is obtained from the transient simulations carried out in Hspice circuit simulator.

The performance of the modulator is evaluated for six different wireless standards

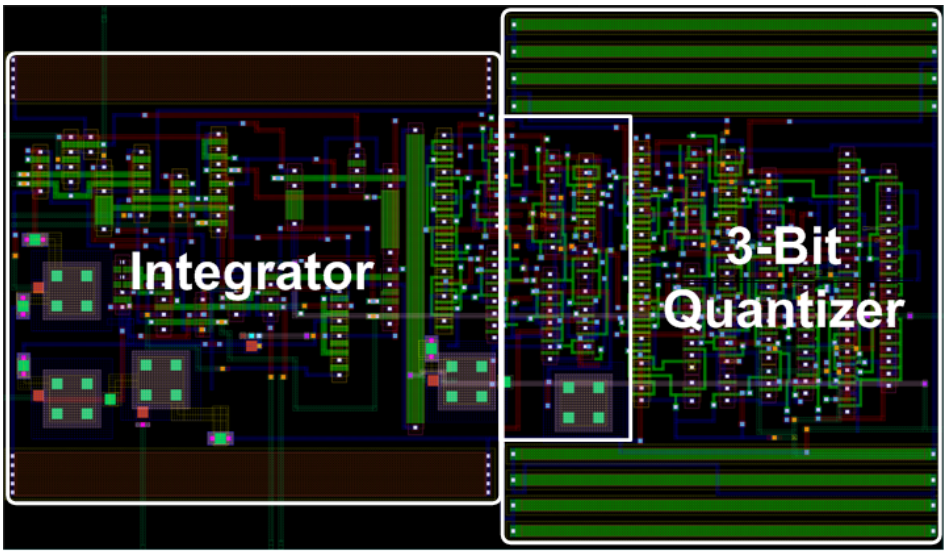


Figure 5.8: Layout of a single path of the proposed multi-mode reconfigurable TI symmetric cross-coupled $\Sigma\Delta$ modulator

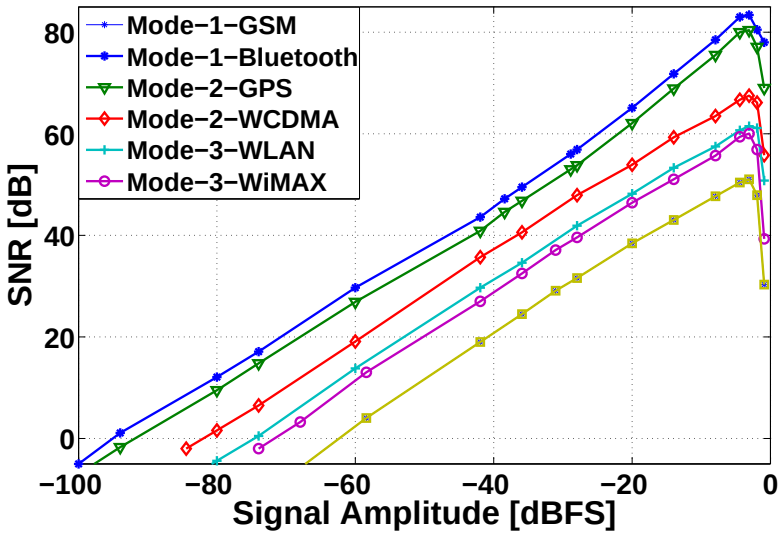


Figure 5.9: The variation of SNR against input amplitude

using different sinusoidal signals. The power spectral densities of the six different wireless standards are shown in Figure 5.10. The power consumption of the modulator is 1.93mW from a 1V power supply. To compare proposed architecture with the other previously reported state-of-the-art $\Sigma\Delta$ modulators the following figure of merit (FoM) was used:

$$Figure\ of\ Merit(FoM) = \frac{P}{2^{ENOB} \times F_N} \tag{5.4}$$

where P and F_N refer to the power consumption and Nyquist rate of the modulator, respectively. The performance of the transistor-level simulated triple-mode reconfigurable TI cross-coupled $\Sigma\Delta$ modulator, in Hspice, is summarized in Table 5.1.

Table 5.1: Performance summary of the proposed cross-coupled multi-standard architecture

Wireless Standard	Architecture	Mode/Order/ quantizer bits	Fin (MHz)	BW (MHz)	OSR	SNR [dB]	ENOB (bits)	Required ENOB (bits)	Power (mW)	FoM (pJ/ Conversion)
GSM	Un-extended	1/2/(2)	0.1	0.2	128	83.4	14.14	12-14	1.89	0.524
Bluetooth	Un-extended	1/2/(2)	0.5	1	32	80.2	13.029	13	1.89	0.226
GPS	Extended	2/3/(2+1)	1	2	20	67.8	10.97	10	1.9	0.474
WCDMA	Extended	2/3/(2+1)	2	3.84	16	61.5	10.5	6-8	1.9	0.342
WLAN	Dual Extended	3/4/(2+1)	10	22	10	60.82	9.81	8-14	1.93	0.0978
WiMAX	Dual Extended	3/4/(2+1)	12.25	28	8	51.03	8.76	7-11	1.93	0.159

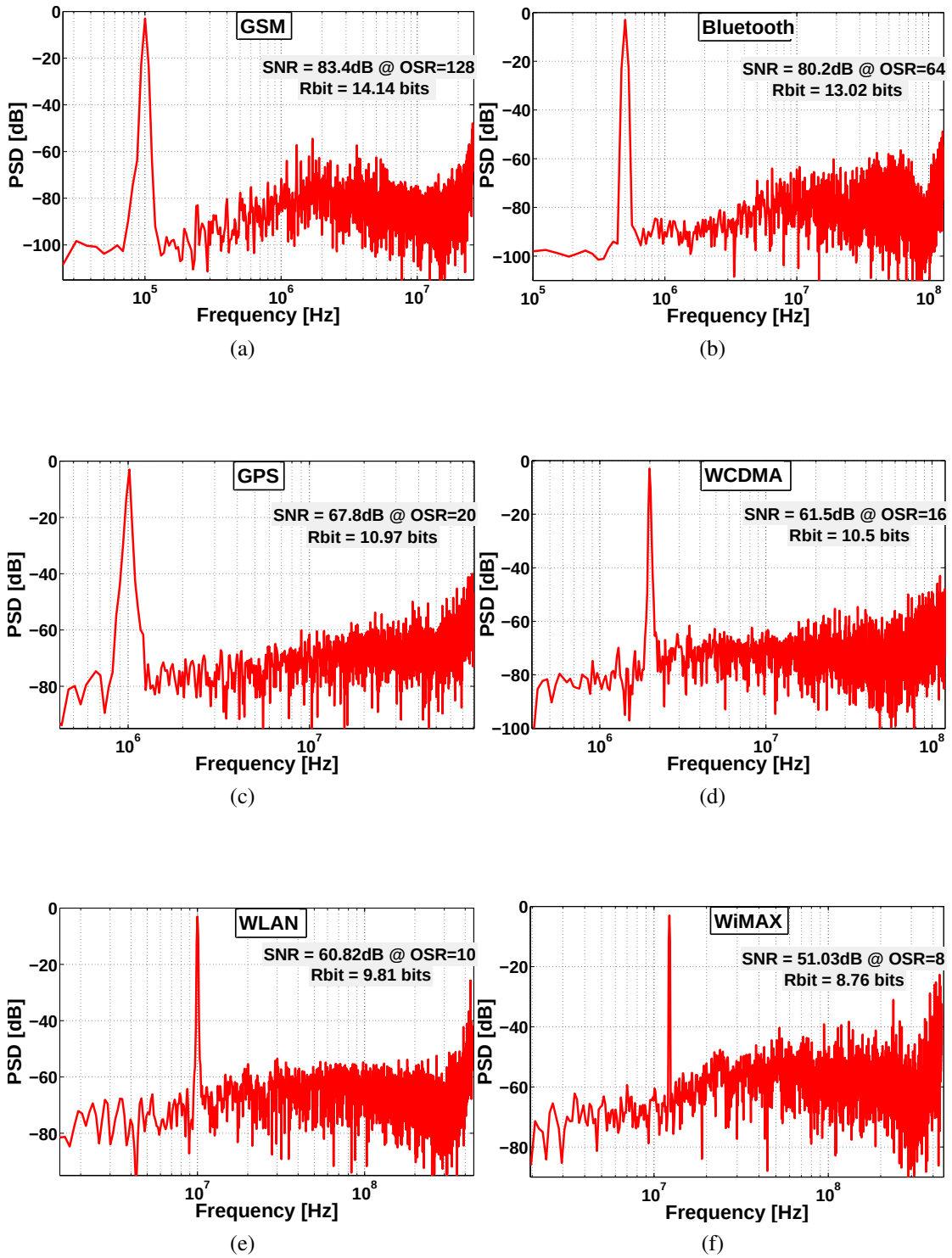


Figure 5.10: Output power spectra of the switched-capacitor circuit of the proposed architecture for (a) GSM using Mode-1; (b) Bluetooth using Mode-1; (c) GPS using Mode-2; (d) WCDMA using Mode-2; (e) WLAN using Mode-3 and (f) WiMAX using Mode-3

Through Monte Carlo analysis, the worst case performance degradation of the proposed multi-standard architecture due to process variation and temperature variation are estimated. Monte Carlo analyses of 1000 runs were performed for which the threshold voltage (V_{th}) and the temperature are varied independently with randomly selected values around the nominal value, following a gaussian distribution. Figure 5.11(a) shows

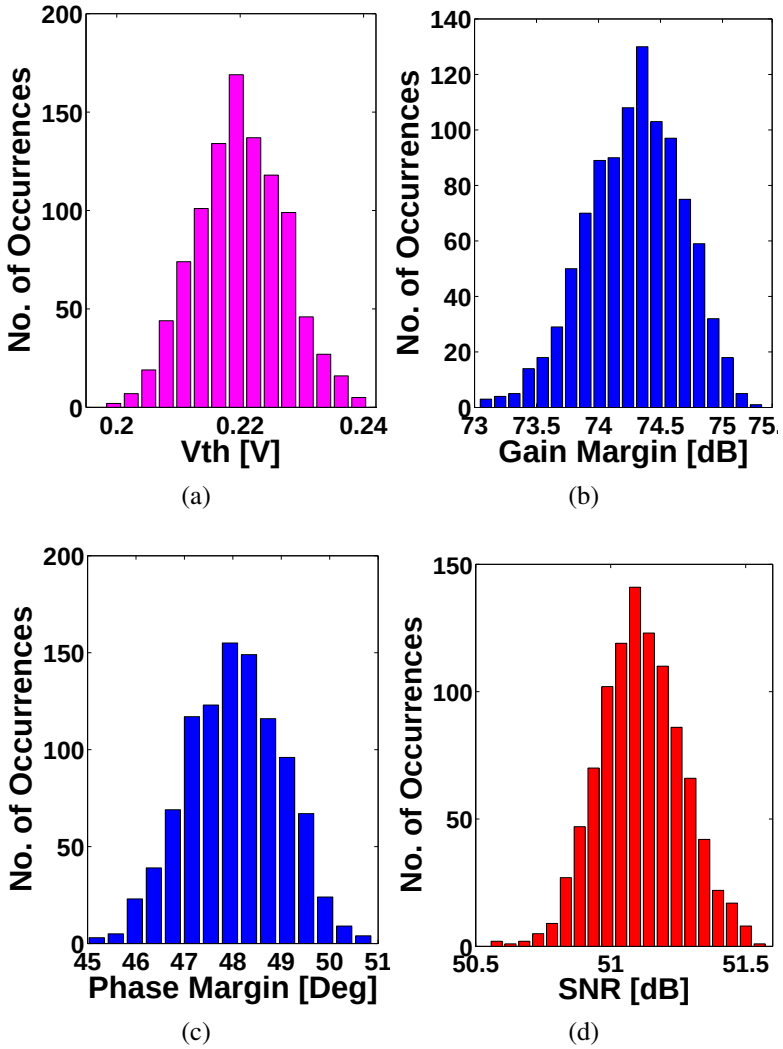


Figure 5.11: (a) Monte Carlo simulation of process variation; (b) corresponding variation in opamp gain margin; (c) opamp phase margin; and (d) SNR of the proposed reconfigurable architecture for the worst case (WiMAX using Mode-3)

the histogram of V_{th} values with $3\sigma = 10\%$ from the nominal value. The corresponding histograms of the opamp gain margin, opamp phase margin and the SNR of the proposed reconfigurable architecture for the worst case (i.e. WiMAX using Mode-3) are shown in Figure 5.11(b), Figure 5.11(c) and Figure 5.11(d) respectively. The SNR in the worst case degrades by a tolerable range of 1.4 dB. The histogram of temperature, with gaussian distributed values, ranges from -50 ^{o}C to 100 ^{o}C is shown in Figure

5.12(a). Similarly, the corresponding histograms of the opamp gain margin, opamp phase margin and the SNR of the proposed reconfigurable architecture for the worst case (i.e. WiMAX using Mode-3) are shown in Figure 5.12(b), Figure 5.12(c) and Figure 5.12(d) respectively. Here too the SNR degrades only by a tolerable range of 1.4 dB in the worst case. Therefore, variation in process and temperature do not degrade the overall performance of the proposed multi-standard architecture.

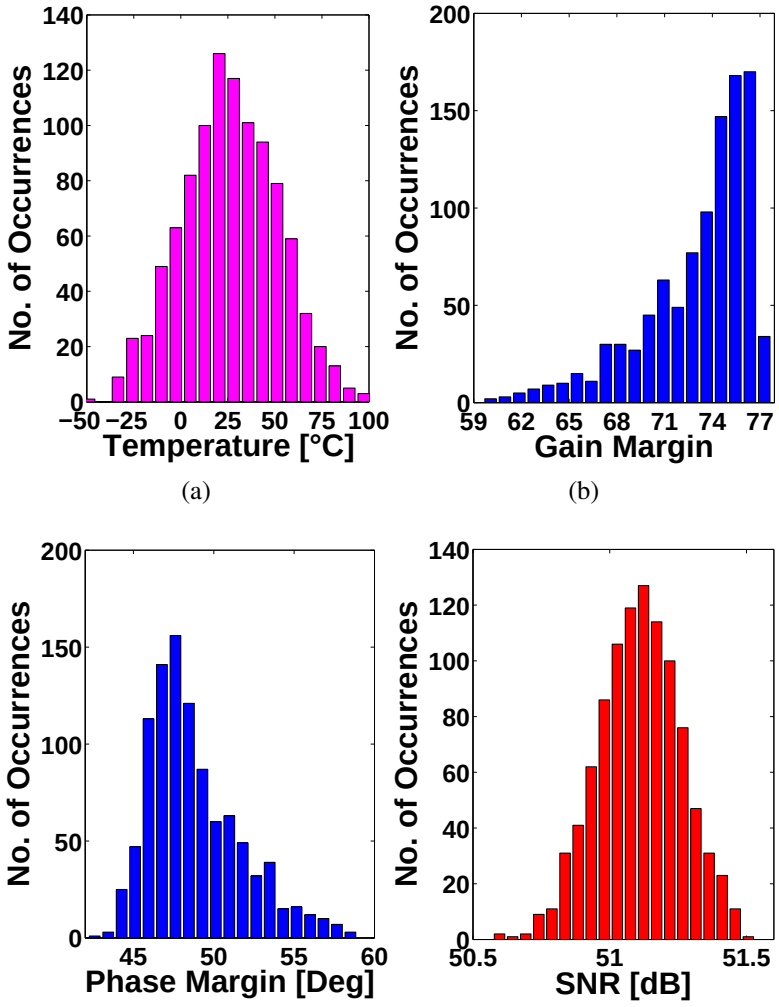


Figure 5.12: (a) Monte Carlo simulation of temperature; (b) corresponding variation in opamp gain margin; (c) opamp phase margin; and (d) SNR of the proposed reconfigurable architecture for the worst case (WiMAX using Mode-3)

A state-of-the-art comparison of the proposed triple-mode reconfigurable TI cross-coupled $\Sigma\Delta$ modulator with the previously reported $\Sigma\Delta$ modulators is given in Table 5.2. The efficiency of the proposed architecture can be clearly understood from the FoM values. The power consumption of the modulator is tremendously decreased by less hardware, TI operation, low OSR, low supply voltage, flexible switching and the

Table 5.2: Performance comparison of the proposed $\Sigma\Delta$ modulator with the state-of-the-art modulators (*simulation-results)

Work	Year	CMOS Process	VDD (V)	Topology	No. of Integrators	F_N (MHz)	SNDR [dB]	Fs (MHz)	Power (mW)	FoM (pJ/ Conversion)
This Work*	2015	45nm	1	Cross-Dual	2	28	51.03	224	1.93	0.159
				Extended	2	22	60.82	220	1.93	0.098
				Cross	2	3.84	61.5	61.44	1.9	0.342
				Extended	2	2	67.8	40	1.9	0.474
				Cross	2	1	80.2	32	1.89	0.342
				Unextended	2	0.2	83.4	25.6	1.89	0.474
(Rusu *et al.*, 2006*b*)*	2006	0.18µm	1.8	Cascaded 2-2	4	20	62.86	160	42	1.85
				Cascaded 2-2	4	4	75	64	17.8	0.968
				Feedforward-2	2	0.2	83	32	8.3	3.58
(Silva *et al.*, 2009)*	2009	0.18µm	1.8	Cascaded 2-2	4	28	65.9	160	74.6	2.32
				Cascaded 2-2	4	22	63.9	176	74.6	2.63
				Cascaded 2-2	4	3.84	71.2	64	17	1.43
				Cascaded 2-2	4	2	73.7	32	12.7	1.61
				2^{nd} order $\Sigma\Delta$	2	1	76.3	64	6.3	1.18
				2^{nd} order $\Sigma\Delta$	2	0.2	85.7	25.6	4.2	1.33
(Gerosa *et al.*, 2006)*	2006	0.35µm	2.2	Cascaded 2-1	3	22	68	200	18.9	1.3
				Cascaded 2-1	3	3.84	72	91.7	7.4	1.8
				2^{nd} order $\Sigma\Delta$	2	1	81	90	5.5	1.7
				2^{nd} order $\Sigma\Delta$	2	0.2	96	48.6	4.6	1.1
(Burger and Huang, 2001)*	2001	0.25µm	2.5	3^{rd} order $\Sigma\Delta$	3	0.4	72	104	8	6.16
				3^{rd} order $\Sigma\Delta$	3	4	52	184.3	8	6.16
(Miller and Petrie, 2003)*	2003	0.18µm	2.7	2^{nd} order $\Sigma\Delta$	2	1	77	23	30	5.2
(Rusu *et al.*, 2006*b*)*	2003	0.13µm	1.2	Cascaded 2-1	3	3.84	61.7	38.4	4.3	1.13
(Rusu *et al.*, 2006*a*)*	2006	0.18µm	1.8	3^{rd} order FF $\Sigma\Delta$	3	20	54	160	39	4.76
				3^{rd} order FF $\Sigma\Delta$	3	4	77	64	23	0.99
				3^{rd} order FF $\Sigma\Delta$	3	0.2	96	32	18	1.75
(Seyedhosseinzadeh and Yavari, 2012)*	2012	90nm	1	Cascaded 2-2	4	25	76.8	200	37	0.26
				Cascaded 2-1	3	3.84	80.8	62.5	12	0.34
				2^{nd} order $\Sigma\Delta$	2	1	85	62.5	5	0.34
				2^{nd} order $\Sigma\Delta$	2	0.5	89.5	62.5	5	0.41
(Jose *et al.*, 2011)	2009	0.18µm	1.8	Cascaded 2-2-2	4	20	54	200	35	4.27
				Cascaded 2-2	4	2	68	64	20	4.87
				2^{nd} order $\Sigma\Delta$	2	0.2	82	64	11	5.35
(Du and Tiew, 2007)	2007	0.18µm	1.8	Cascaded 2-2-2	6	16	48.5	64	27.5	7.9
				Cascaded 2-2-2	6	4	78.9	64	27.5	0.95
				Cascaded 2-2	4	1	76	64	6.3	1.22
(Bos *et al.*, 2009)	2009	90nm	1.2	Cascaded 2-1 multirate	3	4	65	80	6.83	1.07
				Cascaded 2-1 single rate	3	4	58	80	6.43	2.48
				2^{nd} order $\Sigma\Delta$	2	1	76	90	3.7	0.72
				2^{nd} order $\Sigma\Delta$	2	0.2	77	50	3.43	2.97
(Bilhan and Maloberti, 2009)*	2009	90nm	1.2	Cross 2-path	2	4	56	60	1.56	0.76
(Fakhoury *et al.*, 2009)	2009	65nm	1.2	4-channel Cascaded 2-2	4	25	52	208	110	13.5
(Kuo *et al.*, 2010)	2010	0.18µm	1	Cascaded 2-2	4	0.04	84	2	0.66	1.28

usage of just two same integrators to realize 2^{nd}, 3^{rd} and 4^{th} order NTF responses. Hence, the modulator meets the required performance specifications for six different communication standards while its total area is near the area of a multi-bit 2^{nd} order $\Sigma\Delta$ modulator. The excellent value of FoM of the proposed architecture verifies its feasibility for wide-band multi-standard wireless applications.

5.5 Chapter Summary

An efficient triple-mode hexa-standard reconfigurable TI symmetric cross-coupled $\Sigma\Delta$ modulator is presented in this chapter. The newly introduced dual extended noise cross-coupling technique is incorporated with the proposed architecture to gain power and hardware efficiency. NTFs of order 2^{nd}, 3^{rd} and 4^{th} are obtained by flexible switching between unextended, extended and dual extended noise cross-coupling paths, respectively. An improved peak SNR of 83.4/ 80.2/ 67.8/ 61.5/ 60.8/ 51.03 dB is achieved in the channel bandwidth of 0.2/ 1/ 2/ 3.84/ 22/ 28 MHz for GSM/ Bluetooth/ GPS/ WCDMA/ WLAN/ WiMAX mode with low over-sampling ratio and minimum hardware. The feasibility and efficiency of the cross-coupling technique in low-power multi-standard scenarios can be verified from system-level simulations and Hspice based circuit-level simulations. It consumes only 1.93mW from a 1V power supply. The sensitivities of the proposed model to the finite opamp DC gain, bandwidth, slew rate, channel mismatch and cross-coupled coefficients mismatch have also been analyzed in this chapter.

CHAPTER 6

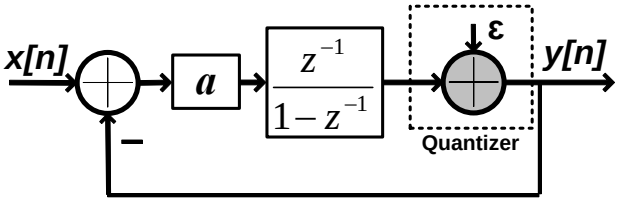
A DIFFERENTIAL QUANTIZER BASED ERROR FEEDBACK MODULATOR FOR ANALOG-TO-DIGITAL CONVERSION

A differential quantizer based error feedback modulator (DQEFM) intended for digitizing analog signals and its comparison to the traditional interpolative $\Sigma\Delta$ analog-to-digital conversion is presented in this chapter. Differential quantizer based error feedback modulator technique can perform well in high-precision and low-power applications. Furthermore, the chapter also describes the design, analysis and implementation of a novel differentially quantized bandpass analog-to-digital conversion technique for digital radio application.

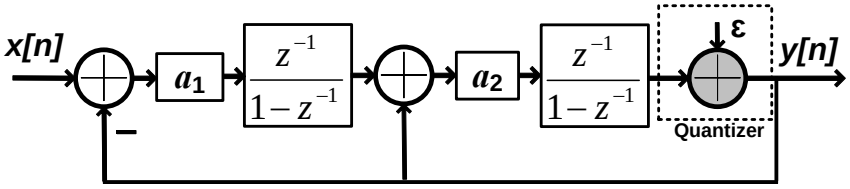
The organization of the chapter is as follows. The traditional $\Sigma\Delta$M is reviewed in Section 6.1. Section 6.2 explores the proposed lowpass DQEFM and its validation using behavioural simulations. Non-ideality analysis and the scalability of the DQEFM to design higher order modulators are illustrated in Section 6.3 and Section 6.4, respectively. Section 6.5 reviews the conventional feedback and feedforward bandpass (BP)-$\Sigma\Delta$M. Section 6.6 presents the proposed BP-DQEFM architecture and its validation using behavioural simulations. Non-ideality analysis and the scalability of the BP-DQEFM approach to design higher order modulators are illustrated in Section 6.7 and Section 6.8, respectively. The switched capacitor (SC) model of the conventional and proposed architecture using Hspice is described in Section 6.9. Finally, Section 6.10 portrays the inferences from this chapter.

6.1 Traditional Sigma Delta Modulator

The generic structure of the first and second order $\Sigma\Delta$M (Boser and Wooley, 1988) is shown in Figure 6.1(a) and Figure 6.1(b), respectively. The signal transfer function (STF), the noise transfer function (NTF) and the overall output of the two architectures,



(a)



(b)

Figure 6.1: Block diagram of the traditional ΣΔM. (a) first order ΣΔM architecture (b) second order ΣΔM architecture (Norsworthy *et al.*, 1997)

with $a = 1$, $a_1 = 0.5$ and $a_2 = 2$ (Maloberti, 2007), are given in Equations (6.1), (6.2), (6.3) and (6.4).

$$STF_{\Sigma\Delta 1} = z^{-1}, \quad NTF_{\Sigma\Delta 1} = 1 - z^{-1} \tag{6.1}$$

$$Y(z)_{\Sigma\Delta 1} = z^{-1}X(z)_{\Sigma\Delta 1} + (1 - z^{-1})E(z)_{\Sigma\Delta 1} \tag{6.2}$$

$$STF_{\Sigma\Delta 2} = z^{-2}, \quad NTF_{\Sigma\Delta 2} = (1 - z^{-1})^2 \tag{6.3}$$

$$Y(z)_{\Sigma\Delta 2} = z^{-2}X(z)_{\Sigma\Delta 2} + (1 - z^{-1})^2E(z)_{\Sigma\Delta 2} \tag{6.4}$$

Here $STF_{\Sigma\Delta i}$, $NTF_{\Sigma\Delta i}$, $X(z)_{\Sigma\Delta i}$, $E(z)_{\Sigma\Delta i}$ and $Y(z)_{\Sigma\Delta i}$ represents STF, NTF, input signal, quantization noise and the final output of the i^{th} order ΣΔM, respectively. The implementation uses delayed integrators with proper gains to get the desired STF and NTF. However, the traditional trade-off between bandwidth and resolution in ADCs, resulting from the submicron CMOS technology limitation, always remain a bottleneck for ΣΔ modulators. The performance of ΣΔM is bounded by the dynamic range of the opamp and output voltage swing of the integrator, which in turn depends on signal magnitude and quantization noise. The problems due to opamp saturation and resulting quantizer over-range will also contribute to performance degradation (Maloberti,

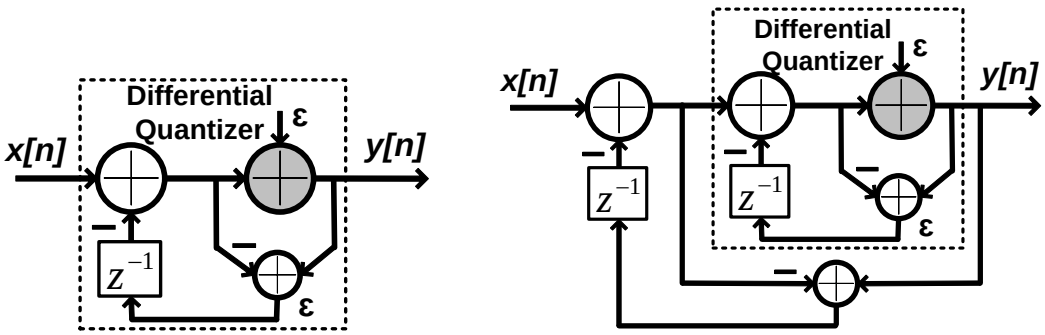


Figure 6.2: Block diagram of the proposed DQEFM. (a) First order DQEFM architecture (b) Second order DQEFM architecture

2007), (Schreier *et al.*, 2005).

6.2 Proposed Differential Quantizer based Error Feedback Modulator (DQEFM) Architecture

The first order DQEFM architecture, which is also the basic building block of this particular domain of proposed DQEF modulators, is illustrated in Figure 6.2(a). Here $x[n]$, $y[n]$ and ε represents input, output and quantization noise sequences. The DQEFM are devoid of integrators, which are replaced by differential quantizer, in order to produce the noise shaping high pass transfer function $(1 - z^{-1})$. The quantization error is extracted from the difference between the input and output of the quantizer, and is fed back to the input of the modulator, hence the name differential quantization. The second order DQEFM architecture, which is built from the basic building block of Figure 6.2(a), is shown in Figure 6.2(b). The STF, NTF and the final output of the first and second order DQEFM is given by Equations (6.5), (6.6), (6.7) and (6.8).

$$STF_{DQ1} = 1, \quad NTF_{DQ1} = 1 - z^{-1} \tag{6.5}$$

$$Y(z)_{DQ1} = X(z)_{DQ1} + (1 - z^{-1})E(z)_{DQ1} \tag{6.6}$$

$$STF_{DQ2} = 1, \quad NTF_{DQ2} = (1 - z^{-1})^2 \tag{6.7}$$

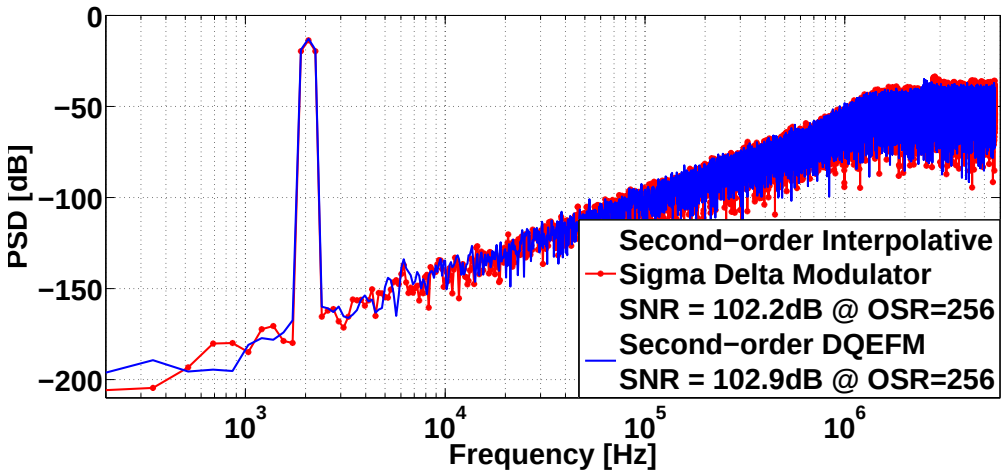


Figure 6.3: Comparison of ideal output spectra

$$Y(z)_{DQ2} = X(z)_{DQ2} + (1 - z^{-1})^2 E(z)_{DQ2} \tag{6.8}$$

Here STF_{DQi}, NTF_{DQi}, $X(z)_{DQi}$, $E(z)_{DQi}$ and $Y(z)_{DQi}$ represents STF, NTF, input signal, quantization noise and the final output of the i^{th} order DQEFM, respectively. The mathematical equivalence can be easily verified by comparing Equations (6.1) and (6.3) with (6.5) and (6.7), respectively. The proposed second order DQEFM, shown in Figure 6.2(b), has been simulated and compared with the traditional interpolative second order $\Sigma\Delta$ counterparts of Figure 6.1(b) using Simulink and the output spectra are plotted in Figure 6.3. An OSR of 256, a 1-bit quantizer and 65536 samples were used for all the simulations. Owing to the presence of large idle tones in the output spectra, first order modulators are usually avoided.

In Table 6.1, the peak signal-to-noise Ratio (SNRp) and overloading level (OL) of the traditional second order $\Sigma\Delta$M and the proposed second order DQEFM, with OSR ranging from 16 to 256, is presented. Though both the architectures matches in SNR performance, the proposed scheme shows significant improvement in overloading levels because the error feedback mechanism recovers the information lost owing to the quantizer overload and hence poses wider dynamic range (Maghari *et al.*, 2008).

The conventional second order $\Sigma\Delta$M of Figure 6.1(b) and the proposed second order DQEFM, shown in Figure 6.2(b), have been simulated using Simulink and plotted the SNR against input magnitude over the range -100 dBFS to 0 dBFS in Figure 6.4. The second order DQEFM shows wider stable dynamic range of 96 dB compared to the second order $\Sigma\Delta$M dynamic range of 90 dB. The feasibility of the proposed DQEFM

Table 6.1: Performance summary of conventional second order ΣΔM and proposed second order DQEFM.

	Traditional second order ΣΔM		Proposed second order DQEFM	
OSR	SNRp (dB)	OL	SNRp (dB)	OL
16	42	0.7	42	0.85
32	57	0.7	57	0.85
64	74	0.7	74	0.85
128	88	0.65	88	0.8
256	103	0.65	103	0.8

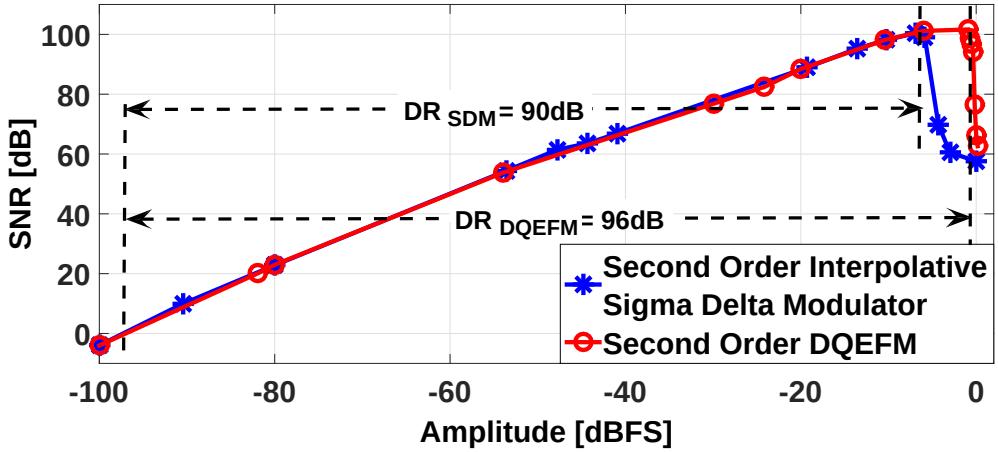


Figure 6.4: SNR variation versus input magnitude for the second order ΣΔM and DQEFM architectures. (SDM represents interpolative sigma delta modulator)

technique is clear from the simulation results and it serves as a best candidate for high-speed, wide-band and low-power applications.

6.3 Non-Ideality Analysis of the DQEFM architecture

The major circuit-level non-idealities that degrades the DQEFM performance are clock jitter ($\Delta\tau$) at the input sampler, finite slew rate (SR), gain bandwidth product (GBW), DC gain, switch thermal noise and opamp noise. To get a precise discrimination with the traditional ΣΔM the behavioural-level noise models of (Malcovati *et al.*, 2003) were used for the analysis.

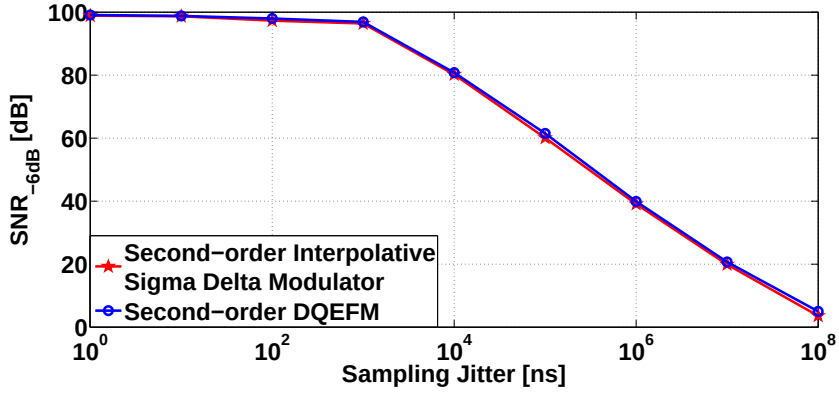
To evaluate the effect of various circuit non-idealities on the proposed second or-

Table 6.2: Non-ideality effects of the proposed second order DQEFM and traditional second order ΣΔM

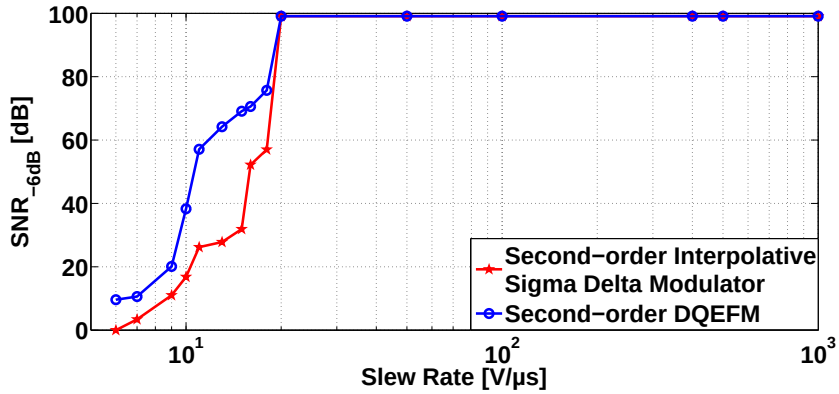
Modulator Parameter	Parameter value	DQEFM SNR_{-6dB}	ΣΔM SNR_{-6dB}
Ideal modulator	-	99.1 dB	99.1 dB
Switch thermal noise	C_s = 1.25 pF	94.9 dB	94 dB
Input referred opamp Noise	V_n = 73 μVrms	94.8 dB	94.8 dB
All non-idealities	Δτ = 16 ns, C_s = 1.25 pF, V_n = 73 μVrms, GBW = 100 MHz, SR = 20 V/μs, A_{dB} = 60 dB	92.4 dB	87.4 dB

der DQEFM, it has been simulated by considering one non-ideality at a time and then the combined effect of all the non-idealities. The sampling frequency used was 11.03 MHz. Input magnitude of -6 dB with reference to the full-scale level is used to compare the SNR (SNR_{-6dB}). Figure 6.5(a) - 6.5(d) compares the SNR performance of the second order DQEFM with the second order interpolative ΣΔM when non-idealities such as sampling jitter, opamp finite SR, finite GBW and finite DC gain are introduced independently.

In Table 6.2, the ideal modulator performance and the effect of switch thermal noise and input referred opamp noise are compared. The modulators show a similar performance and sensitivity to switch thermal noise, input referred opamp noise, input sampling jitter and opamp finite SR, whereas the GBW requirement for the proposed DQEFM scheme is slightly relaxed. The most important aspect of the proposed DQEFM is its low opamp DC gain requirement. A 10-20 dB DC gain is sufficient for DQEFM to achieve the ideal performance whereas the traditional interpolative ΣΔM requires an opamp DC gain of at least 50-60 dB. This is because the opamp serves as a simple voltage follower or a unity gain buffer in DQEFM architecture in contrast to the integrator function in traditional interpolative ΣΔM.



(a)



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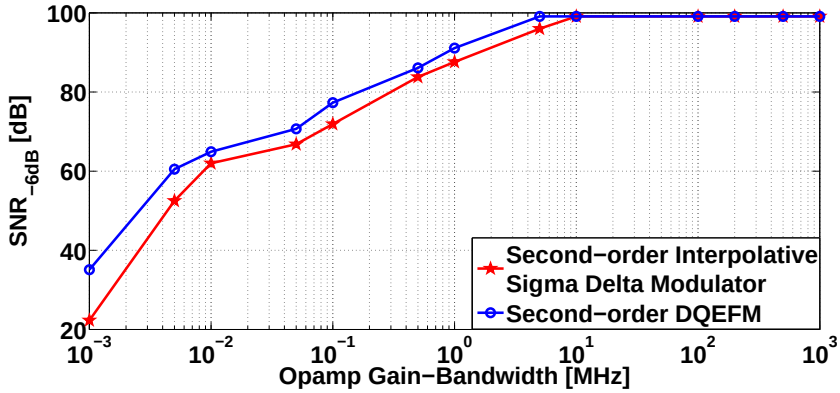
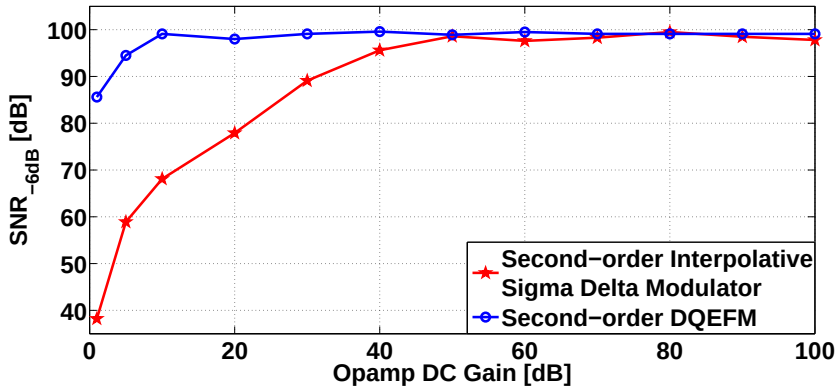


(c)



(d)

Figure 6.5: SNR performance variation with (a) sampling jitter (b) slew rate (c) opamp gain bandwidth (d) opamp DC gain for the second order $\Sigma\Delta$M and DQEFM architectures

The combined impact of all the non-idealities on the SNR performance is obtained by simulating DQEFM with clock jitter ($\Delta\tau$ = 16 ns), switches kT/C noise (Cs = 1.25pF), input referred opamp noise (V_n = 73 μVrms) and an opamp of finite gain bandwidth (GBW = 100 MHz), slew rate (SR = 20 V/μs) and DC gain of 60dB (1e3), and it is compared with second order interpolative $\Sigma\Delta$M, as shown in Figure 6.6.

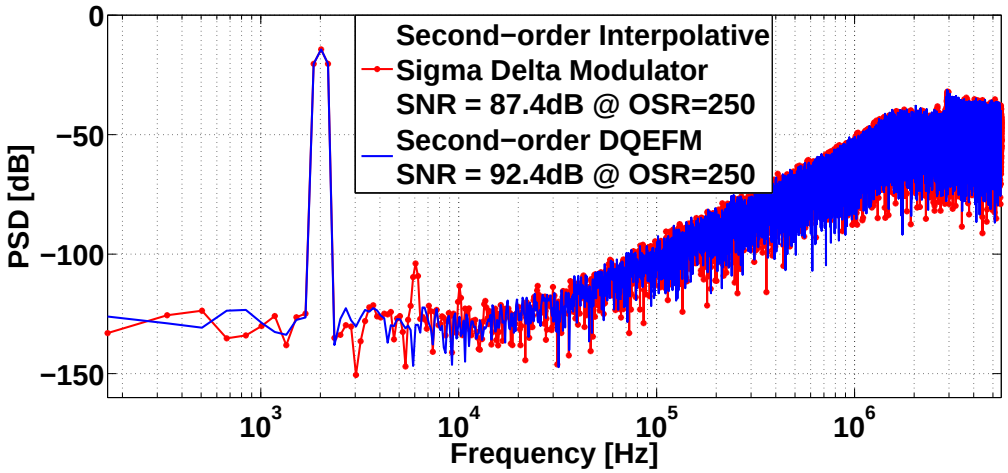


Figure 6.6: Comparison of output spectra considering all the non-idealities

The presence of one non-ideality enhances the impact of other non-idealities due to its additional noise contribution. From Figure 6.6 we can conclude that the presence of non-idealities drastically degrade the $\Sigma\Delta$M performance, compared to the proposed scheme.

6.4 Scalability of the Proposed DQEFM Technique

The feasibility of the DQEFM technique, to design higher order noise shaping converters, is illustrated by implementing MASH 2-1 and MASH 2-2 structures (Hayashi *et al.*, 1986), (Maghari *et al.*, 2006) as demonstrated in Figure 6.7(a) and Figure 6.7(b), respectively.

In both structures the quantization error, ε_1, associated with the first stage of the modulator is fed as the input to the second stage. The output of two stages are combined, using appropriate digital cancellation logic, to obtain the overall output $y[n]$ of the modulator. The quantization error of first stage is completely cancelled during this process and the overall output will contain only the quantization error of second stage

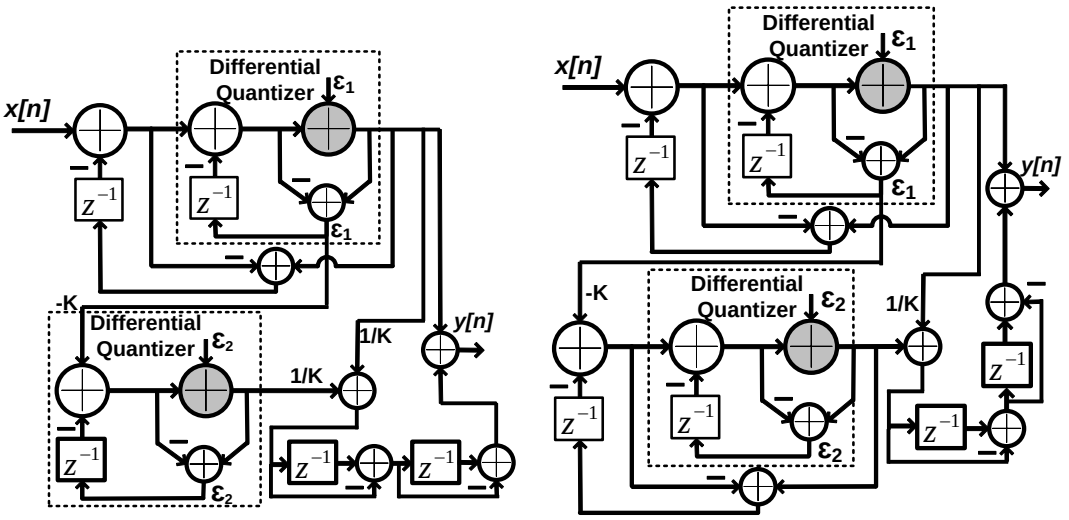


Figure 6.7: Multi-stage noise shaping (MASH) using DQEFM technique. (a) MASH 2-1 DQEFM architecture (b) MASH 2-2 DQEFM architecture

(ε_2). Similarly the STF, NTF and the overall output are given by

$$STF_{DQ21} = 1, \quad NTF_{DQ21} = (1 - z^{-1})^3 \tag{6.9}$$

$$Y(z)_{DQ21} = X(z)_{DQ21} + (1 - z^{-1})^3 E(z)_{DQ21} \tag{6.10}$$

$$STF_{DQ22} = 1, \quad NTF_{DQ22} = (1 - z^{-1})^4 \tag{6.11}$$

$$Y(z)_{DQ22} = X(z)_{DQ22} + (1 - z^{-1})^4 E(z)_{DQ22} \tag{6.12}$$

The output spectra of the MASH 2-1 and the MASH 2-2 DQEFM architectures are depicted in Figure 6.8.

In Table 6.3, the SNRp and overloading level (OL) of the traditional MASH 2-1 and MASH 2-2 $\Sigma\Delta$M and the corresponding proposed DQEFM, with OSR ranging from 16 to 256, is presented. Hence the proposed DQEFM architecture is a better replacement for interpolative $\Sigma\Delta$Ms with a wide range of advantages and can be exploited to any extent by utilizing the knowledge of $\Sigma\Delta$M.

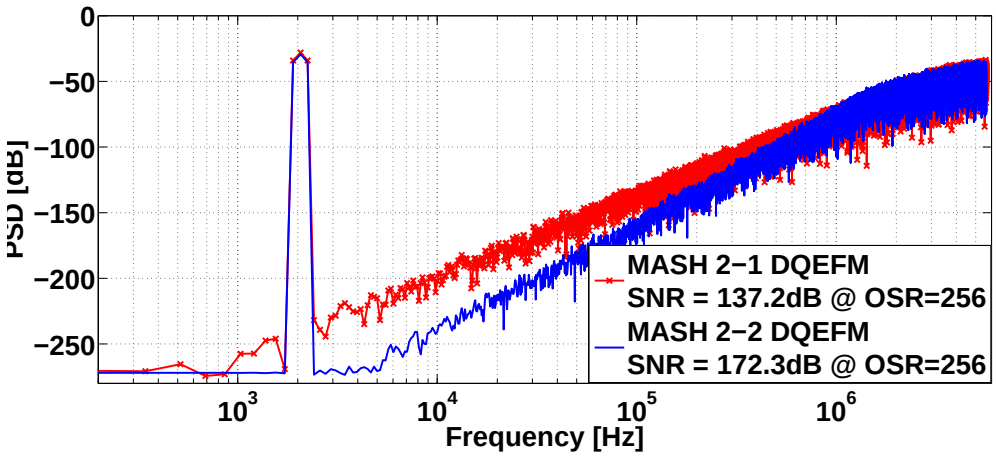


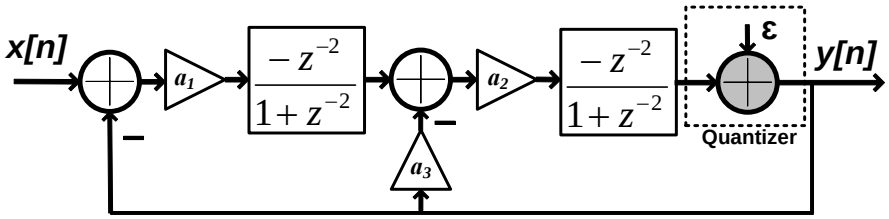
Figure 6.8: Comparison of output spectra of the MASH 2-1 and the MASH 2-2 DQEFM

Table 6.3: Performance summary of MASH 2-1 and MASH 2-2 $\Sigma\Delta$ modulator, and corresponding DQEFM

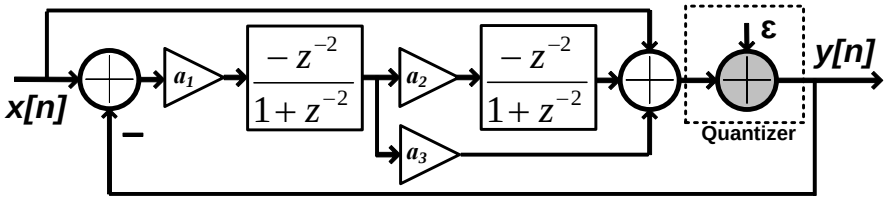
	Traditional $\Sigma\Delta$ modulator				Proposed DQEFM			
	MASH 2-1		MASH 2-2		MASH 2-1		MASH 2-2	
OSR	SNRp (dB)	OL	SNRp (dB)	OL	SNRp (dB)	OL	SNRp (dB)	OL
16	56	0.75	64	0.7	56	0.8	64	0.8
32	77	0.7	92	0.7	77	0.8	92	0.8
64	96	0.7	119	0.65	96	0.8	119	0.75
128	119	0.65	144	0.6	119	0.8	144	0.75
256	138	0.65	171	0.6	138	0.75	171	0.7

6.5 Conventional Bandpass Sigma Delta Modulator

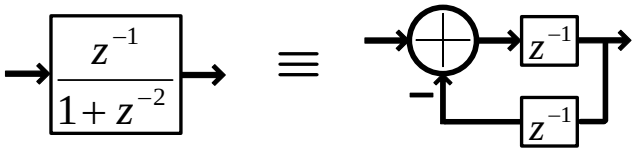
The BP-$\Sigma\Delta$M is derived from the lowpass (LP) prototype, by applying the transformation $z^{-1} \Rightarrow -z^{-2}$ (Norsworthy *et al.*, 1997), (Rabiner and Gold, 1975). The resonator forms the basic building block of traditional BP-$\Sigma\Delta$M and a typical BP resonator with double delay from input to output can be expressed as $-z^{-2}/(1+z^{-2})$. The simple integrators in the LP-$\Sigma\Delta$Ms are replaced by resonators and the frequency range around DC ($z=1$) will be mapped to $f_s/4$ ($z=i$), as a result of this transformation (Momeni *et al.*, 2008). The basic block diagram of the conventional second order feed-back BP-$\Sigma\Delta$M (BP-FB$\Sigma\Delta$M) (Jantzi *et al.*, 1993), (Longo and Horng, 1993) is shown in Figure 6.9(a).



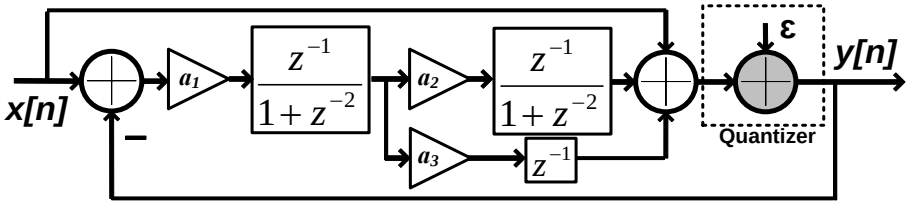
(a)



(b)



(c)



(d)

Figure 6.9: Block diagram of the (a) conventional second order BP- FBΣΔM (b) conventional second order BP- FFΣΔM (c) two-delay-loop resonator (d) conventional second order BP- FFΣΔM using two-delay-loop resonator.

The STF, NTF and the overall output of the second order BP-FB$\Sigma\Delta$M, with a_1 = 0.5, a_2 = 2 and a_3 = 1 (Song, 1995), are given by,

$$STF_{BPFB\Sigma\Delta2} = z^{-4}, \quad NTF_{BPFB\Sigma\Delta2} = (1+z^{-2})^2 \tag{6.13}$$

$$Y(z)_{BPFB\Sigma\Delta2} = z^{-4}X(z)_{BPFB\Sigma\Delta2} + (1+z^{-2})^2 E(z)_{BPFB\Sigma\Delta2} \tag{6.14}$$

Here the terms $STF_{BPFB\Sigma\Delta i}$, $NTF_{BPFB\Sigma\Delta i}$, $X(z)_{BPFB\Sigma\Delta i}$, $E(z)_{BPFB\Sigma\Delta i}$ and $Y(z)_{BPFB\Sigma\Delta i}$ represents STF, NTF, input signal, quantization error and the overall output of the i^{th} order BPFB-$\Sigma\Delta$M, respectively. Figure 6.9(b) shows the conventional second order feedforward BP-$\Sigma\Delta$M (BP-FF$\Sigma\Delta$M). A highly linear $\Sigma\Delta$M operation is achieved by the feedforward architecture (Rusu and Ismail, 2005), since the resonator processes only the quantization noise. The overall output of BP-FF$\Sigma\Delta$M is given by

$$\begin{aligned} Y(z)_{BPFF\Sigma\Delta2} =& X(z)_{BPFF\Sigma\Delta2} + \\ & \frac{(1+z^{-2})^2}{[1+(2-a_1a_3)z^{-2}+(1+a_1a_2-a_1a_3)z^{-4}]} E(z)_{BPFF\Sigma\Delta2} \end{aligned} \tag{6.15}$$

Here the terms $X(z)_{BPFF\Sigma\Delta i}$, $E(z)_{BPFF\Sigma\Delta i}$ and $Y(z)_{BPFF\Sigma\Delta i}$ represents input signal, quantization error and the overall output of the i^{th} order BP-FF$\Sigma\Delta$M, respectively. At circuit-level, the relaxed settling time requirements make a two-delay-loop (TDL) resonator (Momeni *et al.*, 2008), (Keskin *et al.*, 2003), shown in Figure 6.9(c), far superior to integrator based implementation. The proposed differential quantizer technique, which is discussed in the following section, also uses double-delay based circuit implementation. Hence, to have a uniformity and fairness in the analysis the conventional BP-FF$\Sigma\Delta$M is modified with TDL resonator as demonstrated in Figure 6.9(d). The overall output of the BP-FF$\Sigma\Delta$M is modified as

$$\begin{aligned} Y(z)_{BPFF\Sigma\Delta2} =& X(z)_{BPFF\Sigma\Delta2} + \\ & \frac{(1+z^{-2})^2}{[1+(2-a_1a_2-a_1a_3)z^{-2}+(1-a_1a_3)z^{-4}]} E(z)_{BPFF\Sigma\Delta2} \end{aligned} \tag{6.16}$$

The coefficient values a_1 = 0.5, a_2 = 0.5 and a_3 = 1 for Equation (6.15) and a_1 = -0.5, a_2 = 0.5 and a_3 = 0.5 for Equation (6.16) results in the same STF and NTF. The implementation of conventional BP resonators follows biquad approach which needs two opamps (Singor and Snelgrove, 1995; Schreier and Snelgrove, 1989; Jantzi *et al.*, 1991, 1993). However, there are single opamp resonator implementations utilizing multi-clock phase sampling and correspondingly higher sampling rate (Francesconi *et al.*, 1995).

The conventional trade-off between bandwidth and resolution in ADCs, resulting from the submicron CMOS technology limitation, always remain a bottleneck for $\Sigma\Delta$ modulators. The performance of $\Sigma\Delta$M is limited by the dynamic range of the opamp and output voltage swing of the integrator, which depends on signal amplitude and quantization noise. The problems due to opamp saturation and resulting quantizer overrange will also contribute to performance degradation (Maloberti, 2007), (Schreier *et al.*, 2005).

6.6 Proposed Differential Quantizer based Bandpass Error Feedback Modulator Architecture

The first-order LP-DQEFM architecture, which is also the basic building block of this particular domain of proposed DQEF modulators, is illustrated in Figure 6.10(a). Here $x[n]$, $y[n]$, a and ε represents input, output, scaling coefficient and quantization noise sequences. The second order LP-DQEFM architecture, which is built from the basic building block of Figure 6.10(a), is shown in Figure 6.10(b). The DQEFMs are devoid of integrators/resonators, which are replaced by differential quantizer, in order to generate the noise shaping transfer function, that is, $(1 - z^{-1})$ in the case of first-order LP-DQEFM and $(1 + z^{-2})$ in the case of first-order differential quantizer based bandpass error feedback modulator (BP-DQEFM). The first and second-order BP-DQEFM architectures are depicted in Figure 6.10(c) and Figure 6.10(d). The quantization error is extracted from the difference between the input and output of the quantizer, and is fed back to the input of the modulator, hence the name differential quantization. The error feedback mechanism recovers the information lost owing to the quantizer overload and hence poses wider dynamic range (Maghari *et al.*, 2008). In order to realize the

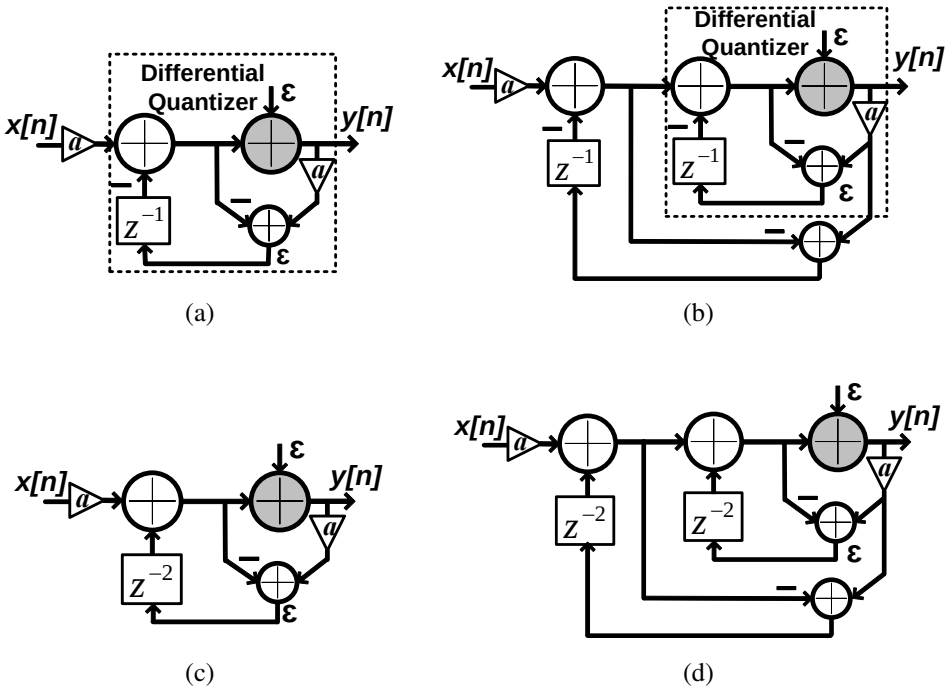


Figure 6.10: Block diagram of the proposed DQEFM (a) first order LP-DQEFM architecture (b) second order LP-DQEFM architecture (c) first order BP-DQEFM architecture (d) second order BP-DQEFM architecture

noise shaping characteristics, the fed-back quantization error is delayed by one clock cycle for LP-DQEFM and two clock cycles for the BP-case, as illustrated in Figure 6.10. The scaling coefficient (a) is introduced to limit the signal level at each and every node within the supply rails and thereby ensure stability. The STF, NTF and the overall output for the LP and BP-DQEFM, both first and second order, are given by Equations (6.17), (6.18), (6.19), (6.20), (6.21), (6.22), (6.23) and (6.24). A unity scaling coefficient ($a = 1$) is considered for deriving these equations.

$$STF_{LPDQ1} = 1, \quad NTF_{LPDQ2} = 1 - z^{-1} \tag{6.17}$$

$$Y(z)_{LPDQ1} = X(z)_{LPDQ1} + (1 - z^{-1})E(z)_{LPDQ1} \tag{6.18}$$

$$STF_{LPDQ2} = 1, \quad NTF_{LPDQ2} = (1 - z^{-1})^2 \tag{6.19}$$

$$Y(z)_{LPDQ2} = X(z)_{LPDQ2} + (1 - z^{-1})^2 E(z)_{LPDQ2} \tag{6.20}$$

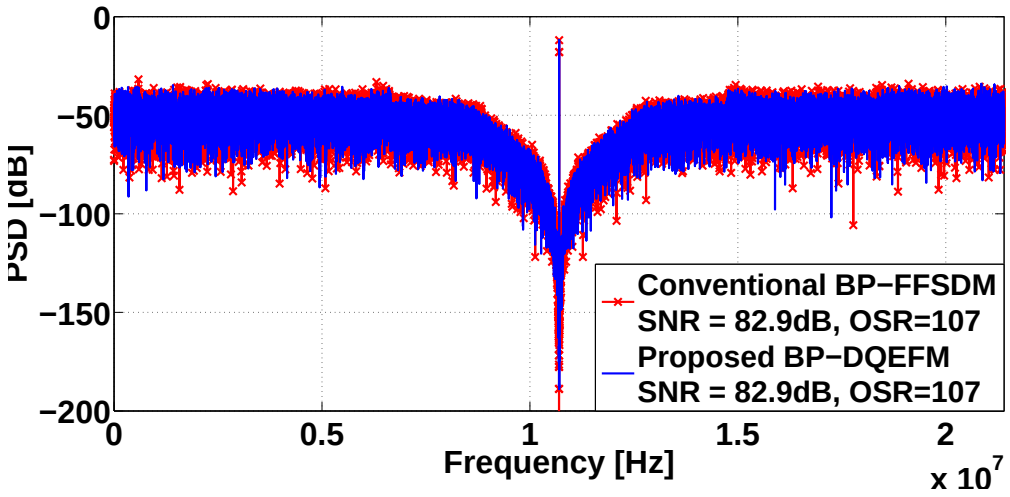


Figure 6.11: Comparison of ideal output spectra

$$STF_{BPDQ1} = 1, \quad NTF_{BPDQ1} = 1 + z^{-2} \tag{6.21}$$

$$Y(z)_{BPDQ1} = X(z)_{BPDQ1} + (1 + z^{-2})E(z)_{BPDQ1} \tag{6.22}$$

$$STF_{BPDQ2} = 1, \quad NTF_{BPDQ2} = (1 + z^{-2})^2 \tag{6.23}$$

$$Y(z)_{BPDQ2} = X(z)_{BPDQ2} + (1 + z^{-2})^2 E(z)_{BPDQ2} \tag{6.24}$$

Here STF_{LPDQi}, NTF_{LPDQi}, $X(z)_{LPDQi}$, $E(z)_{LPDQi}$ and $Y(z)_{LPDQi}$ represents STF, NTF, input signal, quantization error and the output of the i^{th} order LP-DQEFM, respectively, and STF_{BPDQi}, NTF_{BPDQi}, $X(z)_{BPDQi}$, $E(z)_{BPDQi}$ and $Y(z)_{BPDQi}$ represents the corresponding terms in the BP-DQEFM architecture. The mathematical equivalence to BP-$\Sigma\Delta$Ms can be easily verified by comparing Equation (6.14) with (6.24). The proposed second order BP-DQEFM, shown in Figure 6.10(d), has been simulated and compared with the conventional feedforward second order BP-$\Sigma\Delta$ counterparts of Figure 6.9 using Simulink and the output spectra are plotted in Figure 6.11. The conventional BP-FF$\Sigma\Delta$M, using TDL resonator of Figure 6.10(c), were chosen (Momeni *et al.*, 2008), (Keskin *et al.*, 2003). An OSR of 107, scaling coefficient a = 0.25, a 1-bit quantizer, and 65536 samples were used for all the simulations. In the case of multi-bit quantizer, the signal to the quantizer must be amplified by $1/a$ or a suitable coefficient value so as to avoid quantizer overloading.

Table 6.4: Performance summary of conventional BP-ΣΔM and proposed BP-DQEFM

	Conventional second order BP-ΣΔM		Proposed second order BP-DQEFM	
OSR	SNRp (dB)	OL	SNRp (dB)	OL
16	42	0.85	42	0.85
32	57	0.9	57	0.93
64	74	0.95	74	0.95
128	88	0.9	88	0.85
256	103	0.7	103	0.7

In Table 6.4, the SNRp and overloading level (OL) of the conventional second order BP-ΣΔM and the proposed second order BP-DQEFM, with OSR ranging from 16 to 256, is presented. Both the architectures have similar SNR performance and overloading levels.

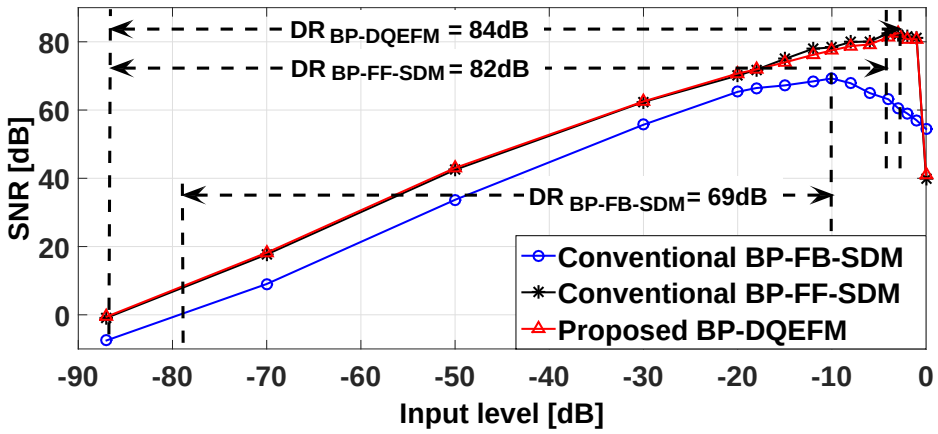


Figure 6.12: SNR performance variation with input signal amplitude for the second order conventional BP-FBΣΔM, conventional BP-FFΣΔM and proposed BP-DQEFM architectures

The conventional second order BP-FBΣΔM of Figure 6.9(a), conventional second order BP-FFΣΔM of Figure 6.9(d) and the proposed second order BP-DQEFM, shown in Figure 6.10(d), have been simulated using Simulink and plotted the SNR against input amplitude swept from -100 dB to 0 dB in Figure 6.12. The conventional second order FBΣΔM has a dynamic range of only 69 dB, whereas the proposed second order BP-DQEFM shows a slightly wider stable dynamic range of 84 dB compared to the 82 dB dynamic range of the conventional second order FFΣΔM. The efficiency and feasibility of the proposed DQEFM technique is clear from the simulation results.

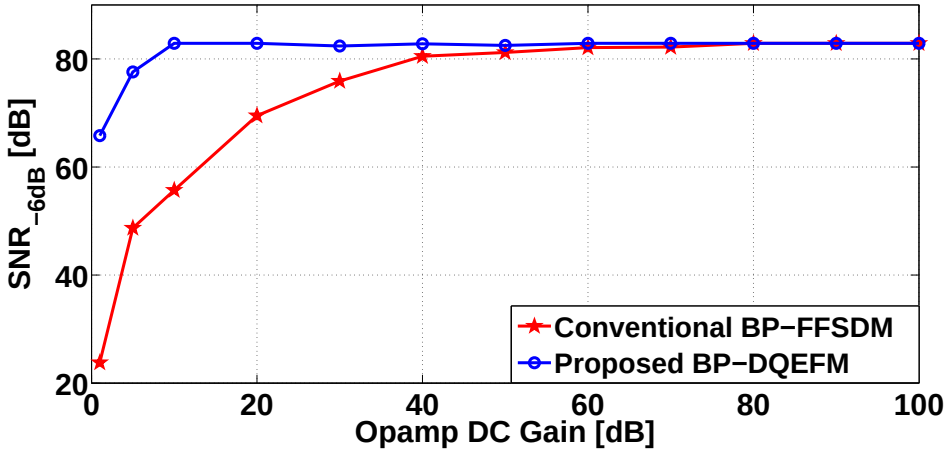


Figure 6.13: SNR performance variation with opamp finite DC gain for the second order conventional BP-FF$\Sigma\Delta$M and proposed BP-DQEFM architectures

6.7 Non-Ideality Analysis of the Bandpass Architecture

The major non-idealities that affect the performance of switched capacitor (SC) BP-DQEFM are clock jitter ($\Delta\tau$) at the input sampler, finite slew rate (SR), gain bandwidth product (GBW), DC gain, switch thermal noise and opamp noise. In order to have a fair comparison with the conventional BP-$\Sigma\Delta$M the behavioural-level noise models of (Brigati *et al.*, 2000) were used. To evaluate the effect of various circuit non-idealities on the proposed second order BP-DQEFM, it has been simulated by considering one non-ideality at a time and then the combined effect of all the non-idealities. The sampling frequency used was 42.8 MHz and the scaling coefficient was chosen to be a = 0.25. Input amplitude of -6 dB with reference to the full-scale level is used to compare the SNR (SNR_{-6dB}). In Table 6.5, the ideal modulator performance and the effect of various circuit non-idealities are compared. The modulators show a similar performance and sensitivity to switch thermal noise, input referred opamp noise, input sampling jitter, opamp finite SR and finite GBW. Figure 6.13 compares the SNR performance of the second order BP-DQEFM with the second order BP-FF$\Sigma\Delta$M when finite DC gain is introduced independently. The most important aspect of the proposed DQEFM is its low opamp DC gain requirement. A 10-20 dB DC gain is sufficient for BP-DQEFM to achieve the ideal performance whereas the conventional BP-FF$\Sigma\Delta$M requires an opamp DC gain of at least 50-60 dB. This is because the opamp serves as a simple SC sample and hold (S/H) or a unity gain buffer in DQEFM architecture in contrast to the integrator/resonator function in conventional $\Sigma\Delta$Ms. The combined impact of all the non-idealities on the SNR performance is obtained by simulating DQEFM

Table 6.5: Non-ideality effects of the proposed BP-DQEFM and conventional BP-FFΣΔM

Modulator Parameter	Parameter value	BP-DQEFM SNR_{-6dB}	BP-ΣΔM SNR_{-6dB}
Ideal modulator	-	82.9 dB	82.9 dB
Sampling jitter	$\Delta\tau$ = 8 ns	64.8 dB	64.8 dB
Switch thermal noise	C_s = 0.5 pF	80.4 dB	79.9 dB
Input referred opamp noise	V_n = 4.4 mV_{rms}	58.6 dB	58. 4dB
Opamp finite bandwidth	GBW = 250 MHz	81.9 dB	81.9 dB
Opamp finite slew rate	SR = 280 V/µs	81.9 dB	81.9 dB
Saturation voltage	Vmax = $\pm$1 V	81.9 dB	81.9 dB
Opamp finite DC gain	A_{dB} = 60 dB	81.9 dB	80.4 dB
All non-idealities	$\Delta\tau$ = 8 ns, C_s = 0.5 pF, V_n = 4.4 mV_{rms}, GBW = 250 MHz, SR = 280 V/µs, A_{dB} = 60 dB	57.5 dB	57.4 dB

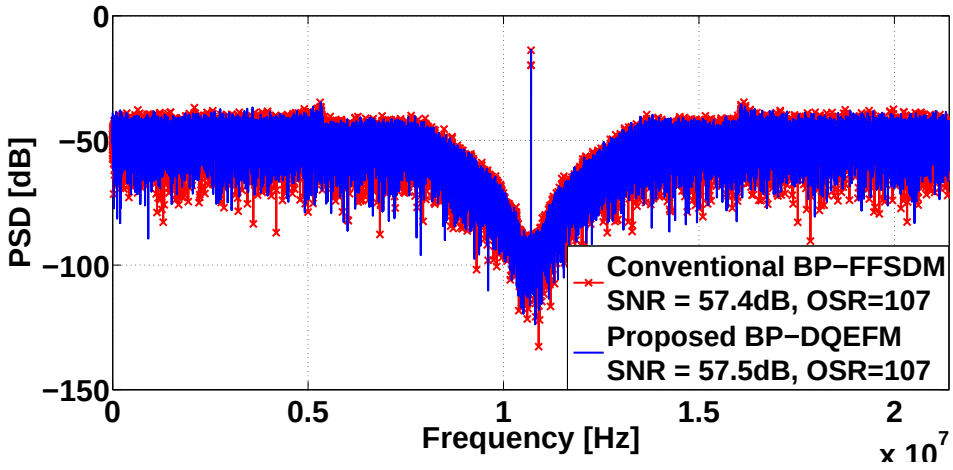
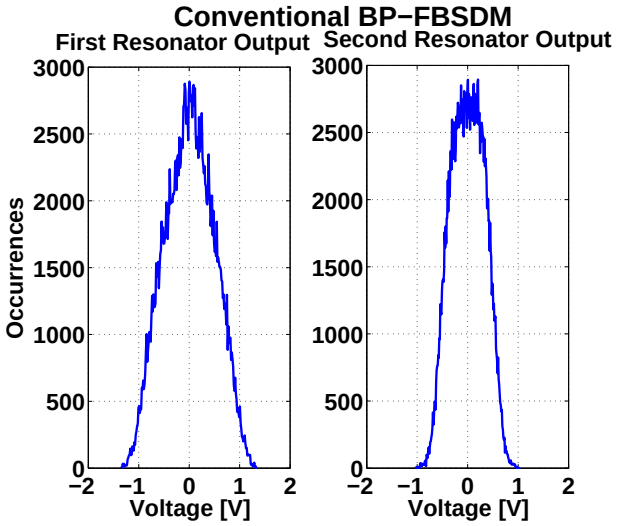


Figure 6.14: Comparison of output spectra considering all the non-idealities

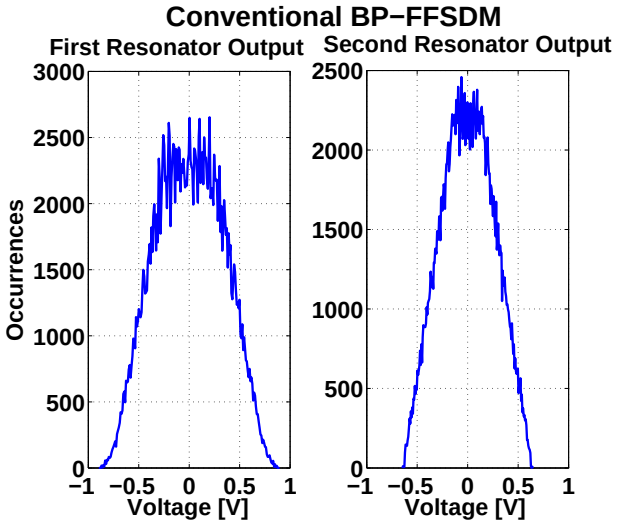
with clock jitter ($\Delta\tau$ = 8 ns), switches kT/C noise (C_s = 0.5 pF), input referred opamp noise (V_n = 4.4 mV_{rms}) and an opamp of finite gain bandwidth (GBW = 250 MHz), slew rate (SR = 280 V/µs) and gain (A_{dB} = 60 dB), and it is compared with the second order BP-FF$\Sigma\Delta$M, as shown in Figure 6.14. The presence of one non-ideality enhances the impact of other non-idealities due to its additional noise contribution. From Figure 6.14 we can conclude that the presence of non-idealities degrades the performance of BP-FF$\Sigma\Delta$M and BP-DQEFM in a similar way.

In order to have an overview about the output swings and stability, the simulated output histograms for the conventional BP-FB$\Sigma\Delta$M, conventional BP-FF$\Sigma\Delta$M and proposed BP-DQEFM are compared in Figures 6.15(a) - 6.15(c), respectively. In the case of $\Sigma\Delta$Ms, resonator output histograms were taken, whereas for DQEFMs the forward path adder output histograms were considered as they are devoid of resonators. Intuitively, the first resonator/adder poses the most critical opamp in the architecture for which the output swing is expected to be relaxed to a greater extent. This is necessary to suppress the non-linearity and overloading in low-power supply $\Sigma\Delta$Ms. In this view, the proposed BP-DQEFM shows better result with significant reduction in the output swing, as can be verified from Figures 6.15(a) - 6.15(c). The output swing of the second resonator/adder is limited to ± 1 V for all the three architectures.

The open-loop DC gain non-linearity of the opamp contributes harmonic distortion in the modulator output spectrum, which limits the SNRp at large signal levels. Figures 6.16(a) - 6.16(c) compares the influence of this gain non-linearity on the modulator output spectra for the conventional BP-FB$\Sigma\Delta$M, conventional BP-FF$\Sigma\Delta$M and proposed BP-DQEFM when a 5% non-linearity is introduced. Conventional BP-FB$\Sigma\Delta$M is the most affected one with a third-order harmonic component at -79.11 dB below the signal amplitude, as shown in the spectrum of Figure 6.16(a). Figure 6.16(b) shows the case of conventional BP-FF$\Sigma\Delta$M, where the harmonic component is reduced to -111.9 dB, since the resonator processes only the quantization noise (Rusu and Ismail, 2005). The proposed BP-DQEFM shows the most suppressed tonal characteristics at -112.9 dB, as shown in the spectrum of Figure 6.16(c). Hence, the reduced output swing makes proposed BP-DQEFM architecture least sensitive to opamp DC gain non-linearity.



(a)



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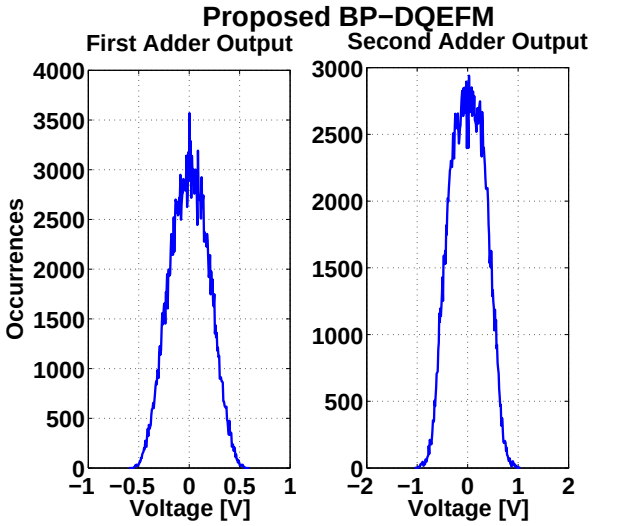
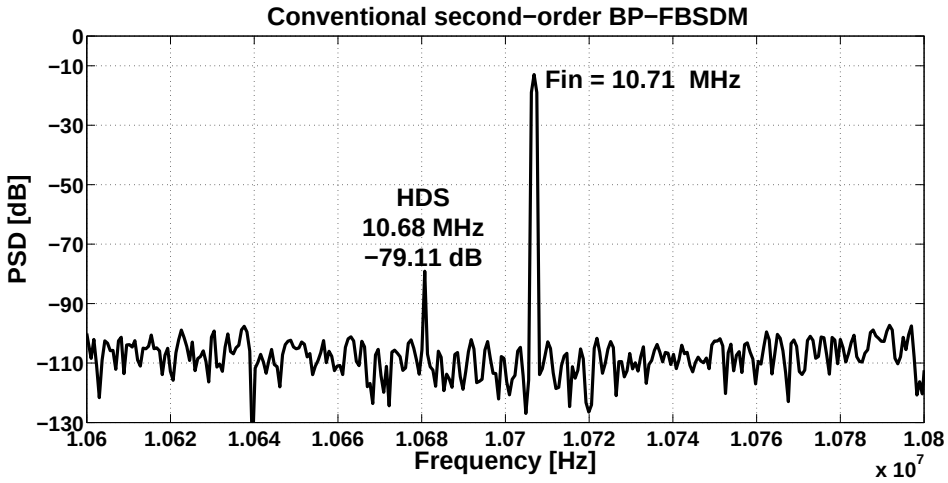
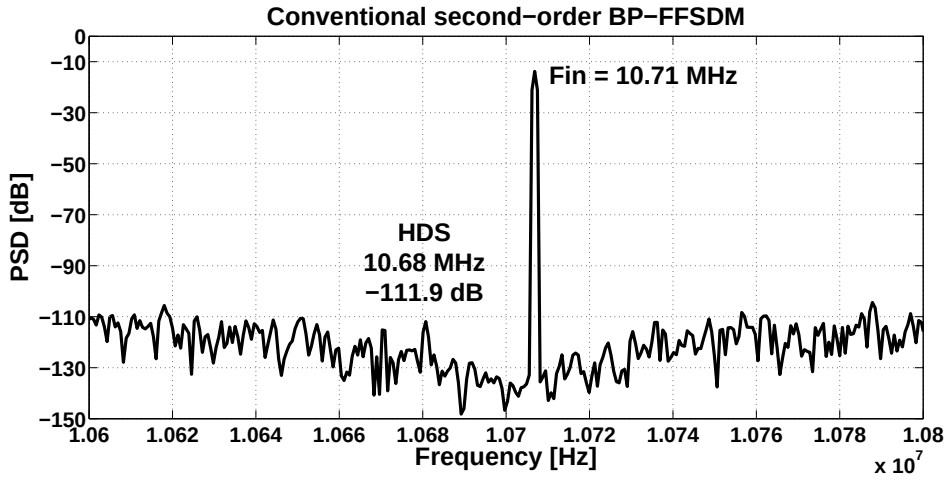


(c)

Figure 6.15: Output histograms (a) conventional BP-FB$\Sigma\Delta$M (b) conventional BP-FF$\Sigma\Delta$M (c) proposed BP-DQEFM



(a)



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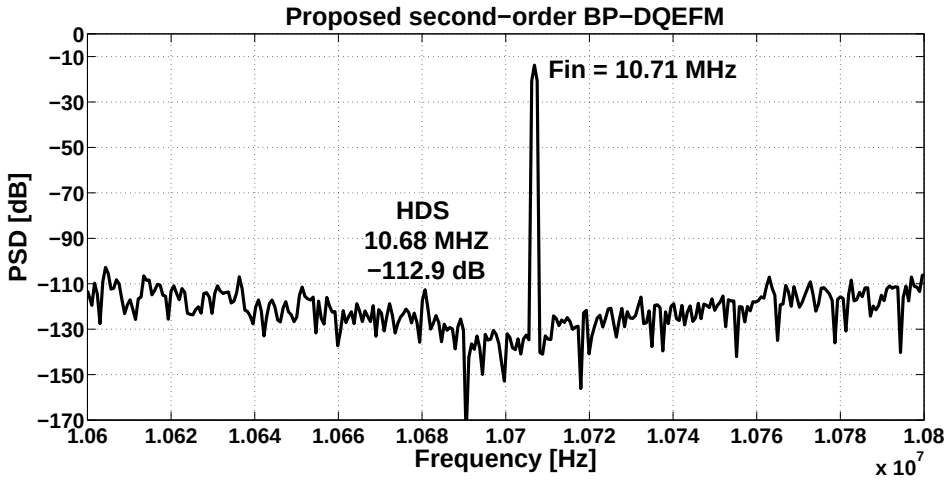


(c)

Figure 6.16: Output spectrum with 5% opamp gain non-linearity of second order (a) conventional BP-FB$\Sigma\Delta$M (b) conventional BP-FF$\Sigma\Delta$M (c) proposed BP-DQEFM

6.8 Scalability of the Proposed BP-DQEFM Technique

The feasibility of the BP-DQEFM technique, to design higher order noise shaping converters, is illustrated by implementing bandpass MASH (BP-MASH) 2-1 and BP-MASH 2-2 structures (Schreier *et al.*, 2005), (Maghari *et al.*, 2006) as demonstrated in Figure 6.17(a) and Figure 6.17(b). In both structures the quantization error, ε_1, associated with the first stage of the modulator is fed as the input to the second stage. The output of two stages are combined, using appropriate digital cancellation logic, to obtain the overall output $y[n]$ of the modulator. The quantization error of first stage is completely cancelled during this process and the overall output will contain only the second stage quantization error (ε_2). As shown in Figure 6.10(a) - 6.10(d) scaling coefficient can be introduced in BP-MASH also to limit the signal level fairly well below the supply rails. The STF, NTF and the overall output are given by

$$STF_{BPDQ21} = 1, \quad NTF_{BPDQ21} = (1 + z^{-2})^3 \tag{6.25}$$

$$Y(z)_{BPDQ21} = X(z)_{BPDQ21} + (1 + z^{-2})^3 E(z)_{BPDQ21} \tag{6.26}$$

$$STF_{BPDQ22} = 1, \quad NTF_{BPDQ22} = (1 + z^{-2})^4 \tag{6.27}$$

$$Y(z)_{BPDQ22} = X(z)_{BPDQ22} + (1 + z^{-2})^4 E(z)_{BPDQ22} \tag{6.28}$$

The output spectra of the BP-MASH 2-1 and the BP-MASH 2-2 DQEFM architectures are depicted in Figure 6.18. In Table 6.6, the SNRp and OL of the MASH 2-1 and MASH 2-2 for the conventional $\Sigma\Delta$M and the proposed DQEFM, with OSR ranging from 16 to 256 is presented.

Hence the proposed BP-DQEFM architecture is the most efficient replacement for BP-$\Sigma\Delta$Ms with a wide range of advantages and can be exploited to any extent by utilizing the knowledge of $\Sigma\Delta$M.

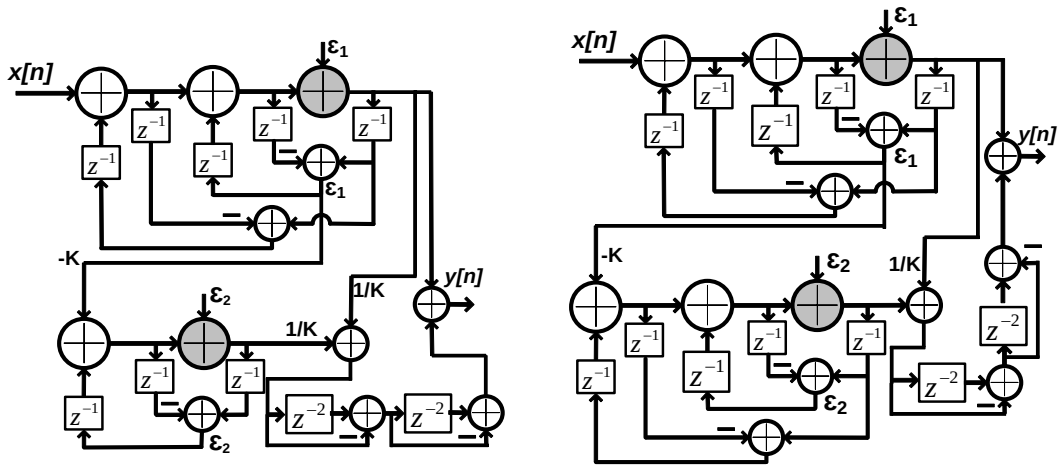


Figure 6.17: BP-MASH using DQEFM technique (a) BP-MASH 2-1 DQEFM architecture (b) BP-MASH 2-2 DQEFM architecture

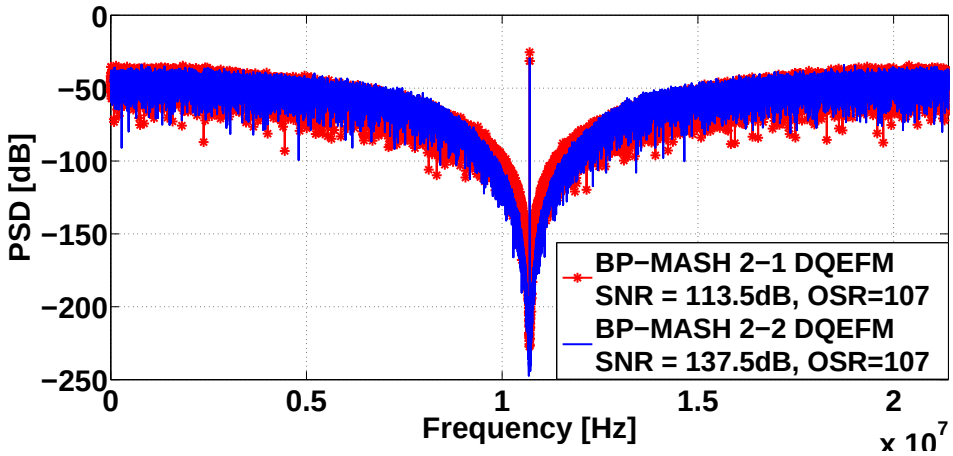


Figure 6.18: Comparison of output spectra of the BP-MASH 2-1 and the BP-MASH 2-2 DQEFM

Table 6.6: Performance summary of the conventional BP-MASH 2-1 and BP-MASH 2-2 $\Sigma\Delta$M and the corresponding Proposed DQEFM

	Conventional BP-MASH-$\Sigma\Delta$M				Proposed BP-MASH-DQEFM			
	MASH 2-1		MASH 2-2		MASH 2-1		MASH 2-2	
OSR	SNRp (dB)	OL	SNRp (dB)	OL	SNRp (dB)	OL	SNRp (dB)	OL
16	56	0.85	64	0.6	56	0.85	64	0.6
32	77	0.8	92	0.6	77	0.8	92	0.6
64	98	0.75	119	0.55	98	0.8	119	0.6
128	119	0.75	145	0.55	119	0.78	145	0.6
256	140	0.7	171	0.55	142	0.75	171	0.55

6.9 Circuit-Level Implementation

A folded-cascode opamp configuration with a class AB output buffer, which is the OTA, shown in Figure 4.6 (Baker, 2008), is used to build the integrators, voltage followers and switched capacitor (SC) sample and hold (S/H) circuit. Table 4.3 shown in the earlier chapter gives the performance summary of the OTA. It has a gain of 75 dB, unity gain-bandwidth of 144 MHz and a phase margin of 60 degree.

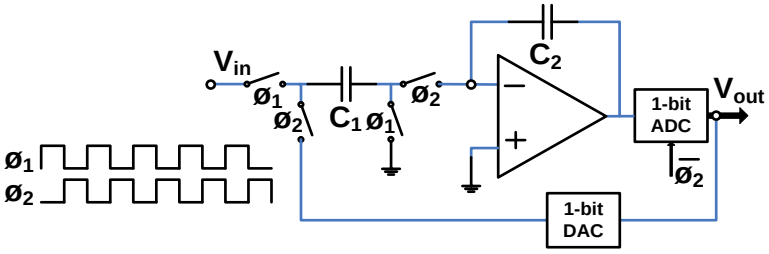
The single-ended SC based circuit-level implementation of the traditional interpolative $\Sigma\Delta$M modulator and the proposed DQEFM, first order and second order, are shown in Figures 6.19(a) - 6.19(d).

A wide swing clocked comparator (one bit ADC), which uses long-length MOSFETs, were used to get a better immunity to kick-back noise (Baker, 2008). The preamplifier associated with the clocked comparator and the switch provided at the input to the comparator isolates the feedback switches and capacitance from the clocked comparator (Maghari *et al.*, 2008), (Johns and Martin, 2008) and thus eliminates kick-back noise. The complete circuit was simulated in 45 nm CMOS process, with a supply of 1V. An OSR of 256 and a 1-bit quantizer were used for the simulation. The two non-overlapping clock phases, 1 and 2, were used to operate the SC model. The clock frequency was set as 11.3 MHz. Any imperfections associated with the analog subtraction and analog loop filter can be compensated by tuning the feedback capacitances, C_{f1} and C_{f2}.

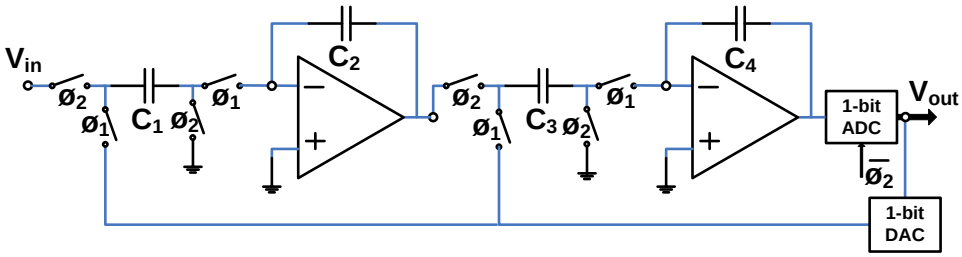
A sinusoid of frequency 2 kHz with a bandwidth 22.05 kHz was considered as the input. The SC models has been simulated using Hspice in 45nm CMOS process with a power consumption of 0.22mW and 0.50mW for the first and second order DQEFM, respectively, and the output spectra of second order $\Sigma\Delta$M and DQEFM are depicted in Figure 6.20.

The single-ended SC based circuit-level implementation of the TDL resonator (Momeni *et al.*, 2008), (Keskin *et al.*, 2003), the conventional second order BP-FF$\Sigma\Delta$M using TDL resonator and the proposed second order BP-DQEFM are shown in Figure 6.21(a), Figure 6.21(b) and Figure 6.21(c), respectively.

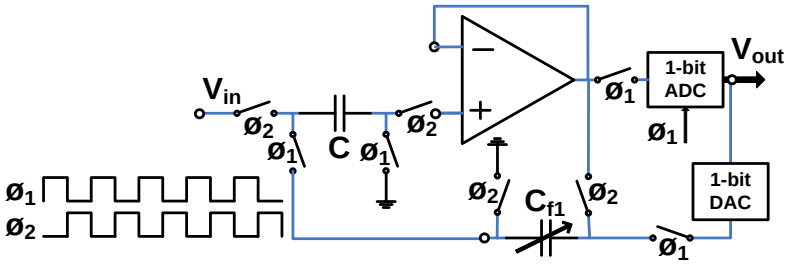
The SC half-delayed S/H circuit (Momeni *et al.*, 2008), shown in dotted line box of



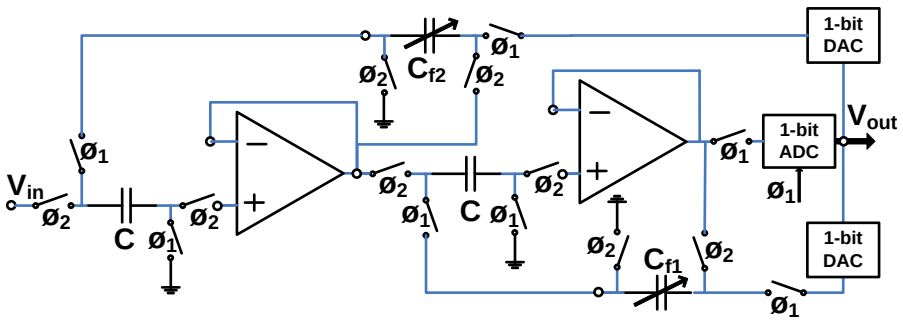
(a)



(b)



(c)



(d)

Figure 6.19: Switched-capacitor circuit implementation of (a) first order interpolative ΣΔM (b) second order interpolative ΣΔM (c) first order DQEFM (d) second order DQEFM (single-ended is shown for simplicity)

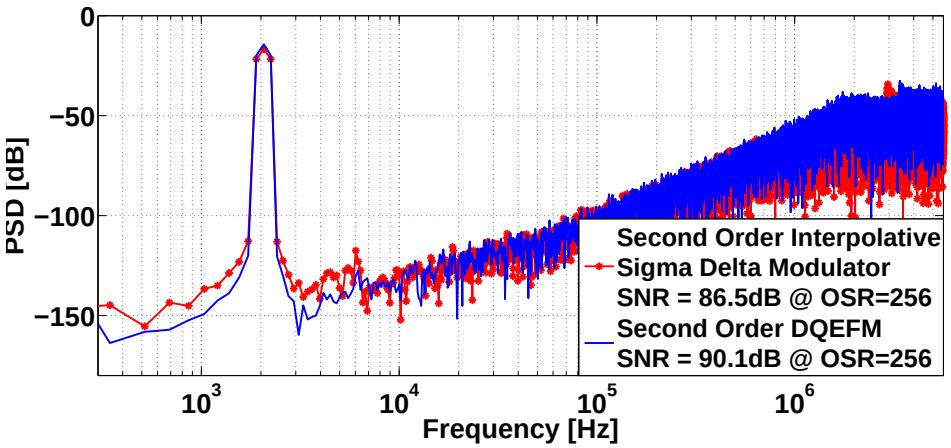
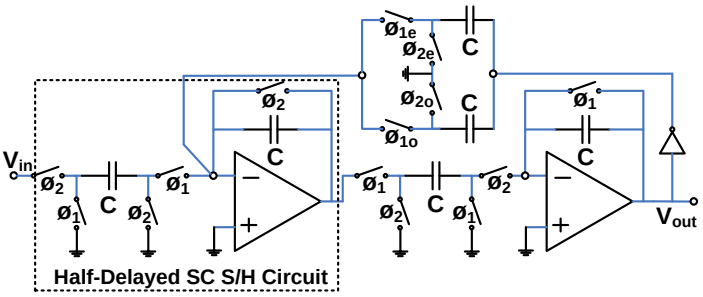


Figure 6.20: Output spectra of the second-order interpolative ΣΔM and DQEFM architectures from Hspice

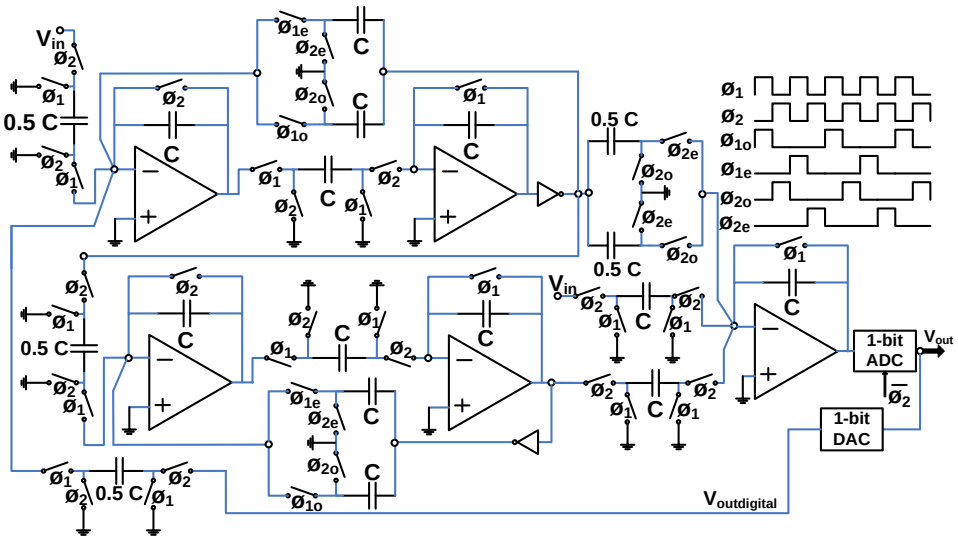
Figure 6.21(a), is the basic building block of the conventional and the proposed architecture. It uses two different capacitors for sampling and holding phase, which facilitates the realization of scaling coefficients, and is operated by two-phase non-overlapping clock. In the SC two-delay-loop (TDL) resonator of Figure 6.21(a), the forward unit delay is provided by serially connected half-delayed SC S/H circuit. The feedback unit delay is provided by parallel SC network consisting of two capacitors, each of which holds the charge for one clock cycle. The conventional second order BP-FFΣΔM of Figure 6.21(b) is implemented using two serially connected TDL resonators, a feedforward adder and a 1-bit quantizer in a ΣΔ loop.

Figure 6.21(c) shows the proposed second order BP-DQEFM, which is implemented by using a combination of delayed and delay-free S/H circuit. In delay-free S/H circuit both sampling and holding operation takes place in the same clock phase and produces an inverted S/H output, whereas in delayed S/H circuit, sampling and holding operation takes place in two different non-overlapping clock phase and produces a non-inverted S/H output with a half clock-cycle delay ($z^{-1/2}$). The subtraction operation to extract the quantization noise is achieved by the combination of delayed and delay-free S/H circuit. A parallel SC network consisting of two capacitors, each of which holds the charge for three half-clock cycles, provides the necessary feedback delay.

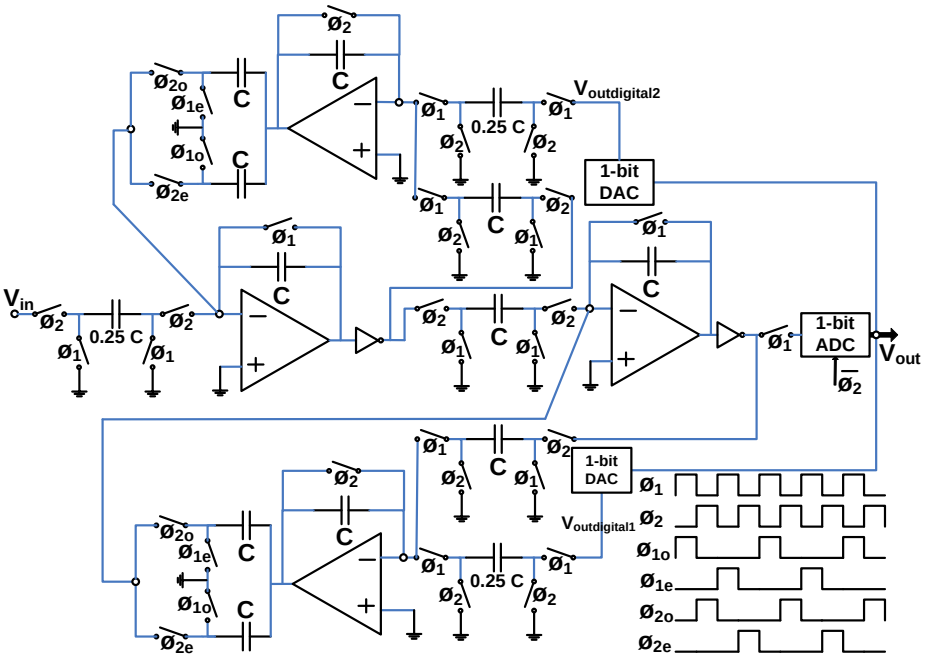
Unlike conventional BP-FFΣΔM, the proposed BP-DQEFM is hardware efficient, because BP-DQEFM does not require the feedforward adder and thus it needs one opamp less as compared to the conventional BP-FFΣΔM. The complete circuit, both conventional and proposed, were simulated in 45 nm CMOS process, with a supply of



(a)



(b)



(c)

Figure 6.21: Single ended switched-capacitor circuit implementation of (a) TDL resonator (b) conventional second order BP-FF$\Sigma\Delta$M using TDL resonator (c) proposed second order BP-DQEFM using SC S/H circuit.

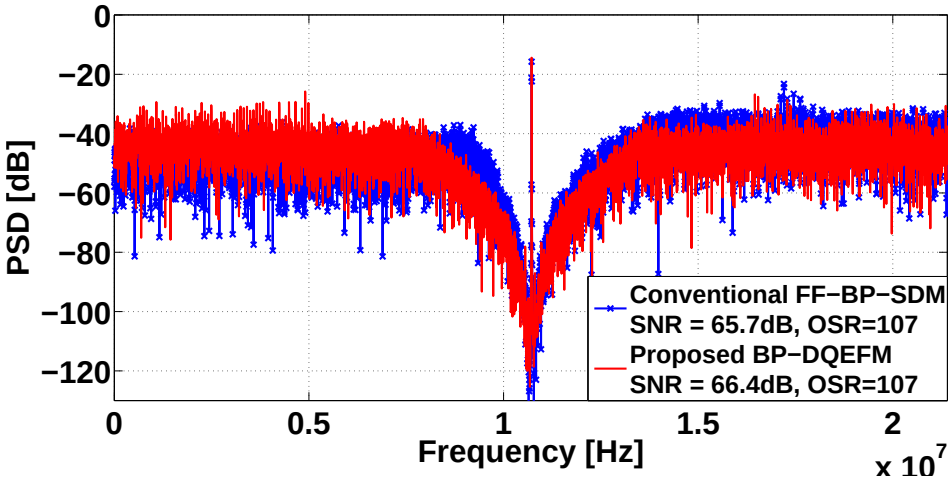


Figure 6.22: Output spectra of the switched-capacitor circuit implementation of the conventional second order BP-FF-$\Sigma\Delta$M and proposed second order BP-DQEFM architectures from Hspice

1V using Hspice. An OSR of 107 and a 1-bit quantizer were used for the simulations. The clock frequency was set as 42.8 MHz. A 10.7 MHz digital radio IF signal with a bandwidth 200 kHz was considered as the input. The two non-overlapping clock phases, Φ_1 and Φ_2, were used to operate the complete SC capacitor model and the output spectra are depicted in Figure 6.22. Any imperfections associated with the analog subtraction and analog loop filter can be compensated by tuning the feedback capacitances. The simulations using Hspice in 45 nm CMOS process shows a power consumption of 0.62 mW and 0.95 mW for the proposed and the conventional, respectively.

Unlike interpolative $\Sigma\Delta$Ms, the shaping of the quantization noise in DQEFM modulators does not depend on the accuracy of any complex loop filter and hence the circuit requirements are reduced extensively. The circuit-level feasibility of the proposed DQEFM technique to design high-precision noise shaping converters is clear from the simulation results.

6.10 Chapter Summary

We propose a novel differentially quantized error feedback noise shaping modulator and a differentially quantized bandpass error feedback noise shaping modulator, intended for analog-to-digital conversion, and its mathematical equivalence to $\Sigma\Delta$M has been validated with mathematical analysis and simulations. The differential quantizer based replacement to integrator/resonator and $\Sigma\Delta$ loop itself reduces the sensitivity

of DQEFM technique to circuit non-idealities, particularly opamp DC Gain. The proposed DQEFM outperforms the traditional interpolative $\Sigma\Delta$M in terms of dynamic range performance and influence of opamp DC Gain, and is very likely to be useful for high-precision and low-power data conversion applications.

CHAPTER 7

CONCLUSION

This chapter offers a recapitulation of the major objectives, highlights the contributions of research work carried out and a few perspectives for future work.

7.1 Summary of the Thesis

This research sheds light on advanced and more sophisticated $\Sigma\Delta$ modulator architectures for future high-speed wireless telecommunication systems. The thesis introduces novel noise shaping ADC architectures, its theoretical fundamentals, implementation methodologies, high-level validations and state-of-the-art comparisons, which could be employed in high-precision data conversion applications, specifically in the context of rising complexity of the present multi-channel electronic systems. The intensive dependence on digital systems have motivated the interest in cost and power efficient high-precision data converters. Noise-shaped ADC architectures is the most cost-efficient methodology for high-resolution digitization which are compatible with DSP ICs.

- The thesis commences with an overview of the related research in the field of $\Sigma\Delta$ based analog-to-digital-conversion for wireless transceivers and discusses the relevance of this research in the light of cited previous research works.

- The thesis initially proposes a novel TDM based 3^{rd} order CT incremental $\Sigma\Delta$ modulator with ELD compensation. The incremental operation and high-precision characteristics of the proposed modulator, makes it suitable for time-multiplexed multi-sensory data acquisition systems. The sensitivity of the modulator to ELD is analyzed and compensated through efficient mechanism. The less number of cycles per conversion and relaxed bandwidth requirements of the active blocks makes it suitable for low-power multi-channel applications. A circuit-level behavioural simulation of the proposed modulator for high frequency application

has been done using the behavioural simulator SIMSIDES (José and del Río, 2013).

- The primary technical contribution of the thesis is the modelling and architectural exploration of TI cross-coupled $\Sigma\Delta$ modulators. By the introduction of time interleaving technique the proposed architecture operates at half the sampling rate, which significantly brings down the power consumption. N-path architecture achieves the same SNR of single-path architecture with a lower order loop filter with benefits in terms of stability and complexity. With a mission of achieving enhanced noise shaping characteristics, the thesis proposes a novel ESLD compensated TI extended noise shaping based cross-coupled multi-path SMASH $\Sigma\Delta$ modulator. The ESLD of stage-II, which leads to quantization noise leakage between individual stages, is modelled in stage-I and the ESLD compensation and cancellation of the stage-I quantization error is perfectly achieved by feedback compensation mechanisms, which has been demonstrated analytically and through behavioural and circuit-level simulations. The low hardware requirement of the proposed architecture compared to DNC-SMASH model (Han and Maghari, 2014) has also been illustrated. Moreover, the input referred stability is enhanced by the newly proposed architecture. Hspice simulations validate the proposed architecture in 45 nm CMOS technology. It consumes only 385 μW from a 1V power supply and provides 11-bit performance for -6dB input level.

- A new cross-coupled $\Sigma\Delta$ modulator architecture, called the dual extended noise shaping architecture is proposed for high performance analog-to-digital conversion. The technique enables the advantage of achieving an NTF order twice the number of cross-coupled paths with greatly relaxed circuit specifications and without significant increase in power and area. The practical implementation of extra coupling branches typically uses added switched-capacitors and does not require an extra opamp and hence capable of greatly relaxing the circuit specifications. Dual extended noise shaping based bandpass cross-coupled $\Sigma\Delta$ modulators for advanced wireless transceivers has also been presented.

- The significant progress in the broadband communication systems and the newly emerging wireless systems has led to the evolution of wide-band wireless technology and development of more sophisticated sub-micron CMOS integrated solutions. The multi-standard cellular capability covering GSM/ Bluetooth/ GPS/ WCDMA/ WLAN/ WiMAX for wide range of applications created the necessity to develop multi-mode, portable, power and area efficient ADC architectures. The thesis proposes a triple-mode hexa-standard reconfigurable TI cross-coupled $\Sigma\Delta$ modulator. Enhanced noise shaping characteristics, obtained by TI cross-coupling $\Sigma\Delta$ paths, have been utilized for the modulator design. The cross-coupled paths and the building blocks are reconfigured to adapt the requirements of wide hexa-standard specifications. Using MATLAB and sigma-delta toolbox, the behavioural-level simulation of the proposed reconfigurable architecture is performed, verifying its performance and flexibility to hexa-standard scenarios. Circuit-level realization of the architecture is verified in 45 nm CMOS technology using Hspice and implementation is done in Cadence tools. An improved peak SNR of 83.4/ 80.2/ 67.8/ 61.5/ 60.8/ 51.03 dB is achieved in the channel bandwidth of 0.2/ 1/ 2/ 3.84/ 22/ 28 for GSM/ Bluetooth/ GPS/ WCDMA/ WLAN/ WiMAX mode with low OSR and minimum hardware. The sensitivities of the proposed model to the finite opamp DC gain, bandwidth, slew rate, channel mismatch and cross-coupled coefficients mismatch are also been analyzed.

- A novel differential quantizer based error feedback modulator for analog-to-digital-conversion is proposed in the thesis. The major challenges associated with the design of higher order $\Sigma\Delta$ modulators are loop stability issues due to its inherent non-linearity, integrator associated non-idealities, optimization of the integrator scaling coefficients and low operating bandwidth due to the accumulation of samples. An excellent alternative in the class of oversampling and noise shaping converters, that can mitigate these problems associated with $\Sigma\Delta$ modulator, is the newly introduced differential quantizer based error feedback modulator (DQEFM). The switched capacitor (SC) model of the architecture is done in Hspice. A detailed comparison with the traditional $\Sigma\Delta$ modulators is also in-

cluded in the chapter. A bandpass version of the differentially quantized error feedback modulator, intended for digital radio applications, is also proposed and presented. The differential quantizer based replacement to integrator/resonator and $\Sigma\Delta$ loop itself makes the DQEFM technique less sensitive to circuit non-idealities, hardware efficient and power efficient, and is very likely to be useful for high-speed, wide-band, high-precision and low-power data conversion applications.

7.2 Future Work

This section discusses on future perspectives of my research by pointing out some of the possible forms to improve and extend the work presented in the thesis.

- The applications of $\Sigma\Delta$ modulators has increased in the past few years, especially for high data rate and resolution requirements. Overloading prediction estimation uses the multiple-input describing function (Vander Velde, 1968), (Ardalan and Paulos, 1987) or other prediction algorithms to predict its overloading levels and thus improve the stability of the entire reconfigurable modulator. Describing function analysis (Vander Velde, 1968), (Ardalan and Paulos, 1987) is an approximation for analyzing nonlinearity by quasi-linearization, which is the approximation of the non-linearity by a linear system that depends on the amplitude of the input (Vander Velde, 1968). Also in (Baird and Fiez, 1994), it is shown that the multi-bit quantization is non-linear and has a limiting overloading level. The accurate prediction of stability limits of the multi-bit quantizer remains a problem to be explored.

- In cross-coupled $\Sigma\Delta$ modulator design, the peak SNR is determined by the scaling and cross-coupled coefficients. Therefore, selecting the optimum value of these coefficients is very important for optimum performance (Jose *et al.*, 2008). More efficient designs of $\Sigma\Delta$ modulator architectures, in terms of ERBW and

area/power efficiency, necessitates to explore a number of different design objectives simultaneously in the design space in order to obtain the best sets of target electrical characteristics/specifications. Multi-objective optimization (Deb, 2001) are employed where optimal decisions need to be taken in the presence of trade-offs between two or more conflicting objectives. A significant amount of research can be done for improving the performance of the proposed efficient $\Sigma\Delta$ modulator architectures, both at system-level and transistor-level, using multi-objective optimizing algorithms.

- The bandpass $\Sigma\Delta$ modulator based ADCs has opened a door towards the realization of fully-monolithic, low-cost, low-power communication devices, since it allows several transceiver stages to be moved to the digital domain. This way, better noise immunity, more robustness and flexibility may be achieved, leading to potential improvements in performance and power consumption, and cost reduction. Following this trend of moving to the digital domain as many blocks as possible, it is possible to digitalize the RF signal (Bazarjani *et al.*, 1999) coming from the antenna before any mixing. This way, by moving the mixing to the digital domain, a perfect matching between mixers is achieved and, therefore, no high performance channel-selection filters are required. Efficient digitization for direct-RF sampling wireless systems is a challenging domain to be explored in future.

- Internet of things (IoT) (Tan and Wang, 2010) is the future wireless phenomenon that enables the connections of the physical and the logical worlds forming the next link in the chain of ubiquitous communication systems. Hardware/ power-efficient $\Sigma\Delta$ modulator based data processing system for next generation VLSI transceivers in IoT is a prominent area to be explored.

- In the thesis, we concentrated mainly on the design and implementation of efficient $\Sigma\Delta$ modulator architectures. The decimation filter design and the complete system-level perspective of the entire transceiver needs to be performed for evaluating the next-level modelling issues and challenges.

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LIST OF PAPERS BASED ON THESIS

I. Refereed Journals

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3. **Jos Prakash A.V** and Babita R. Jose, A Low Cost Design of Time Division Multiplexing Based 3^{rd} Order Continuous-Time Incremental $\Sigma\Delta$ Modulator with Excess Loop Delay, *Journal of Low Power Electronics,* vol. 10, no. 3, pp. 495-505(11), September 2014. (Impact Factor: 0.526)

4. **Jos Prakash A.V,** Babita R. Jose, and J. Mathew, A Differentially Quantized Bandpass Error Feedback Modulator for ADCs in Digital Radio, Submitted to *Springer Circuits Systems and Signal Processing*.

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2. **Jos Prakash A.V.,** Babita R. Jose and J. Mathew, TDM Based 3^{rd} Order CT Incremental $\Sigma\Delta$ Modulator for Low Frequency ADC Application, *proceedings of International Conference on Next Generation Computing and Communication Technologies (ICNGCCT)* held at Dubai, pp. 220-225, April 2014, ISBN 978-93-83303-42-7. (Got the Outstanding Paper Presentation Award during the event).

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4. **Jos Prakash A.V.** and Babita R. Jose, A Low-Power Reconfigurable Cross-Coupled $\Sigma\Delta$ Modulator for Multi-Standard Wireless Applications, *proceedings of Fourth International Conference on Advances in Computing and Communications (ACC-2014)*, IEEE Computer Society's CPS, pp. 130 - 133, 27-29 Aug. 2014, DOI 10.1109/ICACC.2014.37. ISBN 978-1-4799-4364-7 (Won Best Paper Award in the 27^{th} Kerala Science Congress, 27 to 29 January 2015. The Award carries a certificate of merit, a cash prize of Rs. 10,000/- and a contingency grant of Rs. 100,000/- (Rupees one lakh only) for two years for pursuing further research).

5. Sabarinath , **Jos Prakash A.V.,** Babita R. Jose, and J. Mathew, Overloading Prediction in Symmetric Cross Coupled Low-Pass Sigma Delta Modulators, *International Conference on Information and Communication Technologies (ICICT) 2014*, 3 - 5 December, 2014, Elsevier Procedia Computer Science, vol. 46, 2015, pp. 1223-1229, ISSN 1877-0509,
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7. **Jos Prakash A.V.,** Babita R. Jose and J. Mathew, A Novel Excess Sturdy-MASH-Loop-Delay Compensated Cross-Coupled Multipath Time-Interleaved $\Sigma\Delta$ Modulator, *IEEE* 29^{th} *International Conference on VLSI Design (VLSID)* Kolkata, IEEE, pp. 246 - 251, 4-8 Jan. 2016, DOI:10.1109/VLSID.2016.59, INSPEC Accession Number:15855990.

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