A TRIPLE-MODE FEED-FORWARD SIGMA-DELTA MODULATOR DESIGN FOR GSM / WCDMA / WLAN APPLICATIONS

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ABSTRACT - This paper presents a cascaded 2-2-2 reconfigurable sigma-delta modulator that can handle GSM, WCDMA and WLAN standards. The modulator makes use of a low-distortion swing suppression topology which is highly suitable for wide band applications. In GSM mode, only the first stage (2^{nd} order ∑-Δ ADC) is turned on to achieve 88dB dynamic range with over-sampling ratio of 160 for a bandwidth of 200KHz; in WCDMA mode a 2-2 cascaded structure (4^{th} order) is turned on with 1-bit in the first stage and 2-bit in the second stage to achieve 74 dB dynamic range with over-sampling ratio of 16 for a bandwidth of 2MHz and a 2-2-2 cascaded MASH architecture with a 4-bit in the last stage to achieve a dynamic range of 58dB for a bandwidth of 20MHz. The novelty lies in the fact that unused blocks of second and third stages can be switched off taking into considerations like power consumption. The modulator is designed in TSMC 0.18um CMOS technology and operates at 1.8 supply voltage.

I. INTRODUCTION

Mobile Telecommunication has experienced tremendous growth since the progressive development of wireless communication systems. Several mobile telecommunications standards are used worldwide in the transition from the second generation (2G) digital system into the third generation (3G) system. The most popular standard for 3G systems is WCDMA, supported by the third generation partnership project (3GPP). 4G mobile systems will be further integrated with Wireless Local Area Networks (WLAN). A user will employ the WLAN mode whenever the mobile terminal is within range of a WLAN access point [1]. WLAN-enabled cell phones are expected to contain multimode cellular capability. A suggestion is to encompass GSM and WCDMA operation, in addition to WLAN [2].

Sigma-delta modulator is the most promising candidate to achieve high resolution over a wide variety of bandwidth requirements in multi-mode receivers. The advantage of sigma-delta ADCs in providing high resolution with low precision components lies on the use of over-sampling and noise shaping. As bandwidth requirement increases, the over-sampling ratio decreases which results in a decrease in the resolution. Designing sigma-delta modulators that can achieve high resolution and wide bandwidth remains challenging. Several researchers have proposed multi-standard sigma-delta ADC for wireless receiver applications like GSM/WCDMA/WLAN etc

A multi-mode cascaded ∑Δ architecture have been reported in [3] whose wide range of programmability of input frequency and dynamic range descends from modulator order programmability. Another reconfigurable ∑Δ modulator for a triple standard receiver has been introduced in [4] where a feedback path from the last stage to the third stage is done in order to further suppress the quantization noise power. Yet another multi-standard sigma-delta ADC has been explored in [5]. All these make use of traditional topology which is increasingly sensitive to circuit imperfections, especially at very low oversampling ratios. In this work, we present a triple-mode low-distortion swing suppression (feed-forward) topology [6] which has reduced sensitivity to opamp nonlinearities, for use in wideband applications like WLAN.

Based on the triple-standard Zero-IF/Low-IF approach, GSM/WCDMA/WLAN triple-mode receiver architecture is proposed in Figure 1. In this architecture, three sets of band filters and LNAs are required for GSM/WCDMA/WLAN selection. The multi-standard ADC is shared by these three standards. Table I summarizes the channel bandwidth and dynamic range requirements of the base-band ADC for the three standards, obtained from the Simulink model of the receiver.

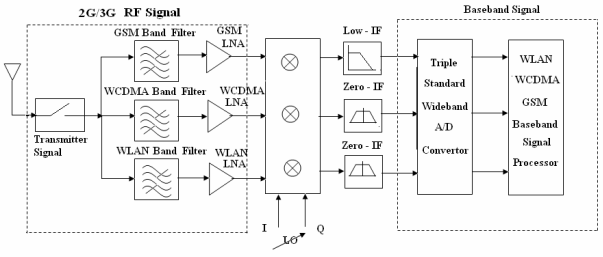

Fig.1. Triple Standard Wideband Receiver Architecture

TABLE I: ADC REQUIREMENTS FOR MULTI STANDARD RECEIVER

Wireless Standard	Frequency (MHz)	Channel Bandwidth	Dynamic Range
GSM	890-915(Tx) 935-960(Rx)	200 KHz	80 dB
WCDMA	1850-1910 (Tx) 1920-1980 (Rx)	5 MHz	60 dB
WLAN	2401-2473	20 MHz	50 dB

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The paper is organized as follows. Section I is the introduction. Section II focuses on selecting the appropriate architecture for the multi-standard [3][4] ∑Δ modulator given the wireless receiver specifications. Section III describes a switched-capacitor (SC) ∑-Δ modulator operating from 1.8V supply and implemented in TSMC 0.18um CMOS technology. Section IV provides the simulation results. Finally, Section V concludes the paper.

II. MODULATOR ARCHITECTURE

This Section explores tradeoffs among the wide variety of ∑-Δ modulator architectures that can be used to implement a ∑-Δ A/D converter suitable for low power and high integration triple-standard receiver. The search for an optimal wideband ∑-Δ topology has been performed by varying the order L, the over-sampling ratio M and the number of bits B in the quantizer as shown in Table II

TABLE II: COMPARISON OF ∑Δ MODULATOR ARCHITECTURES

Wireless Standard	Order	OSR	F_{CLK} (MHz)	Bits B	SNR (dB)
GSM	2	64	25.6	1	78
	2	128	51.2	1	80
	2	160	64	1	88
	3	64	25.6	1	105
WCDMA	3	16	80	2	68
	4	16	64	2	73
	4	20	100	1	88
	5	16	80	1	94
WLAN	4	5	100	4	52
	5	4	80	4	50
	6	5	100	3	64
	6	8	160	4	65

For signals of very wide bandwidth, such as in WLAN receiver, over-sampling ratio cannot be very high (4 or 5) because the achievable clock frequency is constrained by the process technology. Therefore the only solution is by increasing the order L and quantizer bits M in order to achieve the required solution. The dynamic range of a ∑Δ modulator is given by

$$DR = \frac{3}{2}\frac{2L+1}{\pi^{2L}} M^{2L+1}.(2^B - 1)^2 \qquad (1)$$

For low-data rate applications, such as GSM receiver, over-sampling ratio (M) can be made higher, due to much smaller signal bandwidth. For higher order or multi-bit modulators the complexity becomes higher, and for higher sampling frequency the requirements of analog building blocks becomes more demanding.

Taking into account the above considerations, a cascaded 2-2-2 structure with multi-bit quantizer is proposed which is shown in Fig. 2. A second order single bit ∑Δ modulator has been selected as the first stage in order to meet the specifications of GSM mode. Here, we choose a low-distortion swing suppression topology [6], which is highly suitable for wide band applications because of its relaxed requirements on the analog building blocks. The unused blocks in the second and third stages are switched off while working in the GSM mode, taking into account the design considerations like power consumption. In the WCDMA mode, the 4th order modulator (2-2 cascaded) is switched to operation by closing the switch labeled W thus making it programmable. In the WLAN mode, a sixth order modulator (2-2-2 cascaded) is switched to operation by closing the switches labeled S, in order to get more than 50 dB SNDR.

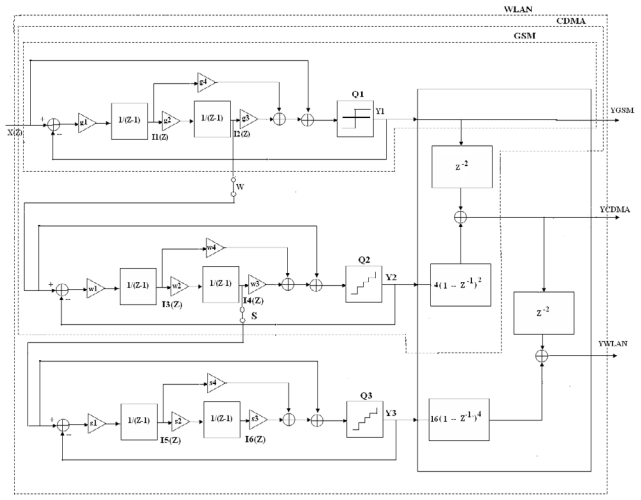

Fig.2. Programmable Sigma-delta Modulator for GSM/WCDMA/WLAN

The novelty lies in the fact that the input to the second and third stages can be directly taken from the output of the second integrator of the preceding stages, since the integrators are only processing the quantization noise.

The modulator output in GSM mode is the output of the first stage

$$Y_{GSM}(z) = X(z) + (1 - z^{-1})^2 Q_1(z) \qquad (2)$$

and the output of the second stage is given by

$$Y_2(z) = I_2(z) + (1 - z^{-1})^2 Q_2(z) \qquad (3)$$

where

$$I_2(z) = -g_1 g_2 z^{-2} Q_1(z) \qquad (4)$$

The modulator output in W-CDMA mode is given by the output of the modified cascaded modulator.

$$Y_{CDMA}(z) = z^{-2} X(z) + g_5 (1 - z^{-1})^4 Q_2(z) \qquad (5)$$

where $g_5 = \dfrac{1}{g_1 g_2}$ is the digital coefficient and the digital transfer functions are

$$H_1(z) = z^{-2} \text{ and } H_2(z) = g_5 (1 - z^{-1})^2 \qquad (6)$$

Proceeding in this manner, we have the modulator output in the WLAN mode as

$$Y_{WLAN} = z^{-4} X(z) + g_6 (1 - z^{-1})^6 Q_3(z) \qquad (7)$$

where $g_6 = \frac{1}{(g_1 g_2)(w_1 w_2)}$ g6 = 1/ (g1g2) (w1w2) is the gain coefficient in the digital cancellation filter

The optimal set of coefficient for the three standards are given in Table III

Table III: COEFFICIENTS OF THE TRIPLE-MODE SIGMA-DELTA MODULATOR

GSM		WCDMA		WLAN	
Coefficients	Value	Coefficients	Value	Coefficients	Value
G1	0.5	W_1	0.5	S_1	0.5
G2	0.5	W2	0.5	S2	0.5
G3	4.0	W3	4.0	S3	4.0
G4	4.0	W4	4.0	S4	4.0

Several behavioral simulations were carried out using a set of Simulink models [7][8], which takes into account switched-capacitor circuit non-idealities like sampling jitter, kT/C noise and operational amplifier parameters such as the finite DC gain, finite bandwidth, and slew-rate and saturation voltage. Also the effect of DAC non-linearity and the coefficient mismatch were simulated to obtain the specifications of analog building blocks.

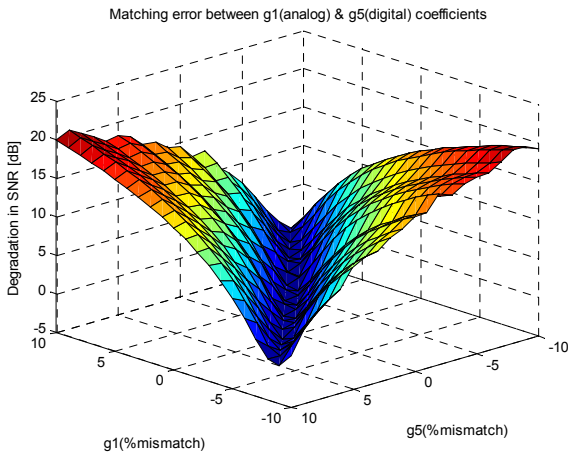

Fig. 3: Degradation of SNR with coefficient mismatch

Multi-stage Noise Shaping (MASH) ∑Δ modulators are sensitive to coefficient mismatches. Those coefficients are implemented in the switched-capacitor ∑Δ modulator by capacitor ratios. This necessitates the study of sensitivity analysis of matching error between analog and digital gain coefficients. Fig. 3 depicts the sensitivity of matching between analog and digital gains on the performance of the modulator. The 3-D plot shows the influence in signal-to-noise ratio as the percentage of mismatch between the analog (g_1) and digital (g_5) coefficients are varied from 0 to 10%, both in the positive and negative direction. It is observed that there is a degradation of more than 20 dB in the peak signal-to-noise ratio.

III. CIRCUIT-LEVEL DESIGN

The configurable sigma-delta modulator has been designed in TSMC 0.18um CMOS technology, operating from 1.8V supply voltage. The circuit-level implementation of the 2nd order ∑Δ modulator with feed forward signal path used in the first stage is shown in Fig 4. The proposed sigma-delta modulator for GSM/WCDMA receiver was implemented as a fully differential switched capacitor circuit (SC) circuit, which has been simulated using Cadence/Spectre. The design of the individual circuit blocks like Operational Transconductance Amplifiers (OTA), switches, capacitors and comparators has been done based on the behavioral simulation results. The forward signal path was implemented by connecting a passive SC network to the input of the quantizer. The integrators were implemented in a fully differential configuration and employ the bottom-plate sampling technique to minimize signal-dependent charge-injection and clock feed through. The optimum values of the switches size, which yields a minimum time constant, have been used. The sizes of the sampling and integrating capacitors were governed by the noise requirements and matching requirements. The values of sampling and integration capacitors for GSM/WCDMA mode are successively 2pF, 1pF, 0.5pF, 0.2pF and 4pF, 2pF, 1pF, 0.4pF. The goal in selecting OTA was to choose a topology, which can meet the integrator requirements at minimum power dissipation. Reduced integrator output swings allowed us to choose the fully differential folded-cascode OTA for all integrators.

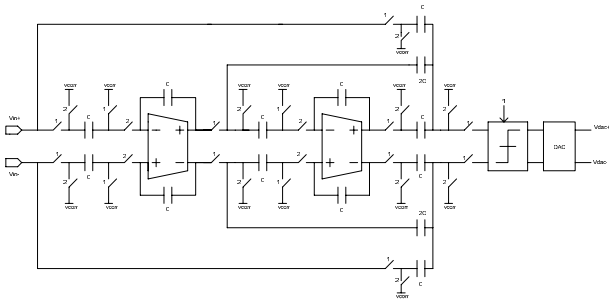

Fig. 4: The first stage 2nd order feed forward single-bit ∑Δ modulator

Since the DC gain requirement is not so demanding, this is a good selection because of its high operation speed / power consumption ratio. The output common-mode voltage was also stabilized using a dynamic switched-capacitor common-mode feedback (CMFB) circuit whose linearity is good enough for this application and does not require extra power consumption.. The performance summary of the front-end OTA is presented in Table IV. The load capacitances and the OTAs have been scaled down to minimize the power. The single-bit quantizer is implemented with a regenerative latch followed by an SR latch. The comparator hysteresis is 7.9mV and the comparator offset is 3.8mV, which is less than 0.5LSB. The single-bit DAC is a simple switch network connected to reference voltages. The 4-bit quantizer from the third stage is implemented with a 4-bit flash A/D converter and the 4-bit D/A converter is implemented in a fully differential SC configuration.

The sampling capacitances are combined with sixteen small unit capacitance to realize the 4-bit DAC. No DEM circuit is

used because the behavioral simulations suggested that there are no distortions associated with the 4-bit DAC nonlinearity.

TABLE IV: SUMMARY OF THE FRONT-END OTA

OTA Specification	Value
DC Gain	68 dB
GBW (C_L = 2pF)	340 MHz
SR (C_L = 2pF)	160 V/us
Phase Margin	64 degree
Output Swing	2V (differential)
Maximum Current	2.1 mA
Power dissipation	3.78 mW
Technology	0.18 um CMOS

IV. SIMULATION RESULTS

Fig 5 shows the modulator output spectrum for a 0.5V/10MHz input signal and an OSR of 5. These results show that a high linearity can be achieved due to the low-distortion sigma-delta modulator architecture, multi-bit quantization and modified cascaded architecture.

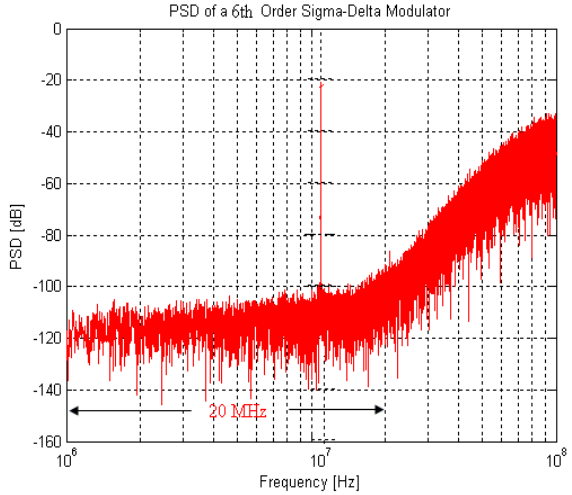

Fig. 5: Modulator Output Spectrum in WLAN mode

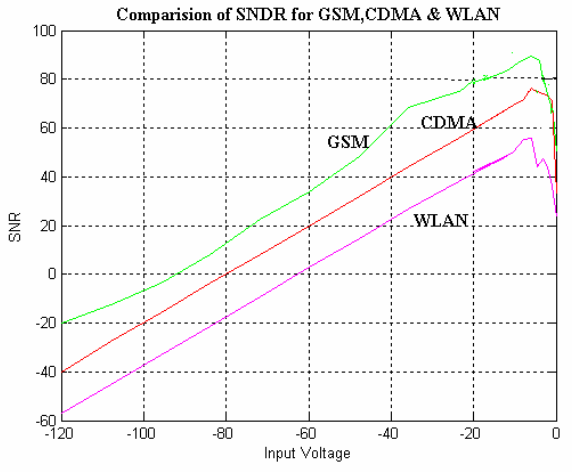

Fig. 6: SNDR versus input level for GSM/WCDMA/WLAN mode.

Fig 6 presents simulated signal-to-noise plus distortion ratio (SNDR) versus input signal amplitude, for GSM/WCDMA/WLAN standards. Simulation results show a peak SNDR of 88dB@-4dBFS in GSM mode a peak SNDR of 73dB@-6dBFS in WCDMA mode, and a peak SNDR of 58dBdB@-6dBFS in the WLAN mode.

TABLE V: SUMMARY OF THE PERFORMANCE OF THE MULTI-STANDARD MODULATOR

Supply voltage	TSMC 0.18um CMOS process 1.8V		
Mode and Architecture	GSM Feed forward 2nd order	WCDMA 2-2 modified cascaded	WLAN 2-2-2 modified cascaded
Sampling Frequency	64 MHz	64 MHz	200 MHz
Signal Bandwidth	200 kHz	2 MHz	20 MHz
OSR	160	16	5
Peak SNDR	88 dB	73 dB	58 dB

V. CONCLUSIONS

A GSM/WCDMA/WLAN multi-standard sigma-delta modulator has been proposed in this paper. This programmable sigma-delta ADC uses low-distortion swing suppression topology which is used here to achieve a high linearity in wideband applications. A 4th order modified cascaded modulator with single-bit in the first stage and 2-bit in the second stage is used to achieve the required dynamic range for WCDMA mode and a 2-2-2 cascaded MASH architecture has been selected for the WLAN standard. In GSM mode the second and third stages are switched off to reduce the power dissipation.

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