A Triple-mode Sigma-delta Modulator Design for Wireless Standards

Babita R. Jose, P. Mythili, Jawar Singh*, Jimson Mathew*
Cochin University of Science and Technology
*University of Bristol, UK.

Abstract

This work presents a triple-mode sigma-delta modulator for three wireless standards namely GSM/WCDMA and Bluetooth. A reconfigurable ADC has been used to meet the wide bandwidth and high dynamic range requirements of the multi-standard receivers with less power consumption. A highly linear sigma-delta ADC which has reduced sensitivity to circuit imperfections has been chosen in our design. This is particularly suitable for wide band applications where the oversampling ratio is low. Simulation results indicate that the modulator achieves a peak SNDR of 84/68/68 dB over a bandwidth of 0.2/3.84/1.5 MHz with an oversampling ratio 128/8/8 in GSM/WCDMA/Bluetooth modes respectively.

1. Introduction

Reconfigurability is a major focus of recent RF transceiver IC designs which has been used to increase both the integration and adaptability to multiple RF communication standards. In accordance with various wireless specifications defined by the telecom standards, the transceiver systems are becoming more digital to increase the flexibility and multi-mode capability. When different standards do not operate simultaneously, circuit blocks of a multi-standard handset can be shared. This has the advantage of low power consumption, small chip area, long talk time, and most importantly, have the potential for low cost.

New architectures and circuit techniques need to be explored in the design of fully integrated, multi-standard RF transceivers. One of the more notable challenges lies in the design of low power, high dynamic range base band blocks which will coexist on the same substrate as the RF front-end components. A wide dynamic range sigma-delta modulator can be used to meet the different dynamic range, linearity and signal bandwidth requirements of multiple communication standards.

A triple-mode and power-efficient A/D converter capable of meeting the requirements of GSM, WCDMA and Bluetooth is presented. The architecture uses a low-distortion swing suppression SDM which has reduced sensitivity to opamp non-linearities. The technique is effective for very low oversampling ratios (OSRs) where the ADCs are increasingly sensitive to circuit imperfections and require high-quality analogue components.

Figure 1 depicts a reconfigurable GSM/WCDMA/Bluetooth receiver with low IF-zero IF architecture [1]. A switch selects between the three standards. The multi-standard receiver has a very low IF (100 KHz) for GSM and zero IF for WCDMA. The same design is used to digitize the signal in Bluetooth standard [2]. Three RF filters have been used to select appropriate signal bands. One set of LNA and mixer have been shared between WCDMA and Bluetooth standard due to the proximity of their signal bands. Base band components in the I and Q paths include a ploy-phase filter, VGA and ADC shared among the three standards. Table I summarizes the channel bandwidth and dynamic range requirements of the base-band ADC for the three standards, obtained from the Simulink model of the receiver.

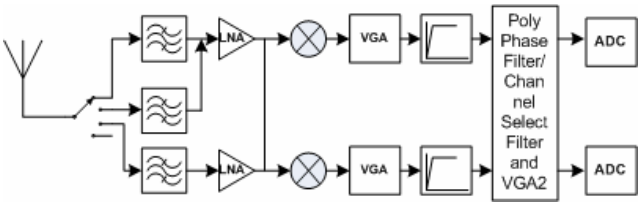


Figure 1. Reconfigurable low IF-zero IF receiver architecture for GSM/WCDMA/Bluetooth standards

Table 1. ADC specifications in different standards

Wireless Standard	Channel Bandwidth	Dynamic Range
GSM	200 KHz	80 dB
WCDMA	3.84 MHz	60 dB
Bluetooth	1.5 MHz	60 dB

The paper is organized as follows. Section 1 is the introduction. Section 2 focuses on selecting the appropriate architecture for the multi-standard [3] $\sum\Delta$ modulator given the wireless receiver specifications. Section 3 describes the various non-idealities of switched-capacitor (SC) sigma-delta modulator in MATLAB Simulink environment. Section 4 provides the simulation results. Finally, Section 5 concludes the paper.

0-7695-3068-0/07 $25.00 © 2007 IEEE
DOI 10.1109/ICIT.2007.61

2. Modulator architecture

The target specifications of the A/D converter are defined by the triple-standard wireless receiver requirements: 80 dB/60 dB/60 dB over 200 KHz/3.84 MHz/1.5 MHz with minimum power dissipation. Sigma-delta A/D converters suitable for dual-mode receivers have already been published [4-7]. Table 2 summarizes the performance of some of the published triple-mode ∑Δ ADC [8-10]. A triple-mode cascaded ∑Δ architecture for GSM/UMTS/WLAN has been reported in [8] whose wide range of programmability of input frequency and dynamic range descends from modulator order programmability. Another reconfigurable ∑Δ modulator for a triple standard receiver has been introduced in [9] where a feedback path from the last stage to the third stage is done in order to further suppress the quantization noise power. Yet another multi-standard sigma-delta ADC has been explored in [10]. All these make use of traditional topology which is increasingly sensitive to circuit imperfections, especially at very low oversampling ratios. In this work, we present a triple-mode low-distortion swing suppression (feed-forward) topology [11] which has reduced sensitivity to opamp nonlinearities, especially for use in wideband applications.

Table 2. Performance summary of the published triple-mode ∑-Δ ADCs

	Triple-mode ∑-Δ ADCs		
	[8]	[9]	[10]
Order	2-1-1	2-1-1-1	2-2
No. of bits	1/1/1	1/1.5/3	2.5/2.5
Fs (MHz)	138/245/320	51.2/100/10	23/46
BW (MHz)	0.271/3.84/2	0.2/5/20	0.2/1.5/1
DR (dB)	103/82/66	94/88/56	70/51/50
CMOS Process	0.35 um	0.18 um	0.18 um
Power	58/82/128	---	5.8/5/11

In order to achieve an optimum trade-off between bandwidth, resolution and power for ∑Δ A/D converters, the design performance requirements are used in conjunction with technology-related constraints, like sampling frequency. For use in wide band applications like WCDMA/Bluetooth, oversampling ratio cannot be very high, because the maximum sampling frequency of CMOS SC circuits is limited by the speed of the technology. However, to maintain the required performance at a reduced OSR, it is necessary to increase the dynamic range by using alternative solutions. The dynamic range of a ∑Δ modulator is given by

$$DR = \frac{3}{2}\frac{2L+1}{\pi^{2L}} M^{2L+1}.(2^B - 1)^2 \qquad (1)$$

where L is the order of the modulator, M is the oversampling ratio and B is the number of bits of the quantizer.

Generally there are two different approaches for implementing ∑Δ modulators for multi-standard wireless receivers. The high-order single-loop multibit ∑Δ modulator is an attractive approach [4, 6]. By using an aggressive high-order noise transfer function combined with multibit feedback it is possible to achieve a high signal-to-noise ratio (SNR) at a low oversampling ratio. The main drawback of this approach is that high linearity of the feedback D/A converter of the modulator is required. Therefore, the overall sigma-delta converter linearity and resolution are limited by the precision of the multibit D/A converter. Another very attractive approach to realize a wideband and high dynamic range ∑Δ A/D converter is to replace the high-order single-loop modulator with a cascade of sigma-delta modulators [7]]. Cascaded sigma-delta structures realize high-order noise shaping by cascading sigma-delta stages of second-order or first-order to avoid instability. Reducing the quantizer's resolution to 1-bit may eliminate the dependence on feedback D/A converter linearity. One way to achieve further reduction of quantization noise is to use a multibit quantizer in the final stage.

To overcome some of the problems, a modified cascaded ∑Δ modulator architecture is proposed for the triple-mode A/D converter which is shown in figure 2. Our architecture selection involves two key design issues [11, 12]. One is the 2nd order sigma-delta modulator with feed-forward signal path, which has reduced sensitivity to opamp nonlinearities. The other key issue is an architectural approach, which combines the merits of modified cascaded topology and multibit quantization in the last stage to make all quantization noise negligible at low OSR. To meet the required specifications for WCDMA and Bluetooth mode, a 2-2 cascaded architecture with 1-bit quantizer in the first stage and 4-bit quantizer in the second stage was chosen. The 2nd order 1-bit ∑Δ modulator from the first stage is used for the GSM mode. In this case, the second stage is switched off to reduce the power dissipation. The scaling coefficients have been used to achieve the peak signal-to-noise and distortion ratio (SNDR), to control the input of the second stage and to utilize the full dynamic range of the next stage. By combining these techniques the performance improvements of the ∑-Δ modulator are significant.

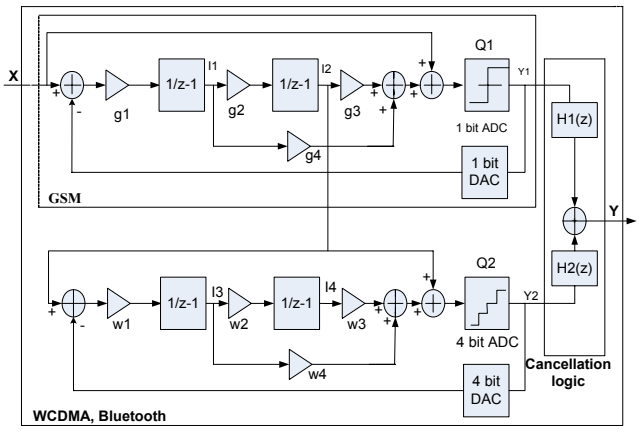


Figure 2. Block diagram of a triple-mode sigma-delta modulator

The output of the first stage of the modulator is given by

$$Y_1(z)=X(z)+\frac{(1-z^{-1})^2}{1+(g_1g_4-2)z^{-1}+(1+g_1g_2g_3-g_1g_4)z^{-2}}Q_1(z) \tag{2}$$

The output of the integrators, I_1 and I_2 are given by

$$I_1(z)=\frac{g_1z^{-1}(1-z^{-1})}{1+(g_1g_4-2)z^{-1}+(1+g_1g_2g_3-g_1g_4)z^{-2}}Q_1(z) \tag{3}$$

$$I_2(z)=\frac{g_1g_2z^{-2}}{1+(g_1g_4-2)z^{-1}+(1+g_1g_2g_3-g_1g_4)z^{-2}}Q_1(z) \tag{4}$$

From equations (3) and (4), it is observed that the integrators process only the quantization noise.
Therefore, the integrator output swings of the proposed architecture are reduced compared with the traditional one and then the operational amplifier requirements are greatly relaxed. Since the output of the second integrator contains only quantization noise, this output has been used as input for the second stage. Therefore, the output of the second stage is given by

$$Y_2(z)=\frac{g_1g_2z^{-2}}{1+(g_1g_4-2)z^{-1}+(1+g_1g_2g_3-g_1g_4)z^{-2}}Q_1(z)+\frac{(1-z^{-1})^2}{1+(w_1w_4-2)z^{-1}+(1+w_1w_2w_3-w_1w_4)z^{-2}}Q_2(z) \tag{5}$$

where Q_1 (z), Q_2 (z) are the quantization errors of the first and second stages respectively and g_1, g_2, g_3, g_4, w_1, w_2, w_3, w_4 are the analog coefficients.

The final modulator output after the cancellation logic is given by

$$Y(z)=z^{-2}X(z)+\frac{1}{g_1g_2}\frac{(1-z^{-1})^4}{1+(w_1w_4-2)z^{-1}+(1+w_1w_2w_3-w_1w_4)z^{-2}}Q_2(z) \tag{6}$$

where the digital coefficient is $d=1/g_1g_2$ and the digital transfer functions are $H_1(z)=z^{-2}$ and $H_2(z)=d\,(1-z^{-1})^2$.

The optimal coefficients for generating the maximum peak signal to noise and distortion ratio (SNDR) are: $g_1=g_2=w_1=w_2=0.5$, $g_3=g_4=w_3=w_4=4$. The simulated integrator outputs histograms of the 4th order cascaded sigma-delta modulator with -4dB/1 MHz sine wave input is shown in Figure 3.

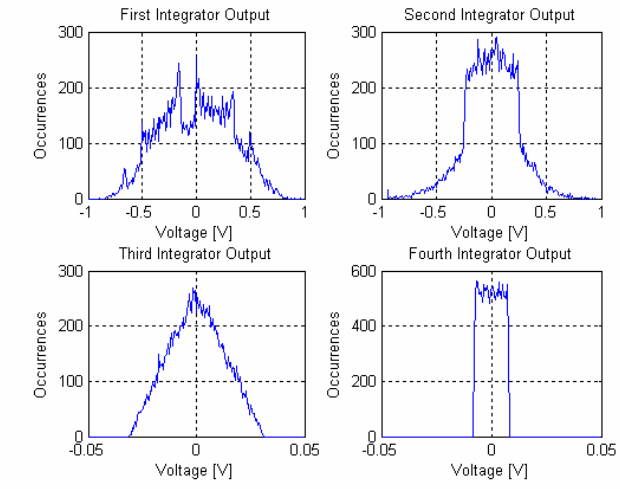


Figure 3. Integrator output swings

3. Behavioral modeling of circuit nonidealities

The behavioral simulations [13, 14] have been used to investigate the overall circuit non-idealities effects and to establish the analog blocks requirements. The behavioral simulations were done using Matlab/Simulink environment. The first integrator is the critical block because its non-idealities affect the overall performance of ∑-Δ modulator. Several non-idealities of the SC integrator have been included in the behavioral model: finite OTA DC gain, slew-rate and gain-bandwidth limitations, capacitor mismatch, OTA noise and thermal noise, clock jitter. The open-loop dc gain of the amplifier is not only finite but can be nonlinear also. Such non-linearities occur, when the integrator implementation is based on an amplifier with input-dependent gain. The effect of nonlinear dc transfer function of OTA is also considered in our behavioral simulations. In the behavioral model we have considered that the OTA presents an open-loop gain whose dependency on the output voltage can be approximated by a polynomial function:

$$A_v = A_0(a_0 + a_1 v + a_2 v^2 + a_3 v^3 .....) \qquad (7)$$

where the second-order nonlinear coefficient is negative and of a module quite large than that of the first order.

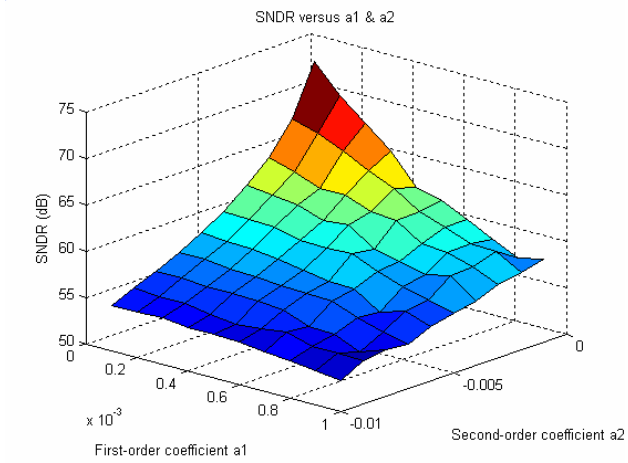


Figure 4. 3D Simulation for non-linear dc gain

The distortion performance is estimated by analyzing the harmonics at the modulator output. Figure 4 shows the 3-D simulation result, where the first-order coefficient (a_1) changes from 0.01% to 0.1% and second-order coefficient (a_2) changes from 0.1% to 1%, keeping the DC gain at 1000. For slew-rate (SR) and gain-bandwidth (GBW) limitations of OTA we used the modeling approach interpreting these effects as a nonlinear gain, [13]. Using the behavioral simulations we have estimated the OTA requirements for a specified dynamic range. Simulation results show the proposed modulator can tolerate an OTA dc gain of 60 dB without performance degradation, the OTA bandwidth needs to be at least 160 MHz and the slew rate at least 150V/us. Switches thermal noise and the OTAs noise are the main noise sources affecting the modulator performance. These effects have been simulated at the system-level by using a noisy integrator model as in [14] and the simulation results are in figure 5. The effect of jitter on the sampling of the input signal has also been considered in the simulation.

Figure 5 compares the power spectral densities (PSD) at the output of the modulator, when two of the most significant non-idealities in the first integrator are taken into account, with the PSD of the ideal modulator. The spectra show how the kT/C noise increases the in-band noise floor, while the slew-rate produces harmonic distortion. It is evident that the non-ideal effects resulting from practical circuit limitations add up and contribute to increase the in-band noise-plus-distortion and therefore can become a severe limitation to the performance achievable from a given architecture.

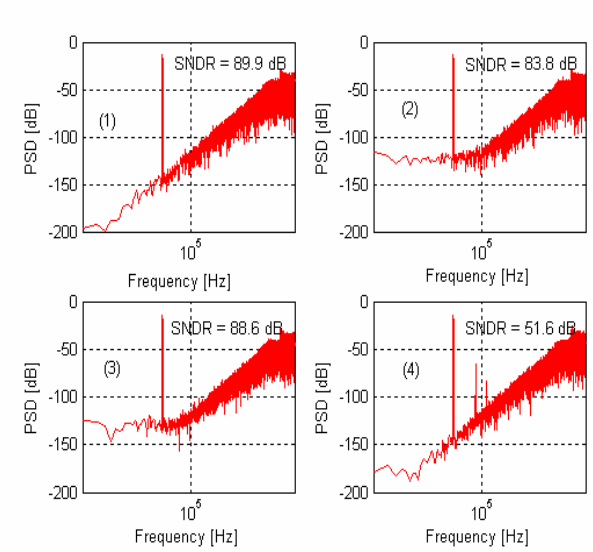
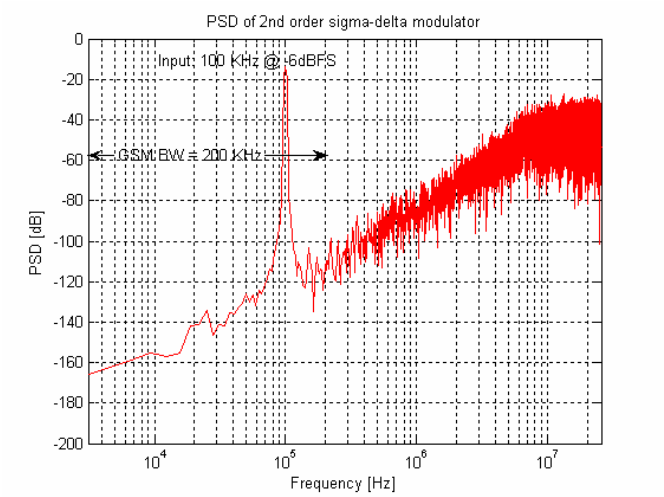


Figure 5. PSD of (1) the ideal modulator; (2) with sampling jitter, $\Delta\tau$ = 4 ns; (3) with kT/C noise, C_s = 1.25 pF; (4) with SR = 50 V/μs.

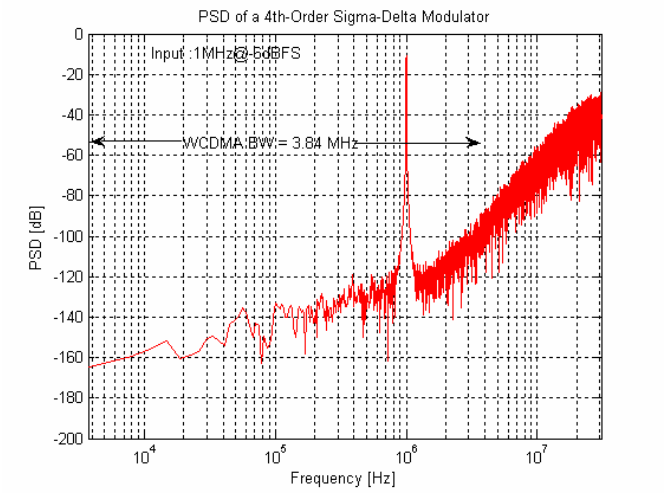
Also the effect of DAC non-linearity and the coefficient mismatch were simulated to obtain the specifications of analog building blocks.

4. Simulation results

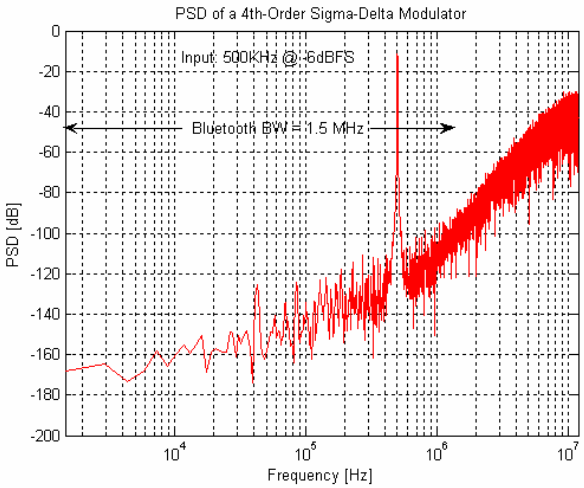
The output spectra for the three modes of operation namely GSM, WCDMA and Bluetooth are shown in figure 6. In GSM mode, the sampling frequency is 51.2 MHz and the input signal is 100 KHz/0.5 V. A sampling frequency of 24 MHz and an input signal of 1 MHz/0.7 V has been used in WCDMA mode. In Bluetooth mode, the sampling frequency is 61.44 MHz and the input signal is 500 KHz/0.7 V. The results show that a high linearity can be achieved due to the low-distortion sigma-delta modulator architecture, multi-bit quantization and modified cascaded architecture.



(a) Modulator output spectrum in GSM mode



(b) Modulator output spectrum in WCDMA mode



(c) Modulator output spectrum in Bluetooth mode

Figure 6. Output spectra for the three modes

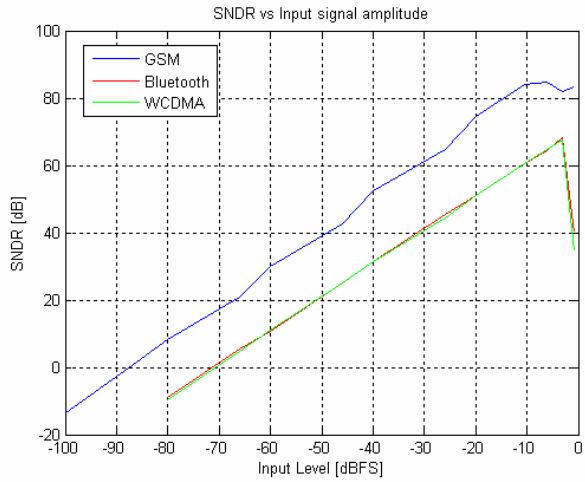


Figure 7. SNDR versus input signal amplitude

Figure 7 presents the simulated SNDR versus input signal amplitude, for GSM/WCDMA/Bluetooth standards. Simulation results show a peak SNDR of 84dB@-6dBFS in GSM mode a peak SNDR of 68dB@-3dBFS in WCDMA mode, and a peak SNDR of 68dBdB@-3dBFS in the Bluetooth mode. The overall performance of the proposed sigma-delta modulator in GSM/WCDMA/Bluetooth modes is summarized in Table 3.

Table 3. Performance summary of different standards

Supply voltage	TSMC 0.18um CMOS process 1.8V			
Standard	Sigma-delta modulator	OSR	Clock Frequency [MHz]	Maximum SNDR [dB]
GSM	2nd order	128	51.2	84
WCDMA	2-2 cascaded	8	61.44	68
Bluetooth	2-2 cascaded	8	24	68

5. Conclusions

A GSM/WCDMA/Bluetooth multi-standard sigma-delta modulator has been proposed in this paper. This programmable sigma-delta ADC uses as low-distortion swing suppression topology to achieve a high linearity in wideband applications. A 2nd order modulator with single-bit quantizer is used for GSM standard to achieve the required dynamic range. A 2-2 cascaded MASH architecture has been selected for the WCDMA and Bluetooth applications. The second stage is switched off to reduce the power dissipation while working in the GSM mode.

6. References

[1] A. Savia, A. Ravindran, and M. Ismail, "A reconfigurable low IF-zero IF receiver architecture for multi-standard wide area wireless networks," *ICECS*, U.A.E, pp. 935-937, Dec. 2003.

[2] H. Yoon, H. Kim, and M. Ismail, "A CMOS radio receiver architecture for ISM/UNII multi-standard wireless applications", *ICECS*, U.A.E., pp.16-19, Dec. 2003.

[3] X. Li, and M. Ismail, *Multi-standard CMOS wireless receivers: analysis and design*. Boston: Kluwer, 2002.

[4] T. Burger and Q. Huang, "A 13.5mW 185-Msample/s sigma-delta modulator for UMTS/GSM dual-standard IF Reception," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1868-1878, Dec. 2001.

[5] G. Gomez and B. Haroun, "A 1.5 V 2.4/2.9 mW 79/50 dB DR sigma-delta modulator for GSM/WCDMA in a 52-364. 0.13 um digital process, " *In IEEE ISSCC Conference Digest of Technical Papers*, San Francisco, CA, 2002, pp. 242-244.

[6] M. R. Miller and C. S. Perie, "A multi-bit sigma-delta ADC for multimode receivers", *IEEE Journal of Solid-State Circuits*, vol. 38, No. 3, 2003, pp.475-482.

[7] A. Dezzani and E. Andre, "A dual-mode WCDMA/GPRS sigma-delta modulator," In *IEEE ISSCC Conference Digest of Technical Papers*, San Francisco, 2003, pp. 58-59.

[8] Andrea Xotta, Andrea Gerosa and Andrea Neviani, "A multi-mode ∑Δ analog-to-digital converter for GSM, UMTS and WLAN," *IEEE International Symposium on Circuits and Systems, vol.3,* 23-26 May 2005, pp. 2551-2554.

[9] Ling Zhang, Vinay Nadig and Mohammed Ismail, "A high order multi-bit ∑Δ modulator for multi-standard wireless receiver," *IEEE International Midwest Symposium on Circuits and Systems*, pp. III-379 – III-382, 2004.

[10] B. Jalali-Farahani, and M. Ismail, "A low power multi-standard sigma-delta ADC for WCDMA/GSM/Bluetooth applications," *IEEE Northeast Workshop on Circuits and Systems*, pp.241-243, June 2004.

[11] J. Silva, U. Moon, J. Steensgaard, and G. C. Temes, "Wideband low-distortion delta-sigma ADC topology," *Electronics Letters,* vol. 37, no. 12, pp. 737-738, June 2001.

[12] Silva, J., Wang, X., Kiss, P., Moon, U. And Temes, G. C., "Digital techniques for improved Delta Sigma data conversion", *proc. Custom Integrated Circuits Conference*, 2002, pp. 183-190.

[13] Brigati, S., Francesconi, F., Malcovati, P., Tonietto, D., Baschirotto, A., and Maloberti, F., "Modeling sigma-delta modulator non-idealities in SIMULINK(R)", *proc. IEEE International Symposium on Circuits and Systems 1999 (ISCAS99),* pp. 384-387.

[14] P. Malcovati, et al, "Behavioral modeling of switched-capacitor sigma-delta modulators", in *IEEE Trans. Circuits Syst. II*, vol.50, no. 3, 2003, pp. 3