Preparation and Characterization of High-k Aluminum Oxide Thin Films by Atomic Layer Deposition for Gate Dielectric Applications

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Preparation and Characterization of High-k Aluminum Oxide Thin Films by Atomic Layer Deposition for Gate Dielectric Applications

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Ph. D Thesis in the field of Applied Physics

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December 2011

Cover Page Illustration: ALD of TMA & H_2O

Dedicated to my Parents........

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Certificate

Certified that the thesis entitled " **Preparation and Characterization of High-k Aluminum Oxide Thin Films by Atomic Layer Deposition for Gate Dielectric Applications** " submitted by **Ms. Anu Philip** is an authentic record of research work carried out by her under my supervision at the Department of Instrumentation in partial fulfilment of the requirements for the award of degree of Doctor of Philosophy of Cochin University of Science and Technology and the work embodied in this thesis has not been included in any other thesis submitted previously for the award of any other degree.

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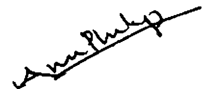
Declaration

I hereby declare that the thesis entitled "**Preparation and Characterization of High-k Aluminum Oxide Thin Films by Atomic Layer Deposition for Gate Dielectric Applications**" submitted for the award of degree of Doctor of Philosophy of Cochin University of Science and Technology is based on the original work done by me under the guidance of **DR. K. Rajeev Kumar**, Associate Professor, Department of Instrumentation, Cochin University of Science and Technology, Cochin - 682 022 and this work has not been included in any other thesis submitted previously for the award of any other degree.



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"It is difficult to say what is impossible, for the dream of yesterday is the hope of today and the reality of tomorrow"

Robert H. Goddard

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Preface

The great commercial success of the microelectronics industry over more than 50 years is to a large extent based on the unique properties of SiO_2, which is grown by thermal oxidation. However the aggressive scaling of complementary Metal-Oxide Semiconductor (CMOS) is driving the SiO_2 based gate dielectrics to its physical limits stated as in the International Technology Roadmap for Semiconductors (ITRS). Currently several alternative high-k materials like Al_2O_3, ZrO_2, HfO_2, Y_2O_3, La_2O_3 and TiO_2, as well as mixed oxides containing SiO_2 (silicates) or Al_2O_3 (aluminates) and metals like Hf, Zr, or La are being studied extensively. In order to successfully integrate a gate dielectric material having higher dielectric constant into a state-of-the-art semiconductor device technology, its electrical device performance (carrier mobility, stability, reliability) has to match or exceed that of SiO_2. The outstanding electrical properties already acquired using SiO_2 clearly presents a significant challenge for any alternative gate dielectric candidate. Many dielectrics appear favorable in some of these areas. But very few materials are promising with respect to all guidelines. While research is ongoing, much work is still required . The new high-k material will also require new manufacturing process to lay down a thickness of one molecular level at a time. As feature size approaches ever small dimensions, process control at the atomic level becomes more important. This is more significant in the case of deposition of gate dielectric materials for MOSFET and high aspect ratio Dynamic Random Access Memories (DRAMs) trench capacitors.

Atomic layer deposition (ALD) has received increasing attention over recent years owing to its unique aspects of thickness and compositional controllability at the nanoscale. As critical layers in leading-edge devices scale to the nanometer regime, ALD is becoming recognized as not only an enabling technology, but also as the only viable technology for applications such as the gate dielectric and copper carrier/seed layers at and beyond the 32nm product generations. With the capabilities of this nanoprocessing technique having finally integrated with the technological demands of the

marketplace, ALD is establishing additional inroads into manufacturing floor, as well as other applications outside of mainstream semiconductor processing.

Aluminum oxide film has received increasing attention because of its wide applications in electronic & optoelectronic devices and in protective & ion barrier layers. Al_2O_3 is an excellent dielectric because of its large band gap (8.7eV), large band offsets with silicon. It also serves as a good diffusion barrier. Though Al_2O_3 has relatively low dielectric constant (~9), this is twice (3.9) that of the widely used SiO_2.

The present work focuses on the development of an automated Plasma Enhanced Atomic Layer Deposition System (PEALD) and deposition and characterizations of ultra thin aluminum oxide high-k layers for gate oxide applications. The proposed thesis is entitled **"Preparation and Characterization of High-k Aluminum Oxide Thin Films by Atomic Layer Deposition for Gate Dielectric Applications"** and consists of seven chapters followed by the concluding section.

Chapter 1 provides a brief description of the current relevance and major requirements of high-k materials for gate dielectric applications. A short review of leading gate oxide materials is also drawn. The motivation for the present study and the major objectives are also discussed in this chapter.

The experimental techniques adopted for sample preparation and various characterization methods used in the present study are covered in **chapter 2.**

Chapter 3 deals with the development of Plasma Enhanced Atomic Layer Deposition system (PEALD). The system consists of reaction chamber, plasma chamber, substrate holder, substrate temperature control system, precursor delivery system including precursor pulsing, ALD sequence controller and Exhaust system. Each part of the system are discussed in detail. Nano layers of aluminum oxide were deposited in the system using TMA (Trimethyl aluminum) and water as precursors. System

parameters were optimized in order to obtain better quality films. The general review of atomic layer deposition (ALD), variants of ALD methods and ALD precursors are also addressed in this chapter.

A theoretical model is proposed in **Chapter 4** which is an extension of R. L Puurenen model. The present model can explain more detailed surface chemisorption mechanism for the adsorption of metal and ligands during ALD. Six possible chemisorption mechanisms are proposed and related parameters like ligand to metal ratio (L/M), concentrations of metal atoms and methyl groups adsorbed per nm^2 are calculated and compared against reported values. The growth per cycle (GPC) was theoretically calculated and compared with its experimentally obtained values. The variation of GPC with OH concentration is also presented.

Chapter 5 describes the details of preparation of alumina (Al_2O_3) thin films by Atomic Layer Deposition (ALD) technique. Optimized deposition parameters for getting high quality films and compositional analyses of the samples using EDS and XPS. XRD results are described, here. Surface morphology studied of the sample using SEM, FESEM and AFM. Are also presented in this chapter.

Chapter 6 deals with fabrication and characterization of $Al/Al_2O_3/p$-Si MOS capacitors. The electrical and dielectric properties of MOS structures were studied from Capacitance-Voltage(C-V) and conductance-Voltage (G-V) characteristics. The frequency, bias voltage and temperature dependence of electrical and dielectric properties of the above structure were studied in detail, results and analysis are included here.

Chapter 7 presents the details of an investigation on the formation of alumina nano particles on the cold wall of ALD System. As nano particle find important technological applications, we have investigated then further and results are presented here. An explanation for their formation based on physical sorption mechanism is also included in this chapter.

The summary of the research work and the relevant results obtained from the present study are outlined in the concluding section. The scope for future work is also presented.

Part of the thesis has been published in the following Journals:

- Studies on the adsorption of aluminium and methyl groups on silica for TMA/H_2O process in atomic layer deposition of aluminium oxide nano layers, **Anu Philip**, Rajeev Kumar, Bull. Mater. Sci (2010) 33, 2, pp 97–102.
- Explanation for the appearance of alumina nanoparticles in a cold wall Atomic Layer Deposition system and their characterization, **Anu Philip**, Subin Thomas, Rajeev Kumar, Vacuum (2010) 85 ,pp 368-372.
- Design and fabrication of automated plasma enhanced atomic layer deposition system for the deposition of ultra thin dielectric films, **Anu Philip**, Johney Issac, K. Rajeev Kumar, Jl. of Instrum. Soc. of India (2010) 40, 4, pp 311-14.
- Effect of frequency and bias voltage on the electrical and dielectric properties of Al/Al_2O_3/ p-Si MOS structure at room temperature (under review)
- Temperature dependence of electrical and dielectric properties of MOS devices constructed by atomic layer deposited Alumina on p-Si (communicated).
- Calculation of growth per cycle (GPC) of atomic layer deposited aluminum oxide nanolayers and dependence of GPC on surface OH concentration (communicated)

Other publications to which author has contributed

- Iodization of antimony thin films: XRD, SEM and optical studies of nanostructured SbI_3, D. Bharathi Mohan, **Anu Philip,** C.S. Sunandana, Vacuum (2008) 82,6 pp 561-565.

Conferences papers

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- "Influence of frequency on the dielectric properties and ac conductivity of $Al/Al_2O_3/p\text{-}Si$ (MOS) capacitor", The 55th DAE-Solid State Physics Symposium (DAE - SSPS 2010) Manipal, India (2010).
- "Electrical Characterization of high-k Aluminum Oxide gate dielectric prepared by atomic layer deposition ", National conference on Nanophotonic Materials (NCNM)" Cochin, India (2008).
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1

High-k Dielectrics for Gate Oxide Applications

1.1 Introduction

Microelectronics has undergone enormous development in recent years with an ever increasing performance of integrated circuits. This development has been made possible by modern CMOS technology, notably the down-scaling of transistor dimensions that leads to an exponential increase in the number of transistors on a chip. The downscaling and performance improvement of transistors have so far followed a trend predicted by Gorden. E. Moore, the Intel cofounder, in 1960's. However this may become difficult in the very near future due to a number of issues related to excessive power consumption and heat generation in integrated circuits. Therefore, the semiconductor industry is looking for alternate performance boosters, in particular by introducing new materials and new device architecture in place of traditional, standard silicon CMOS technology.

In order to be well-prepared with options to continue scaling during such a scenario, nearly a decade of research and development has been conducted by various groups. The different approaches include, introduction of high - k gate dielectric, low-k interconnects, replacement of bulk silicon with strained silicon-on-insulator (sSOI), high mobility channel material like germanium, GaAs, graphene etc. and non planar CMOS device structures like FinFET.

As the scaling has clearly reached fundamental material limits, especially for gate oxide, further scaling can be realized only by introducing new materials with higher k values. If the thickness of the standard SiO_2 based gate dielectric drops below the tunneling limit, gate leakage current will increase tremendously. For an oxide thickness of 1.5 nm at 1.5 V the leakage current density would be $100 A/cm^2$ which is obviously undesirable

for low power applications [4]. To prevent tunneling currents, physically thicker dielectric layers are required. As the gate dielectric become physically thicker, transistor requires a material with high dielectric constant to maintain its electrical characteristics. In 2007 a hafnium based high-k dielectric material was introduced for the first time by Intel.

1.2 Evolution of semiconductor devices

In 1947 W. Shockley, J. Bardeen and W.H. Brattain at the Bell Laboratory invented the bipolar transistor. The invention of the transistor, a solid state amplifier, resulted in a revolution in the field of semiconductor devices. J. Kilby at Texas Instruments first demonstrated the concept of Integrated Circuits (IC) in 1959. This concept together with the fabrication of the first Metal Oxide Semiconductor Field Effect Transistor (MOSFET) by D. Kahng and M.M. Attala in 1960 provided the basis for the evolution of microelectronics industry.

The principle of a surface field effect transistor was already proposed in the early 1930's by Lilienfeld and Heil. The experimental verification of the surface field effect, however, could not be demonstrated for more than 30 years. Since then, the MOSFET has become by far the most important electronic device for very large scale integrated (VLSI) circuits such as microprocessors and semiconductor memories. Scaling of solid-state devices results in cost effectiveness and improves performance and power consumption. This has historically given companies with the latest technology a large competitive advantage in the market. As a result, over the last four decades the microelectronics industry has scaled transistor feature size from 10μm to ~22 nm [1-6]. This reduction in feature size was in accordance with the prediction made by Gorden. E. Moore in 1965, which later became famous as Moore's law. It states that the number of transistors on a chip will double every two years [7-8]. Figure 1.1 shows the Moore's law plot of CPU transistor count against the date of introduction [9].

Figure 1: Moore's law - plot of CPU transistor counts against dates of introduction

In 1971 Intel introduced their first microprocessor 4004 which contained only 2300 transistors with 10μm technology. This was followed by 8008 having 3500 transistors in 1972 and by Pentium 4 in 2000 with 4.2 million transistors. Semiconductor industry was aware of the scaling limits and began a search for alternative methods by 1990's. In 2002 Intel unveiled several technology breakthroughs including the 90nm [10] process technology, strained silicon, high-speed copper interconnects and new low-k dielectric materials. With these and allied technologies the industry was able to follow the Moore's law up to a transistor count of 188 million per chip and minimum feature size of 60nm.

During certain periods, there were major changes within the industry as it moved from Si bipolar to p-channel metal-oxide semiconductor (MOS), then to n-channel MOS, and finally to complementary MOS (CMOS) planar transistors in the 1980s, which has remained as the dominant technology for the past three decades. The big challenge in going forward is that the end of planar CMOS transistor scaling is almost near as the transistor size has approached few nanometers and it is unclear how the industry is going to evolve after reaching this limit.

The introduction of high-k gate oxide in 2007 was a breakthrough in microelectronics as Intel developed 45nm technology processors with hafnium based material as gate dielectric. Today, nano-electronics is the most successful commercial manifestation of the nanotechnology, with the 32nm CMOS technology in volume production with 2.6 billion transistors and 22nm processor introduced 3D transistors. Currently, research is being conducted towards integration of CMOS devices below 22 nm.

1.3 Relevance of high-k materials in microelectronics

The dramatic performance improvements in microelectronics over the past few decades have been accomplished by severe reduction in the size of memory and logic devices. The capacitance density (C/A) is directly proportional to k value and inversely propositional to thickness of the dielectric layer as given by the equation:

$$\frac{C}{A} = \varepsilon_o k / t_{ox} \qquad 1.1$$

where t_{ox} and k are the thickness and relative dielectric constant of the high-k material respectively.

Scaling demanded drastic decrease of the SiO_2 thickness to achieve ever-higher capacitance densities. Fundamental limits of SiO_2 as a dielectric material, imposed by electron tunneling, will be reached as the film thickness approaches ~1 nm. This thickness is already at a level where severe problems start to occurring .At thickness the dielectric will not be able to effectively withstand voltages and tunneling current. Another problem related to the SiO_2 scaling is reliability; the requirements for reliability are even more difficult to meet than the leakage current requirements. The solution for the aforementioned problems related to SiO_2 scaling is to select a gate dielectric with a higher permittivity than that of SiO_2 (k =3.9) which can provide a lower equivalent oxide thickness at higher physical thickness.

The equivalent oxide thickness (*EOT*) of a material is defined as the thickness of the SiO_2 layer that would be required to achieve the same capacitance density as the high-k material in consideration. *EOT* is thus given by

$$EOT = \left(\frac{3.9}{k}\right) * t_{ox} \qquad 1.2$$

Numerous high-k materials ranging from Al_2O_3 ($k \sim 9$) to perovskites ($k \sim$ 102–104) are being actively investigated, in order to identify a long term promising material. However, finding a suitable high-k material is a major challenge because the selected material must have a higher resistivity, act as a good barrier layer, be thermally stable, and form an ideal interface with silicon. SiO_2 films can be conveniently formed via oxidation of the silicon substrate. In contrast, high-k materials must be formed by deposition. Atomic layer deposition (ALD) has emerged as a very promising technique for depositing high-k thin films for the microelectronics industry. ALD can deposit films with atomic layer thickness control and can conformally coat high aspect ratio structures. Most high-k dielectric materials have been

successfully deposited by ALD [11]. ALD is also very well suited for depositing various types of composites that combine the desirable properties of different materials.

1.4 Material requirements for high-k gate dielectrics

There is a set of material and electrical requirements for a viable alternate high-k gate dielectric material [1,12,13]. Major requirements include:

- Larger energy band gap with higher barrier height to Si substrate and metal gate to reduce the leakage current.
- Large k value.
- Good thermodynamic stability on Si to prevent the formation of a low-k SiO_2 interface.
- Good kinetic stability
- High amorphous-to-crystalline transition temperature to maintain a stable morphology after heat treatment.
- Low oxygen diffusion coefficients to control the formation of a thick low-k interface layer.
- Low defect densities in high-k bulk films and at the high-k/Si interface with negligible C-V hysteresis (< 30 mV).
- Low fixed charge density ($\sim 10^{10} cm^{-2} eV^{-1}$).
- Low high-k/Si interface state density ($\sim 10^{10} cm^{-2} eV^{-1}$).
- High enough channel carrier mobility (~90% of SiO_2/Si system).
- Good reliability and a long life time.

In addition, the new high-k gate dielectric material must be compatible with current CMOS fabrication process flow and other materials used in the CMOS integrated circuits. In the following sections the most important high-k requirements are discussed in detail.

1.4.1 Dielectric constant, Energy gap and Barrier height

To date, however, there is no single material that is capable to satisfy all the requirements for an ideal gate oxide. It is crucial to use a material with a high dielectric constant (k) value to replace SiO_2 as the gate dielectric material.

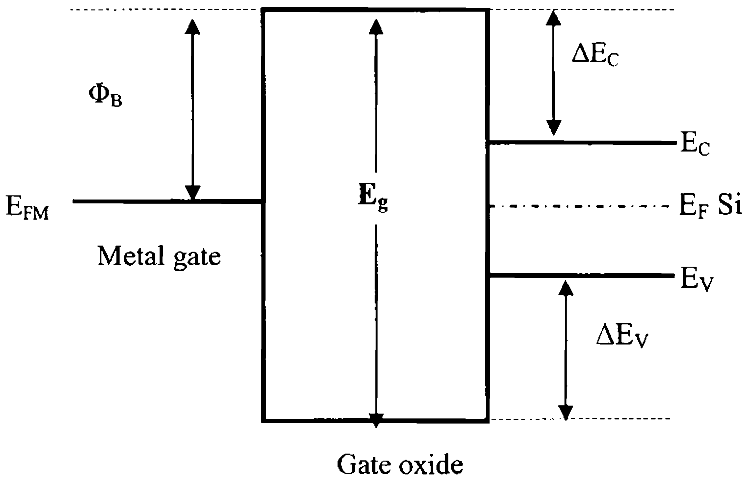

Figure 1.2: Shows a schematic band diagram of a MOS structure

Figure 1.2 shows the energy band diagram of a MOS structure where E_g indicates band gap. A small energy band gap is usually equivalent to a small barrier height for the tunneling process. When electrons travel from gate to Si substrate, the barrier height will be the potential difference between the gate and dielectric (Φ_B); when electrons travel from the Si substrate to the gate, the barrier height will be the conduction band offset of the dielectric layers to Si (ΔE_c). For an electron direct tunneling conduction mechanism, the leakage current density through thin gate dielectric will increase exponentially with the decrease of barrier height [14-16]. Therefore, a high-k gate dielectric material with a large conduction band offset to Si will be preferred to avoid an unacceptable high leakage current through the gate dielectric.

Simple metal oxides with a conduction band offset less than 1.0eV will be inappropriate for the gate dielectric applications with a Si substrate. Robertson *et.al.* theoretically calculated the energy band gap and band offsets of many high-k gate dielectric materials [17-18]. Energy band gap and band offsets of different high-k materials are included in Table 1.2. In gate dielectric materials, there is a general tendency of inverse correlation between the band gap size and the dielectric constant [6], so that it becomes difficult to meet the leakage current requirement.

1.4.2 Thermodynamic stability

A potential gate oxide insulator must be thermodynamically stable on silicon surface. Current microprocessor device fabrication process usually take place at high temperatures (>1000^0 C). During this process the dielectric must remain in a solid state. If a thin high-k gate dielectric material is thermodynamically unstable on Silicon, it tends to react with Si at an elevated temperature and an interface layer will be formed between the high-k layer and Si substrate. This interface layer usually has a low k value and acts as a series capacitor with the high-k dielectric layer. This low-k interface will deteriorate the electrical properties of the final high-k gate stack structure.

1.4.3 Kinetic stability

The new high-k material should be compatible with existing process conditions. Assuming we choose an amorphous oxide material, this requires that the oxide remains amorphous when annealed up to 1000°C for 5 seconds. This is strenuous condition in that SiO_2 is an excellent glass former but most other high-k materials are not. Aluminum Oxide (Al_2O_3) is a reasonably good glass former and is the best. Ta_2O_5 is moderately good glass former, but was eliminated because it is reactive. All other oxides crystallize bellow 1000°C. This problem can be overcome by alloying the desired oxide with a glass former like SiO_2 or Al_2O_3 giving either a silicate or aluminate. This is how the industry now retain the stability against crystallization close to 1000°C .

1.4.4 High quality interface

SiO_2-Si interface offers the best interface quality (interface trap density D_{it}~$10^{10}eV^{-1}cm^{-2}$) for the Si channel area of the MOSFETs. A comparable interface quality will be expected between the high-k gate dielectric and Si. However, almost all high-k materials exhibit one or two orders of magnitude high interface state density and significant flat band voltage shift (ΔV_{FB}), mainly due to a high fixed charge density. The origin of the high interface defect density is still under intensive investigation. Lucovsky et al. [19] reported that bonding constraints of the high-k materials may play a significant role in determining high-k/Si interface quality. Experimental results showed that if the average number of bonds per atom is over 3 for a metal oxide, an over-constrained high-k/Si interface will form and the D_{it} will increase exponentially. Similarly, a metal oxide with a low coordination number will form an under-constrained high-k/Si interface, which will also lead to a high interface state density and poor device performance. In addition, formation of metal silicide at the interface will also generate unfavorable bonding conditions to the device characteristics. Ideally, no metal oxide or silicide should be present at or close to the SiO_2/Si interface. In addition, the gate oxide/Si substrate interface must have minimum oxide fixed charges and interface trap charges to minimize carrier scattering at the channel (to maximize mobility). Amorphous layers are generally preferred for gate oxides to minimize electrical and mass transport along the grain boundaries and therefore to minimize the gate leakage current.

1.4.5 Amorphous-to-crystalline transition temperature

A polycrystalline gate dielectric layer will suffer a high leakage current because their grain boundaries may serve as a leaky path [19-20]. Variation in the grain size and crystal orientation of the polycrystalline films may also cause a non-uniform dielectric property within the dielectric films, which will become a reliability concern for practical application. Although single crystal oxides may theoretically solve the problems caused by grain boundaries and provide films with good quality, at present they can only be

grown by molecular beam epitaxy (MBE) deposition method [21,22]. It will be a great challenge to incorporate MBE deposition into the traditional CMOS fabrication process flow due to the inherent low throughput. In contrast, high quality amorphous high-k gate dielectrics can be easily deposited by commercial ALD equipment. Amorphous high-k gate dielectric layers will also offer reproducible and isotropic dielectric properties. Almost all metal oxides of interest tend to crystallize either during deposition or after heat treatment. For traditional CMOS fabrication process flow, heat treatment above 1000°C will be needed for the source/drain and poly-Si dopant activation after ion implantation. Therefore, an amorphous-to-crystalline transition temperature above 1000°C will be required. For example, HfO_2 and ZrO_2 will crystallize at very low temperature (~500°C) [23-24]. Of all the high-k candidate materials, only Al_2O_3 can stay amorphous at 1000°C temperature. However, Al_2O_3 does not have a sufficient high dielectric constant (k) value, adding a third element into the material may increase the amorphous-to-crystalline transition temperature [25]. For example adding a small layer of Al_2O_3 with HfO_2 layer will enhance crystallization temperature of HfO_2.

1.5 High-k materials

The choice of a material with higher dielectric constant than silicon dioxide can give the same equivalent oxide thickness with a higher physical thickness. Several high-k materials were identified suitable for gate oxide but many of them did not have all the desired properties. High-k materials under investigation include Al_2O_3, Y_2O_3, CeO_2, HfO_2, ZrO_2, Ta_2O_5, TiO_2, La_2O_3, and Nb_2O_5. The dielectric constants of these ALD grown films vary from 3.9 to 300. Searching for the best high-k candidate is not an easy task since each of these materials does impose some challenges. Table 1.2 lists the major high-k candidates and their properties.

Material	E_g (eV)	k- value	ΔEc (eV)	ΔEv (eV)	Stability with Si	Crystal structure	Ref.
SiO_2	9	3.9	3.5	4.4	yes	Amorphous	[1,2]
Si_3N_4	5	7.5	2.4	1.8	yes	Amorphous	[1,2]
Al_2O_3	8.7	8.5-10.5	2.8	4.9	yes	Amorphous	[26-29]
Ta_2O_5	4-4.5	20-35	0.3	3.1	no	Orthorhombic	[37-40]
TiO_2	3-3.5	30-100	1.2	1.2	yes	Tetragonal	[1,6,27,42,44]
$BaSrTiO_3$		200-300			no		[47]
La_2O_3	4.3	27	2.3	0.9	yes	Hexagonal, Cubic	[1,41]
Y_2O_3	5.6	12-20	2.3	2.6	yes	Cubic	[1,30]
CeO_2	5.5	26					[31-33]
HfO_2	5.7	35	1.5	3.4	yes	Monoclinic Cubic, Tetragonal	[34]

Table 1.2: Leading high-k candidates with their properties

Material	Eg (eV)	k- value	ΔEc (eV)	ΔEv (eV)	Stability with Si	Crystal structure	Ref.
ZrO_2	5.8	25	1.4	3.3	yes	Monoclinic Cubic, Tetragonal	[34-36]
$Hf_xSi_{1-x}O_y$	6	15-25			yes		[50]
$Zr_xSi_{1-x}O_y$	6	15-25	1.5	3.4	yes		
$SrTiO_3$		300			no	Cubic	[4,47-49]
$SrZrO_3$	5.4	180			no		[47-49]
Gd_2O_5	5.4	12-23	3.2	3.9	yes	Amorphous	
Sr_2TiO_4	5.2	50			no		[56-57]
$LaAlO_3$	5.7	25	1.8		yes		[51]
Nb_2O_5		50-200			no		[43,45,46]

Table 1.2: Leading high-k candidates with their properties

1.6 Major applications of high-k materials

High-k materials have a wide array of applications other than gate oxides. Some of their important applications are listed below:

- Storage capacitor dielectrics
- Pinhole-free passivation layers for OLEDs
- High aspect ratio diffusion barriers for Cu interconnects
- Adhesion layers
- Highly conformal coatings for micro fluidic and MEMS applications
- Coating of nano-porous structures
- Other nanotechnology and nano-electronic applications.
- Fuel cells, e.g. single metal coating for catalyst layers
- Bio MEMS
- Electroluminescence
- Protective coatings

1.7 Process issues for gate stack fabrication

Not only the specific deposition technique but the pre-deposition surface clean and post-deposition treatments also play a remarkable role in device performance. The pre-deposition clean includes standard cleaning 1 (SC-1) for removing any organic contaminants by oxidation, standard cleaning 2 (SC-2) for removing metallic (ionic) contaminants on the wafer, and dilute HF dip for removing native oxide present on the wafer substrate. Post high-k deposition anneal (PDA) in N_2 at mild temperature (600°C-700°C) and forming gas (90% N_2+10% H_2) annealing at 400° C are helpful to improve the high-k quality and reduce the leakage current for a given physical thickness [52-53]. However, the trace amount of oxygen in an inert ambient anneal during high-k PDA can be sufficient to cause the low-k interfacial layer growth at the high-k/Si interface [54-55]. An NH_3 anneal prior to high-k deposition was proposed to minimize the low-k interfacial layer growth during high-k PDA [56]. Deposition of passivation layers also help to reduce interface effects.

1.8 Status of the work

Atomic layer deposition (ALD) technique, which is considered to be the choice of technology for dielectric deposition in chip manufacturing and other applications is well developed Internationally especially in North Europe, South Korea and US. But the contribution of India in this important field is little. In 2008 Cambridge Nanotech-a leading ALD supplier announced that the shipment of its 100th ALD System to the Tata Institute of Fundamental Research (TIFR) in Mumbai, India and this was the first commercial system in India. At national level ALD high-k works are going on mainly at Indian Institute of Science, Bangalore and RRCAT Indore. Therefore it is of utmost importance to initiate and scale up the activities in ALD and high-k research in the country to understand the process, to develop facility and to generate man power in this field.

1.9 Motivation for the present work

Based on the above discussions it is clear that high-k materials are promising for microelectronic devices. There are a number of materials with k value much higher than SiO_2. Aluminum Oxide (Al_2O_3) is one high-k candidate having overall superior behavior for MOSFET application, except its comparatively low k value. Even though there are many materials having higher k values, investigations reveal that they are far behind Al_2O_3 in many aspects. For example Hafnium oxide has a higher k value but it always has stability and interface problems. Therefore Al_2O_3 has its own role in every high-k stacks to reduce their negative characteristics just like a passivation layer. The potential of this material is not yet revealed completely and compounds of Al_2O_3 with higher-k materials are under investigation for gate oxide and super capacitor applications.

The great challenges which are still open and day to day dramatic improvements in this field make us curious about the evolution of nano field effect transistors and about the best suited deposition technique 'ALD'. Semiconductor processing has been one of the main motivation for recent developments in ALD which can easily fabricate thin films on various substrates like silicon, Ga-As, Ge, graphene, and polymers.

In the present work Al_2O_3 samples were prepared by ALD, which is known as the technique for the future. The reason for choosing the well known-yet still to be explored Al_2O_3 as our material is given in the previous paragraph. We expect that this study would provide the basis for moving to high-k multi-compounds. The main objectives of the present work are as follows.

- Design, fabrication and perfection of a homemade Plasma Enhanced Atomic Layer Deposition System (PEALD).
- Optimization of system parameters in thermal and plasma mode.
- Atomic Layer Deposition of Aluminum Oxide thin films using TMA and Water. Optimizations of deposition parameters to obtain high quality films.
- Theoretical study on chemisorption mechanism involved during ALD of Al_2O_3 using TMA and water. Calculation of growth per cycle and its variation with OH concentration.
- Structural, compositional, optical and electrical characterization of Atomic Layer Deposited - Al_2O_3 thin films.
- Fabrication of MOS capacitors.
- Frequency and temperature dependence of Electrical and dielectric characteristics of MOS capacitors.

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2

Experimental Techniques for Deposition and Characterization of High-k Materials

This chapter presents the various deposition techniques used for the growth of high-k dielectric thin films. The various characterization tools employed for analyzing the films. are also described

2.1 Introduction

Growth techniques do play a solid role in physical and chemical characteristics of thin films as well as bulk powders. It is also observed that various physical constants, and characteristics of the thin films, are entirely different from that of the bulk material. The structural, electrical and optical properties of thin films are found to be highly sensitive to the technique adopted, the substrate chosen, deposition conditions, the presence of defects and impurities and the film thickness. The appropriate choice of an experimental technique thereby helps in tailoring a material with controlled, reproducible and well defined properties so as to suit a technological application. Once the films are grown, the structural, compositional, morphological, optical and electrical analytical tools give a better understanding of the film behavior and characteristics. On the reverse, these characterization techniques help in optimizing the growth conditions to get device quality films.

The present work was aimed at the growth of high–k dielectric material for Metal Oxide Semiconductor (MOS) capacitor applications. Atomic Layer Deposition technique was used for the oxide deposition. Thermal evaporation was used to deposit metal electrodes (aluminum) to complete the MOS structure. The present chapter also discuss about the various characterizations tools, which were used to optimize the properties of film as well as powder samples.

2.2 Deposition techniques for thin films

Thin film technology is one of the oldest arts and one of the newest sciences. Thin films have been used for more than half a century in making electronic devices, optical coatings, hard coatings, and decorative parts. A thin film has one of its linear dimensions very small compared to the other two and is characterized by a large surface to volume ratio. Any thin film deposition process involves the following sequential steps:

- Transition of the condensed phase (solid or liquid) into the gaseous state (atomic/molecular/ionic species)
- Transport of the vapor from the source to the substrate
- Condensation of the vapor upon arrival on the substrate

The deposition techniques are broadly classified into two - physical and chemical depending on how the atoms/molecules/ions/clusters of species are created for condensation process [1].

The properties of thin films can be governed by the deposition method. Almost all thin film deposition and characterization methods require either a vacuum or some sort of reduced-pressure ambient. Direct techniques like evaporation, sputtering, laser assisted deposition, chemical vapour deposition etc are widely used for thin film fabrication. The decisions of whether to evaporate, sputter, or chemically deposit thin films for particular application is not always obvious and has fostered a lively competition among these alternative technologies.

Various physical and chemical methods have been realized for thin film deposition of metal oxides. The main Physical methods involved are sputtering, thermal and electron beam evaporation, pulsed ion beam evaporation [2], pulsed laser deposition (PLD) and electrophoresis [3]. Spray pyrolysis [4, 5], dip-coating [6], chemical vapor deposition (CVD) [7], atomic layer deposition (ALD) [8] and sol-gel synthesis [9, 10] fall under the stream of chemical methods. CVD and ALD are the commonly used methods to deposit metal oxide thin films. Table 2.1 compares CVD and ALD to Physical techniques such as molecular beam epitaxy, sputtering, evaporation, and pulsed laser deposition.

Table 2.1: Comparison of various deposition techniques

Attribute	*CVD*	*ALD*	*MBE*	*S*	*E*	*PLD*
Thickness uniformity	Good	Good	Fair	Good	Fair	Fair
Film density	Good	Good	Good	Good	Poor	Good
Step coverage	Vary	Good	Poor	Poor	Poor	Poor
Interface quality	Vary	Good	Good	Poor	Good	Vary
# of Materials	Fair	Good	Good	Good	Fair	Poor
Low-temperature deposition	Vary	Good	Good	Good	Good	Good
Deposition rate	Good	Fair	Poor	Good	Good	Good
Industrial application	Good	Good	Fair	Good	Good	Poor

CVD -Chemical Vapour Deposition, ALD -Atomic Layer deposition, PVD-Physical Vapour Deposition, MBE -Molecular Beam Epitaxy , S - Sputtering, E- Evaporation, PLD- Pulsed Laser Deposition

The undisputed advantage that CVD and ALD offer over physical techniques is the ability to coat complex geometries due to their non line-of-sight process capabilities. Comparisons of other characteristics such as cost, complexity, environmental impact, compositional control, and deposition temperature are not as clear cut and depend upon the specifics of the application-driven process. In the present study we adopted ALD for depositing gate oxide material and thermal evaporation for metal electrode deposition. These techniques are discussed in detail in the following sections.

2.2.1 Atomic Layer Deposition

For future deposition of ultra-thin high-*k* materials, the need to deposit conformal films with precise thickness control becomes much more critical. ALD is a CVD-derived thin film deposition technique that appears

to be the most promising technique for the deposition of ultrathin films of high-k materials for future microelectronics applications [11-14]. ALD is based on the application of sequential, self-limiting surface reactions. ALD may be considered as a type of CVD where the gas phase precursors are introduced alternately instead of simultaneously.

Figure 2.1 illustrates the sequential, self-limiting surface reactions that define ALD. Two sequential surface reactions, A and B, produce the ALD thin film growth. Because there are only a finite number of chemical species on the surface, both reactions are self-limiting. The chemical species are exchanged during each surface reaction. In the A reaction, the gas phase precursor reacts with the chemical species left by the B reaction. In the B reaction, the gas phase precursor reacts with the chemical species left by the A reaction. ALD is achieved by repeating the surface reactions in an ABAB... sequence.

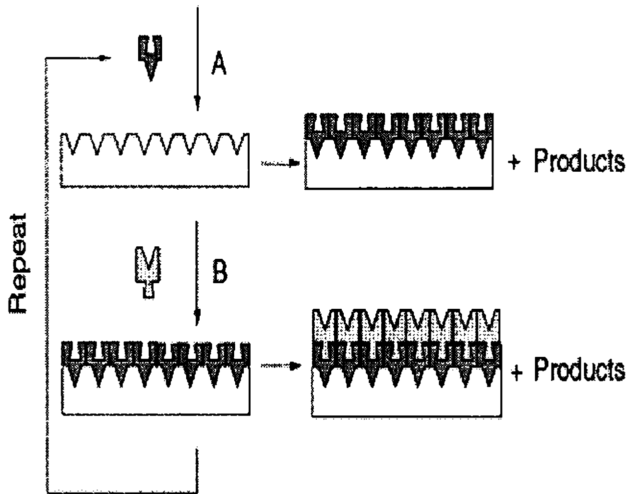

Figure 2.1: Two sequential, self-limiting surface reaction that define ALD

ALD does not require line-of-sight for deposition and high surface area to volume ratio structures and complex geometries can be conformally coated. ALD techniques exist for depositing a variety of substances including oxides, nitrides, and metals. A detailed discussion on ALD is included in chapter 3.

2.2.2 Thermal evaporation by resistive heating

Thermal evaporation is a simple and convenient technique widely used for the deposition of thin films of metals, alloys and many compounds. The process, in general, involves heating up of a source material until it evaporates and condenses on a cold target surface, referred to as the substrate. If carried out in vacuum, the evaporation temperature can be considerably lowered and the formation of oxides and incorporation of impurities in the growing layer can be minimized. Moreover, at pressures as low as 10^{-6} or 10^{-5} mbar, the mean free path of vapor atoms shall be of the same order as the vacuum chamber dimensions. Therefore, the particles can travel in straight lines from the evaporation source towards the substrate without being significantly scattered [15].

In thermal evaporation technique, the average energy of vapor atoms reaching the substrate surface is generally low. Here, a refractory metal (tungsten or tantalum) strip or shaped filaments are heated directly by attaching the ends to a low voltage, high current supply to evaporate the charge. The characteristics and quality of the deposited film shall depend on the substrate temperature, rate of deposition, substrate to target distance, base pressure, etc. The homogeneity of the film depends on the geometry of the evaporation source and the distance from the source material to the substrate. Excellent and detailed reviews on the know-how of the technique have been discussed by Holland [16].

2.3 Characterization tools

Structural, electrical and optical characterizations of the deposited thin films are done by various characterization tools. The following sections briefly describe various techniques that are used in the present study.

2.3.1 Thin film thickness

Thickness is one of the most important thin film properties to be characterized since it plays an important role in the film properties unlike a bulk material. Reproducible properties are achieved only when the film thickness and the deposition parameters are kept constant. Film thickness

may be measured either by in-situ monitoring of the rate of deposition or after the film deposition. The thicknesses of the thin films prepared for the present work was measured by stylus profiler (Dektak 6M) or by Spectroscopic Ellipsometry.

Stylus profiler

The stylus profiler takes measurements electromechanically by moving the sample beneath a diamond tipped stylus. The high precision stage moves the sample according to a user defined scan length, speed and stylus force. The stylus is mechanically coupled to the core of a linear variable differential transformer (LVDT). The stylus moves over the sample surface. Surface variations cause the stylus to be translated vertically. Electrical signals corresponding to the stylus movement are produced as the core position of the LVDT changes. The LVDT scales an ac reference signal proportional to the position change, which in turn is conditioned and converted to a digital format through a high precision, integrating, analog-to-digital converter [17]. The film whose thickness has to be measured is deposited with a region masked. This creates a step on the sample surface. Then the thickness of the sample can be measured accurately by measuring the vertical motion of the stylus over the step.

Ellipsometer

An ellipsometer can be used to measure the refractive index and the thickness of semi-transparent thin films. It can be used to measure film thickness ranging from 2 nm to several micrometers [18]. The principle of this instrument is to measure and simulate the changes in the polarization state of a light beam reflected from transparent layers, such as a dielectric layer. When a light transmits through a dielectric layer, the phase of the incoming wave will depend on the refractive index of the dielectric material.

Figure 2.2 is a schematic of the ellipsometer equipment and its reflection model. As shown in figure, an ellipsometer is made up of a laser source, a polarizer, a quarter wave plate, a detector, and an analyzer [19]. The quarter wave plate can provide a state of polarization which can be

varied from linearly polarized light to elliptically polarized light by varying the angle of the polarizer. After the beam is reflected from the high-k dielectric layer, it will be analyzed with the analyzer. It is noteworthy to point out that using an ellipsometer to measure the high-k film thickness is a fast and nondestructive method, which are its major advantages.

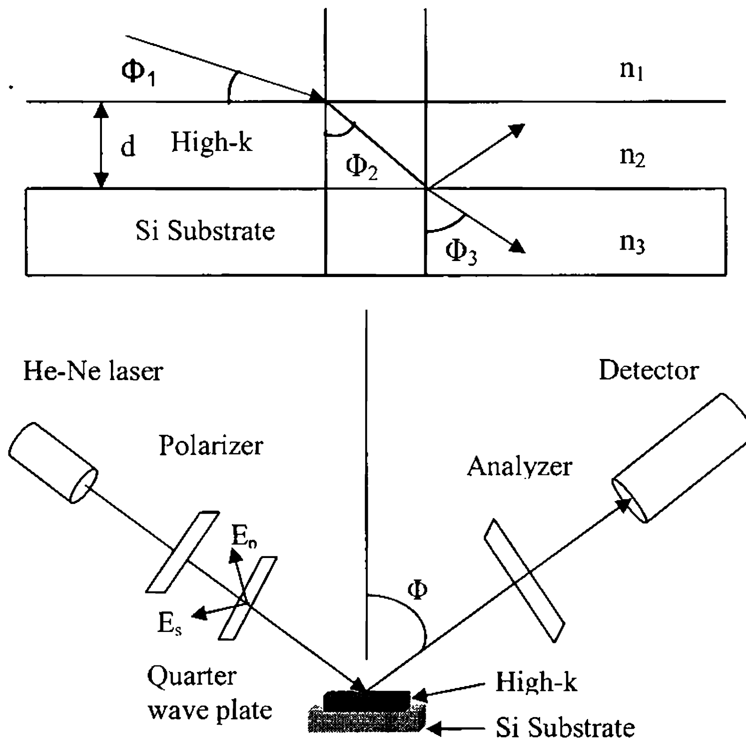

Figure 2.2: Schematic of an ellipsometer system and light reflection model.

2.3.2 Structural characterization

Powder X-Ray diffraction

The crystallographic or amorphous nature of a sample very well influences its electrical and optical properties. X-ray diffraction (XRD) studies are generally used for structural analysis. Any material has a characteristic diffraction pattern, whether present in pure state or as one constituent of a mixture of substances. This fact is made useful in the

diffraction method of chemical analysis. The advantage of the technique is that it discloses the presence of a substance, as that substance actually exists in the sample and not in terms of its constituent chemical elements. Hence, diffraction analysis is useful whenever it is necessary to know the state of chemical combination of the elements involved or the particular phase in which they are present. Compared with ordinary chemical analysis the diffraction method has the advantage that it is usually much faster, requires only very small quantity of sample and is non-destructive.

The basic law involved in the diffraction method of structural analysis is the Bragg's law [20]. When monochromatic beam of X-rays impinge upon the atoms in a crystal lattice, each atom acts as a scattering source. The crystal lattice presents a series of parallel reflecting planes to the incident X-ray beam. The intensity of the reflected beam at certain angles will be maximum when the path difference between two reflected waves from two different crystal planes is an integral multiple of λ. This condition is termed as Bragg's law and is given by,

$$2d\sin\theta = n\lambda \qquad (2.1)$$

where, n is the order of diffraction, λ is the wavelength of X-rays, d is the spacing between consecutive parallel planes and θ is the glancing angle [20].

X-ray diffraction studies give a whole range of information about the crystal structure, orientation, average crystalline size and stress in the powder. Experimentally obtained diffraction patterns of the sample are compared with the standard powder diffraction files published by the International Centre for Diffraction Data (ICDD).

In the present study, the thin film and bulk samples were structurally characterized by recording their XRD patterns. The filtered copper Kα radiation (λ = 1.5414 Å) was used for recording the diffraction pattern. The average grain size, t of the film can be calculated using the Scherrer's formula .

$$t = \frac{0.96\lambda}{\beta\cos\theta} \qquad (2.2)$$

Here, β is the full width at half maximum in radians.

Glancing angle x-ray diffraction (GXRD)

It is sometimes very difficult to analyze thin films due to their small diffracting volumes, which result in low diffracted intensities compared to the substrate and background. This combination of low diffracted signal and high background make it very difficult to identify the phases present. So, special techniques must be employed when analyzing thin films. The most common technique for analyzing thin films as thin as 100 Å is to use a grazing incidence angle arrangement. Glancing angle diffraction techniques are used when the information needed lies within a thin layer of the material [21].

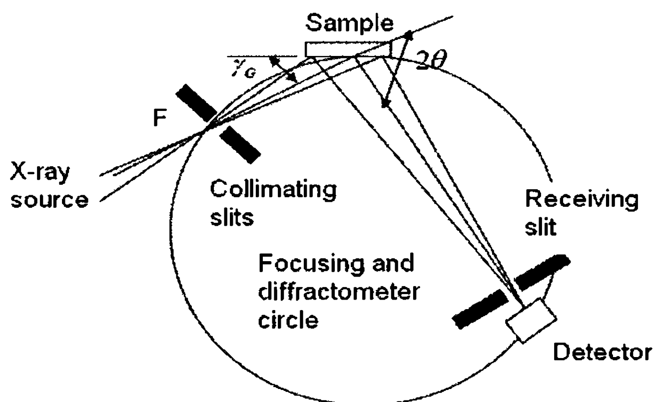

Figure 2.3: Seemann-Bohlin diffractometer. The point F is either the focal point on an x-ray tube or the focal point of a focusing monochromator.

Figure 2.3 shows Seemann-Bohlin parafocusing geometry which is commonly used in the study of thin films. For the Seemann-Bohlin geometry (Figure 2.3) the incident X rays impinge on a fixed specimen at a small angle, γ_G (typically 1° to 3°) and the diffracted X rays are recorded by a detector that moves along the focusing circle. This method provides good sensitivity for thin films, due to parafocusing and the large diffracting volume, which results from γ_G being small and the X-ray path length in the film being large (proportional to $1/\sin\gamma_G$). By increasing the path length of the incident X-ray beam through the film, the intensity from the film can be

increased, while at the same time, the diffracted intensity from the substrate can be reduced. Overall, there is a dramatic increase in the film signal to the background ratio. Since the path length increases when the grazing incidence angle is used, the diffracting volume increases proportionally. This is the reason for the increased signal strength. During the collection of the diffraction spectrum, only the detector rotates through the angular range, thus keeping the incident angle, the beam path length, and the irradiated area constant.

2.3.3 Morphological analysis

Surface morphology is an important property while going for multilayer device fabrication. Roughness of the thin film surface plays a vital role, especially while making interfaces. Some of the characterization tools used to study the surface of thin films is described below.

Scanning Electron Microscope (SEM)

The scanning electron microscope (SEM) uses electrons rather than light to form an image. SEM has several advantages over an ordinary light microscope [22]. The SEM has a large depth of field, which allows a large amount of the sample to be in focus at a time. The SEM also produces images of high resolution, which means that closely spaced features can be examined at a high magnification. Preparation of samples is relatively easy since most SEMs only require that sample should be conductive. If the sample is non conducting a thin layer of coating is necessary. The combination of higher magnification, larger depth of focus, greater resolution, and ease of sample observation makes the SEM one of the most heavily used instruments in current research areas.

In a typical SEM, electrons are thermionically emitted from a tungsten or lanthanum hexaboride (LaB_6) cathode and are accelerated towards an anode. Alternatively, electrons can be emitted via field emission. The most common is the Tungsten hairpin gun. Tungsten is used because it has the highest melting point and lowest vapour pressure of all metals, thereby allowing it to be heated for electron emission. A voltage is applied to

the loop, causing it to heat up. The anode, which is positive with respect to the filament, forms powerful attractive force for electrons. This causes electrons to accelerate towards the anode. The anode is arranged, as an orifice through which electrons would pass down to the column where the sample is held.

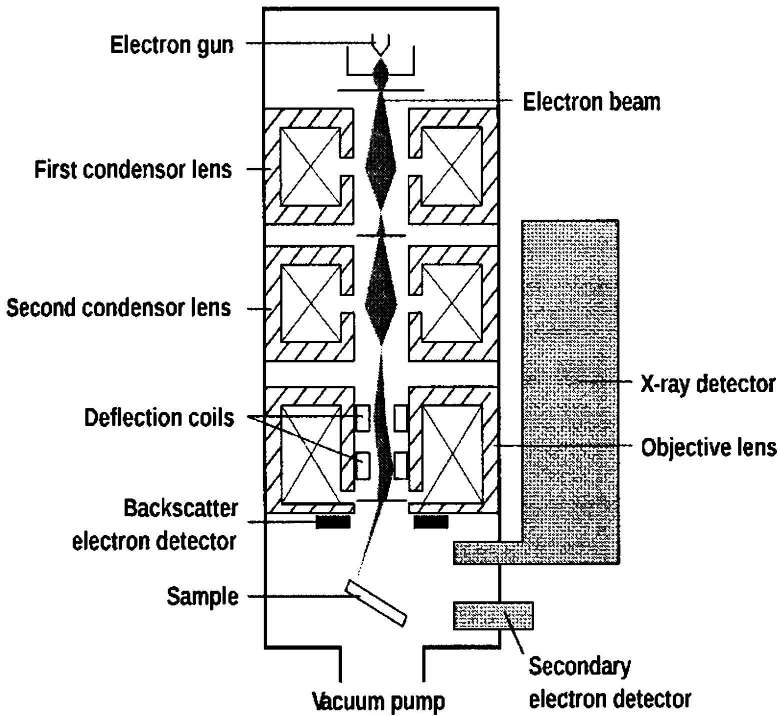

Figure 2.4: The schematic diagram of a SEM

The electron beam, which typically has an energy ranging from a few hundred eV to 100 keV, is attracted through the anode, is made to pass through a condenser lens, and are focused to very fine point on the sample by the objective lens (Figure 2.4). The electron beam hits the sample, producing secondary electrons from the sample. These electrons are collected by a secondary detector or a backscatter detector, converted to a voltage, and then amplified. The amplified voltage is applied to the grid of the CRT that causes the intensity of the spot of light to change. The image

consists of thousands of spots of varying intensity on the face of a CRT that correspond to the topography of the sample.

The spatial resolution of the SEM depends on the size of the electron spot, which in turn depends on the electron energy and the magnetic electron optical system which produces the scanning beam. To ensure that the information recorded in the image arises only from the sample surface, the column must always be at vacuum. Or else, there are chances for contamination of the sample and the electron beam, instead of being directed onto the sample, would induce ionization in any background gas that would affect the measurement being made on the sample. In the present work, JEOL JSM 6390 LV was used for SEM analysis.

Atomic Force Microscopy (AFM)

The atomic force microscope (AFM) is a very high resolution type of scanning probe microscope, with resolution of fractions of a nanometer, more than 1000 times better than the optical diffraction limit. It can, therefore, probe into the fine details of a sample surface [23].

In atomic force microscopy, a tip integrated to the end of a spring cantilever, is brought within the inter atomic separations of a surface, such that the atoms of the tip and the surface are influenced by inter atomic potentials. As the tip raster across the surface, it bounces up and down with the contours of the surface. By measuring the displacement of the tip (*i.e.* the deflection of the cantilever), one can theoretically map out the surface topography with atomic resolution.

The AFM is essentially identical in concept to the scanning profilometer, except that the deflection sensitivity and resolution are improved by several orders of magnitude. The AFM can operate well in ambient air or in a liquid environment making it an important tool in studying biological systems, polymers, insulators and semiconductor materials. Two important modes of an AFM are contact mode and the tapping mode. In the contact mode, the static tip deflection is used as the feedback signal. In the tapping mode, the cantilever is externally oscillated at or close to its resonance frequency. The oscillation amplitude, phase and

resonance frequency are modified by tip-sample interaction forces; these changes in oscillation with respect to the external reference oscillation provide information about the sample's characteristics.

The AFM provides us with a true three dimensional surface profile compared to the two dimensional SEM image, with atomic resolution in ultra high vacuum environments. But an AFM can only image a maximum height of the order of micrometers and a maximum scanning area of around 150 by 150μm whereas SEM can image an area on the order of millimeters by millimeters with depth of field of the order of millimeters.

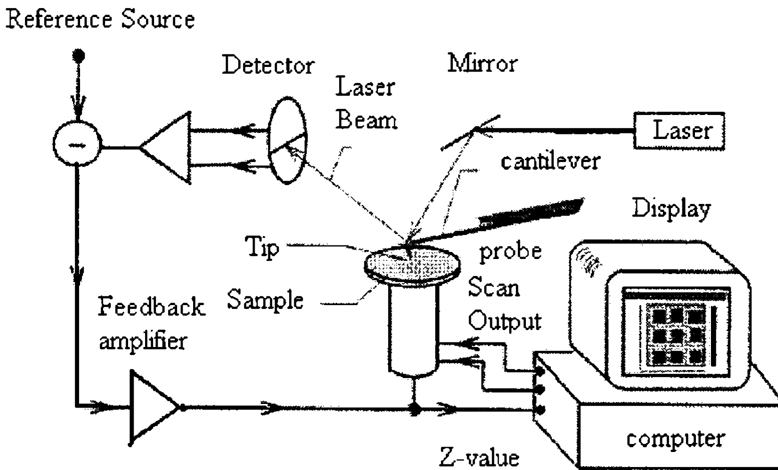

Figure 2.5: The essential elements of an AFM

Transmission Electron Microscopy (TEM)

Transmission electron microscopy (TEM) is an imaging technique whereby a beam of electrons is focused onto a specimen causing an enlarged version to appear on a fluorescent screen or layer of photographic film or to be detected by a CCD camera. The first practical transmission electron microscope was built by Albert Prebus and James Hillier at the University of Toronto in 1938 using concepts developed earlier by Max Knoll and Ernst Ruska. Electrons are generated by a process known as thermionic discharge in the same manner as the cathode in a cathode ray tube, or by field emission; they are then accelerated by an electric field and focused by

electrical and magnetic fields onto the sample. The electrons can be focused onto the sample providing a resolution far better than is possible with light microscopes, and with improved depth of vision. Details of a sample can be enhanced in light microscopy by the use of stains. Similarly with electron microscopy, compounds of heavy metals such as osmium, lead or uranium can be used to selectively deposit in the sample to enhance structural details. The electrons that remain in the beam can be detected using a photographic film, or fluorescent screen [24]. So areas where electrons are scattered appear dark on the screen, or on a positive image.

An additional class of these instruments is the electron cryomicroscope, which includes a specimen stage capable of maintaining the specimen at liquid nitrogen or liquid helium temperatures. This allows imaging specimens prepared in vitreous ice, the preferred preparation technique for imaging individual molecules or macromolecular assemblies. Another type of TEM is the scanning transmission electron microscope (STEM), where the beam can raster across the sample to form the image. In analytical TEMs the elemental composition of the specimen can be determined by analyzing its X-ray spectrum or the energy-loss spectrum of the transmitted electrons. Modern research TEMs may include aberration correctors, to reduce the amount of distortion in the image, allowing information on features on the scale of 0.1 nm to be obtained. Monochromators may also be used which reduce the energy spread of the incident electron beam to less than 0.15 eV.

From TEM images, size of the nanoparticles can be determined. Parallel lines in the high resolution transmission electron micrograph (HRTEM) represents planes in the crystal lattice and distance between them corresponds to d spacing. By comparing these d spacing values with the JCPDS data, one can identify the orientation of the planes in the synthesized material. Selective area electron diffraction (SAED) is the map of the reciprocal lattice which will also give the signature of various planes in which material has been grown. Depending on the crystalline nature of the material, the SAED pattern will be orderly arranged spots, distinguishable ring or fused rings. But in the case of quantum dots concentric rings were

observed in the SAED. The d spacing of the planes corresponding to the rings can be determined by the following equation

$$Dd = CL\lambda \quad (2.3)$$

Where L is the effective camera length, λ is the de-Broglie wavelength of the accelerating electrons, D is the ring diameter of a standard electron diffraction pattern and d is the inter planar spacing [24]. The term C in the right hand side of the equation is referred to as the camera constant. TEM, operating at an accelerating voltage of 200 kV was used for confirming nanoparticles in the present work.

2.3.4 Compositional analysis

Compositional analysis helps to check stoichiometry of the deposited films. Some of the characterization tools used in the present investigation is described below.

Energy Dispersive Spectrometer (EDS) analysis

Energy Dispersive Spectrometer (EDS) analysis is used for determining the elemental composition of a specimen. It often works as an integrated feature of SEM and cannot operate on its own without the latter [24, 25]. During EDS analysis, specimen is bombarded with an electron beam inside the scanning electron microscope. The bombarding electrons (primary electrons) collide with the specimen atoms knocking some of the electrons off in the process. The vacancy in the specimen atoms created by the ejection of an inner shell electron is eventually occupied by a higher energy electron from an outer shell. During this transition, the transferring electron gives up its excess energy in the form of X-rays

The amount of energy released by the transferring electron depends on which shell it is transferring from, as well as which shell it is transferring to. Furthermore, the atom of every element releases X-rays, unique in energy during the transferring process, characteristic of that element. Thus, by measuring the energy of X-rays emitted by a specimen during electron beam

bombardment, the identity of the atom from which the X-ray was emitted can be established.

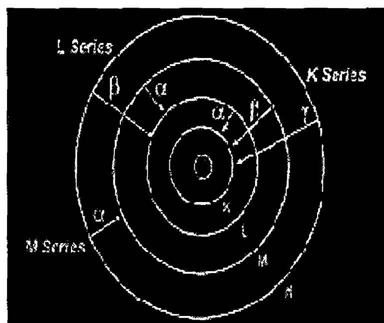

Figure 2.6 : The emission of X-rays during EDS

The output of an EDS analysis is an EDS spectrum, which is a plot of how frequently an X-ray is received for each energy level. An EDS spectrum normally displays peaks corresponding to the energy levels for which the most X-rays had been received. Each of these peaks is unique to an atom, and therefore corresponds to a single element. The higher a peak in a spectrum, the more concentrated the element is in the specimen. An EDS plot not only identifies the element corresponding to each of its peaks, but the type of X-ray to which it corresponds as well. For example, a peak corresponding to the amount of energy possessed by X-rays emitted by an electron in the L-shell going down to the K-shell is identified as a $K\alpha$ peak. The peak corresponding to x-rays emitted by M-shell electrons going to the K-shell is identified as a K_β peak as shown in figure 2.6. We have used JEOL Model JED – 2300 for EDS analysis.

X-ray Photoelectron Spectroscopy (XPS)

X-ray Photoelectron Spectroscopy is also known as electron spectroscopy for chemical analysis or ESCA. In XPS, radiation from an X-ray source strikes the sample. The deep inner shell electrons are excited and both core and valence band electrons are ejected with characteristic energy and release of x-ray photoelectrons [24,25].Electronic transitions are shown

in the Figure 2.7. Depending on the atomic structures, the wavelength of the X-ray will be different. Electrons emitted from atoms within a few atomic layers of the surface escape and are energy analyzed. Results provide quantitative and qualitative information about oxidation states of surface and near-surface atoms, surface impurities, and fundamental interactions between surface species. Standard XPS provides excellent chemical information but restricted spatial data. If, however, a lens with a narrow acceptance angle is placed at the energy analyzer's entrance, small area XPS (SAXPS) provides an image of surface features with a resolution of 280 pm.

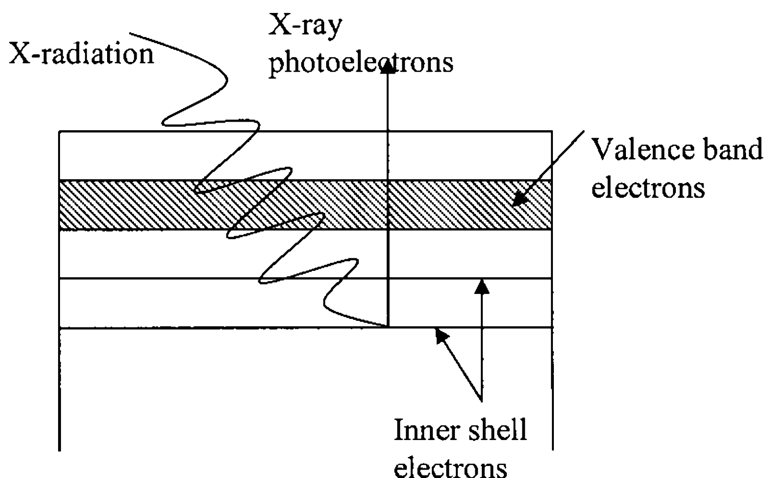

Figure 2.7: The electronic transitions due to the incident x-rays.

If the X-ray source is monochromatic, the electron's kinetic energy is used to measure its binding energy from the relation X-ray energy minus binding energy equals kinetic energy. The most common source creates X-rays by bombarding either Al or Mg targets with high energy electrons to produce 1486.6eV and 1253.6eV photons, respectively. Increasingly, synchrotron radiation (the tangential photon flux formed when high energy charged particles are deflected) is the source of choice. The photon energy, ranging from infrared to X-ray, is resolved by a monochromator into a monoenergetic, high flux beam that provides much greater experimental

flexibility than a fixed frequency X-ray source. XPS with Al Kα radiation source (1486.6 eV) was used in the present investigation.

2.3.5 Optical studies

Fourier Transform Infrared Spectroscopy

Fourier Transform Infrared (FTIR) spectroscopy is a measurement technique for collecting infrared spectra. Instead of recording the amount of energy absorbed when the frequency of the infra-red light is varied, the IR radiation is guided through an interferometer. After passing through the sample the detected signal is the interferogram signal. Performing mathematical Fourier Transform on this signal results in a spectrum identical to that from conventional (dispersive) infrared spectroscopy.

FTIR spectrometers are cheaper than conventional IR spectrometers because building interferometers is easier than the fabrication of a monochromator. In addition, measurement with a single spectrum is faster for the FTIR technique because the information of all frequencies is collected simultaneously. This allows multiple samples to be collected and averaged together resulting in an improvement in sensitivity. Because of its various advantages, virtually all modern infrared spectrometers are FTIR variety instruments.

We have used a Thermo Nicolet Avatar 370 FTIR instrument for part of the work presented in this thesis. The spectral range of this instrument is 7000 to 400 cm^{-1}. Its resolution is 0 9 cm^{-1} in the mid-IR range.

Transmission spectroscopy

Intrinsic optical absorption of a single photon across the band gap is the dominant optical absorption process in a semiconductor. When the energy of the incident photon (hν) is larger than the band gap energy, the excitation of electrons from the valence band to the empty states of the conduction band occurs. The light passing through the material is then absorbed and the number of electron hole pairs generated depends on the number of incident photons S_0 (ν) (per unit area, unit time and unit energy). The frequency ν is related to the wavelength λ by the relation, λ= c/ν, where

c is the velocity of light. The photon flux $S(x,v)$ decreases exponentially inside the crystal according to the relation

$$S_{(x,y)} = S_{o(v)} e^{-\alpha x} \tag{2.4}$$

where, the absorption coefficient α, ($\alpha(v) = 4\pi k\upsilon/c$) is determined by the absorption process in semiconductors and k is the extinction coefficient. For the parabolic band structure, the relation between the absorption coefficient (α) and the band gap of the material is given by [26],

$$\propto = \frac{A}{h\nu}\left(h\nu - E_g\right)^r \tag{2.5}$$

where, r = 1/2 for allowed direct transitions, r = 2 for allowed indirect transitions, r = 3 for forbidden indirect transitions and r = 3/2 for forbidden direct transitions. A is the parameter which depends on the transition probability. The absorption coefficient can be deduced from the absorption or transmission spectra using the relation,

$$I = I_0 e^{-\alpha t} \tag{2.6}$$

where, I is the transmitted intensity and I_0 is the incident intensity of the light and t is the thickness of the film. In the case of direct transition, from equation 2.5, $(\alpha h\nu)^2$ will show a linear dependence on the photon energy (hν). A plot of $(\alpha h\nu)^2$ against hν will be a straight line and the intercept on energy axis at $(\alpha h\nu)^2$ equal to zero will give the band gap energy. The transmissions of the thin films were recorded using Varian, Cary 5000 spectrophotometer in the present studies.

2.3.6 Electrical characterizations

Measurement Setup

In order to obtain the electrical properties of the high-k gate dielectric films and MOS structures, Capacitance-Voltage (C-V) and Current-Voltage (I-V) measurements were performed. An Agilent 4284A

precision LCR meter was used for high-frequency C-V measurement. A Keithly 485 pico-ampere meter and Agilent 4155C semiconductor parameter analyzer were used for I-V measurement. A Labview 6 program (National Instruments) was used to control the measurements and record the results. The measurement equipment setup for the C-V and I-V measurements is very important to obtain accurate measurement results. Since small gate electrode areas (10^{-3}-10^{-5} cm^2) are usually used for the MOS capacitors, only very weak electrical signals can be detected, for example in the present study the capacitance value was in a range of 10-100 pF and the leakage current value was in a range of 10-100 pA.

The probe station (Signatone S-1160) together with its wiring was encapsulated inside a light-proof Al-made black box to ensure a completely dark environment for measurement. The black box was electrically grounded to shield against environment and exterior interferences, such as electrical noises, light, heat, and vibration. A dry ambient should be ensured inside the black box because the moisture may induce a high leakage current. In addition, the cabling, cable routing, and the measurement chuck should also be carefully connected. A tri-axial gold-plated hot chuck and co-axial and tri-axial cables were connected with the probe station to improve the sensitivity of the electrical measurements.

Capacitance-Voltage (C-V) measurement

The Capacitance-Voltage (C-V) technique is the most commonly used tool for the electrical characterization of high-k gate dielectrics and metal gate electrodes. Many important electrical properties of high-k gate dielectrics, including dielectric constant, EOT, flat band voltage, fixed charges, bulk charges, and interface state density can be extracted from the high frequency (HF) C-V measurement. The work function of the metal gate electrodes can also be calculated from the C-V measurement by plotting the flatband voltage and EOT of MOS capacitors with various thicknesses. The inversion capacitance can provide the information of the Si substrate doping concentration. In addition, carrier generation- recombination lifetime can also be extracted by using C-t data. All of these electrical properties from the

C-V measurement may provide critical device and process information for high-k and metal gate research. The exact methods to extract MOS parameters from experimentally obtained C-V curve are explained detail in chapter 6.

During the C-V measurement, a small sinusoidal AC drive signal is superimposed on a linear DC voltage ramp to sweep over the bias range from accumulation region to inversion region. The frequency of this sinusoidal ac voltage can be varied from 20 Hz to 1MHz. A frequency (above 100 kHz) is commonly considered as the high frequency. Capacitance, conductance, and impedance values can be determined by selecting an appropriate equivalent circuit model for the device being characterized. Parallel mode was used to measure the differential capacitance (C_{dif}) and the conductance (G) at the same time. The impedance (Z) can be calculated based on the C_{dif} and G. The Agilent 4284A precision LCR meter applies the high-frequency drive signal through the metal gate electrode via probe needle. The measurement signal is picked up through the backside of the substrate, via the gold-plated chuck. The gold-plated chuck should be electrically floating to avoid diverting the drive signal to the ground. It should be noted that when the polarity of the measurement is reversed the drive signal is applied to the substrate and the signal is measured at the gate via the probe needle. The additional capacitance of the chuck on which the substrate rests will complicate the interpretation of the measurement data. Besides, the chuck itself will act as an antenna, which may pick up noise from the environment.

During a C-V measurement of the MOS capacitor, small-signal AC may lose energy due to the presence of series resistance. This serious resistance may cause serious errors while extracting the various MOS parameters from experimentally obtained C-V curve. Series resistance usually arises due to varies reasons such as the contact between the probe needle and gate electrode, native oxide on the metal gate, the contact between the Si and chuck, resistance of the bulk Si substrate, and non-uniform doping distribution of the bulk Si. Efforts such as buffered HF dip were made prior to the aluminum back deposition to minimize the series

resistance. Backside Al deposition improves the contact between the Si substrate to the gold-plated chuck. Si substrate resistance can also be reduced by using highly doped substrates. Despite all of these efforts, it is almost impossible to completely get rid of the series resistance effects on the C-V measurement. A series resistance correction is necessary before extracting any useful information from the C-V curves. A general approach of series resistance measurement and correction has been proposed by Nicollian et. al [27]. When the MOS capacitor is biased in an accumulation condition, the series resistance (R_s) and oxide capacitance C_{ox} can be calculated by the following relations, [27,28].

$$R_S = \frac{G_m}{{G_m}^2+\omega^2 {C_m}^2} \tag{2.7}$$

$$C_{ox} = C_m[1 + (\frac{G_m}{\omega C_m})^2] \tag{2.8}$$

where C_m and G_m are the experimentally measured accumulation capacitance and conductance and ω is the angular frequency. The absence of peak in the G-V curve means that series resistance produces the dominant loss, completely masking the interface loss. Hence by eliminating series resistance effect, corrected capacitance (Cc) and the corrected conductance (Gc) can be determined with calculated Rs by using the following relations [27,28]:.

$$C_C = \frac{({G_m}^2+\omega^2 {C_m}^2)C_m}{a^2+\omega^2 {C_m}^2} \tag{2.9}$$

$$G_C = \frac{({C_m}^2+\omega^2 {C_m}^2)a}{a^2+\omega^2 {C_m}^2} \tag{2.10}$$

Where $a = G_m - ({G_{ma}}^2 + \omega^2 {C_m}^2)R_s$

Current-Voltage (I-V) Measurement

DC Current-Voltage (I-V) Measurement is another important electrical characterization method. In this study we used both HP 485 pico-

ampere meter and HP 4155C semiconductor parameter analyzer for I –V analysis. I-V mainly used to measure the leakage current density and the conduction mechanism of the MOS capacitors with a high-k gate dielectric layer. In addition, they can also be used for some reliability characterization of the high-k gate dielectrics and metal gate electrodes, including time-dependent dielectric breakdown (TDDB), charge to breakdown (QBD), and stress-induced leakage current (SILC). The HP 4155C semiconductor parameter analyzer can also be used for quasi static C-V measurement.

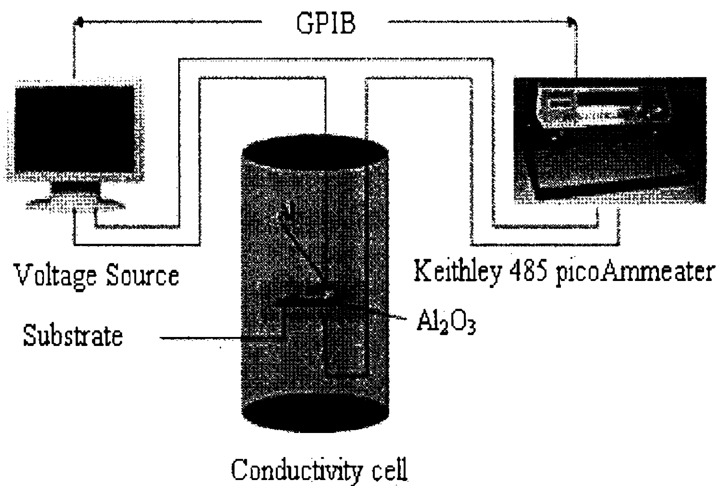

Figure. 2.8: Block diagram of I-V measurement set up

Figure 2.8 shows the block diagram of our I-V measurement set up. During the I-V measurement, a ramped or stepwise DC bias is applied on the top gate electrode of an MOS capacitor via the probe needle. The probe needle serves as both the DC bias source and current signal detector. A computer controlled ALSPC-02 data acquisition card is used as voltage source and Keithley 485 pico ammeter for current measurement. If a ramped DC bias is used, measured current may be contributed by two components - leakage current and displacement current. A slow ramp DC bias, e.g., 0.01V/second, should be used to minimize the displacement current component, especially when the leakage current is very small. If a stepwise DC bias is used, a relatively long delay time (1-2 seconds), is

preferred. However, if the delay time is too long, the DC bias will serve as a constant voltage stress, causing an excessive high leakage current due to electron trapping. In our experiments we chose a delay time of 100ms.

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3

Design and Fabrication of Plasma Enhanced Atomic Layer Deposition System (PEALD)

The first step towards accomplishing the objectives of present work is the design and fabrication of an ALD system and establishment of operating conditions to achieve deposition in ALD mode. This chapter gives the basics of atomic layer deposition and design, fabrication and optimization of the home made ALD system in detail.

3.1 Introduction

The design of a new system is the result of an engineer's imagination, shaped by a long list of known requirements and limitations of costs and construction. Several design revisions eventually result in the construction of an experimental system. During the fabrication and testing of an experimental system, the list of requirements is extended with (some) previously unknown items. In a research project with only one possibility to construct an experimental system, the challenge is to look beyond the newly found design requirements and focus on the research issues.

The semiconductor technology node is now undergoing a transition to 22nm and smaller dimensions. The thickness of the gate dielectric must also decrease with the decrease in gate length. The current trend in integrated circuit (IC) manufacturing, to decrease feature sizes while increasing aspect ratios and complexity, requires process control at atomic level. This can be easily attained by ALD. The drive for shrinking device dimensions has indeed contributed to the development of ALD which is presently experiencing major design breakthroughs. Already ALD has emerged as the method of choice for demanding applications [1]. This is evident from a rapidly increasing number of new materials, processes and reactor designs as well as users in both industry and academia.

3.2 Atomic Layer Deposition (ALD)

ALD is a modified form of chemical vapour deposition technique (CVD) based on alternating saturative surface reactions. As distinct from the chemical vapour deposition technique, in ALD the precursor vapours are pulsed into the reactor alternately, one at a time, separated by purge or evacuation. Each precursor exposure step saturates the surface with a monolayer of that precursor. The monolayer thickness is dependent on the reactivity of the precursor with the surface. This results in a unique self-limiting film growth mechanism with a number of advantageous features, such as excellent conformality, uniformity, and simple and accurate film thickness control.

Table 3.1: Alternative names for the ALD method.

Name	Acronym	Comments
Atomic Layer Epitaxy	ALE	original name, but should be used for epitaxial films only
Atomic Layer Deposition	ALD	general, covers all kinds of films
Atomic Layer Growth	ALG	like ALE, used less
Atomic Layer Chemical Vapour Deposition	ALCVD	emphasizes the relation to CVD
Molecular Layer Epitaxy	MLE	emphasizes molecular compounds as precursors
Digital Layer Epitaxy	DLE	emphasizes the digital thickness control
Molecular Layering	ML	dates back to Russian literature
Alternating Layer Deposition	ALD	emphasizes the alternating introduction of the precursors

ALD was developed in the late 1970s by T. Suntola and co- workers in Finland and introduced worldwide with a name of atomic layer epitaxy (ALE) [1-7]. The motivation behind developing ALD was the desire, to

make thin film electroluminescent (TFEL) flat panel displays. Since the mid 1990s, interest in ALD technology has increased rapidly in the silicon-based microelectronics industry. This interest is a direct consequence of the ever-decreasing device dimensions and the increasing aspect ratios in integrated circuits (IC). Traditional thin film deposition techniques such as chemical vapour deposition (CVD) and physical vapour deposition (PVD) are expected to meet major conformality problems during the next few years and now ALD is considered as a promising alternative candidate. At the same time, film thicknesses are shrinking so that ALD's major drawback, the low deposition rate, is becoming less important [8].

3.2.1 ALD cycle

In ALD, the film growth takes place in a cyclic manner. In the simplest case, one cycle consists of four steps:

(i) Exposure of the first precursor
(ii) Purge by gas flow, or evacuation of the reaction chamber
(iii) Exposure of the second precursor
(iv) Purge by gas flow or evacuation of the chamber

This cycle is repeated as many times as necessary to obtain the desired film thickness.

Figure 3.1 illustrates sequence scheme for a simple two precursor ALD cycle with each cycle consisting of four steps. (i) Exposure of precursor #1 which reacts with the surface in a saturating manner until a monolayer has been chemisorbed and no further adsorption take place. Since the reaction stops when one mono layer is formed, the process is called 'self-limiting'. (ii) Excess precursor and by-product is then evacuated or purged out. (iii) Exposure to precursor #2 leads to a reaction of precursor #2 with the already adsorbed mono layer of precursor # 1 on the surface in a second self-limiting reaction, thus depositing a second layer of atoms onto the first. The second reaction must also return the surface to a state in which it is ready to react with the first reactant. (iv) This is followed by another

evacuation or purge. Additional reactants having suitable complementary self-limiting reactions can be used to form ternary compounds, doped compounds, graded compositions, or nanolamination that can show properties that are dramatically improved over homogeneous materials [7-12].

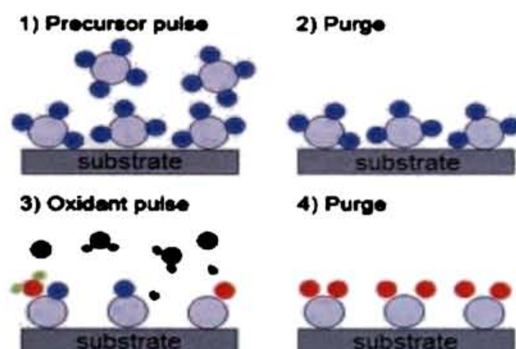

Figure 3.1: Schematic of an ideal four-step, two precursors ALD cycle.

The self-limiting growth mechanism gives ALD a number of advantageous features such as [6,12]:

- accurate and simple thickness control
- large-area and large batch capabilities
- excellent conformality
- no problems with varying vaporization rates of solid precursor
- good reproducibility
- straightforward scale-up
- capability to produce sharp interfaces
- favours precursors highly reactive toward each other, thus enabling effective material utilization and short cycle times
- high quality materials can be obtained at low processing temperatures
- capability to prepare multilayer structures (nano-laminates) in a continuous process

Most of the ALD processes reported are based on the above

described exchange reactions between molecular precursors. Another possible reaction type is additive with elemental precursors but because only a few metals are volatile enough, the applicability of these reactions is limited. A quite rare third reaction type, as well, involves a self-limiting adsorption of a precursor followed by its decomposition by an appropriate energy pulse or by its reduction using an appropriate reductant. In a majority of the ALD processes reported, the reactions are activated thermally under isothermal conditions.

The alternate pulsing or separate dosing of reactants is definitely the most characteristic feature of ALD and almost distinctive as the self-limiting growth mechanism of one monolayer. A common misconception is that ALD growth always proceeds in a layer-by-layer manner, but this is often not the case as only a fraction of a monolayer may be deposited practically in each cycle. Reasons for the less than a monolayer per cycle growth are the limited number of reactive surface sites and the steric hindrance between bulky ligands in the chemisorption layer [9]. Another important characteristic feature of ALD is its wide range of processing temperature window [12].

3.2.2 Variance of ALD

Though ALD was originated as a thermal method, several modifications were added as time passed. All the objectives were towards improving the film characteristics and lowering the deposition temperature. Two major ALD methods are thermal ALD and plasma assisted ALD.

Thermal ALD

Thermal ALD is the most researched type of ALD, because it mostly resembles CVD whereas the hardware configuration is also relatively simple. It typically consists of a heated vacuum chamber in which substrates are coated by the alternate pulsing of precursor vapours, separated by purge gas flows. The whole ALD processing cycle can often be regarded as a sort of "pulse-train", commonly referred to as "travelling wave". This pulse-train starts at one end of the reactor moves over the substrate surface, where deposition occurs, and disappears into the pump at the other end. Two reactor concepts currently exist: the cross flow concept, where the flow of

precursors is parallel to substrate surface; and the perpendicular flow concept, in which the precursors are introduced from the top of the reactor and flow perpendicular towards the substrate going downwards into the pump.

Figure 3.2: Thermal ALD reactor using cross flow concept.

Radical enhanced ALD

In Radical enhanced ALD, Thermal ALD hardware is adapted to include a remotely placed radical source. Plasma is created in the source at low pressure (<1.33mbar) from a source gas, most commonly being O_2, N_2, H_2, and mixtures thereof. It is attempted to deliver the generated radical species to the substrate surface, in a similar fashion as a normal precursor vapour dosing would be performed, i.e. via a tubular inlet.

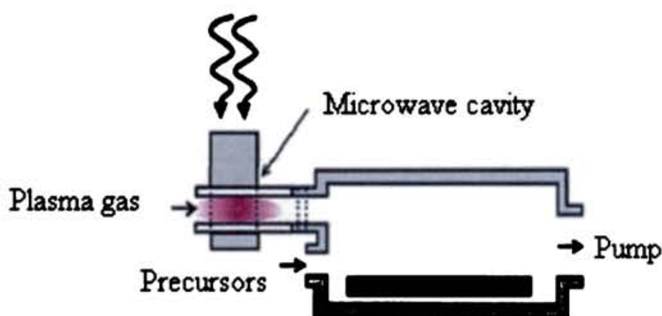

Figure 3.3: Radical enhanced ALD using microwave concept.

Direct plasma ALD

A common plasma configuration is the parallel plate concept, as shown in Fig. 3.4. The plasma is generated in between two parallel placed electrodes that are spaced ~1-5 cm apart, from a source gas at low pressure (1-0.013 mbar).

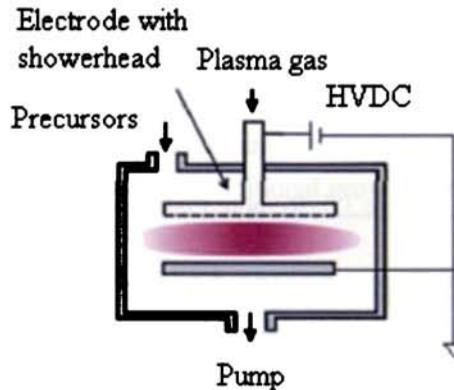

Figure 3.4: Direct Plasma ALD reactor using HVDC power

A RF (or a high voltage DC of the order of 1kV is applied, in this case called DC plasma) voltage is applied to the top electrode. The substrate is residing on the lower, grounded counter-electrode, and the substrate plays 'directly' a role in the plasma generation. To improve the uniformity of the plasma, the top electrode commonly consists of a showerhead gas distributor, through which source gases is fed into the plasma chamber. For the same reason, in some cases, the precursor is fed through the same showerhead.

Remote plasma ALD

Plasma is not in direct contact with the substrate in the remote plasma ALD. The configuration with a RF source for plasma is shown in figure 3.5. The distance between the plasma source and the substrate is few tens of cm. Figure 3.5 shows the schematic diagram of remote plasma set up.

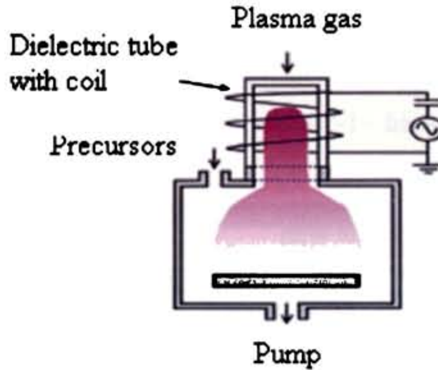

Figure 3.5: Remote Plasma ALD.

3. 2. 3 Advantages of Plasma Enhanced ALD (PEALD)

Thermal ALD method is the most popular method to deposit nano-scale thin films. But in some application areas, plasma is needed to improve film quality and process time. PEALD or Plasma Assisted ALD (PAALD) allows deposition at significantly lower temperature with better film properties compared to that of thermal ALD. At present, remote plasma ALD is used mainly for deposition on flexible substrates. In our lab we have developed a remote plasma ALD system by modifying a direct plasma ALD unit. Advantages and disadvantages of PEALD compared to thermal ALD are given in Table 3.1.

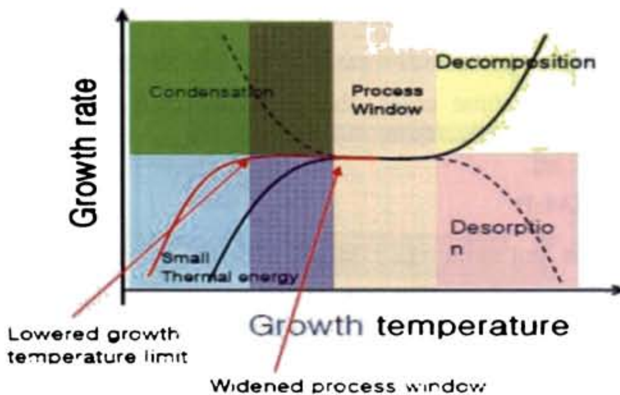

Figure 3.6: ALD process window

Table 3.1: Characteristic advantages of Remote Plasma ALD

Advantages	*Disadvantages*
Lower deposition temperature	More complicated chamber design
Broader no. of chemistry - possible	More complicated reaction - chemistry
Denser films	Potentially poor conformality
Higher throughput	Slower (not always)
In situ plasma treatments	Damage to films (not always)
Lower impurity	Additional growth parameters

Growth characteristics of PEALD are shown in Figure 3.6. When the ALD process is performed at temperatures which provide sufficient thermal energy for chemical reactions, the growth rate usually remains constant. This temperature range is often called the 'ALD process window'.

This nearly constant growth rate for a range of growth temperature during ALD provide better reproducibility in film thickness than other film deposition methods, such as chemical vapour deposition. However, at growth temperatures greater than this temperature range, the growth rate usually increases, caused by disturbances in the self-limiting process due to thermal decomposition of the precursor. However, for a few material systems, the growth rate decreases with increasing growth temperature which may be due to reduction in adsorption site density on the depositing surface.

The use of plasma generally reduces the growth temperature due to the high reactivity of radicals in the plasma. Due to lowered growth temperature the process window is effectively widened (Figure 3.6). There is a high degree of versatility in the materials used for PEALD. This is due to the high reactivity of radicals generated, which allows to perform many chemical reaction schemes which are impossible with thermal ALD. These two advantages make the remote plasma based technique superior than thermal ALD.

3.3 ALD precursors

Chemical film deposition processes are controlled by the choice of source materials. The chosen precursor can exist in the solid state, as liquids or in the vapour state. The choice of precursors is the key issue in a successful design of an ALD process. The main requirements for ALD precursors are [12]

- Volatility
- No self decomposition
- Aggressive and complete reactions
- No etching of the film or substrate materials
- Easy to synthesis and handle
- Un-reactive volatile by-products
- Sufficient purity
- Inexpensive
- Non-toxic and environment friendly

The precursors used in ALD can be divided in two main groups: inorganic and metalorganic. Metalorganic reactants can further be classified in to those containing a direct metal–carbon bond, that is, organometallic reactants [9,18] and those containing no direct metal–carbon bond. Typically, for inorganic reactants, elements and halides have been used; for organometallic reactants, alkyls and cyclopentadienyls have been used. For other metalorganic reactants, alkoxides, diketonates, amides, and amidinates have been used in ALD experiments. Table 3.2 summarizes which types of reactants have been used for which elements and it is clear that a wide range of precursors are available for almost all metals and nonmetals [9-15].

Table 3.2: Various metal reactants used in atomic layer deposition

Material	elements	halides	alkyls	cyclopentadienyls	alkoxides	B-diketonates	Alkylamides,silyl amides	amidinates
Mg	✓			✓		✓		
Mn	✓	✓				✓		
Zn	✓	✓	✓				✓	
Ga	✓	✓	✓			✓		
Cd	✓	✓	✓					
In	✓	✓	✓			✓		
Sn	✓	✓	✓					
Ti		✓			✓		✓	
V		✓			✓	✓		
Cr		✓				✓		
B		✓			✓			
C		✓						
Al		✓	✓		✓			
Si		✓	✓		✓			
Cu		✓				✓		✓
Ge		✓	✓					
As		✓						
Zr		✓		✓	✓	✓	✓	
Nb		✓			✓			
Mo		✓						
Sb		✓						
Hf		✓			✓		✓	
Ta		✓			✓		✓	
W		✓					✓	
Pb		✓			✓	✓		
Hg			✓					
Sc				✓		✓		
Sr				✓		✓		
Ni						✓		✓
Y				✓		✓		
Ru				✓		✓		

Pt	✓	✓		
Ca		✓		
Ba		✓		
La		✓		✓
Fe		✓		✓
Co		✓		✓
Pd		✓		
Ce		✓		
Pr			✓	
Nd		✓		
Sm		✓		
Eu		✓		
Gd		✓		
Dy		✓		
Ho		✓		
Bi			✓	

3.4 Design and fabrication of an automated plasma enhanced atomic layer deposition system

Our homemade plasma enhanced atomic layer deposition system consists of the following major parts:

1) Reaction chamber
2) Plasma chamber
3) Substrate holder and substrate temperature control system
4) Precursor delivery system including precursor pulsing
5) ALD sequence controller
6) Exhaust system

The deposition system is controlled by a computer, running a dedicated Visual Basic (VB) application. It is able to control and monitor all solenoid valves operations. A Programmable sequence controller is used to avoid time lag by overload of the processor in the control system.

3.4.1 ALD reaction chamber

ALD processes can be performed in different types of reactors over a wide pressure range from atmospheric to ultrahigh vacuum. The reactor type can be divided into two groups: inert gas flow reactors operating under viscous flow conditions at pressures higher than or equal to 0.13mbar, and high or ultrahigh vacuum reactors operating under molecular flow conditions. From the viewpoint of cost effectiveness of the process, flow reactors operating under viscous flow are more popular. This is primarily due to (1) purging of a properly designed flow reactor is much more rapid than evacuation of a high vacuum chamber, thus reducing the process time, and (2) operating a UHV system is significantly costlier and challenging than low vacuum systems. Our system is capable of working both in purging as well as evacuation mode. Considering the cost and ease of maintenance we have chosen viscous flow mode for most of our studies.

It is important to note that the reactor wall can be hot or cold type. Hot wall reactors maintain the entire reactor at or near the deposition temperature. The primary advantage of hot wall reactors is that, there is no chance for precursor condensation on the wall and there is no secondary reactions are possible. But in cold wall chamber the chance for precursor condensation is high and secondary reaction may occur, which leads to the formation of particles on the cold surface. Our chamber is basically cold wall type and the entire chamber can be divided as two zones hot and cold. Temperature of hot zone can be produced by a heater which is resistively heated and vary from room temperature to 500^0C. Substrate holder is placed on the surface of heater. Outer wall of the chamber is water cooled which create a temperature gradient region referred to as cold zone. Temperature of this cold wall can vary from room temperature to 150^0C.

The system comprises of a cross flow type, cylindrical deposition chamber made of corrosion resistant Stainless Steel 316L. Volume of the chamber is approximately three litres. The chamber walls are water cooled. Several feed through are attached to the walls of the chamber for gas inlet, vacuum gauges, thermo couple, ac and dc high voltage provision, Langmuir

probe etc. Figure 3.2 shows a detailed schematic illustration of ALD reaction chamber.

Using this ALD system we had successfully grown thin films of aluminum oxide in the hot zone. We have observed simultaneous formation of alumina nano particles in cold zone during some of the trials. As recently nano sized particles have attracted much attention since they play crucial roles in certain advanced technologies, we have carried out a detailed characterization of these alumina particles. The detailed theory and growth mechanisms involved in both film and particles formation at each zone will be explained in chapter 7 in terms of TMA and H_2O reaction. The capability of dual nature of this system to produce films and particles is again confirmed by producing ZrO_2 film and powder using zirconium-tert-butoxide and water.

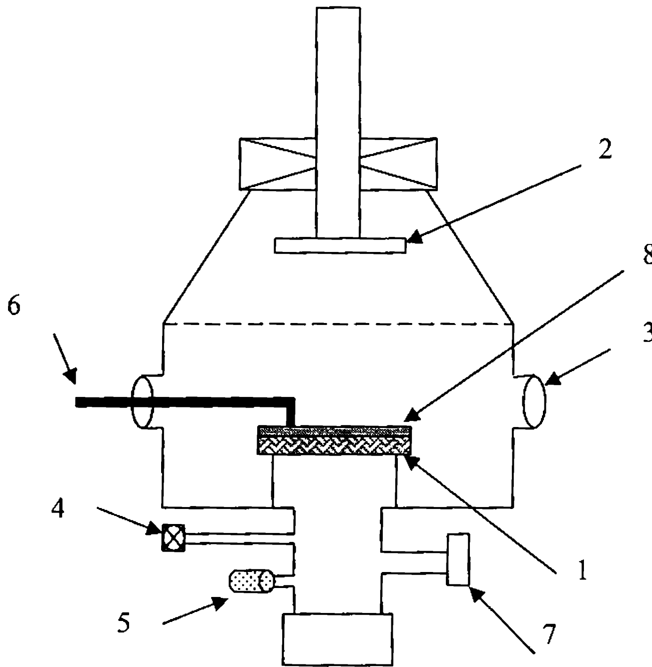

Figure 3.7: Schematic diagram of ALD reaction chamber (1-heater, 2-Top electrode for DC plasma, 3-view port, 4-needle valve, 5-air inlet, 6- thermo couple,7-To pump, 8-Substrate holder .

The bottom of the reactor chamber is connected to a throttle valve and diffusion pump (DP). The DP is connected to a backing pump. The top of the chamber is closed by a large plane stainless steel (SS) lid with an o-ring seal during thermal ALD.

3.4.2 Plasma chamber

In most ALD process the precursors used are usually metalorganics which results in porosity, low density and high impury contaminated films [19].These problems can be minimized by applying plasma. But, the damages of plasma on the substrate and thin films should be carefully considered. Therefore, much effort has been devoted to understand the damage mechanisms and to find ways to avoid these damages in plasma enhanced processes.

Our chamber design is adequate to work in dual-thermal as well as plasma-mode. Plasma mode can be direct or remote. Direct Plasma is developed inside the chamber between two electrodes. Top electrode which is attached to the top lid and with proper insulation was designed in such a way as to vary the distance between the electrodes. Chamber body acts as bottom electrode. A high voltage power supply act as DC source and Langmuir probe is inserted in to the chamber in order to study the plasma parameters. Figure 3.9 shows the schematic diagram of a direct plasma chamber.

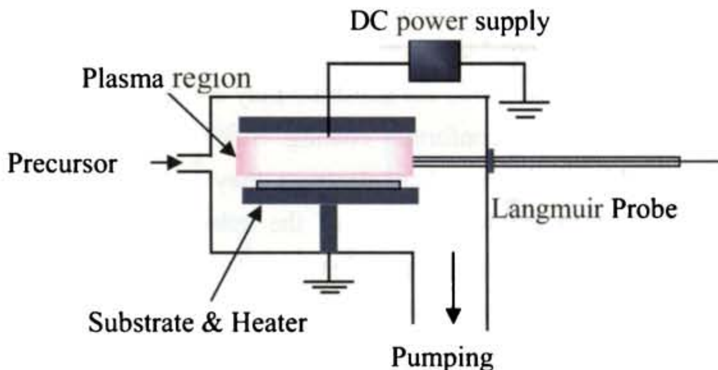

Figure 3.8: Schematic diagram of a direct plasma chamber

With direct plasma assisted deposition also carbon content and the presence of pores in the film resulting from direct exposure to the plasma were noticed to some extent. It was observed that these can be further minimised with the use of remote plasma.

Design of remote plasma chamber

Basic schematic of the remote plasma chamber and different components with suitable material which can withstand temperature and low pressure of the setup used are shown in Figure 3.9. Here a glass tube that can sustain medium temperature and low pressure is used for the plasma region of the chamber. This tube can be replaced by quartz tube at later stages if required. In order to produce plasma, DC voltage was applied between the electrodes, placed inside the tube. Various precautions and safety features were included to make sure that no spark-discharge or any other unwanted incidents happen during the operation of the reactor. Special concern was given for maintaining proper distances between the electrodes and grounded parts and keeping the electrodes clean.

Plasma was confined within a small region between the electrodes within the glass tube and plasma properties could be changed either by changing the spacing between the electrodes or by changing the voltage. Positively charged active chemical species in the plasma are attracted towards the substrate by biasing the substrate negatively. Even though some electrons move towards the substrate they generally die out soon after they come out of the plasma region by various recombination or capture mechanisms. This is a condition which is desired, since electrons with high kinetic energy moving towards the substrate may cause damages to the film and also may cause non-conformal coating. Since slow positive particles possess lesser kinetic energy than electrons they will neither cause film damage nor arise in the temperature of the substrate. This condition is suitable for a polymer or plastic type substrate to withstand.

The magnitude of negative potential applied to the substrate holder is responsible for the speed and thus kinetic energy with which positive particles get attracted towards the substrate. Thus we have a control over the

energy of the chemical species approaching the substrate surface which provides an added parameter to the process.

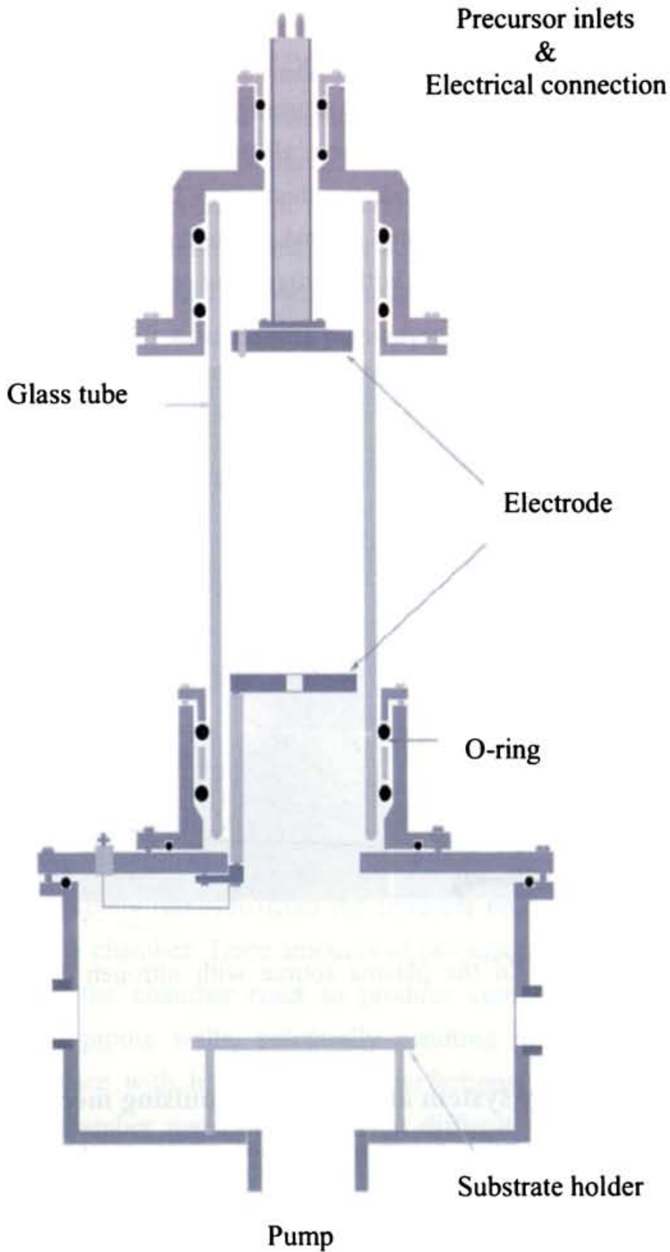

Figure 3.9: Schematic diagram of remote plasma chamber

Development of remote plasma

Plasma is a state of matter in which a certain portion of the particles are ionized. In this experiment we use DC plasma as the ion source. The plasma is generated by applying a HVDC supply 5kV between two electrodes. Figure 3.9 shows the DC plasma arrangement. Plasma properties are dependent upon the distance between electrodes, applied potential, chamber pressure and type of gas inside the chamber. A Langmuir probe was attached to the chamber for studying plasma characteristics. Figure 3.10 shows photographs of plasma source with nitrogen and argon at a pressure of 0.1mbar.

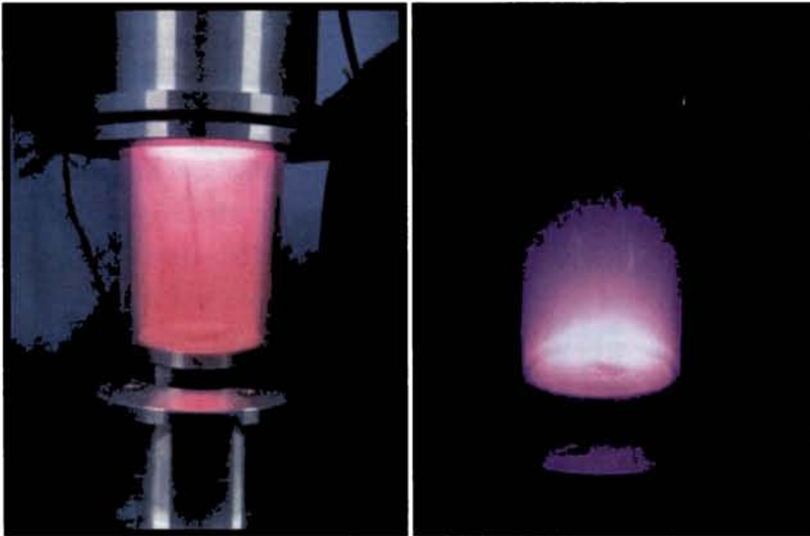

Figure 3.10: Photographs of the plasma source with nitrogen and argon plasma

3.4.3 Precursor delivery system and precursor pulsing mechanism

Since ALD relies on a reaction sequence which reaches surface saturation at each step, the design of precursor delivery systems for ALD reactors is simpler than that of CVD systems where precise control of precursor delivery to maintain a uniform flux is required. ALD is said to be 'self-limiting'. That is, ALD 'half-reactions' proceed until the available

reaction sites are used up, after which no more precursors react. In this way, the surface catalysis aspect of ALD ensures the deposited layer is absolutely uniform in thickness. ALD achieves conformal deposition on high aspect ratio features because surface reaction sites are an ingredient of the reaction, and are consumed by the reaction. Therefore uniform homogeneous concentrations of precursors are not necessary in the reaction space to achieve conformal deposition. It is merely necessary to provide enough of each precursor to consume substantially at all available surface sites.

Variations of ALD processes may involve multiple precursors and may use any number of chemical pathways. Oxidation pathways, using an alkylamino metal precursor and an oxidizing agent, are popular for depositing oxide layers. Reduction pathways, using a metal halide precursor and a reducing agent, are also popular for depositing metal layers. Layers of mixed chemistry, such as nitrides, oxynitrides, and the like, may also be deposited by using two or more chemical precursors sequentially pulsed into the reaction chamber. Other variations on the process itself feature pumping out the reaction chamber to high vacuum between pulses, or continuously purging the reaction chamber with a non-reactive gas while pulsing reactants through the reaction space.

ALD processes are to be carefully managed. It is desired that precursors react on the surface of the substrate, not in the space above the substrate, to achieve a self-limiting surface reaction. Thus,. one precursor must be completely removed from the chamber before another precursor is pulsed into the chamber. Trace amounts of precursors lingering in feed lines and sides of the chamber react to produce compounds that deposit on chamber and piping walls, potentially resulting in contamination of the substrate surface with impurities or imperfections. Some precursors have affinity for chamber materials, making it difficult and time consuming to evacuate them from the chamber. Moisture or oxygen impurities in any materials used as precursors or purge gases are particularly undesirable in an ALD process. Complicating the task of managing these challenges is the fact that process features such as valves and seals leak, and the smallest leaks in an ALD process can seriously degrade the results obtained. Therefore ALD

process and delivery system should be capable to manage these challenges. For liquid precursors, there are two options: (i) delivery via carrier gas and (ii) delivery via precursor volatilization. The system that we have developed has capability of both type of precursor delivery.

Carrier gas assisted liquid precursor delivery is accomplished with the help of a bubbler. A bubbler works by bubbling a high purity carrier gas (Argon/Nitrogen) at a pressure lower than atmospheric pressure through a volatile liquid precursor. The precursor vapour is carried by nitrogen gas flow into deposition chamber. Since the carrier gas pressure is higher than the chamber exhaust, the pressure gradient is sufficient to cause the gas mixture to flow into the reactor. Under conditions where the precursor's equilibrium vapour pressure is maintained, the mass flow of precursor into the reactor is proportional to the nitrogen carrier gas flow rate and the precursor vapour pressure. Bubblers are best used for volatile liquid precursors. Consistent and reproducible precursor delivery ultimately depends on the bubbler design and on the vaporization kinetics of the precursors. Low volatility liquid precursors can be delivered with a bubbler, but reproducibility tends to be poor. If precursor heating is used to increase the vapour pressure, care must be taken to avoid precursor decomposition in the bubbler and to prevent downstream condensation of the precursors prior to the deposition chamber.

In the present experiments both TMA and H_2O have sufficient vapor pressure (13 mbar and 31mbar respectively) at room temperature and the operating chamber pressure vary from 0.12 mbar - 0.48 mbar. Thus, adopting option (ii) was a natural choice, since precursors can be easily introduced into the reaction chamber via pressure differential driven flow. In addition, each precursor was separated by a purge. In the case of chemicals with low vapour pressure the source was heated to a temperature below its boiling point which will generate an increased vapor pressure. In addition, all the flow lines carrying precursors were heated to higher temperature to avoid vapour condensation.

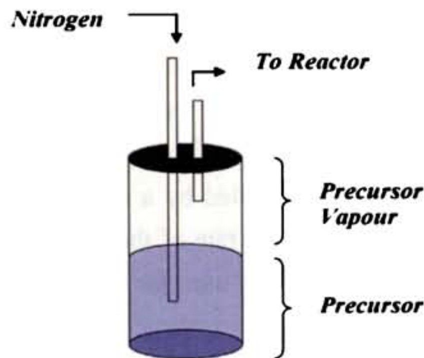

Figure 3.11: Schematic diagram of a bubbler.

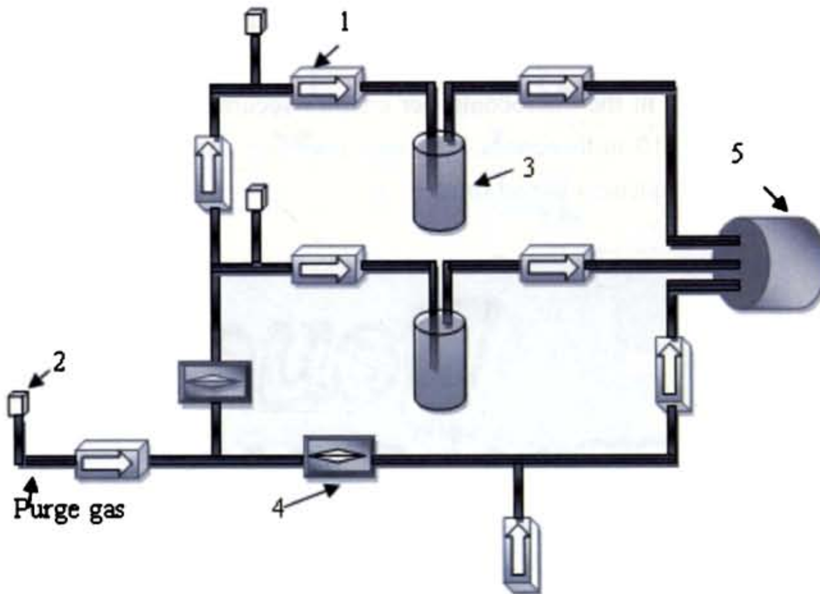

Figure 3.12: Delivery part of ALD system (1-Solenoid valve, 2-needle valve, 3-bubbler, 4-mass flow meter, and 5.chamber inlet)

Figure 3.12 shows the schematic diagram of precursor delivery part which consist of solenoid valves (Avcon), bubblers (SS316), mass flow meters (BRONKHORST) and needle valves. The entire precursor lines were

evacuated. Under this reduced pressure, precursor vapour were pulsed in to reaction chamber by means of solenoid valves. Alternate pulsing of precursors was achieved using solenoid valves which have response time <100ms installed between the precursor source and the reaction chamber. Solenoid valve operation was controlled by a sequential controller using a visual basic (VB) program. The flow rate of the inert gas was measured by mass flow meters. Needle valves were used for fine control of the flow rates of carrier gas.

3.4.4 ALD sequence controller

The sequence controller is built around an 8-bit microcontroller AT89C2051 with a PC interface through a serial port. A user friendly interface written in Visual Basic is used to provide input data for defining the sequences, various timings, number of cycles etc. An interrupt based timing subroutine running in the microcontroller enables accurate control of valve timings in unit of 10 milliseconds. The user interface also provides visual indication of the sequences in real time.

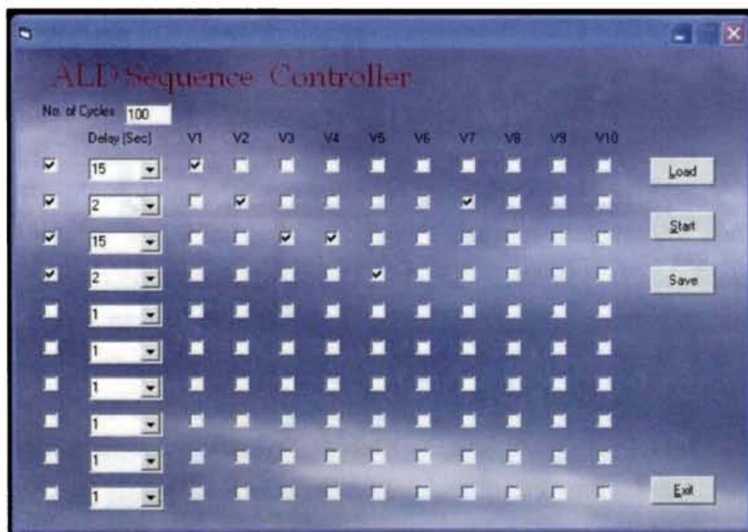

Figure 3.13: User friendly interface for controlling ALD cycles

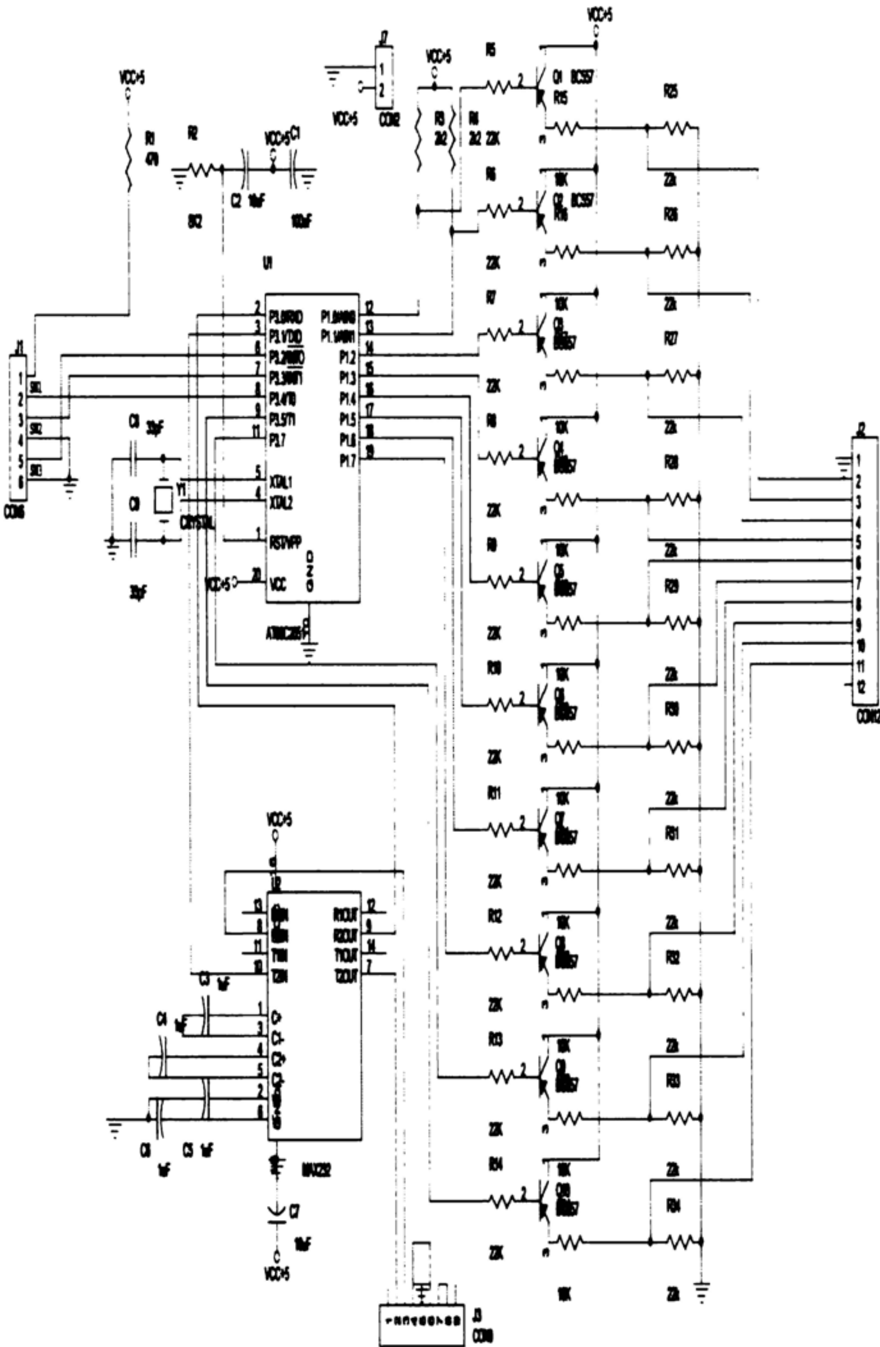

Figure 3.14: Circuit diagram of hardware part of ALD sequential controller

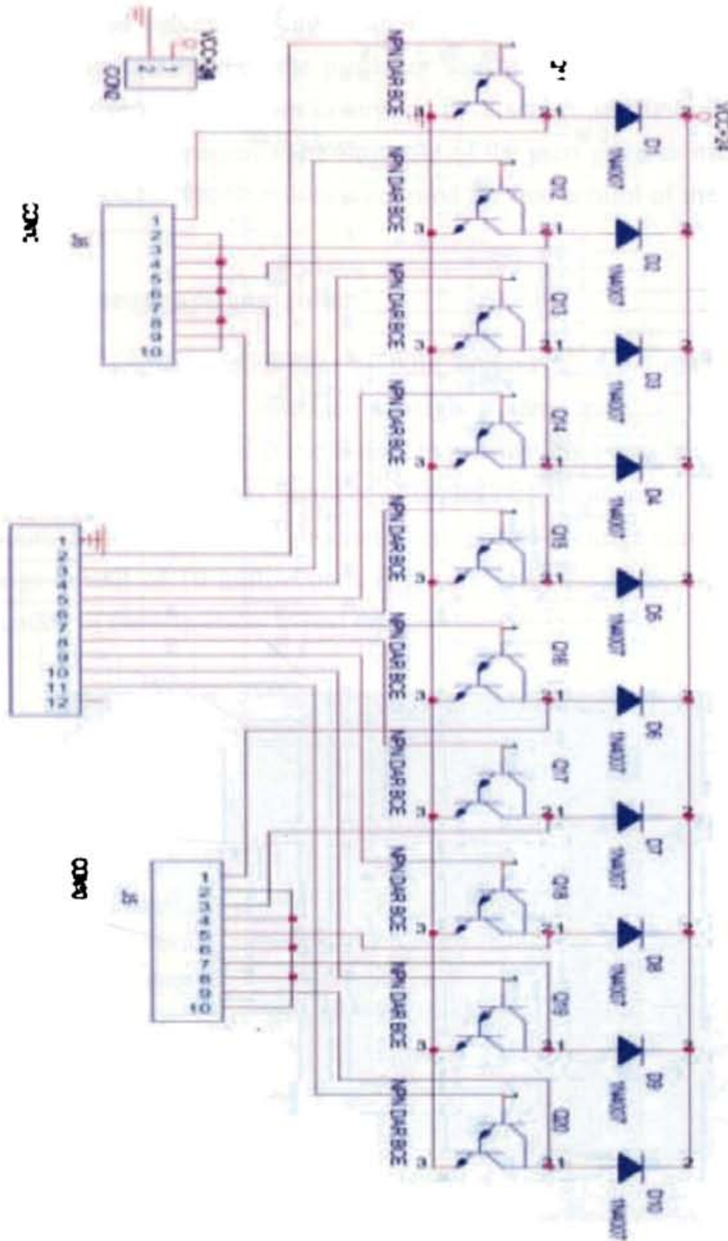

Figure 3.14: Circuit diagram of hardware part of ALD sequential controller

Figure 3.15: Photograph of thermal Atomic Layer Deposition system

Figure 3.16: Photographs of Plasma Enhanced Atomic Layer Deposition facility.

3.4.5 Exhaust system

A vacuum pumping system consisting of a $12M^3/h$ rotary pump and a 4 inch diffusion pump that can achieve an ultimate vacuum of $1x\ 10^{-5}$ mbar is used to evacuate the ALD chamber. A penning gauge is used to measure high vacuum in the chamber and two pirani gauges are used to measure rotary vacuum at different points in the system. A liquid nitrogen trap was placed between the chamber and vacuum pump. The pumping system has provision to choose a high or low vacuum for a specific deposition. Most of our depositions were conducted in low vacuum.

3.5 Optimisation of system parameters

To summarize our efforts in the area of design and fabrication of automated plasma enhanced atomic layer deposition system the gas flow in the chamber is plotted against time. Observations indicate that a reactor configuration that offers proper provisions for purging the reactants after each precursor exposure is the most critical aspect in the successful design of ALD reactors.

By adjusting needle valves, the flow rates can be set at different values up to 1000 SCCM. The flow rates of purge gas and each precursor line at 200 SCCM, 400 SCCM, and 500 SCCM are plotted against the time. This is shown in figure: 3.17. From the graph it can be understood that within 15 seconds the gas flow attains a steady state in all investigated flow ranges. The cycle times used in most of the alumina experiments were around 35 seconds. This shows that the system attains a steady state within one cycle of operation itself (which was later proved to be < 0.12nm thickness of alumina film) which is a good indication of the quality of the machine.

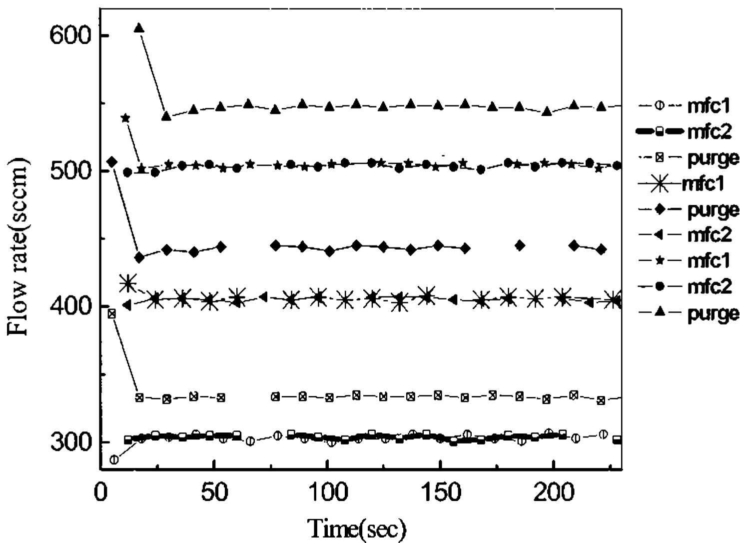

Figure 3.17: Time vs. Flow rates graph

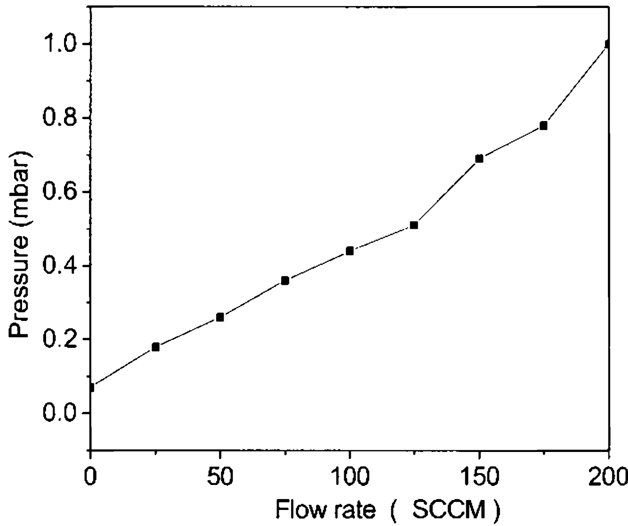

Figure 3.18 Flow rate vs. backing pressure

3.6 ALD-Al_2O_3 using TMA and H_2O

Blanket film depositions were initially conducted in order to investigate system behavior and to determine the operating conditions (cycle sequence) required to perform ALD using Trimethyl Aluminum (TMA) and water as precursors for the deposition of Al_2O_3. TMA (99.9%) was purchased from Sigma-Aldrich and used as aluminum precursor source while deionized (DI) water was used as the oxygen precursor. Both precursors were maintained at room temperature. Depositions were carried out at substrate temperatures in the range room temperature to 300^0C and chamber pressure of 0.12 mbar to 0.79 mbar. P-type silicon <100> wafers were used as substrates. Prior to film deposition, wafers were thoroughly cleaned by standard RCA procedure; after which they were rinsed with DI water and dried under nitrogen before being loaded into the ALD chamber. The chamber was evacuated to a base pressure of 0.026mbar and the substrates were kept at this pressure for 1 hour. Subsequently, an N_2 flow was initiated until the required chamber pressure reached, after which the substrate holder was heated to the desired deposition temperature. After an additional 5-10 min time period, ALD cycles were started. The ALD deposition cycle

consisted of: (1) TMA pulse, (2) N_2 purge, (3) H_2O pulse, and (4) N_2 purge. Details of the deposition conditions are explained in chapter 5.

Successful layer by layer ALD process with sufficient exposure and purge time and full saturation of the surface, should in principle result in extremely uniform layers. Non uniformity of the deposited layers can occur in initials cycles. Insufficient purge steps results vapour phase reaction between precursors and results increased CVD like growth rate. Limited and excess amount of precursors may also cause distinct growth rate than expected. However not all uniformity problems are caused by critical process parameters. The major advantage of ALD compared to CVD is its non-critical nature of process parameters.

Thickness uniformity is one of the characteristic features of ALD. In order to confirm this uniformity we measured the thickness of Al_2O_3 samples prepared in our system at different location using an ellipsometer. Figure 3.19 shows the 2D plot of thickness variation on Si substrate at an area $4cm^2$.

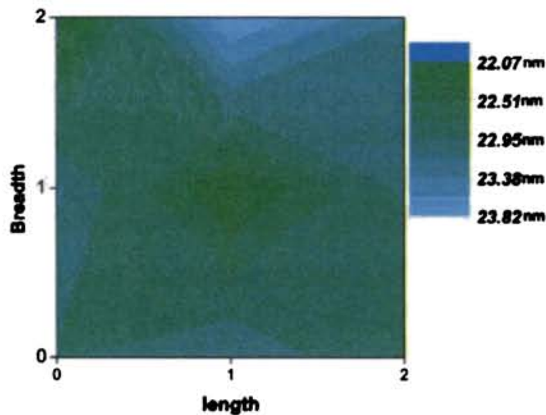

Figure 3.19: 2D plots showing thickness variation in nm over a wafer surface of area of 2cm×2cm.

3.7 Conclusions

We successfully designed and fabricated a compact and inexpensive automated Atomic Layer Deposition system for depositing ultra-thin films, which can be used in a wide variety of research and industrial applications.

Our system is capable to work as thermal ALD and as plasma enhanced ALD. System capabilities were confirmed by depositing ultra thin Alumina films using TMA and water. System parameters were optimized in order to work in ALD mode.

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4

On Adsorption of Aluminum and Methyl Groups on Silica for TMA/H_2O Process in Atomic Layer Deposition of Aluminum Oxide Nano Layers

In this chapter we propose a detailed chemisorption mechanism during the atomic layer deposition (ALD) of aluminum oxide nano layers using trimethyl aluminum (TMA) and water as precursors. This model is an extension of the model proposed by R. L Puurunen. It can explain more detailed surface reaction mechanism for the adsorption of metal and ligands and a different approach to calculate the maximum number of ligands which yields a more realistic value. It is proposed that during ALD of TMA and water the most probable chemisorption mechanism taking place is combination of complete ligand exchange and complete dissociation .

4.1 Introduction

Since 1970 several research groups have applied ALD technique for depositing conformal inorganic material layers of different thicknesses with atomic level control. The mechanisms which control the growth are not yet sufficiently understood. To understand the detailed growth mechanism, overviews are needed not only for the existing process but also of the knowledge of the surface chemistry of ALD. TMA/H_2O process is considered as the most ideal for ALD of Al_2O_3. In this chapter we discuss the various chemisorption mechanisms undergoing during ALD process. Also we try to present here a more detailed surface reaction mechanism for the adsorption of metal and ligand during the TMA/H_2O process [1]. Three important models which calculate the maximum growth per cycle (GPC) from the size and geometry of the adsorbed ML_z (M-metal, L-ligand, Z-no. of ligands) species is discussed. We propose a new model which is an extension of Puurunen's model which yields a more realistic value of

maximum number of ligands that can be accommodated per nm^2 area. We calculated the GPC of the thin films from geometrical calculation by assuming the surface chemistry proposed here. The dependence of GPC on OH concentration was also studied.

4.2 Various models in literature for calculating maximum growth per cycle

Model I

Ritala *et al.* and Morozov *et al.* [2-5] developed a model; referred to as *Model I*, to estimate the maximum GPC from the size of the ML_n reactant where n is the number of ligands in the orginal TMA molecule. Figure 4.1 (a) shows the schematic illustration of ML_n reactant. The size of the ML_n reactant is calculated from the density of the liquid reactant and the area covered by the reactant assuming a close packed monolayer of ML_n *Model I*, in fact, corresponds to a physisorbed monolayer of the MLn. Because the chemisorbed ML_Z species differs from the ML_n reactant, Model I gives only the best rough estimate of the achievable GPC.

Model II

Ylilammi [2,6] developed a model referred as *Model II*, for calculating the maximum GPC from the size and geometry of the adsorbed ML_Z species. The disadvantage of this model is that we must know the sizes of the ligand L, metal M, bond lengths and bond angles. Figure 4.1 (b) shows size and geometry of chemisorbed ML_Z species. In Model II, the GPC increases in steps with decreasing size of the adsorbed MLz.

Model III

Siimon and Aarik [7] and Puurunen [8,9] developed independently the same model, *Model III*, for calculating the maximum GPC from the size and number of the adsorbed ligands L. A theoretical maximum amount of ligands adsorbed is calculated assuming a close packed monolayer of the ligands. This is calculated for the amount of metal M adsorbed by dividing the amount of metal adsorbed by the L/M ratio in the MLz adsorbate. As

should be expected, the GPC increases with decreasing size of the adsorbate [10]. This model is applied by Puurunen [2] to TMA/H_2O ALD process to calculate GPC. By taking the value of van der Waals radius (VDR) of methyl groups as 0.2nm [11], she obtained a value for maximum amount of methyl groups adsorbed as 7.2 per nm^2.

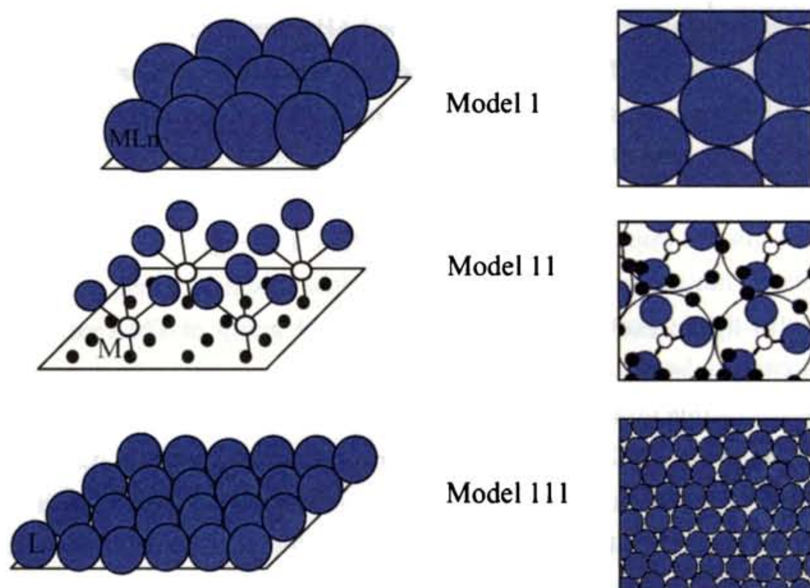


Figure 4.1: Various models which calculate maximum GPC

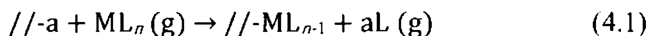
4.3 Detailed chemisorption mechanisms for self terminating reactions

Various classes of chemisorption mechanism have been identified for self terminating reactions of compound reactants in ALD. The mechanisms that have been identified for bonding gaseous reactants on solid supports, in a saturating manner are illustrated with molecule ML_n used.

Ligand exchange

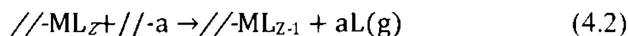
In ligand exchange, the reactant molecule (ML_n) is split on the surface. Ligand (L) combines with a surface group //–a to form a volatile compound that is released as a gaseous reaction by product, aL, and the

remaining part of the molecule is chemisorbed on to the surface as an ML_{n-1} species as shown in equation.



$$//\text{-a} + ML_n\,(g) \rightarrow //\text{-}ML_{n-1} + aL\,(g) \quad (4.1)$$

Ligand exchange reaction can also occur for more than one ligand of the ML_n reactant, or between an adsorbed ML_Z species ($1 \leq z \leq n$) and a surface //–a group. These reactions release ligands as aL and consume additional //–a groups but do not result in bonding more metal M on the surface (reaction of an adsorbed ML_Z species).

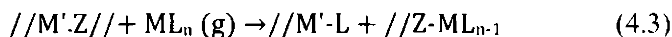


$$//\text{-}ML_Z + //\text{-a} \rightarrow //\text{-}ML_{Z-1} + aL(g) \quad (4.2)$$

In ligand exchange reaction, one methyl group of TMA combines with hydrogen of the surface hydroxyl group and escapes as methane. The remaining methyl groups and the aluminum atom get attached to the oxygen of the OH group [2,12]. If the reaction continues on the surface, we end up with one methyl group connected to the surface via an aluminum atom. Other two methyl groups combine with hydrogen of the surface OH sites and escape as CH_4. Thus the ligand to metal ratio (CH_3 is the ligand and aluminum is the metal in the case of TMA), L/M = 1 for this case and this will result in adsorption of maximum metal atoms (Al) to the surface. This is called complete ligand exchange (CLE). But if the ligand exchange reaction stops at the first step, then two methyl groups will get attached to the surface OH site via an aluminum atom. Under this condition we will have L/M ratio = 2. This is named as partial ligand exchange (PLE). Schematic representation of PLE and CLE is shown in Figure 4.2.

Dissociation

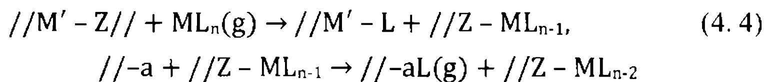
In dissociation, the reactant molecule is split onto reactive M'-Z sites on the surface.



$$//M'\text{-}Z// + ML_n\,(g) \rightarrow //M'\text{-}L + //Z\text{-}ML_{n-1} \quad (4.3)$$

For the usual simple dissociation (SD) and association (AS) [2] we have three methyl groups for a single metal atom and hence the L/M = 3 for them. Simple dissociation is a phenomenon in which a surface siloxane bridge breaks and aluminum atom with two methyl groups of TMA gets attached to the oxygen of the siloxane bridge and the remaining methyl group attaches itself with the silicon atom on the surface. So in this case three methyl groups and one metal (Al) atom get attached to the substrate surface. Dissociation can proceed in another way in the absence of sufficient OH sites. This is shown in Figure 4.2 (d). Here reaction proceeds by breaking one more siloxane bridge. In this case the L/M ratio is 3, which is the same as the simple dissociation and is called complete dissociation (CD).

Consider another situation with less OH concentration but still with sufficient numbers to combine with methyl groups. Dissociation can proceed further on the surface, with a methyl group which is connected to aluminum atom, gets attached to the hydrogen atom of an OH site and escapes as methane. In this case called complete dissociation via ligand exchange (CDLE), there are two methyl groups of the original TMA molecule attached to the silica-one attached to the siloxane bridge via aluminum atom and another directly connected to the silicon atom on the substrate giving an L/M ratio of 2 [2].

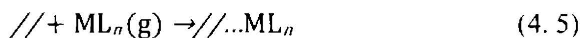


$$//M' - Z// + ML_n(g) \rightarrow //M' - L + //Z - ML_{n-1}, \qquad (4.4)$$
$$//\text{-}a + //Z - ML_{n-1} \rightarrow //\text{-}aL(g) + //Z - ML_{n-2}$$

So for dissociation mechanism we have two L/M ratios, i.e. 2 and 3 which correspond to high and low OH concentration on the surface.

Association

In association, the reactant molecule forms a coordinative bond with a reactive site on the surface and is chemisorbed without a release of ligands [13-18]. Association has also L/M ratio of 3.



$$// + ML_n(g) \rightarrow //...ML_n \qquad (4.5)$$

The different classes of chemisorption mechanisms are schematically illustrated in Figure 4.2.

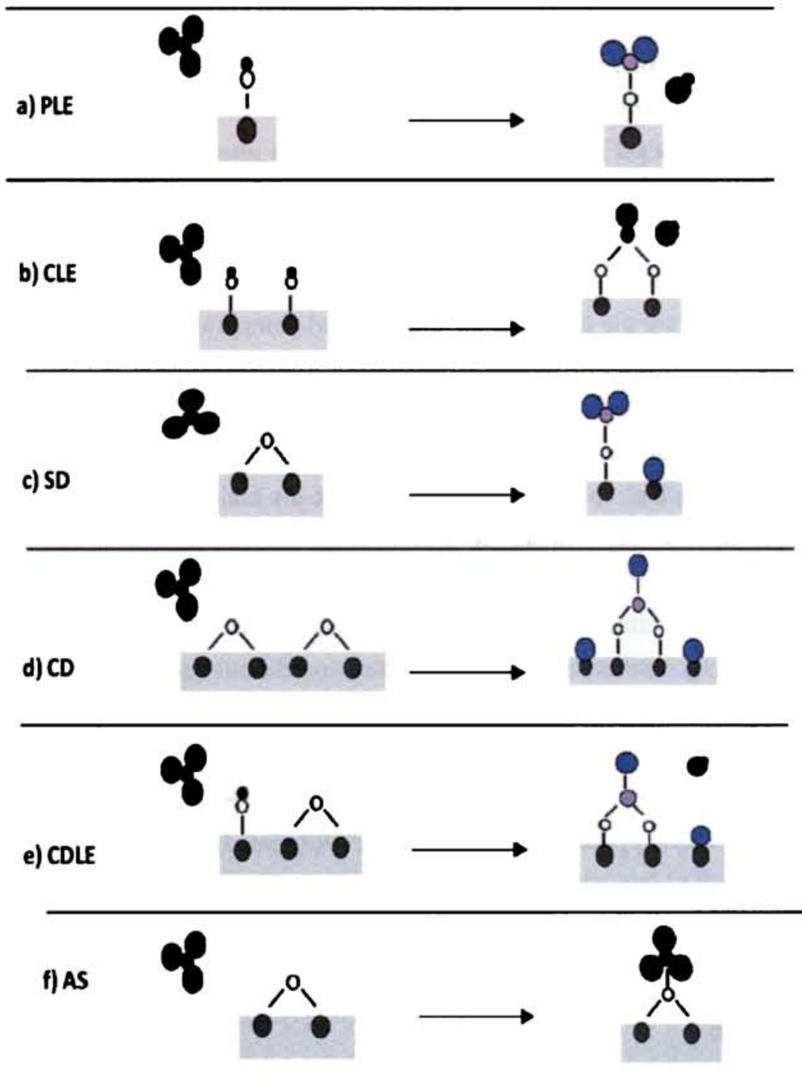


Figure 4.2: Various chemisorption mechanisms

4.4 OH concentration

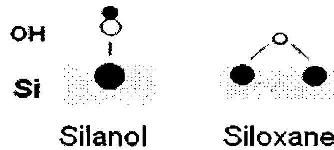


Figure 4.3: Shows schematic diagram of silanol and siloxane bridge.

Let us consider a substrate area (say, silicon covered with an oxide layer) of dimension 1 × 1 nm. The surface of silica naturally has attached to it OH groups from various forms of silanols like free silanols, bridged silanols, geminal silanols and tertiary silanols in addition to siloxane bridges. Figure 4.3 shows schematic diagram silanol and of siloxane bridges.

The nature of the surface generally depends on the wafer cleaning procedures like RCA, Standard Clean 2, and Piranha etc which leave a protective hydrous oxide film on the surface [19]. Considering the VDR of OH group as ~ 0.13nm [11] it can be seen that the maximum number of OH groups that can be accommodated on 1 nm^2 area is 14.79 or ~ 15. Here instead of considering a close packing we have considered square packing, that each OH group effectively occupies an area of a square with sides equal to twice the VDR of OH group. The value obtained is comparable to the reported maximum value of 12 hydroxyl groups per nm^2 [24]. Hence the maximum number of OH groups which can be physically arranged on the surface of the substrate is considered as 15.

4.5 Methyl group concentration

Taking the VDR of methyl group as 0.2 nm, it can be shown that 6.25 methyl groups can be accommodated in 1 nm^2 area following the same reasoning as that for OH groups. This is confirmed by reported experimental values [14]. Out of the maximum 15 OH sites in 1nm^2 area, 8.75 are sterically hindered (shielded) by methyl groups where other methyl groups cannot get attached. Hence a small variation of OH concentration will not affect the methyl group concentration on the substrate surface. As the OH concentration decreases, the methyl group concentration need not decrease

within a good range. This is because 15 is the maximum possible number of OH groups per nm^2 substrate area. In practice, it will be a combination of OH groups and siloxane bridges which exist on the surface, i.e. surface need not contain the maximum number of OH groups at any time but some space can be occupied by the siloxane bridges also. This is especially true above a substrate temperature of 373 K, as above this temperature bridged silanols condense to form siloxane bridges [22]. At higher temperatures the OH concentration decreases and siloxane bridges present on the silica surface start breaking and combine with the methyl groups and Al atoms of TMA.

It is reported that Si-O behaves like a Lewis base [23] and hence this reaction is favoured by Si-O and TMA. This is the process which is called dissociation. Moreover association also can take place with these siloxane bridges as illustrated in the same model. Partial ligand exchange also is a possibility at reduced OH concentrations. VDR of a siloxane bridge (Si–O–Si) is ~ 0.26 nm [11], hence maximum number of siloxane bridges present in 1 nm^2 substrate area is 3.6. Since maximum three methyl groups can be accommodated by one broken siloxane bridge as shown in figure 4.2(c), maximum of ~ 11 methyl groups can be accommodated in unit nm^2 substrate area. But it has already been proved previously that maximum 6.25 methyl groups only can be accommodated per nm^2 area, the methyl group concentration will again be 6.25 under this situation. At the lowest concentration of OH groups of 2 per nm^2 [24], i.e. when the surface is covered predominantly by siloxane, the adsorption process may proceed as depicted in Figure 4.2(d) or 4.2(f), in which two siloxane bridges accommodate three methyl groups or one siloxane bridge accommodates three methyl groups, respectively (This is termed as complete dissociation [CD] and association, respectively).

In both cases it can be shown that the maximum methyl group concentration is 6.25 even at a lower concentration of OH on the surface of the substrate. This methyl concentration predicted here is closer to the observed experimental value 5 - 6 than 7.2 which is predicted earlier by Puurunen in 2005 [2]. In fact a closer look at the original figure (Ref 2, figure22.b) reveals that except two points all other points are closer to the

value 6. The variation of OH sites on the substrate surface may be due to deposition temperature during ALD or substrate pre-treatment before deposition [2,22].

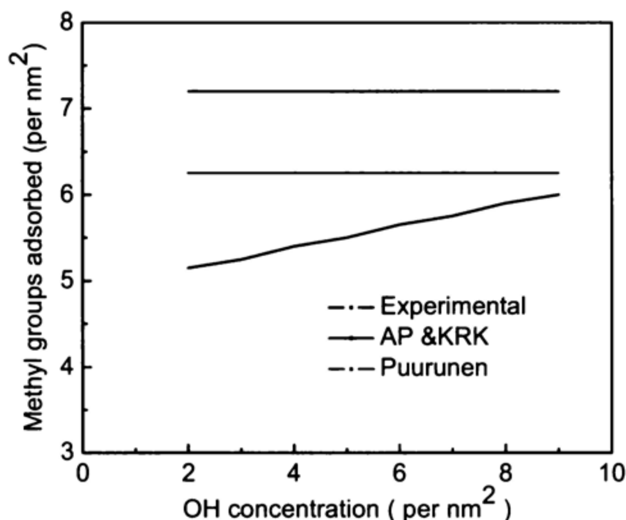


Figure 4.4: Variation of methyl group adsorbed with OH concentration

4.6 Aluminum concentration

For the case of complete ligand exchange (CLE) we have one metal atom for one ligand. Therefore the total number of metal atom per nm² area is obtained by dividing 6.25 by the L/M ratio of 1 in this case as 6.25. For each Al atom adsorbed by CLE two OH sites are used. Therefore for 6.25 Al atoms adsorbed, 12.5 OH sites are required. For partial ligand exchange (PLE), L/M ratio = 2. Here we have one metal atom for two ligands. Therefore the number of metal atoms adsorbed per nm² area is equal to 6.25/2 equal to 3.125 and for 3.125 Al atoms adsorbed, OH sites required are 3.125.

For simple dissociation and association the number of metal atoms per nm² is obtained as 2.08 by considering one metal atom for three ligands. (Here we have to note that all the three methyl groups get attached to the surface either in association with the aluminum atom or two methyl groups

with the aluminum atom and one methyl group alone on the surface site). Since for SD and AS only siloxane sites are present and required number of siloxane sites used for 2.08 Al atoms is 2.08. For CDLE the number of metal atoms per nm^2 area is 6.25/ 2 = 3.125. Since for CDLE one siloxane bridge and one OH site are required for adsorption of one Al atom, 3.125 siloxane bridges and 3.125 OH sites are required.

For complete dissociation (CD) L/M ratio is 3 and hence the number of Al adsorbed is 6.25/3=2.08. But for CD two siloxane bridges are required for adsorption of one Al atom and hence for adsorption of 2.08 Al atoms 2×2.08=4.16 siloxane bridges are required. But we know that only 3.6 siloxane bridges maximum can be accommodated in 1 nm^2 area of the substrate. Therefore the number of maximum Al atoms that can be accommodated by CD is only (2.08/4.16)×3.6=1.8. This is the minimum number of Al atoms accommodated on 1nm^2 area of the substrate when the surface is covered with only siloxane bridges and no OH groups present. The OH/siloxane sites which are not used in the case of each adsorption mechanism are sterically hindered by adsorbed methyl groups. The L/M ratio, concentration of metal atoms, concentration of ligands and OH/siloxane sites used are tabulated in Table 4.1 for different chemisorption mechanisms.

It has to be noted that any of the chemisorption mechanisms or combination of them can be active at any time for any concentration of OH groups. Since CLE consumes more OH sites, this process can dominate only when more OH sites are available on the surface. On the contrary for SD, CD and AS no OH sites are required which make them dominant processes at low and very low OH concentrations.

From an investigation on the dependence of aluminum concentration on OH values we propose a model for the possible adsorption mechanisms which are active at different OH concentrations. For this we assume that CLE takes place on available OH sites and SD or CD take place at the available siloxane sites. Further we assume that whenever possible a combination of these mechanisms occur on the surface with one or the other mechanism dominating.

Table 4.1: Types of chemisorption mechanisms and related parameters.

Type of adsorption mechanism	L/M ratio	No. of Al atoms adsorbed/ nm^2	No.of methyl groups adsorbed/nm^2	No. of OH/ Siloxane sites used
Complete Ligand Exchange	1	6.25	6.25	12.5 OH
Partial Ligand Exchange	2	3.125	6.25	3.125 OH
CDLE	2	3.125	6.25	3.125 OH+ 3.125Silox.
Simple Dissociation (SD)	3	2.08	6.25	2.08 Silox.
Complete Dissociation (CD)	3	2.08(Max. possible 1.8)	6.25	4.16Silox. (Max. 3.6)
Association (AS)	3	2.08	6.25	2.08 Silox.

From Table 4.1, we can see that for an OH concentration of 12.5 the concentration of Al atoms is 6.25 per nm^2. Let us now take an OH concentration of 10 on the surface. (a) Number of Al atoms deposited per nm^2 due to CLE is (6.25/12.5) ×10 = 5, (b) area covered by 10 OH = (1/15) × 10 = 0.67 nm^2, (c) area covered by siloxane bridges = (1- 0.67) = 0.33nm^2, (d) number of siloxanes in this area = (3.6/1) ×0.33 = 1.19, (e) if we assume SD along with CLE the Al atoms that can be accommodated by SD = (no. of Al atoms adsorbed/no. of siloxane sites needed for this for SD) × 1.19 = 2.08/2.08) ×1.19 = 1.19, (f) therefore, total number of Al atoms on the surface due to CLE and SD = 5+1.19 = 6.19 and (g) if we assume CD along with CLE the Al atoms that can be accommodated by CD = (no. of Al atoms adsorbed/no. of siloxanes needed for this for CD) × 1.19 = (1.8/3.6) × 1.19 = 0.595. Repeating these calculations for OH concentrations 8, 6, 4 and 2 we get the following results which are summarized in Table 4.2. Table 4.2 also contains Al value for zero OH concentration (i.e. when there are 3.6 siloxane

bridges on the surface so that no space left for OH groups) taken from Table 4.1.

Table 4.2: Relationship between OH concentration per nm^2 area of the substrate and Al Concentration for different chemisorption mechanisms.

OH concen-ration	Aluminum due to				
	CLE	SD	CD	CLE+SD	CLE+CD
10	5	1.19	0.595	6.19	5.595
8	4	1.69	0.845	5.69	4.85
6	3	2.16	1.08	5.16	4.08
4	2	2.63	1.315	4.63	3.32
2	1	3.13	1.57	4.13	2.57
0	0	3.60	1.80	3.6	1.8

Figure 4.5 shows the number of aluminum atoms adsorbed per nm^2 area of the substrate as a function of OH concentration on the surface. This plot is generated using data from the first and last columns of table 2. We have plotted all the data given in various columns of table 4.2 against OH concentrations and found that data in the last column fits exactly the experimental curve given by Puruunen [2]. Equation for the experimental curve is given as $Y=0.37X+1.68$, whereas the present curve is $Y=0.38X+1.8$. This shows that there is a very good probability of the chemisorption mechanisms to be a combination of CLE and CD with CLE dominating at higher OH concentrations and CD at lower concentrations [1].

As out lined earlier since any or a combination of the adsorption mechanisms can be active any time with differing contributions of each we may get different Al atom concentrations depending upon the experimental conditions. The present curve, most probably shows one possibility of Al atom deposition that can be achieved at various OH concentrations on the substrate surface which satisfies the experimental data. It is likely that the same end effect may be achieved with more complicated combinations of different adsorption mechanisms.

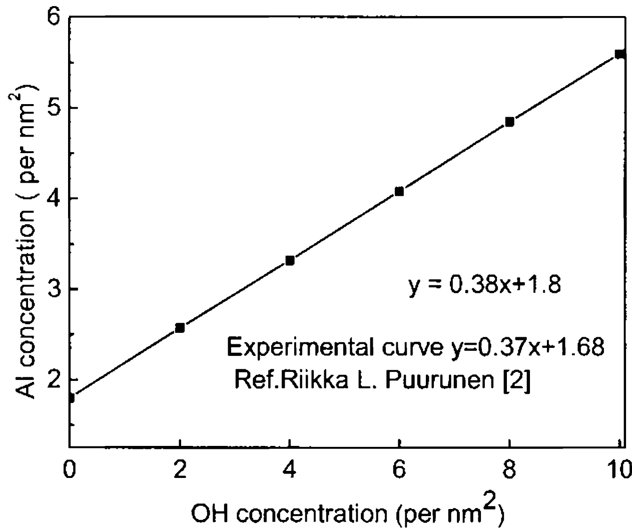


Figure 4.5: Plot of OH concentration vs. number of aluminum atoms adsorbed per nm^2 area of the substrate

The transient pressure measurements during micro pulse dosing of TMA reported earlier by the team of Alan Weimer and S. M. George (Jarod A. Mc Cormik *et. al.* [20] have shown that TMA react with AlOH surface groups and liberate two CH_4 molecules, which supports the dominant CLE surface reaction, mechanism, over PLE.

The present model is in agreement with the adsorbate inhibition model in which the methyl termination inhibits the adsorption of excess TMA gas [26]. This is evident from the fact that Al concentration never exceeds the methyl group concentration on the surface of the substrate.

Figure 4.6 shows the L/M ratio as a function of surface OH concentration which is calculated by assuming constant methyl group concentration of 6.25 and chemisorption mechanism as CD+CLE. Calculated L/M ratio is also in agreement with the reported L/M ratios [2] which are calculated using experimental values.

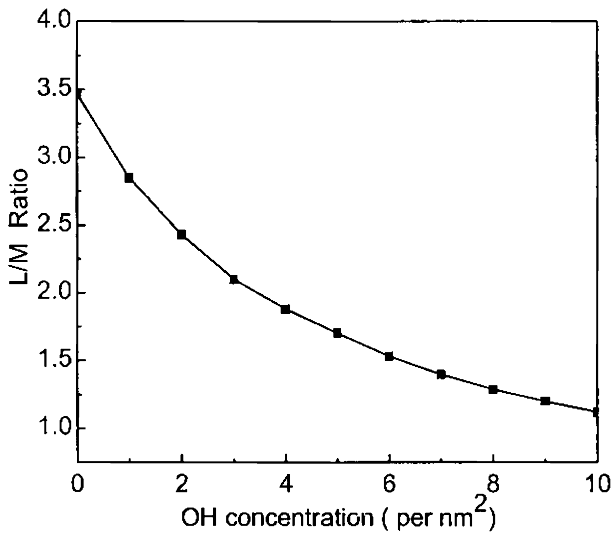


Figure:4.6 L/M ratios plotted against OH concentrations

4.7 Calculation of growth per cycle (GPC)

Growth per cycle (GPC) is defined as the incremental increase in the thickness of the film per cycle of deposition. GPC is an important parameter of ALD technique. In comparison with the similar term 'rate of deposition' for other thin film deposition methods, GPC of ALD yields generally a low value.

Considering the molar mass and density of α- Al_2O_3 as 101.96 gm and 3.99 gm/cc [28,29], we calculated the volume of one molecule of Al_2O_3 as 0.042 nm^3 and radius (r) of one molecule as 0.216nm. Assume that the ALD deposited Al_2O_3 has a face centered cubic close packing as shown in Figure 4.7 which is the densest packing.

Volume of the unit cell shown in Figure 4.7 is 0.229 nm^3. Since total number of atoms in an fcc unit cell is 4, then the effective volume occupied by a single sphere = 0.0573 nm^3.

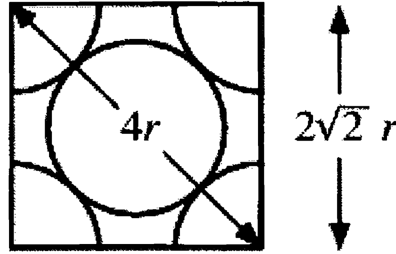


Figure 4.7: A unit cell of face centered cubic close packing.

With maximum OH species on the surface of the substrate taken as approximately 12 per nm^2, a maximum of 6.25 Al atoms can be chemisorbed per nm^2 area [1]. Since two Al atoms are required for the formation of one Al_2O_3 molecule, 3.125 Al_2O_3 molecules per nm^2 area can form under this condition. Assume that 100 cycles of deposition are done. Then 312.5 Al_2O_3 molecules are formed on $1nm^2$ area of the substrate. Total effective volume occupied by 312.5 Al_2O_3 molecules is 17.92 nm^3. Hence total thickness developed above $1nm^2$ area = 17.92 $nm^3/1nm^2$ = 17.92 nm. This yields a growth per cycle (GPC) of 0.1792 nm. Similarly we have calculated GPC for different OH concentrations on the substrate surface which are listed in Table 4.3.

Table 4.3: OH concentration on the substrate surface vs. calculated GPC.

No of OH/nm^2	Calculated GPC(nm)
12	0.179
10	0.160
8	0.139
6	0.117
4	0.095
2	0.075

The range of GPC given in table 4.3 agrees well with various reported values [8,27,28,30-35]. It is important to note that for any particular deposition process the number of surface species strongly depends on the type of substrate and the substrate temperature [2]. Hence the deposition may start with a GPC appropriate for that substrate at that temperature. Later after few cycles of deposition, the substrate will be covered with layers of alumina and the number of the substrate species will change to the characteristic value for alumina. Hence the GPC may change to a new value and continue at that value throughout the rest of the coating [2, 37].

4.8 Density of Al_2O_3 deposited by ALD

The density of as deposited thin films in general is less than that of the bulk value. This is mainly due to the low energy of the evaporants or reactants in various physical and chemical deposition methods. Usually this is compensated by supplying additional energy in the form of substrate heating, plasma enhancement or ion assistance. In atomic layer deposition substrate heating and plasma assistance are regularly employed for improving the film quality. However a high substrate temperature during deposition can also cause re-evaporation of the adsorbed atoms from the substrate surface. Moreover the fact that TMA decomposes approximately at 300°C [2,8,36] imposes an upper limit to the substrate temperature.

From Figure 4.7 we get the volume of a unit cell as $(2\sqrt{2}r)^3$ = 0.23 nm^3. Since this volume contains 4 molecules, no of molecules per nm^3 = 17.44. Mass of 17.44 molecules = 2.95×10^{-21} gm. This yields density of ALD deposited Al_2O_3 as 2.95×10^{-21} gm/nm^3 or 2.95gm/cc. The value of density obtained here is less than the bulk value of alumina [29]. However this is in agreement with the experimentally observed values for amorphous alumina [39-41]. The density of alumina deposited by ALD may also depend on the type of growth mode like two dimensional/ island/ or random growth modes [2,38].

4.9 Calculation of number of monolayers (ML)

Consider figure 4.8, where 5 monolayers of Al_2O_3 are shown. The total thickness (t) consists of total thickness of two unit cells plus one radius (r) at the top side and one radius at the bottom side of the film. Total thickness.

$$t = \left(c * 2\sqrt{2r}\right) + 2r \tag{4.6}$$

where c is the number of unit cells. Therefore

$$c = {(t-2r)}\Big/{2\sqrt{2r}} \tag{4.7}$$

Each unit cell contains effectively 2 monolayers (ML). One radius at the bottom of the film and one radius at the top effectively add one ML to this. Hence the number of $ML_{(n)}$ can be written as $n = (2c + 1)$, ie

$$n = \left\{\left(\frac{t-2r}{\sqrt{2r}}\right) + 1\right\} \tag{4.8}$$

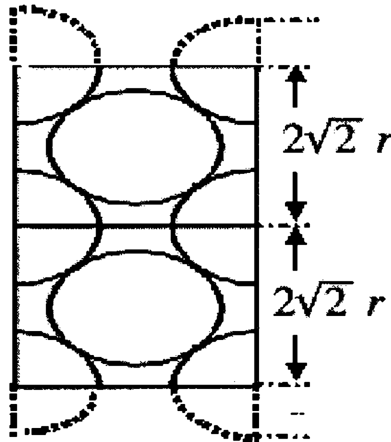


Figure 4.8: Five mono layers, stacked one above the other are shown. The total thickness of the film is the sum of the thicknesses of the two unit cells and the two radii- one at the top and the other at the bottom of the layers.

Using Figure 4.8 the total thickness of the film is calculated as t=1.65 nm. Substituting this value of't' in equation (8) we get the number of ML as n = 5. The total thickness't' developed after 100 cycles of ALD operation for a GPC of 0.179 is 17.9 nm. For this thickness, the number of ML obtained using equation (4.8) is 58.4. In an ideal ALD one expects one ML per cycle. However, this is never observed in practice [2,1,8,10]. This calculation shows that maximum 58.4% of the ideal number of ML value which one expects from the number of cycles only, will be formed during ALD. From Table 4.3 and 4.4 it can be observed that as GPC decreases from 0.179 to 0.075 (which again corresponds to an OH concentration of 12 to 2 on the substrate surface) number of ML decreases from 58.4 to 24.2 most of the reported values [8,10] support this observation. This reduction in the number of ML can be due to the steric hindrance caused by ligand molecules of trimethyl aluminum during its Chemisorption [10], as well as the reduction of the surface sites, where TMA can get attached.

4.10 Mono layer thickness

The mono layer thickness (h) predicted by the equation $h=(M/\rho N_A)^{1/3}$, where M and ρ are the molar mass and density of Al_2O_3 [10] yields a value of 0.39 nm (for a density of 2.95 gm/cc). But in ref 10 mononolayer thickness is considered as the height of a cube containing one product molecule MZ_x which in the present case is Al_2O_3. This gives the absolute value of a monolayer thickness and is of interest only when one monolayer is deposited. In practical applications the film will be composed of several monolayers and the effective thickness of a monolayer is more important. Effective monolayer thickness will be less than the above value due to the face centered cubic close packing of the deposited film. From Fig.4.8 it is evident that a unit cell contains two monolayers and hence the effective thickness of a monolayer is $\sqrt{2}$ r or 0.31 nm. 58.4 ML are formed for 100 cycles of deposition with 0.179 nm GPC. This yields an effective ML thickness of 0.31 nm. It is evident that as the OH concentration on the surface of the substrate decreases from 12 to 2 the number of monolayers decreases from 58.4 to 24.2 for 100 cycles of deposition. It can be

interpreted in another way [10] as 58.4% to 24.2% of a monolayer only is formed in one cycle of deposition corresponding to the maximum and minimum number of surface sites. This data is given in Table 4.4. The monolayer thickness remains the same in all cases and can be approximated to 0.31 nm.

Table 4.4. Variation of percentage of monolayer with OH concentration for a single cycle of deposition.

No of OH/nm^2	% of ML for single cycle of deposition
12	58.4
10	52.0
8	45.2
6	37.9
4	30.7
2	24.2

4.11 Conclusions

A detailed chemisorption mechanism is proposed for the adsorption of methyl groups and aluminum atoms on the silica surface in the ALD of aluminum oxide using TMA/H_2O precursors. Maximum number of methyl groups that can be accommodated on unit nm^2 area of the surface is 6.25. The chemisorption process consists of six different mechanisms: complete ligand exchange, partial ligand exchange, simple dissociation, complete dissociation via ligand exchange, complete dissociation and association. Dependence of the number of metal atoms adsorbed on OH concentration is explained clearly by giving a theoretical explanation for the connection between OH, methyl and Al concentrations. The predicted Al concentration for different OH values agrees very well with reported experimental data.

It is proposed that Al concentration on the substrate surface is due to a combination of two types of chemisorption mechanisms-Complete Ligand Exchange and Complete Dissociation. For high OH concentrations CLE

dominates the process while for low OH concentrations CD dominates. L/M ratios are calculated. These are plotted against surface OH concentrations and compared against observed values and are found to agree well. We have tried to calculate GPC as a function of surface OH concentration. The range of GPC values so obtained matches very well with various reported values. The density of ALD deposited alumina film was calculated to be 2.95 gm/cc. This value is lower than the density of bulk alumina, but agrees very well with various reported experimental values for amorphous alumina films. The number of monolayers (ML) as a function of the total film thickness was calculated and was found to be in the range of 58.4 - 24.2 % of the total number of cycles of deposition. This also means that during one cycle of deposition 58.4 - 24.2% of a monolayer is formed only,which is an experimentally observed fact in atomic layer deposition of alumina. By using the unit cell dimensions of a cubic close packed system, the effective monolayer thicknesses was calculated to be 0.31nm.

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5

Deposition and Characterization of Aluminum Oxide Thin Films Prepared by Atomic Layer Deposition

This chapter describes the details of preparation of alumina (Al_2O_3) thin films by atomic layer deposition technique and their various structural, optical and electrical characterizations.

5.1 Introduction

Many materials were identified as high-k materials that have higher dielectric constant than SiO_2 but not many are compatible with the Si substrate that is used in most of the semiconductor devices. Important concerns include interface quality, film morphology, and reliability. Serious research is still needed in order to identify a promising candidate. In the present work we investigate the high-k dielectric material Al_2O_3,which can be used in complementary metal oxide semiconductor (CMOS) transistors and dynamic random access memory (DRAM) capacitors [1,2]. Characterization of these films are also included in this chapter.

5.2 Al_2O_3 as gate dielectric

As an alternative to oxide/nitride systems, much work has been carried out on high-k metal oxides as they can provide a substantially thicker (physical thickness) dielectric for reduced leakage and improved gate capacitance. Among the group III oxide candidates, aluminum oxide (Al_2O_3) is the most stable and robust material, and has been extensively studied for many applications especially in opto and microelectronics. Regarding its usefulness as an alternate gate dielectric, Al_2O_3 has many favorable properties like large band gap, band offset, kinetic stability, thermodynamic stability on Si up to high temperatures, good interface with silicon, low bulk defect density and is amorphous under the conditions of interest [3-5].

Though Al_2O_3 has relatively low dielectric constant (~9), this is more than twice (3.9) that of the widely accepted SiO_2. In particular the high chemical stability, high radiation resistance, high thermal conductivity and low permeability to alkali impurities make it suitable for application in metal oxide semiconductor (MOS) structures even in drastic conditions. Al_2O_3 was commonly used as protective layer, ion barrier layer and as diffusion barriers [4-6]. Al_2O_3 has several other applications such as passivation layers, and dielectric films in chemical sensors [6-10]. All these applications require films with good homogeneity, low surface roughness and good control of thickness for films of the order of 10Å thick or less. Al_2O_3 is one of the best high-k materials which satisfy almost all the guidelines for an ideal gate oxide.

Table 5.1 list the properties of Al_2O_3.

Properties of Al_2O_3 gate dielectric [1-2]
Dielectric constant value -9.7
Thermo dynamic stability on Si -good
Kinetic stability -good
Crystallization temperature ~1200°C
Resistivity~ high
Dielectric Strength >15MV/cm
Energy band gap ~8.9eV
Conduction band offset -2.8eV
Valence band offset with Si ~3.2eV
Low interface (Al_2O_3/Si) state density ~$10^{10}eV^{-1}cm^{-2}$
Low charge trapping density ~order of $10^{10}cm^{-2}$

In the present work we report the deposition of thin aluminum oxide films as gate oxide using the ALD technique in which excellent control of thickness, homogeneity and low value of surface roughness are achieved.

5.3 Review of Atomic Layer Deposited Al_2O_3 thin films

Alumina is the most studied ALD coated material. Still its versatility is not fully explored and large scale research is going on to pioneer new areas. A brief review of the ALD-Al_2O_3 is presented in this section, that covers only a small part of the entire work done on this material.

The first reports of ALD-Al_2O_3 using TMA and H_2O is by G. S. Higashi and C. G. Fleming in 1989 [11]. Sequential surface reactions of TMA and water vapor were used to deposit Al_2O_3 on Si(100) surfaces. High quality dielectric films were deposited at deposition temperatures of 100 °C. Resistivity of $10^{17}\Omega$-cm, breakdown strengths of 8MV/cm, and interface state densities of 10^{11}states/eV cm^2 was achieved and they suggested possible applications of alumina as a gate insulator or a dielectric passivation layer. C. Soto *et al.* [12] in 1991 discussed the possibility to grow thin films of alumina by the sequential application of TMA and water at room temperature both on high-surface-area alumina and on silicon in ultrahigh vacuum. Both infrared spectroscopy and electron energy-loss spectroscopy (EELS) studies were conducted and proposed a reaction mechanism. Low temperature growth of thin films of Al_2O_3 by sequential surface chemical reaction of trimethylaluminum and H_2O_2 was reported by F. Fan *et al.* in 1991 [13]. Trimethylaluminum (TMA) reacts with H_2O_2 readily at temperatures as low as room temperature, resulted in the identical growth of Al_2O_3. Highly insulating and ideally uniform nature of the grown films were also verified.

The surface chemistry of ALD was reported by S.M George *et. al.* in 1996 [14]. He expressed the basic model by the binary reaction sequence approach for Al_2O_3 atomic layer process using the TMA and H_2O precursors. Numerous applications of ALD films in the field of microelectronics and optoelectronics were also discussed.

Many researchers studied the structural and morphological aspects of ALD-Al_2O_3. In 1996 M. Ritala *et al.* studied [15] the morphological development of $A1_2O_3$ films grown by ALD from $Al(Cl)_3$ and H_2O by means of AFM. Film surface smoothness and RMS roughness of films were also studied. They reported that there is only a weak tendency towards

agglomeration. D. Riiheld *et. al.* [16] developed the optical dielectric muitilayer structures using ZnS and Al_2O_3 as high and low refractive index materials. They also developed various structures include antireflection coatings, neutral beam splitters, high-reflection coatings and Fabry-Perot filters. The optical performance of the fabricated components were studied by comparing their transmittance and reflectance spectra with those calculated for the ideal structures.

In 1997 S. J. Yun *et al.* [17] studied the dependence of growth temperature on ALD-Al_2O_3 film characteristics. TMA and H_2O were used as precursors and results obtained were compared with the films grown using $AlCl_3$ and H_2O. The concentration of impurities in the deposited films were also studied using SIMS and results showed that the contents of C and H in the films grown at 300°C using TMA were approximately six and 10 times higher than those of the film grown at 500°C using $AlCl_3$. In 2000 Gusev *et al.* [18] have done the physical and electrical characterization of ALD-Al_2O_3. They used medium energy ion scattering and high-resolution TEM as analysis tools. They successfully deposited Al_2O_3 films over H-terminated Si without forming an interfacial SiO_2 layer. They control the interface reactions successfully.

Several researchers have extended their study to device level. In 2000 Buchanan *et al.* fabricated [19] *n*MOSFET with ALD-Al_2O_3 as gate oxide and poly-Si gates. Fabricated structures were treated with standard processing conditions (including a rapid-thermal dopant activation anneal at T >1000°C) and electrical characterization. A leakage current of J~10^{-1} A/cm^2 at V_{bias}= V_{FB}+1 V was measured for t_{eq}=13Å, showing a reduction in leakage current of two order compared to SiO_2 of the same t_{eq} value. A trend in fixed charge correlated with Al_2O_3 thickness was also demonstrated, showing that fixed charge increases with decreasing film thickness. They also found that the fixed charge is concentrated near the interface, poly-Si interface. Furthermore, an interfacial layer was identified to contribute ~8 Å to the overall t_{eq} value. The composition of the interface layer is not known, but apparently has a k value larger than that of pure SiO_2. At an effective field of 1MV/cm, the channel carrier mobility value for Al_2O_3 was measured

to be 200 cm^2/Vs. Encouraging drive currents and reliability characteristics were demonstrated for these devices, but the significant mobility degradation clearly indicates some deleterious effects of the ALD-Al_2O_3 which warrant further investigation. The study by Park *et al.* [20] in 2000 demonstrated that boron diffuses through ALD Al_2O_3 during dopant activation anneals, and indeed this may be a serious issue for any alternative dielectric. It was reported that dopant activation anneals of 800–900°C performed on boron implanted poly-Si gates on top of ~60 Å Al_2O_3 caused significant diffusion of boron through the Al_2O_3 film and into the *n*-Si substrate, as evidenced by a flat band shift of ~1.5 V. Secondary Ion Mass Spectroscopy (SIMS) profiles also indicated a significant amount of boron in the substrate after anneal. Furthermore, the addition of an oxynitride layer, grown by an N_2O anneal before Al_2O_3 deposition, greatly reduced the flat band shift to 90 mV. In a different study by Lee *et al.*,[21] phosphorous diffusion from the n^+ poly-Si electrode into ALD-Al_2O_3 was observed under reasonable annealing conditions of 850°C for 30 min. *C–V* analysis showed a flatband shift ΔV_{FB}~670–740mV depending on the particular dopant incorporation process, which corresponds to >$10^{12}cm^{-2}$ of negative fixed charge in the film. These results indicate that phosphorous not only diffused through the Al_2O_3 layer, but also introduced fixed charge into dielectric. The authors propose that phosphorous modifies the Al_2O_3 network, causing negatively charged Al–O dangling bonds. It will continue to be extremely important to identify and understand dopant diffusion in any potential alternative gate dielectric.

In 2000 M. Ritala *et.al* [22] reported a different approach to ALD of oxide thin films. Instead of using water or other compounds for an oxygen source, oxygen is obtained from a metal alkoxide, which serves as both an oxygen and a metal source when it reacts with another metal compound such as a metal chloride or a metal alkyl. These reactions generally enable deposition of oxides of many metals. With this approach, an alumina film has been deposited on silicon without creating an interfacial silicon oxide layer that otherwise form easily. This finding adds to the other benefits of the ALD method, especially the atomic-level thickness control and excellent uniformity. It takes a major step toward the scientifically challenging to

implement process of finding promising gate dielectric for the future generations of metal oxide semiconductor field effect transistors. P. I. Räisänen *et. al.* reported in 2002 [23] ALD deposition of Al_2O_3 using $AlCl_3$ and $Al(OiPr)_3$ precursors. Here also no separate oxygen source is used. In this approach an Al_2O_3 film gets deposited on silicon without an interfacial silicon oxide layer. The film growth rate was 0.8Å cycle. The residual contents of chlorine, hydrogen and carbon in the film deposited at 300°C were 1.8, 0.7 and 0.1%, respectively. The chlorine content diminished rapidly with increasing growth temperature. The permittivities and leakage current densities were comparable to the conventional Al_2O_3 ALD processes for thick films, but the permittivity decreased for very thin films. Post deposition annealing is required to improve electrical properties of thin films.

In 2002 Kim *et al* [24] reported the deposition of Al_2O_3 using TMA and O_3 on Si (100) substrate. In this he reports that the Al_2O_3 films prepared using O_3 have significantly less amount of defect states like Al-Al and OH bonds compared with those prepared by H_2O. He also studied the device quality leakage characteristics, and concluded that Al_2O_3 film prepared with O_3 show a leakage current density one or two orders lower and a smaller flatband voltage shift than that of Al_2O_3 film prepared with H_2O, demonstrating improved interface characteristics. In 2003 S. Jakschik *et. al.* [25] reported the physical characterization of thin ALD-Al_2O_3. Structural characterizations of these films were done using time-of -flight secondary-ion-mass-spectroscopy, XPS and elastic recoil detection. In 2004 K. K. Seong *et. al.* [26] has reported about the Atomic-layer-deposited Al_2O_3 thin films with thin SiO_2 layers grown by *in situ* O_3 oxidation. The growth, thermal annealing behaviors, and electrical properties of Al_2O_3 thin films were studied. The Al_2O_3 films grown on a bare Si substrate had the highest concentration of excess oxygen which resulted in the largest increase in the interfacial layer thickness during post annealing.

Atomic Layer Deposition of Al_2O_3 film on Polyethylene Particles was reported by J. D. Ferguson *et. al.* in 2004 [27]. The presence of an Al_2O_3 film on the low density polyethylene (LDPE) particles was confirmed using

TEM. The TEM images revealed that the Al_2O_3 coating was very conformal to the LDPE particles. The Al_2O_3 coating was also thicker than expected from typical ALD growth rates. This thicker Al_2O_3 coating was explained by the presence of hydrogen-bonded H_2O on the Al_2O_3 surface that increases the Al_2O_3 growth rate during Al $(CH_3)_3$ exposures. On the basis of these results and additional investigations, a model is proposed for ALD -Al_2O_3 on polymers. Al_2O_3 was predicted to be an effective gas diffusion barrier on temperature-sensitive polymeric materials such as LDPE.

Wilson *et al.* 2005 [28] studied the nucleation and growth during ALD-Al_2O_3 on a variety of polymer substrates like polyethylene (PE), polystyrene (PS) poly(methyl methacrylate) (PMMA), polypropylene (PP), and poly(vinyl chloride) (PVC) at 85°C. Quartz Crystal Microbalance (QCM) and surface profilometry measurements were used to study the nucleation and growth of Al_2O_3 ALD on various polymer substrates were studied. This Al_2O_3 ALD growth occurs without specific chemical species that can react with TMA, such as hydroxyl (-OH) groups, on the surface or in the bulk of the polymer. The nucleation of Al_2O_3 ALD is facilitated by TMA diffusion into the polymers and the subsequent reaction of the retained TMA with H_2O. A model is developed for ALD-Al_2O_3 on polymers that are consistent with the QCM measurements and recent Fourier transform infrared (FTIR) investigations. This model establishes an initial foundation to interpret ALD on polymers and will be developed further by future studies.

In 2005 R. L Puurunen [29] published a detailed review on surface chemistry of Atomic Layer Deposition in terms of TMA and water reaction. Review includes the basic characteristics of ALD processing, history of ALD, and presented an overview of the two reactant ALD processes investigated up to 2005. Concepts related to the surface chemistry of ALD are formulated and discussed from a theoretical viewpoint. The discussion is generic for compound-reactant-based ALD processes, where the reactions are truly self-terminating and undesired side reactions are absent. The experimental results for the $AlMe_3/H_2O$ process were reviewed, especially quantitative information about surface chemistry were included in the

conclusions section. The historical assumptions, terminology, and effect of experimental conditions on the surface chemistry of ALD were also discussed. In 2006 Puurunen [30] studied the dependence of Growth rate and refractive index on growth temperature of the Al_2O_3 films. She concluded that growth rate decreased from 0.20 to 0.08 nm/cycle and refractive index increased from 1.52 to 1.65, with increasing temperature. The dielectric constant slightly increased from 6.8 to 8 with increasing growth temperature. Al_2O_3 films grown using O_3 as oxidant show a smaller hysteresis, lower leakage current density, and higher breakdown field strength compared to those using H_2O as oxidant at the same growth temperature. X-ray Photoelectron Spectroscopy results showed that the films grown at lower temperatures have smaller band gap energy. The Al_2O_3 films grown at a temperature as low as 100°C showed reasonable dielectric properties for dielectric film applications on flexible substrates.

In 2006 S. D. Elliott *et al.* [31] reported the Ozone-Based ALD of alumina from TMA with emphasis on Growth, Morphology, and Reaction Mechanism. They reported that growth rate decreases with increasing temperature. Morphological characterizations were done and results indicate that O_3 as the oxygen source yields lower-quality films than H_2O; the films are less dense and rougher, especially at low growth temperatures. In 2006 T.P. Lee [32] reported that OAO ($SiO_2/Al_2O_3/$ SiO_2) dielectric film stacks consisting of Al_2O_3 in place of Si_3N_4 in conventional ONO stacks have good charge retention capability with high charge to breakdown properties required for flash memory device application.

Protection of polymer from atomic-oxygen erosion using Al_2O_3 atomic layer deposition coatings were studied by Russel Cooper *et. al.* in 2007 [33]. Al_2O_3 ALD films with varying thicknesses were grown on the polyamide substrates and ALD-coated polyamide materials were exposed to a hyper thermal atomic-oxygen beam. The mass loss versus oxygen-atom exposure time was measured in situ by the QCM. Al_2O_3 ALD film thicknesses of ~35 Å were capable to protect the polymer from erosion.

The atomic layer deposition (ALD) of Al_2O_3 using sequential exposures of $Al(CH_3)_3$ and O_3 was also reported by Goldstein *et. al.* in 2008

[34]. The in situ Fourier Transform Infrared spectroscopy and QMS (Quadrupole Mass Spectrometry) were also carried out and deposited films were structurally characterized by TEM.

Biocompatibility of atomic layer deposited alumina thin films were studied by D. S. Finch *et.al.* in 2008 [35]. Cell adhesion and growth have been successfully demonstrated on atomic layer-deposited alumina thin films on glass cover slips. The use of an Alamar Blue assay as a measure of biocompatibility suggests that coating glass cover slips with 60nm of ALD alumina results same biocompatibility with the uncoated glass samples.

In 2009 A. S Cavanagh *et.a l* [36] has employed ALD to grow coaxial thin films of Al_2O_3 and Al_2O_3/W bilayers on multi-walled carbon nanotubes. The uncoated and ALD-coated MWCNTs were characterized with TEM and XPS. Al_2O_3 ALD on untreated MWCNTs was found to have nucleation difficulties that resulted in the growth of isolated Al_2O_3 nano-spheres on the MWCNT surface. The formation of a physisorbed NO_2 monolayer provided an adhesion layer for the nucleation and growth of Al_2O_3 ALD films. The Al_2O_3 ALD film also served as a seed layer for the growth of W ALD on the MWCNTs. The W ALD films can significantly reduce the resistance of the W/Al_2O_3/MWCNT wire. The results demonstrate the potential for ALD films to tune the properties of gram quantities of very high surface area MWCNTs.

In 2009 P. F. Carcia reported ALD Al_2O_3 as gas diffusion ultra barrior on polymer substrate [37].Thermo-mechanical properties of alumina films using atomic layer deposition technique was reported by David C. Miller *et.al.* in 2010 [38]. Inter digitalized humidity sensors with ALD coatings of aluminum oxide demonstrated no leakage current relative to uncoated sensors stored in the ambient, indicating Al_2O_3 may be used to limit the effects of H_2O and other chemical species in miniaturized mechanical and electronic devices. The long term durability of such coatings is not known, but may be predicted from the related material characteristics. The film stress and coefficient of thermal expansion for Al_2O_3 were determined using the wafer curvature method. Film stress was also characterized using thermal cycling up to 500°C.

"Atomic Layer Deposition: An Overview" by S. M George in 2010 [40] reported Al_2O_3 ALD as a model ALD system and ALD Al_2O_3 on carbon nanotube, graphene substrates, particles and polymers. This review includes general overview of ALD.

In 2011 Dragos Seghete *et.al.* [40] fabricated latterly graded Al_2O_3 layers by using variant ALD techniques for X-ray optical applications. The transformation of conformal Al_2O_3 ALD films into laterally graded layers is achieved by controlling the reactant source location in the ALD reactor.

Armin Richter reported in 2011 [41] that ALD Al_2O_3 of 5Å thickness acts as the surface passivation layer on silicon substrates. He also reported that four ALD cycles of Al_2O_3 are sufficient to reach the full potential of surface passivation, and even with one atomic layer of Al_2O_3 (one ALD cycle) emitter saturation current densities as low as 45 fA/cm^2 can be reached on boron-diffused emitters.

B. Vermang et.al published a short communication in 2011 about spatially separated atomic layer deposition of Al_2O_3, a new option for high throughput Si solar cell passivation [42].

5.4 Preparation of Al_2O_3 thin films by ALD

Experimental

Atomic Layer Deposition of aluminum oxide was carried out in our homemade ALD reactor. Tri Methyl Aluminum (Sigma Aldrich) and De-Ionized (DI) water were used as precursors and high purity N_2 as the carrier gas. Various substrates used in the present study are glass, quartz and Silicon wafer p(100). Initially the deposition chamber was evacuated to a base pressure of 1×10^{-5} mbar using oil diffusion pump and rotary pump. After attaining this base pressure, chamber was filled with N_2 to medium vacuum level and evacuation is directly switched to rotary mode and remaining part of the deposition is done at rotary vacuum. Purge gas was then admitted to the chamber through mass flow meters. The chamber pressure was adjusted by controlling N_2 flow, which was done by combined controlling of needle valve, mass flow meter, butterfly valves and solenoid valves installed in precursor line. Precursors were initially loaded in SS bubblers and delivered

to the reaction chamber in alternate sequence separated by N_2 purge. The entire ALD cycle was controlled by a sequence controller which was interfaced to a desktop computer. Substrate holder was placed over a sealed heater and in our experiments substrate temperature was varied between 30^0C to 300^0C.

Table 5.2: Various deposition parameters

Pulse time in Seconds				Chamber	Substrate	Flow	Mode	Infer-
TMA	Purge	H_2O	Purge	Pressure (mbar)	Temp (^{0}C)	rates sccm		ence
0.5	5	0.5	5	0.790	350	500	thermal	no film
0.5	15	0.5	15	0.300	150	500	plasma	Poor
0.5	10	0.5	10	0.180	300	500	plasma	good
0.5	15	1	15	0.270	300	500	plasma	good
1	5	1	15	0.260	250	350	plasma	good
1	15	1	15	0.460	250	350	plasma	good
1	15	1	15	0.220	280	50	plasma	good
1	10	1	10	0.430	250	350	thermal	good
3	15	2	15	0.096	210	260	plasma	good
3	15	1	15	0.270	190	260	thermal	good
3	15	2	15	0.140	210	260	thermal	good
2	15	2	15	0.190	225	260	thermal	good
3	15	3	15	0.200	120	260	thermal	good
3	15	3	15	0.560	225	210	thermal	good
3	15	3	15	0.270	120	210	plasma	poor

During deposition nitrogen flow, substrate temperature and chamber pressure were kept constant. Each ALD cycle consisted of (I) 3-second dose of metal precursor (II)15 second nitrogen (argon) purge (III) 2-second dose of water and (IV) another 15 second purge. During purge no precursor was introduced in to the reactor. In order to optimize the atomic layer deposition system experiments were repeated at various substrate temperatures,

precursor delivery time and purge time and different purge rates. Table 5.1 lists some of the experimental conditions that we have studied in detail.

Effect of precursor delivery on growth rate

The liquid precursors used for ALD-Al_2O_3 has sufficient vapour pressure, Tri Methyl Aluminum (13mbar) and water (31mbar), so that they can be used without a carrier gas. The amount of precursor flow is calculated using pressure in the reactor chamber. The pressure value is also affected by the location of the pressure gauge. We treat pressure value as reference to repeat our experiments at a fixed precursor dosage. Based on ideal gas theory a precursor pulse of a constant flow rate for a particular time contains a fixed number of molecules. ALD is a self limiting growth process and growth per cycle depends on the number of sufficient OH sites and sufficient precursor pulsing [29,43].

Table 5.2 gives the observation by varying TMA, H_2O pulsing time from 0.5 to 3 seconds and purge time from 5 to 15seconds. It is clear that the precursor exposure time and purge time is not much critical as in chemical vapour deposition (CVD). This means ALD has a wide range of deposition parameters.

Successful layer-by-layer deposition in an ALD process with sufficient exposure and purge times and full saturation of the surface, should in principle result in extremely uniform layers. Non-uniformity of the deposited layer can be attributed to one (or more) steps in the ALD cycle. Insufficient purge steps and less amount of precursor may cause some vapor phase reactions which leads to an increase in deposition rate that might be localized. Incomplete saturation of one of the two precursors is easily related to the amount supplied (time or concentration) and usually clearly visible as a decay in thickness in the direction of the precursor flow. Even though, if excess amount of precursor is pulsed that doesn't vary the growth rate as the excess precursor is purged out in the next sequence. Long purge does not vary the GPC.

Effect of number of cycles on growth per cycle

Thickness of the ALD grown film is often directly proportional to the number of ALD reaction cycles carried out especially when thicker films are grown. This means the amount of material deposited is less, and growth per cycle is a constant over cycles. During the initial phase of the deposition the growth per cycle is varied over the number of cycles that results variation in GPC. This varying GPC may be due to the fact that, the material deposited by ALD has different surface characteristics than those of the substrate where the film is grown.

ALD process modifies the chemical composition of surface by material deposition. The initial ALD reaction cycles occur usually on the surface of the original substrate and the following cycles on the surface of both the original substrate exposed and ALD deposited material. After few ALD cycles thickness of the film depends on growth per cycle and growth mode. The mechanism of saturating reactions and number of reactive sites may be different on the two materials (substrate and grown material). Thus growth per cycle should vary accordingly with the changes in chemical composition of the surface.

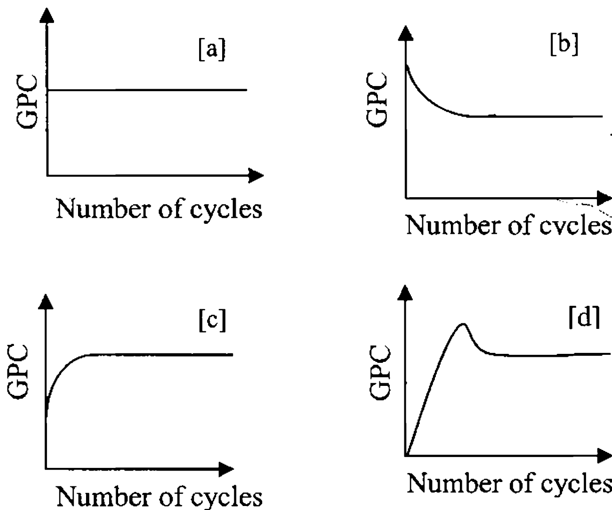

Figure 5.1: Dependence of Growth per cycle on number of cycles (a) linear growth (b) Substrate enhanced growth (c) Substrate inhibited growth of type 1 (d) Substrate inhibited growth of type 2.

ALD process can be divided into four groups (Figure 5.1) on the basis of how growth per cycle varies with number of ALD reaction cycles. They are (1) linear growth (2) substrate enhanced growth (3) Substrate inhibited growth of type 1 (4) Substrate inhibited growth of type 2 [29].

In all groups the GPC is constant after sufficient number of ALD cycles. In linear growth, number of reactive sites on the surface does not change with number of the deposition cycles and hence GPC is constant over the entire cycles. In substrate enhanced growth the number of reactive sites on the substrate surface is higher than ALD grown material, hence GPC is higher in the initials cycles than at the steady regime. In Substrate inhibited growth of type 1 the number of reactive sites on the substrate surface is lower than that of ALD grown surface and hence GPC is lower during initial cycles than steady regime. But in Substrate inhibited growth of type 2 GPC additionally goes through a maximum before setting to a steady value. Island growth seems to occur in substrate inhibited growth of type 2.

Various ALD growth mechanisms

The amount and type of surface sites also affects how the deposited material is arranged on the surface during ALD growth, defined as the growth mode (Figure 5.2). The growth mode is an important characteristic in ALD as it influences several material characteristics such as layer closure, density and roughness. As for the effect of the starting surface on the GPC, three general classes of growth modes can be distinguished [29]. In two-dimensional growth, the precursors chemisorb preferentially in the lowest unfilled material layer. As a result, one monolayer of the ALD-grown oxide covers the original substrate completely while further growth proceeds monolayer by monolayer. As the GPC is typically less than a monolayer, this growth mode is not evident in ALD. When the precursors chemisorb preferentially on the ALD-grown material instead of on the starting surface, growth is established through microscopic islands. With island growth, the ALD precursors are unreactive towards the starting surface and growth is initiated at reactive defects on the substrate. Further growth proceeds symmetrically around these defects until the islands are large enough and

they coalesce into a closed layer. The third growth mode, random deposition, is a statistical growth mode, where material deposits with equal probability on both the starting surface and the ALD layer. A first indication of the type of growth mode is given by the starting surface dependence of the growth curve as the highest GPC typically implies the most efficient substrate coverage. Strong inhibition during the first ALD cycles, on H-terminated Si, has been associated with island growth while linear and substrate-enhanced growth results in the most two-dimensional surface coverage. Better growth and material characteristics are obtained when reactive Si-OH sites are introduced on the surface, but these sites imply the presence of an interfacial SiO_2 layer which adds to the EOT of the gate stack. Figure 5.2 is a schematic representation of the different growth modes in ALD: (a) two-dimensional growth, (b) island growth and (c) random deposition. The arrow indicates the increasing number of ALD cycles. The discussed effects on GPC and growth mode are not strictly related to the type of substrate material, but to any system where the amount and type of available surface sites is not constant during ALD growth. Hence, variations in GPC and deviations from two-dimensional growth are also possible during the ALD of ternary oxides, as their composition determines the type and amount of sites on the exposed surface.

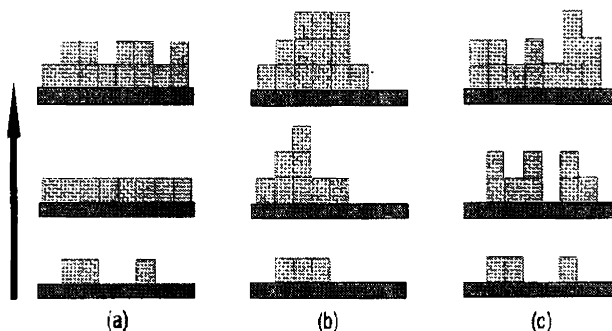

Figure 5.2: Schematic representation of the different growth modes in ALD: (a) two-dimensional growth, (b) island growth and (c) random deposition. The arrow indicates the increasing number of ALD cycles.

Figure: 5.3 (a) and (b) shows Al_2O_3 film thickness as a function of the completed number of deposition cycles for thermal ALD process. The thickness measurements were done using ex situ Spectroscopic Ellipsometry. During deposition the substrate temperature and chamber pressure were kept at 210^0C and 0.20 mbar respectively.

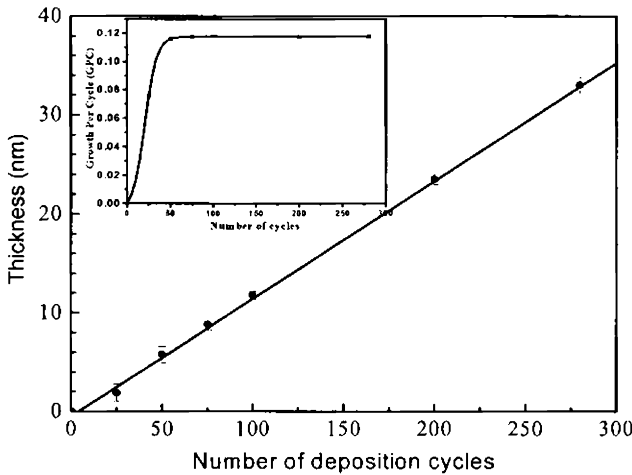

Figure 5.3: (a) Al_2O_3 film thickness as a function of the number of cycles for thicker (no. of cycles > 100) films. Insets shows GPC curve for thicker films.

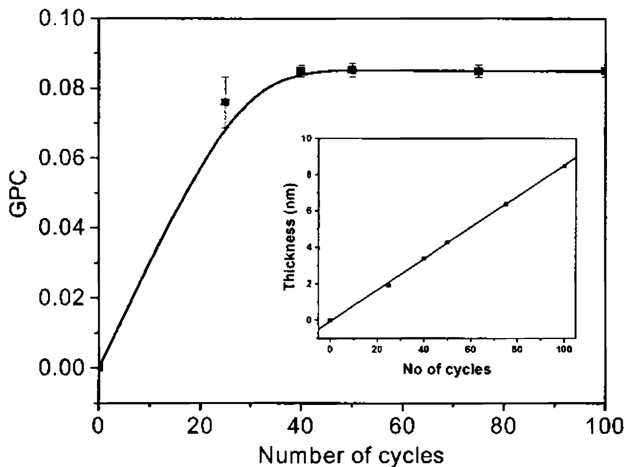

Figure 5.3(b): GPC curve for thinner films, insets shows Liner dependence of thickness on number of deposition cycles for thinner (no of cycles <100) films.

As expected, the thickness increases linearly with number of completed cycles. Growth per cycle (GPC) calculated from the linear fit of the data has a value of 1.17Å/cycle for thicker films and 0.83Å/cycle for thinner films. Insets of Figure 5.2 and Figure 5.3 show the corresponding GPC and thickness. From the nature of GPC curve we can confirm that the present growth model is substrate inhibited growth of type1.

5. 5 Characterizations of Alumina films

5. 5. 1 Compositional analysis

The chemical composition of the films was evaluated using XPS and EDS.

XPS Analysis

XPS spectra of the deposited samples were recorded using an ULVAC-PHI unit (model: ESCA5600 CIM) employing argon ion sputtering (Voltage = 3 kV, pressure 10^{-8} mbar). Al Kα X-ray (1486.6 eV) with a beam diameter of 0.8 mm and power of 400 W was used as the incident beam.

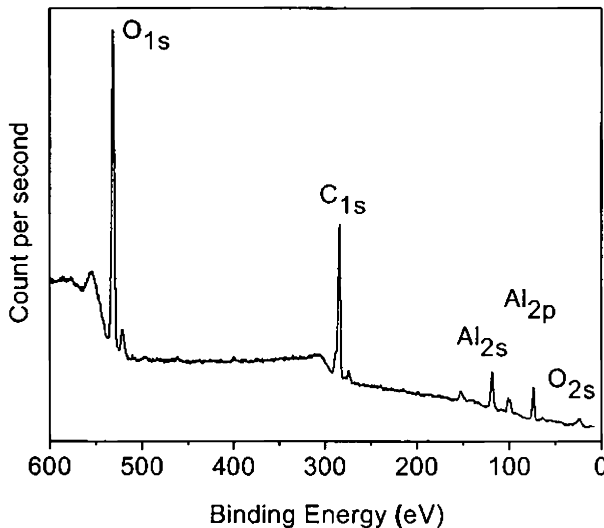

Figure 5.4: XPS spectra of the as deposited ALD-Al_2O_3 film

Figure 5.4 shows the XPS spectra of Al_2O_3 film deposited on p-type silicon wafer. All binding energies were referenced to C_{1s} peak at 284.457 eV. The appearance of Al $_{2s}$ at 118.95 eV and Al_{2p} at 74.64 eV confirms the formation of Al_2O_3. Figures 5.5(a &b) shows XPS peaks of Al_{2p} and O_{1s}. From the figure it is clear that Al_{2p} spectra consists of only a single peak centered around 74.64 eV, which corresponds to Al-O bonds of Al_2O_3 [44,45]. The absence of shoulder region around 72.5eV confirms that the Al-Al bonds are not present in our film. This higher binding energy of Al_{2p} indicated the change of oxidation state of Al from metallic state to Al^{3+} which corresponds to a conversion from sub stoichiometric Al_2O_x to Al_2O_3 [46].

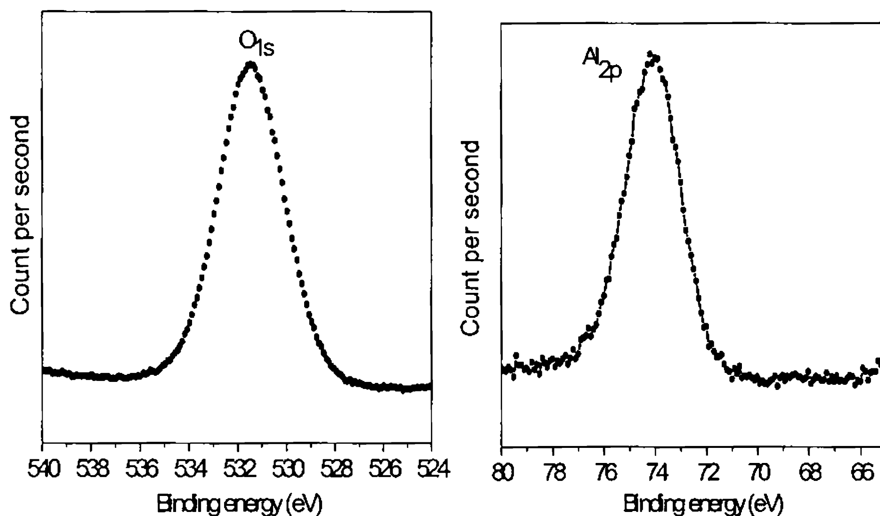

Figure 5.5: (a) O_{1s} (b) Al_{2p} spectra of the as deposited films

EDS Analysis

Atomic concentrations of Al, O and Si of the deposited films were studied by EDS analysis and the results were tabulated in Table 5.3. In the samples which were prepared at optimum condition for thermal ALD, the ratio of the atomic percentages of oxygen and aluminum was found to be very close to the ideal value. The samples prepared at wide range of chamber pressures (0.14-0.56 mbar, Table 5.2) show good results for confirm the fact

that the chamber pressure is not a critical deposition parameter in ALD as compared to CVD.

EDS was taken from different points on the surface and their mean value was taken as the actual composition of each samples. Since we have prepared samples on Si substrate, definitely an interfacial layer of SiO_2 will be present and hence it is difficult to separate the contributions of oxygen from SiO_2 or from the environment. The accuracy of EDS measurement is low and it can provide only total percentage of element present in the sample. We have confirmed our results using XPS analysis and obtained a comparable O/Al ratio of 1.40 from XPS data.

Table 5.3: EDS data of Al_2O_3 film on Silicon wafer

Pressure (mbar)	Element	Mass %	Error %	Atomic %	O/Al ratio
0.180	O	46.08	0.05	59.04	1.4414
	Al	53.92	0.07	40.96	
0.210	O	33.49	0.01	46.41	
	Al	33.75	0.01	27.73	1.6736
	Si	32.75	0.01	25.83	
0.270	O	49.91	0.02	62.69	
	Al	50.09	0.03	37.31	1.6806
0.320	O	49.54	0.01	62.34	
	Al	50.46	0.02	37.66	1.6553
0.400	O	15.92	0.01	24.79	
	Al	17.89	0.02	16.59	1.4943
	Si	66.19	0.01	58.70	

5.5.2 Structural Analysis

Structural characterizations of the prepared thin films were done using Powder XRD and GXRD (glancing angle at 0.5°) using Cu Kα radiation. The XRD patterns are shown in figure 5.6 and 5.7 respectively. The only peak in the powder XRD is that of silicon substrate.

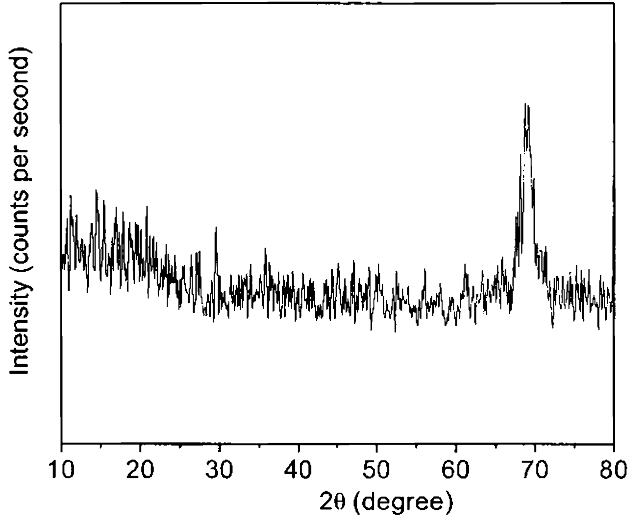

Figure 5.6: Powder X-ray diffraction pattern of ALD coated Al_2O_3 sample deposited over Si wafer.

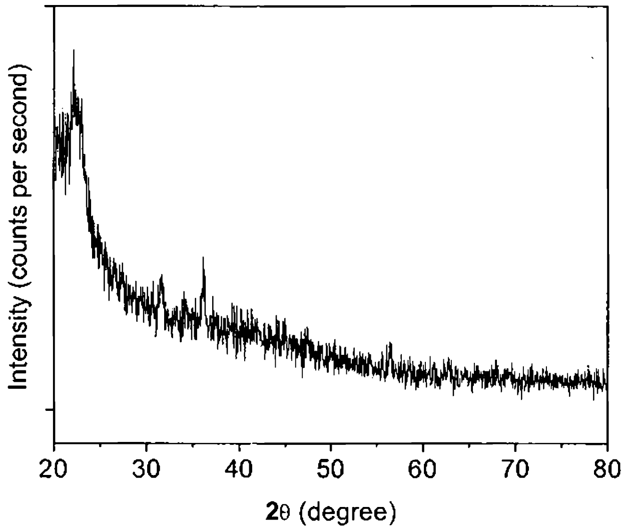

Figure 5.7: GXRD pattern of ALD deposited Al_2O_3 samples.

The absence of sharp peak in both patterns confirms the amorphous nature of alumina which is one of the major requirements for a gate dielectric [4].

5. 5. 3 Surface analyses

The surface morphologies of the as-deposited Al_2O_3 films were studied using Scanning Electron Microscopes (FESEM, SEM) and Atomic Force Microscope (AFM). Figure 5.8 (a) shows a comparison between the coated and uncoated surface. (b) & (c) are the surface coated with 200 cycle with 200 and 1000 times magnification respectively. (d) shows the image of a thick sample (1000 cycles).Some particle formation is observed in thick samples.

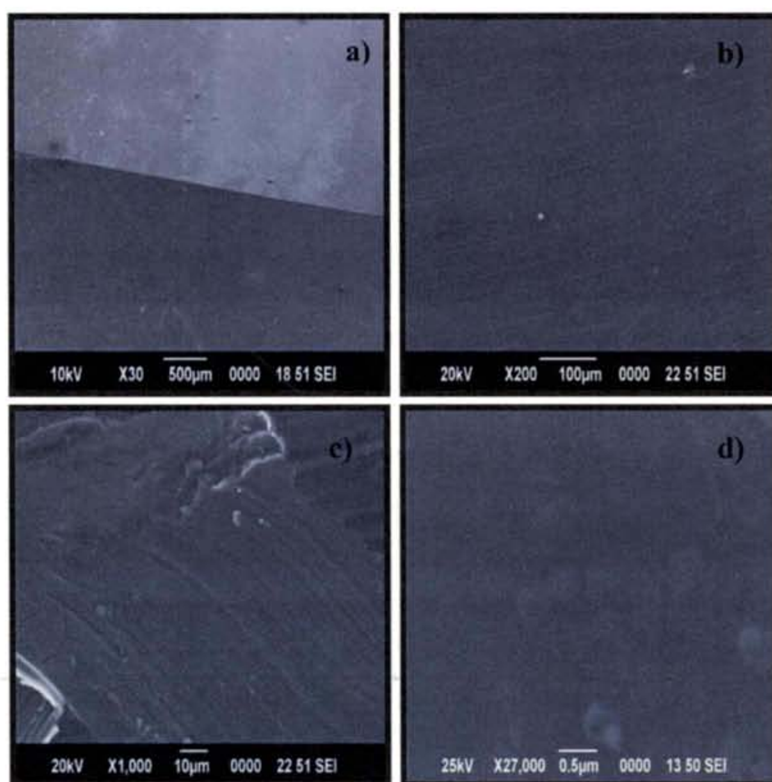

Figure 5.8: SEM images of Al_2O_3 samples (a) coated and uncoated surface, (b) completely coated surface (200 cycle) (c) higher magnification (200 cycle) (d) 1000 cycle ALD-Al_2O_3.

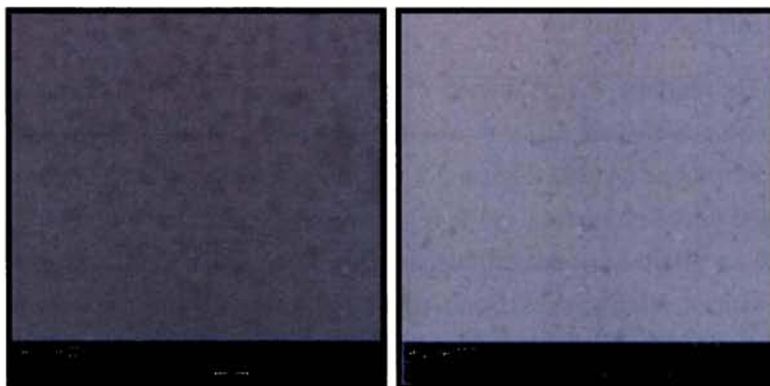

Figure 5.9: FESEM images of Al_2O_3 samples (a) 25ALD cycles, (b) 40 ALD cycles.

Figure 5.9 shows FESEM images of two samples prepared after 25 and 40 cycles of ALD respectively. It is clear that sample prepared with 25 cycles has more islands like structure than the second. In random deposition model, new material units have equal probability on all surface sites. This surface smoothness can also be confirmed using atomic force microscope measurement. Figure 5.10 shows AFM images of ALD deposited samples.

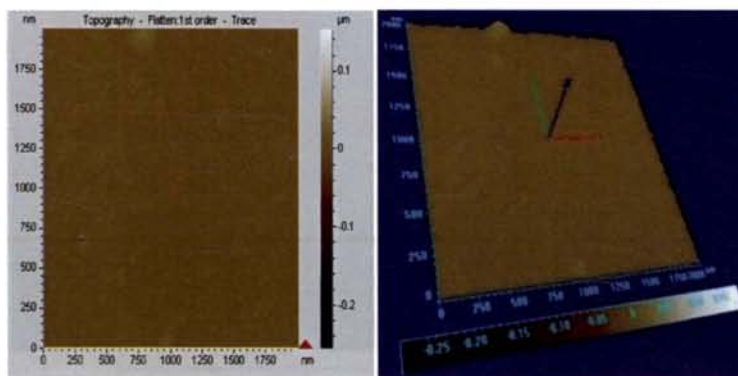

Figure 5.10: AFM image of ALD-Al_2O_3 films on Si(100): (a) 25 cycle (2D), (b) 25 cycle (3D)

AFM examination reveals that there is sharp island or particles formation observed in deposited films with sufficient thickness variation. Root-mean-square (RMS) surface roughness was found to be 1.128nm (over an area of 2 × 2µm^2) which indicate that the present Al_2O_3 samples on silicon are relatively smooth on an atomic-scale. Some particles formation was observed on thick films prepared at 1000cycles.

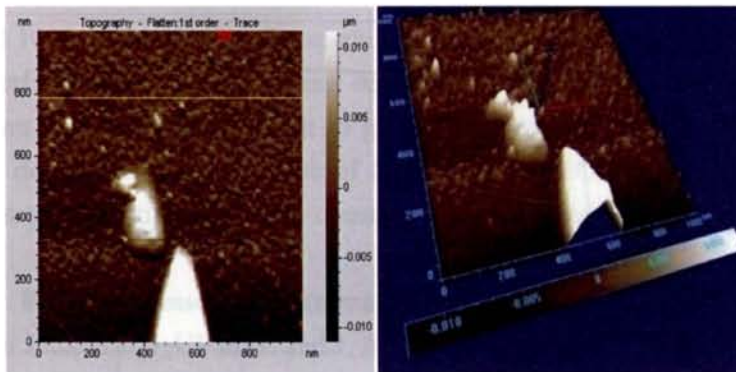

Figure 5.10: AFM image of Al_2O_3 film deposited on Si(100): (c) 50cycles (2D), (d) 3D

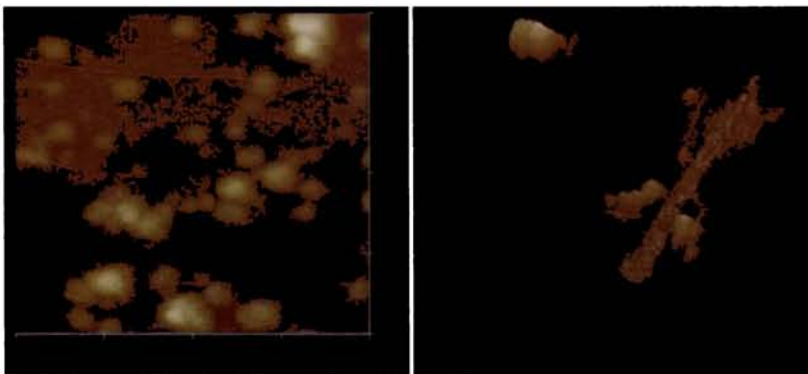

Figure 5.11: AFM images of thick ALD-Al_2O_3 films on Silicon(100) (a)1000 cycles (2D),(b) 3D

5.5.4 Optical properties

Optical Characterization of Al_2O_3 thin films are very important due to their increasing applications as protective and ion barrier layers in electronic and optoelectronic devices. Above 90% transmittance is obtained for 170nm thick samples for whole visible range, which is comparable to that of the best quality films produced by other techniques [46,47].

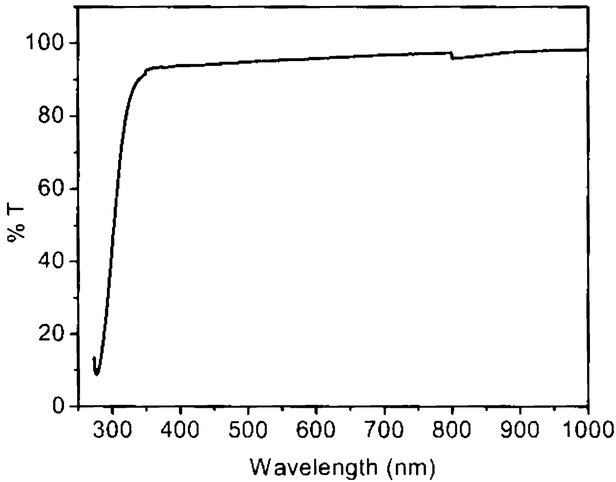

Figure 5.12: Transmission spectra of Al_2O_3 samples

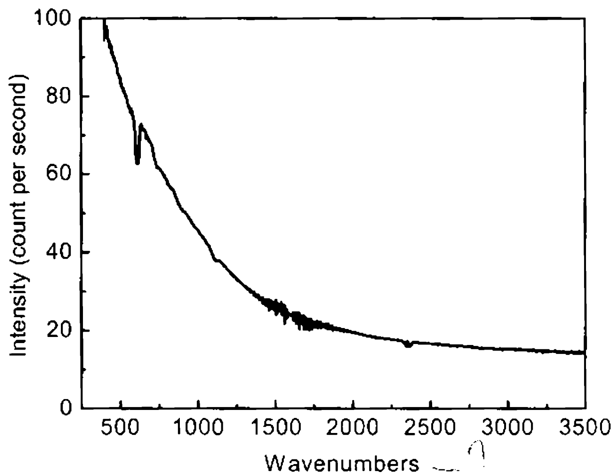

Figure 5.13: FTIR spectra of ALD coated Al_2O_3 film

Figure 5.13 shows the FTIR spectra of Al_2O_3 film (174nm) deposited at 210^0C. In literature FTIR results from thick and amorphous Al_2O_3 samples present a wide band centered around $700cm^{-1}$. This band corresponds to the overlapping of the Al-O stretching mode ($750-850cm^{-1}$) and O-Al-O bending mode ($650-700cm^{-1}$) [27,48-52]. Atomic layer deposited Al_2O_3 usually show a characteristic Al-O-Al band centered around 620 $cm^{-1}$and samples intensity of this band is small. Absence of absorption peak at 1050- 1100 cm^{-1} (Si-O stretching mode) clearly indicates that there is no interfacial SiO_2 formed during deposition. It has been reported in the literature that it is very difficult to get rid of these native SiO_2 formation during deposition. The existence of SiO_2 increases EOT of the films and reduces the effective dielectric constant of the alternate high-k dielectric [52].

Film thicknesses were measured using a spectroscopic ellipsometer (Horiba Jobin Yvon–UVISEL and J. A. Woolman Co. M 2000U) and related parameters like dielectric constant and refractive indices were extracted using a simulation software (Delta Psi).The values of Ψ and ∇ were obtained over a spectral range of 200nm-830nm at an incidence angle of 70°. The best fit model was obtained using a three-layer model that included a roughness layer at the sample surface.

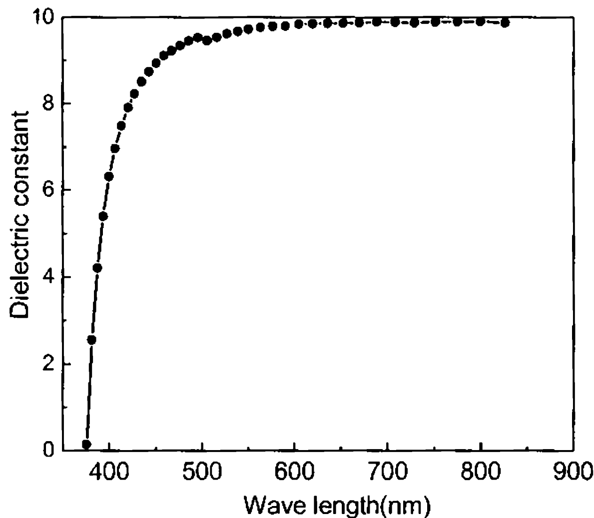

Figure 5.14: Extracted dielectric constant from ellipsometric studies

The figure 5.14 shows the extracted dielectric constant (k) from ellipsometric studies and obtained a value of 9.7 which is very close to experimentally reported values [4,53,54]. Figure 5.15 shows the extracted refractive index versus thickness of the samples. A mean refractive index value of 1.645 was observed at wave length of 550nm which is very close to the reported values [55].

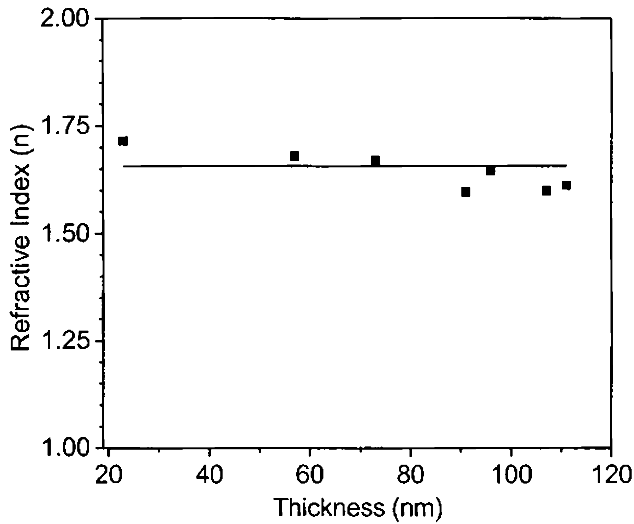

Figure 5.15: Variation of refractive index with thickness

5. 5. 5 Electrical properties

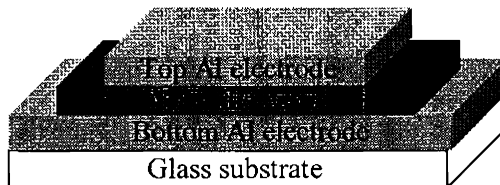

Figure 5.16: MIM capacitor structure

Aluminum oxide (Al_2O_3) is one of the best stable dielectric material. In order to study the dielectric properties of the ALD alumina MIM capacitors were fabricated as shown in Figure 5.16. Aluminum was used as metal electrodes, which were thermally evaporated at a thickness of 100 nm.

The dielectric properties of the fabricated MIM capacitor were studied using LCR meter (Fluke PM6306).

Variation of capacitance with frequency is shown in Figure 5.17 As frequency increases capacitance decreases. The decrease in capacitance value with frequency is more pronounced at low frequencies. The dielectric constant of the different samples were calculated from measured capacitance at a frequency of 10 KHz. The results were tabulated in Table 5.3.

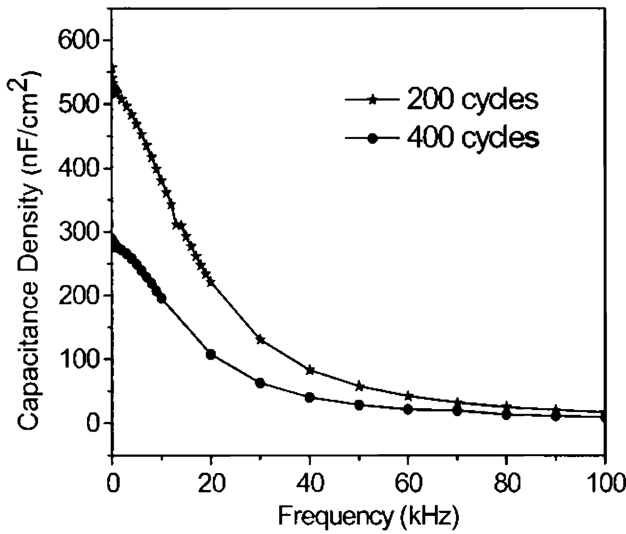

Figure 5.17: Variation of capacitance with frequency

Table 5.3: Dielectric data of MIM capacitors

No of ALD cycles	Thickness of dielectric layer (nm)	Measured capacitance (nF)	Capacitance density	Dielectric constant calculated
100	11	68.61	857.63	9.348
200	22	220.7	380.52	9.797
300	33	23.10	256.67	9.570
400	44	60.40	172.71	9.746

5.6 Conclusions

Al_2O_3 thin films were grown by Atomic Layer Deposition using TMA and water as precursors. The deposition conditions were optimized. Linear dependence of thickness over the number of cycles was verified. The growth per cycle was experimentally calculated and has a value of 1.17Å/cycle. Stoichiometric composition of grown films were studied using XPS and EDAX. Deposited films were structurally, optically and electrically characterized.

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6

Fabrication and Characterization of $Al/Al_2O_3/p$-Si MOS Capacitors

MOS capacitors were fabricated on silicon substrates. ALD deposited Aluminum Oxide was used as dielectric material. Various electrical and dielectric characterization of these structures were done in detail.

6.1 Introduction

As technology demands smaller devices due to various reasons newer processes have to be developed to fabricate nanoscale devices. Metal-Oxide-semiconductor (MOS) type structures play a crucial role in many such devices especially in microelectronics and optoelectronics. In recent years there has been a growing interest in metal oxides as dielectric materials for gate oxide of MOSFETs and stable capacitors in ultra large scale integrated electronic circuits (ULSI). Maintaining the quality and reliability of gate oxides is one of the most critical and challenging tasks in any MOS devices. Study of the MOS structure is a source of a wealth of interesting and important informations from the material science point of view. It also provides an insight into semiconductor surface conditions during device operation. Numerous studies have been conducted and various models were developed for understanding the behavior of oxide-semiconductor interface and the current transport mechanisms in MOS capacitors [1,2,3]. This is essential for the design and manufacture of better-quality, long-lived and faster schottky and MOS structures like capacitors, diodes, transistors and integrated circuits. The performance and reliability of these devices are strongly dependent on the formation of insulator layer (native or deposited), interface states (N_{ss}) localized at the semiconductor-insulator interface and the series resistance (R_s). The electrical and dielectric properties of these devices strongly depend on applied voltage, frequency and temperature. Hence an understanding of the effect of frequency and bias voltage on the

electrical and dielectric properties is very much essential for designing MOS devices.

Nevertheless satisfactory understanding of all details has still not been achieved. At high-frequencies (such that the carrier life time η is much larger than $1/\omega$ where ω-angular frequency of the applied gate voltage) the charges at the interface states cannot follow an ac signal, whereas at low-frequencies they can easily follow the signal. Therefore, the dependence of electrical and dielectric properties on frequency is very crucial while considering the accuracy and reliability of such devices [4-8].

In the present work we report the effect of bias voltage, frequency and temperature on electrical and dielectric properties of Al/Al_2O_3/p-Si structure in which the Al_2O_3 dielectric layer is deposited by ALD.

6.2 Metal-Oxide-Semiconductor structures (MOS)

Metal-Oxide-Silicon (MOS) capacitor is the basic structure used in silicon FET to control the conductive channel by gate bias. Figure 6.1 shows the cross sectional view of a MOS capacitor, where V_G is the applied gate voltage. For an ideal MOS capacitor, both the oxide and the oxide-semiconductor interface are assumed to be free of charges and defect states. Depending on the polarity and magnitude of the applied gate voltage, the carrier concentration and band structure of semiconductor changes resulting in different electrical characteristics of the MOS capacitor.

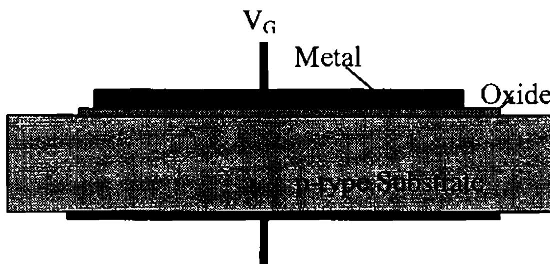

Figure 6.1: Schematic diagram of MOS Capacitor

A MOS structure with Φ_{MS}, which is the work function difference between metal and semiconductor is zero and no interface and mobile

charges in the oxide is called an ideal MOS capacitor. Figure 6.2 shows the energy band diagram of an ideal MOS capacitor, with p-type semiconductor at thermal equilibrium (V_G=0). Φ_M-metal work function, χ_i-electron affinity of the insulator, χ-electron affinity of semiconductor, E_g-energy gap of semiconductor, Φ_B-potential difference between the metal Fermi level and conduction band of the insulator, Ψ_B-potential difference between the intrinsic Fermi level (E_i) and Fermi level (E_F) inside the bulk, E_C-conduction band edge and E_V -valance band edge of the semiconductor. These energy barriers prevent the free flow of carriers from the metal to the silicon or vice versa. Thus the application of a bias across the MOS capacitor does not result in current flow. Rather, an electric field is established in the oxide by surface charge layers that form in the metal and on the silicon-oxide interface [1,9,10].

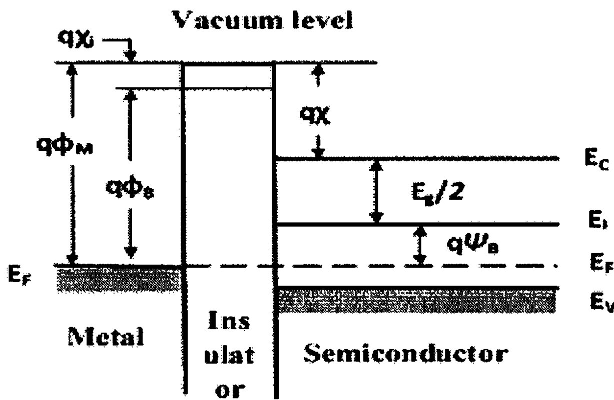

Figure 6.2: Energy-Band diagram of ideal MOS structure in thermal equilibrium constructed from a p-type semiconductor substrate.

For an ideal MOS system, when the applied gate voltage V_G= 0 the energy bands are flat and known as flat band condition. From figure 6.2, the work function difference can be written as follows [2,10]:

$$\Phi_{ms} = \Phi_m - \Phi_s = \Phi_m - \left(\chi + \frac{E_g}{2q} - \Psi_B\right) = 0 \qquad (6.1)$$

Where Ψ_B is negative for p-type and positive for n-type substrates (equation.6.4).

When a gate voltage $V_G \neq 0$ is applied to an ideal MOS structure, the charges are distributed at the semiconductor-insulator or metal-insulator interface with equal amount and opposite polarities. It is assumed that under applied gate voltage V_G, there is no charge transfer throughout the insulator, which means that it has an infinite resistance. Depending on the polarity and magnitude of the gate voltage, the MOS can control the type and value of the current through MOSFET channel. There are mainly three working regions for a MOS capacitor depending upon whether applied gate voltage is positive or negative.

Accumulation:

We consider a MOS structure in which the semiconductor is p-type. When a negative voltage V_G is applied to metal terminal of the MOS structure, it will develop an internal electric field in the oxide in the direction of semiconductor to metal. This electric field piles up holes of p-type semiconductor and accumulate near the interface. The change in the free carrier concentration at the interface bends the band diagram of the semiconductor at the interface as shown in Figure 6.3 (a).

Free electron and hole (n & p) concentrations of semiconductor at the oxide-semiconductor interface are given by:

$$p = N_v exp\left[-\left(\frac{E_F-E_V}{kT}\right)\right] \tag{6.2}$$

$$n = N_c \exp\left[-\left(\frac{E_C-E_F}{kT}\right)\right] \tag{6.3}$$

Where N_c- effective density of states in the conduction band, N_v- effective density of states in the valence band E_F -Fermi level energy, E_V- valance band energy and E_C-conduction band energy. As the hole concentration (p) increases at the interface, E_F-E_V term must decrease.

Therefore, the valance band, conduction band and intrinsic Fermi level bends up at the interface. MOS capacitor in accumulation behaves like a parallel plate capacitor and system capacitance becomes equal to that of oxide capacitance, C_{ox}.

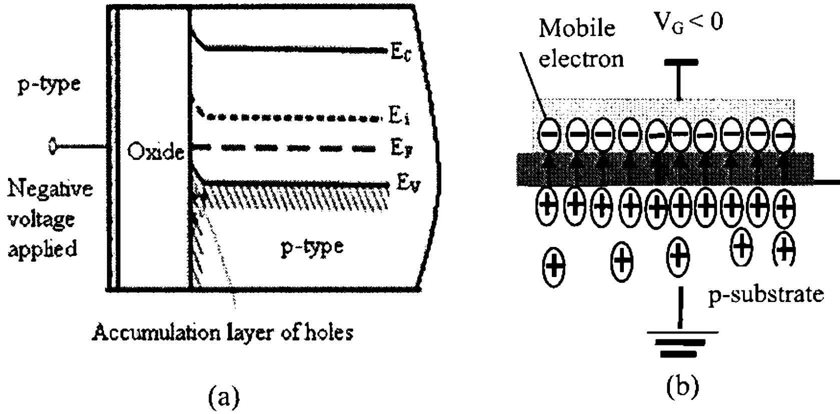

Figure 6.3: Energy band diagram of MOS capacitor in accumulation region (a) Band bending at the interface and (b) Distribution of charges on the gate and semiconductor due to applied gate voltage $V_G< 0$.

Depletion

When a positive voltage V_G, is applied to metal terminal of MOS structure, there develops an internal electric field in the downward direction from metal to semiconductor and the holes at the interface of semiconductor are pushed towards the bulk silicon. As a result the majority carrier density is diminished at the oxide semiconductor interface. This surface region with decreased majority carrier density is called 'depletion region' or 'space charge region'. Only negatively charged acceptor ions fixed to the silicon network remain in the depletion region. From Equation 6.2, the decrease of hole concentration at the interface causes an increase in (E_F -E_V), which results in the bending down of bands at the semiconductor-oxide interface. Cross-section and energy band diagram of MOS capacitor under this condition are depicted in Figure 6.4.

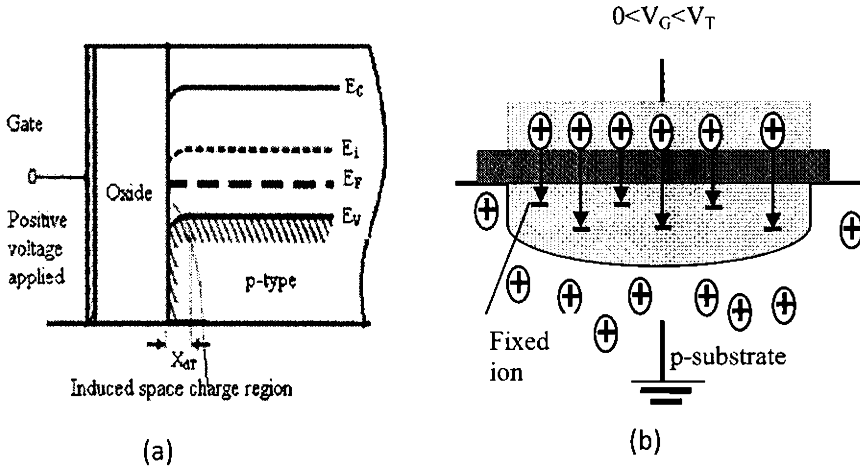

Figure 6.4: (a) Energy band diagram of MOS capacitor in Depletion mode, (b) charge distribution on the metal and semiconductor due to applied gate voltage

Inversion

As we continue to increase positive gate voltage, bands continue bending down and conduction band edge E_C gets closer and closer to the Fermi level E_F. At a certain point, intrinsic Fermi level E_i reaches to the Fermi level E_F where electron and hole concentration at the surface of the semiconductor becomes equal. At this voltage value of V_G, surface of semiconductor behaves like an intrinsic semiconductor with equal electron and hole concentrations.

As the gate voltage V_G is increased further electron concentration on the surface of the semiconductor continues to increase. The value of V_G at which the electron concentration at the surface become equal to the hole concentration in the bulk is called 'Threshold voltage' (V_T). At V_T E_i bends downward by twice the bulk potential. From the intrinsic surface condition upto this point the region is known as 'weak inversion region'. Usually weak

inversion region is considered to be the part of depletion region. The region of band bending for $V_G > V_T$ is called 'strong inversion' or just inversion.

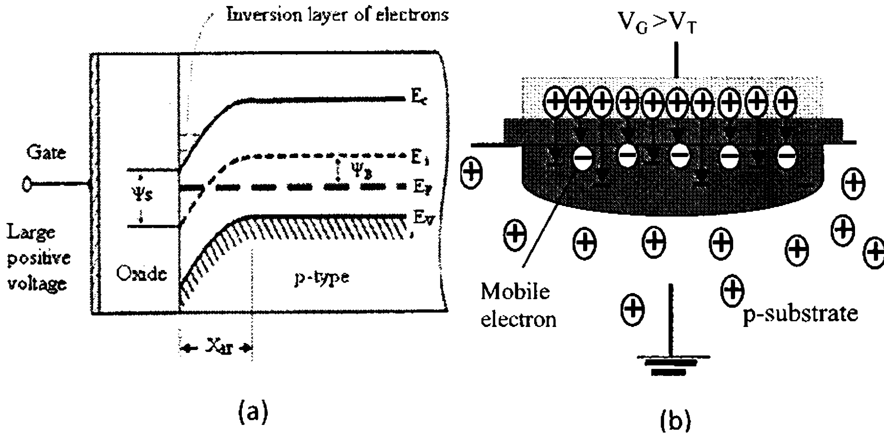

Figure 6.5: (a) Energy band diagram of MOS capacitor in Inversion mode, (b) charge distribution on the metal and semiconductor due to applied gate voltage.

The three working regions of a MOS capacitor are usually described by bulk potential Ψ_B and surface potential Ψ_S (Equations 6.4 & 6.5). Bulk potential is the potential difference between the intrinsic Fermi level and Fermi level inside the bulk, where as surface potential is the potential difference between the intrinsic Fermi level inside the bulk and at the interface.

$$\Psi_B = \frac{E_F - E_{ib}}{q} \tag{6.4}$$

$$\Psi_s = \frac{E_F - E_{is}}{q} \tag{6.5}$$

The internal parameter Ψ_S can be controlled by the external voltage V_G (Equation 6.6). By applying a varying gate voltage V_G, the charge concentration at the surface of the semiconductor can be changed and the surface potential of the system changes accordingly as per the polarity of the applied gate voltage.

$$V_G = V_{ox} + \Psi_s \tag{6.6}$$

Where V_{ox} potential drop across the oxide

When applied gate voltage V_G changes from negative values to zero and to positive values, the sign and magnitude of charge on the silicon surface will change. This change in surface potential will introduce a capacitance in series with the oxide capacitance.

6.3 Capacitance-Voltage (C-V) analysis of MOS capacitors

C-V analysis is considered as one of the most important tool for characterizing MOS systems [1]. In this the differential capacitance is the most essential property, because small-signal measurements determine the changing rate of the charge with voltage. To understand capacitance-voltage measurements properly one must first be familiar with its frequency dependence. The frequency dependence occurs primarily in inversion region, since a certain time is needed to generate the minority carriers in the inversion layer. High and low frequency C-V measurements are often useful among various methods to evaluate the MOS characteristics. Most of the capacitance measurements are performed with admittance bridges or capacitance meters.

By applying Gauss' law, the small-signal equivalent circuit of the MOS capacitor was derived as follows [1,2]:

$$\frac{1}{C} = \frac{1}{C_S(\Psi_S)} + \frac{1}{C_{ox}} \tag{6.7}$$

Equation 6.7 gives the total capacitance of the MOS device as the sum of the silicon capacitance and the oxide capacitance, per unit area in series. The majority and minority carrier response times to ac gate voltages are different. The minority carrier response time is typically as long as 0.01-1s, which is much slower than the frequency of bias at high frequency and hence certainly not instantaneous over the frequency range of interest.

Figure 6.6 clearly shows the ideal C-V characteristics of a MOS capacitor with accumulation, depletion and inversion region. Normalized capacitance value is maximum at accumulation region and equal to the oxide capacitance. For the depletion region, as the silicon capacitance increases by the formation of the depletion layer, the total capacitance decreases as they are in series with each other. Finally for the inversion region total capacitance is the series combination of oxide capacitance and inversion layer capacitance. Depending upon the frequency of the ac voltage applied it is possible to observe two different behaviors. First, if the frequency is low enough, minority carrier generation takes place efficiently and electrons form an inversion layer at the oxide-silicon interface [1]. Therefore, the total capacitance increases and reaches back to its maximum value for positive gate voltages. Second, if the applied frequency is high enough (1MHz) then the minority carriers cannot be generated fast enough and hence cannot form an inversion layer at the oxide-silicon interface. In this case, the capacitance reaches its minimum value and stays constant even if the applied gate voltage is increased to higher positive values.

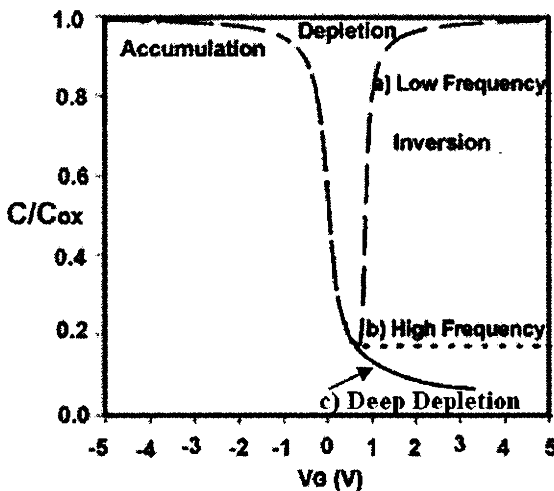

Figure 6.6: Ideal C-V curve for a MOS capacitor (a) low frequency (b) high frequency (c) deep depletion

Usually C-V curve is measured by automatically sweeping gate bias. If sweep rate is too rapid for minority carriers to follow, the system no longer will be in thermal equilibrium with respect to gate bias and resulting C-V curve will differ from thermal equilibrium curve. At room temperature, the minority carrier generation rate will be much smaller than the recombination rate. The sweep rates normally used are too rapid for generation to follow but are slow for recombination to follow. At room temperature the system usually is not in equilibrium when gate bias is swept in the direction of increasing inversion, but it is in equilibrium when gate bias is swept in the direction of decreasing inversion.

If response is too slow for minority carriers to follow the gate bias sweep into inversion, no inversion layer forms. Therefore the charge neutrality must be satisfied by increasing the width of depletion layer wider than the thermal equilibrium and under this condition the capacitance decreases below its thermal equilibrium saturation value. This non equilibrium condition is known as deep depletion [1].

6.4 Non-ideal Effects

In actual MOS capacitors, there are several non-ideal effects that may result in deviation from ideal behavior. The work function difference between the metal and semiconductor due to variation in the doping level of semiconductor material is one such cause of non-ideal effect. To compensate this work function difference an external voltage should be applied to the MOS structure. For this bias condition, the energy bands of Si are flat up to the interface and do not vary with distance. This applied voltage to achieve flat band condition is called the flat band voltage and is represented by V_{FB} for the MOS capacitor. If the oxide material does not contain any oxide or interface trap charge. The V_{FB} can be written as.

$$V_{FB} = \phi_{ms} = \phi_m - \left(\chi + \frac{E_g}{e} - \phi_p\right) \tag{6.8}$$

where Φ_m-metal gate work function, Φ_s-semiconductor work function, χ-semiconductor electron affinity, E_g-semiconductor energy gap,

and Φ_p-position of semiconductor Fermi level above the valance band in the neutral semiconductor bulk . The difference in work functions represents the amount of band bending. The sign of the difference of the metal and semiconductor work functions gives the polarity of applied voltage to be connected to the metal to obtain the flat band condition.

Other non-ideal effects are mainly due to charges present in the oxide and at the semiconductor-oxide interface. It has been established that there are mainly four general types of charges associated with the oxide/Si system as summarized in Figure 6.7. The total charge per unit area is represented by Q (C/cm^2) and the number of charges per unit area (the number density) is represented by the symbol N (number/cm^2).

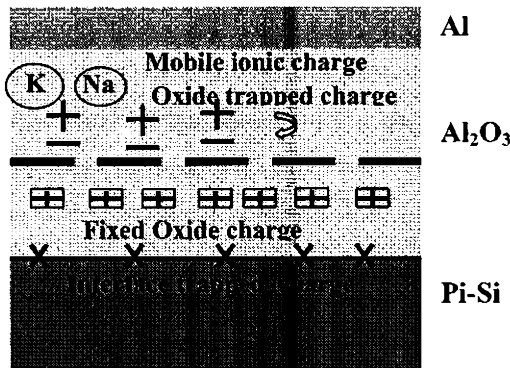

Figure 6.7: Various charges present in MOS structures.

The first type of charge is named as the fixed oxide charge Q_f which is primarily due to the structural defects (such as ionized silicon) in the oxide layer. The density of this type of charge is closely related to the oxidation process. Figure 6.8 shows a comparison of the energy band diagrams for ideal n and p type MOS structure. For these ideal structures, at zero applied voltage on the metal gate, it is a state of flat band. However, because of the difference between the gate metal work function (Φ_m), and the semiconductor work function (Φ_s) many dielectrics exhibit a charge at the silicon surface resulting in a required applied voltage $V_{FB}\neq0$ to achieve a flat band condition.

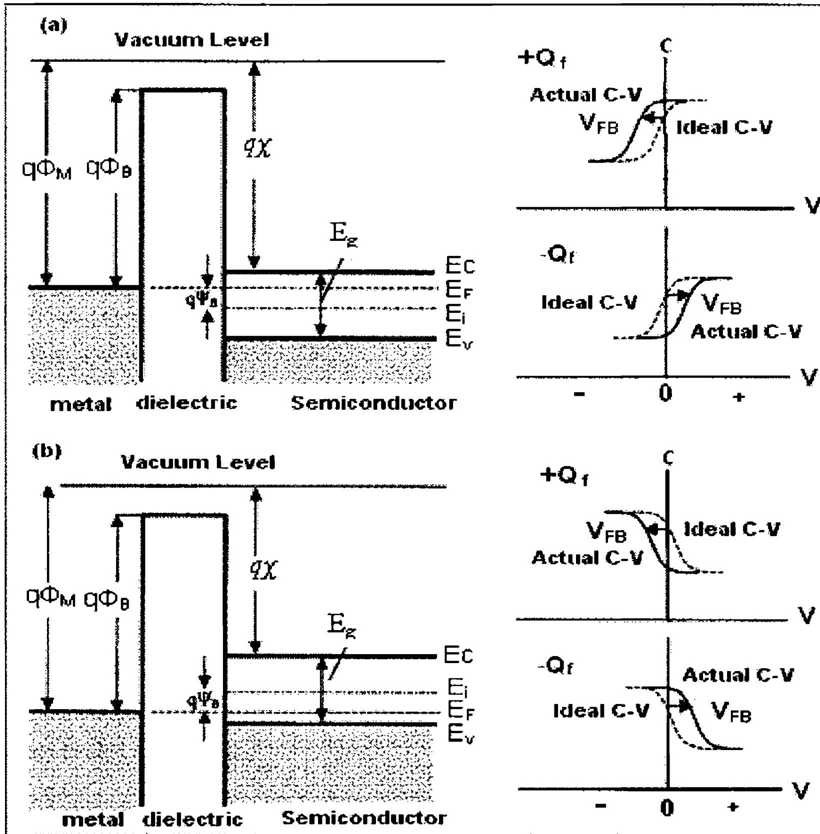

Figure 6.8: Energy-band diagrams and associated high frequency C-V curves for ideal MIS diodes for (a) n-type and (b) p-type semiconductor substrates. For these ideal diodes, $V_G = 0$ corresponds to a flat band condition. For dielectrics with positive (Q_f) or negative ($-Q_f$) fixed charge, an applied voltage (V_{FB}) is required to obtain a flat band condition and the corresponding C-V curve shifts in proportion to the charge in dielectrics .

The simplest and most widely used method for measuring oxide charge density N_{eff} is to infer this density from the voltage shift of C-V curves, caused by the existence of oxide charges, as shown in the right part of Figure 6.8. In both cases (p substrate and n substrate) positive Q_f causes the C-V curve to shift to more negative values of gate bias with respect to the ideal C-V curve. If the oxide charge is negative then the entire C-V curve

is shifted to more positive value with respect to the ideal C-V curve, and negative oxide charge cause the C-V curve to shift to more positive value with respect to the ideal C-V curve. The bias shift of the C-V curve caused by oxide charge Q can be explained by image charges.

Using a n-type substrate as an example, for a certain gate bias without any charge, at depletion region, the ideal depletion layer width is such that negative charge on the gate is balanced by the positive dopant ions in the depletion layer. If positive charge is joined in the oxide as shown in the upper-right side of Figure. 6.7, the above charge balance is interrupted, its image charge (actually electrons for this case) is introduced in the silicon substrate. These additional electrons located at the depletion layer, partly neutralize and reduce the depletion layer width. Because the capacitance of Si (C_s) is inverse to the width of the depletion layer and in series connection to C_{ox}, the actual capacitance with oxide charge Q becomes larger than for the ideal capacitance without Q (Figure 6.8 right top Figure). At strong accumulation, this influence of image charge is omitted because of the accumulation of carriers at the surface of Si from the substrate and absence of depletion region. At strong inversion, for low frequency measurements capacitance value reaches the same saturation value as in the case of accumulation and hence the effect of image charge is absent.

The second type of charges is the oxide trapped charge, Q_{ot}. These are due to holes or electrons trapped in the bulk of the oxide layer and can arise from the ionizing radiation or avalanche injection. Thus, Q_{ot} can have a positive or a negative value. Third type of charge is called mobile ionic charge, Q_m, which is mainly due to ionic impurities such as Li^+, Na^+, and K^+ etc.

The sum of these three different charges in the oxide layer is represented by the effective oxide charge Q_{eff} (and its number density N_{eff}) as given in Equation 6.9.

$$Q_{eff} = Q_f + Q_m + Q_{ot} \tag{6.9}$$

Finally, the fourth and the most important source of non-ideal effects is due to interface trapped charge Q_{it}. Its density per unit area per unit energy is denoted by D_{it}. They are usually located at the oxide-semiconductor interface. It has a positive or a negative value depending on the location with respect to the Fermi level. They originate from structural disorder, oxidation-induced defects, metal impurities and defects caused by radiation or similar bond-breaking processes. Various techniques like Terman's method and simultaneous C-V methods are used to calculate the level of interface trap density. D_{it} plays a major role in the operation of MOS devices causing an increased recombination of the free carriers in the conduction and valance bands. The levels of the Q_{eff} and D_{it} are the important parameters to be controlled during the manufacturing process of the MOS devices.

6.5 Conduction mechanism of insulator

The performance of MOS devices strongly depends on the breakdown properties and the current transport behavior of the gate dielectric films. Therefore the conduction mechanism of the gate dielectric film has attracted many scientists in the field of physics and material science. The conduction mechanisms of the gate dielectric films are found to be very sensitive to the film composition, film processing, film thickness, trap energy level and trap density in the films. However, the conduction behavior of a gate dielectric is generally dominated by one or two mechanisms.

The current conduction mechanisms through the insulating materials, which do not contain free carriers, can be distinctly different from those in doped semiconductors or metals. T. Hori and E. H Nicollian et al. described the conduction mechanism in details in their books [1,9] especially focusing on the conduction mechanism valid in SiO_2. Most introductions on conduction in insulators in this chapter is based on SiO_2, since thermal SiO_2 film could be considered basically an ideal insulator under moderate bias conditions. Although the oxide resistivity is very high, of the order of 10^{15} ohm-cm, it is not infinite. Most amorphous insulators at an electric field (E) in excess of 10^4V/cm show a range of nonlinear current-voltage dependence, and can be interpreted based on certain conduction mechanisms. In the

following part we discuss Fowler-Nordheim (FN) tunneling, Poole-Frenkel (PF) emission, as well as direct tunneling transport, Schottky emission and ohmic behaviour. FN and direct tunneling are substantially independent of the temperature unlike other mechanisms, because of the dependence of tunneling phenomena only on the quantum state of the insulator.

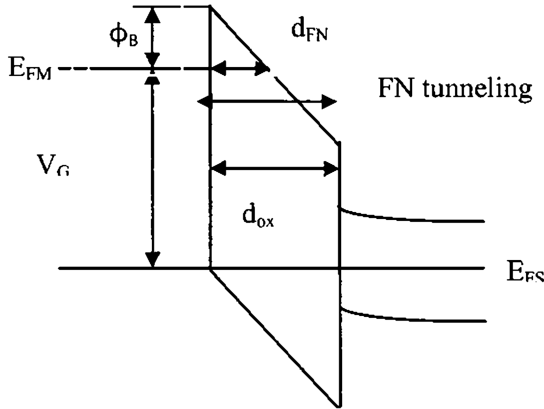

Figure 6.9: Schematic of Fowler-Nordheim tunneling

Where Φ_B-barrier height, E_{FM}-metal Fermi level, E_{FS}- semiconductor Fermi level, d_{OX}-oxide thickness, d_{FN}-tunneling distance, V_G-gate voltage

FN tunneling has been studied extensively in MOS structures where it has been shown to be the dominant current mechanism, especially for thick oxides (>40Å), such as in Figure 6.9. The basic idea is that quantum tunneling of carriers occurs through a triangular potential barrier in the presence of a high electric field. The barrier of the insulator is pulled down by the E- field so far that electron tunneling from the metal Fermi level into the oxide conduction band becomes possible. Once the carriers have tunneled into the insulator they are free to move within the valence or conduction band of the insulator. To check for this current mechanism, experimental I-V characteristics are typically plotted as $\ln(J_{FN}/E^2_{ox})$ vs. $1/E_{ox}$, which is called Fowler-Nordheim plot. Provided the effective mass of the insulator is known (for Al_2O_3, $m_{ox}^*=0.42m_0$), one can fit the experimental

data to a straight line yielding a value for the barrier height under the valid E field.

FN tunneling implies that carriers are injected into the conduction band of the insulator and are free to move through the insulator. However, in deposited insulators, which contain a high density of structural defects, this is not the case. These structural defects cause additional energy states close to the band edges and restrict the current flow by capture and emission processes, thereby becoming the dominant PF emission mechanism. The existence of a large density of shallow traps in deposited films makes PF emission a well characterized mechanism. Field-enhanced thermal excitations of trapped electrons into the conduction band are frequently observed in such films. Other possible processes including ohmic conduction as well as trap assisted tunneling, can be found in the literature [9]. In the simple case for d_{Ox}< 2 nm, direct tunneling dominates when the electrons pass through the full oxide thickness then the gate current is due to direct tunneling. Fowler-Nordheim tunneling and Pool-Frenkel emission with the corresponding J-E functions are described as follows:

$$J = \frac{A}{4\Phi_B} E^2 exp \frac{-2}{E} \Phi_B^{3/2} \tag{6.10}$$

$$J \, \alpha \, E \, exp\left(-\frac{\Phi_B^{-2} \sqrt{E/c}}{\Phi_t}\right) \tag{6.11}$$

where J, E, and Φ_t are current density, electric field, and thermal energy of about 26 meV at room temperature. Φ_B is the potential barrier height, A, and C are constants. For a substrate in strong accumulation, where $E_F > \frac{4\Phi_B^2}{3qBt_{ox}}$, the direct tunneling leads to a similar formula as Fowler-Nordheim tunneling and can be simplified to following with additional constant terms B_1 and B_2.

$$J_{dir} = \frac{q^2 m_{eff} E^2}{8\pi\Phi_B m B_1} exp\left[\frac{-4\sqrt{2m(q\Phi_B)^3 B_2}}{hqE}\right] \tag{6.12}$$

6.6 Fabrication of MOS capacitor

MOS capacitors were fabricated on p-Silicon (100) substrate with ALD-Al_2O_3 as gate dielectric and Aluminum as metal electrode. Since any chemical contamination may ruin the entire device performance and reliability, wafer cleaning is an important and critical step in device fabrication. Prior to depositions substrates were cleaned by standard cleaning procedure which consists of the following steps.

- Standard cleaning 1 (SC-1 is performed with a 1:1:5 solution of NH_4OH (ammonium hydroxide) + H_2O_2 (hydrogen peroxide) + DI water (H_2O) at a temperature of 75 °C for 10 minutes. SC-1 removes any organic contaminates by oxidation. This is followed by transferring the wafers into a DI water bath.
- Dilute HF dip: HF- DI water in composition of 1:10 is prepared and the wafers are dipped in it for 60 seconds after SC-1 process to remove the native oxide present on the wafer substrate.
- Standard clean 2 (SC-2) is performed with a 1:1:6 solutions of HCl + H_2O_2 + H_2O at a temperature of 75°C for 10 minutes. This treatment effectively removes the remaining metallic (ionic) contaminants on the wafer. The cleaning process is followed by dilute HF dip to passivate the Si danging bond with hydrogen.

The native oxide formed on the back surface was etched by buffered HF (HF-DI water in a composition of 1:10). After the oxides etch the samples were cleaned with acetone and Isopropyl Alcohol (IPA).

Aluminum Back contact of MOS capacitor were deposited on back etched wafer by thermal evaporation with a thickness of 100nm.Top aluminum metal electrodes were also patterned by thermal evaporation through shadow mask. Thicknesses and area of the electrodes were measured using a surface profiler (Dektek) and optical microscope. About 50 devices were fabricated on a 1cm×1cm silicon substrate with circular gate of 400μm diameter

At Si/Al_2O_3 interface the periodicity of Si crystal terminates. The dangling bonds of Si lead to interface states; these bonds have to be

passivated. Passivation is done by forming gas annealing (a mixture of $N_2:H_2$ :: 10:1) .The H atoms being light diffuse through dielectric and passivate the dangling bonds, thereby reducing the interface trap states. The fabricated structures were annealed for two hours at 400°C with maximum ramp rate in forming gas at a flow rate of 5 lit/min. Figure 6.10 shows the flow chart of the fabrication process.

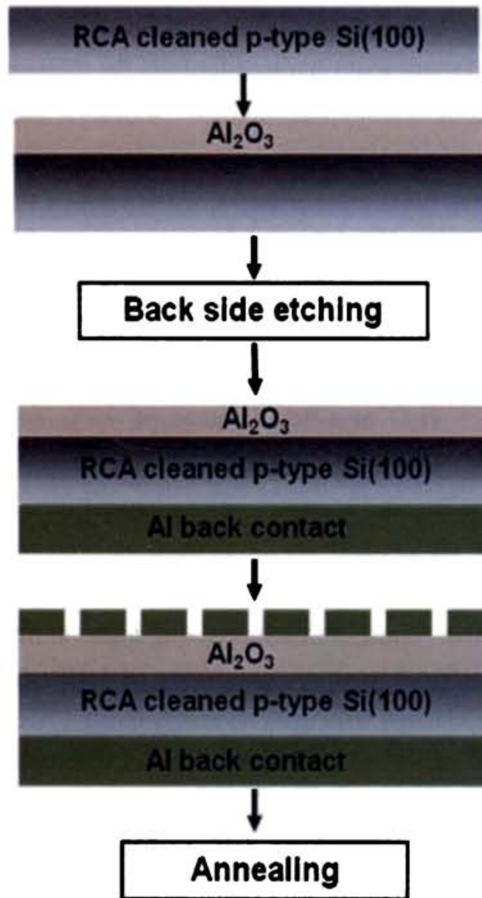

Figure 6.10: Steps involved in the fabrication of MOS capacitors

6.7 Results of electrical and dielectric studies of Al/Al_2O_3/p-Si MOS capacitors

6.7.1 Effect of frequency on Capacitance – Voltage and Conductance – Voltage characteristics

The capacitance-voltage (C-V) and conductance-voltage (G-V) measurements were carried out in the frequency range of 100Hz- 1MHz and temperature range of 300K - 430K respectively. The conductance technique is based on the conductance losses resulting from the flow of majority carriers at the interface to the majority carrier band of the semiconductor when a small ac signal is applied to the metal-oxide- semiconductor (MOS) structures. When the MOS structure is in the depletion the applied ac signal causes the Fermi level to oscillate about the mean position governed by the dc bias [1,3].

In this present study we made use of both Agilent 4284 Precision LCR Meter and Fluke PM 6306 programmable RCL meter with varying test signal of 50 mV_{rms} and hold time of 100 ms. To compensate the cable impedance, open correction were carried out prior to each measurements and the signal is given at the back contact to mitigate the effect of parasitic impedances. The deep depletion depends upon the sweep rate of the test signal, therefore sufficient hold time was selected. In order to avoid deep depletion usually the DC voltage is swept from inversion to accumulation. All measurements were carried out with the help of a computer through an IEEE 488 interface.

Figure 6.11(a) shows the normalized low frequency C-V characteristics of Al/Al_2O_3/Si-p MOS capacitors at a frequency of 1 kHz. Thickness of the sample was measured using an ellipsometer. Maximum capacitance has been observed in the accumulation region and has a value of 1.11nF, which yields a dielectric constant of 9.478. Oxide thickness is extracted from the accumulation capacitance also and has a value of 9.45nm. It was observed that as the thickness of the oxide layer becomes thinner the more rapidly the capacitance changes with gate bias.

At low frequencies ideally the MOS capacitor is in thermal equilibrium under small-signal ac excitation, provided that minority carriers

can respond to variation in the ac field. In practice there will be some hole and electron traps at the Si/Al_2O_3 interface and in the bulk silicon. The system including these traps still will be in thermal equilibrium if all these traps immediately respond to the ac voltage. That is MOS capacitor will be in thermal equilibrium at all values of gate bias below the oxide breakdown field at low frequencies.

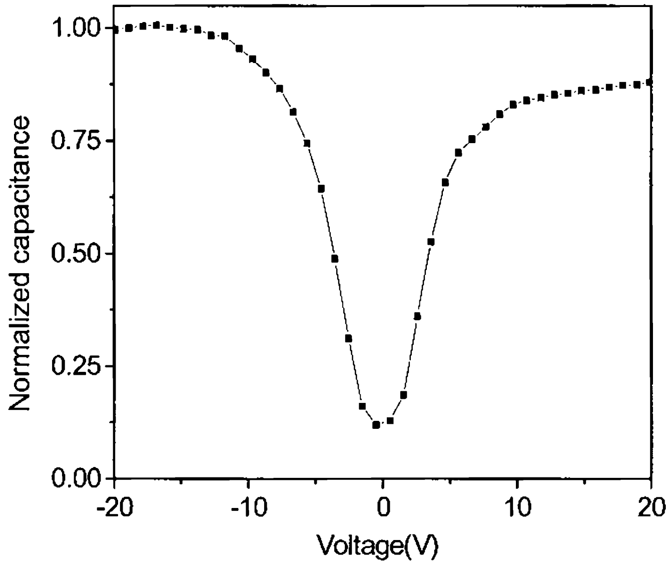

Figure 6.11(a): Normalized low frequency C-V characteristics of an Al/Al_2O_3/p-Si MOS capacitor.

The different regions of MOS capacitor at low frequency are identified as accumulation -20V to -3.29V, depletion between -3.29 to -0.587V and inversion region at voltages above -0.587V. Due to the presence of interface trap charges and other charges the flat band voltage V_{FB} is deviated from the ideal value (-0.83V).

The experimentally obtained normalized high frequency (1MHz) C-V curve of Al/Al_2O_3/p-Si (MOS) is shown in Figure 6.11(b). Accumulation capacitance density obtained is 1.06×10^{-6} F/cm^2 at an electrode area of 1.256×10^{-3} cm^2. Depending upon processing condition and Al_2O_3 thickness dielectric constant of the samples varied from 6.2 to 10.7. The slop of the C-

V curve is less than that predicted by exact charge theory indicating less interface traps density [1] .

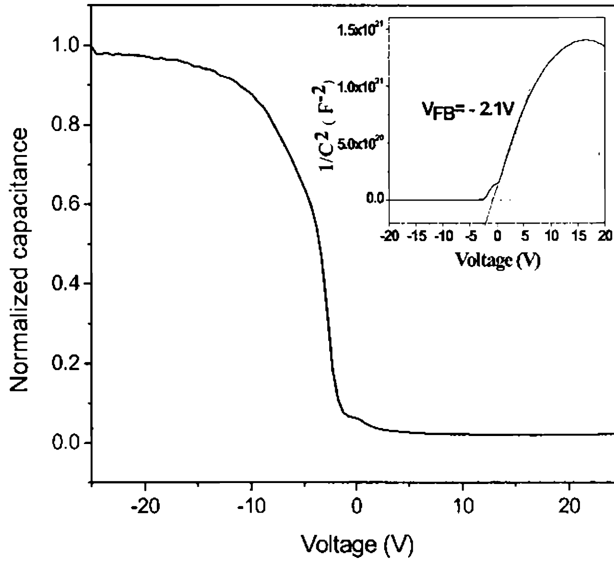

Figure 6.11(b): Normalized high frequency (1 MHz) C-V Characteristics of an Al/Al_2O_3/p-Si (p-type) MOS capacitor. Inset shows the experimentally observed flatband voltage

In practice experimental C-V characteristics are always different from ideal characteristics due the presence of non-ideal effects like interface trap and bulk charges. For the determination of non-ideal effects, it is necessary to calculate theoretical capacitance-voltage behavior of MOS capacitor. For this reason, doping concentration, (N_A) and flat band voltage values of Al/Al_2O_3/p-Si MOS capacitor are extracted by using the experimental high frequency $1/C^2$ versus V_G graph as shown in Figure 6.11(b). The measurements were performed over different devices fabricated on the same wafer for the reliable and reproducible data collection. Therefore, the results here represent an average of different measurements. The doping concentration was experimentally measured by means of four point probe meter (model 280) and has a value of 5×10^{15} cm^{-1}. The flat band voltage value was extracted from $1/C^2$-V plot. Theoretical flat band voltage of the MOS device was calculated by using the equation 6.8 and obtained a

value of (-0.83V). The flat band voltage varies with the presence of oxide charges in the insulator material and is representing by Equation 6.13.

$$V_{FB} = \Phi_{MS} - \frac{Q_{eff}}{C_{ox}} \tag{6.13}$$

$$N_{eff} = {Q_{eff}}/{q} \tag{6.14}$$

Where Q_{eff}- total oxide charge, N_{eff} -Number density of total oxide charge, q-electronic charge.

Inset of Figure 6.11(b) shows the experimentally extracted V_{FB} which has a value of -2.1V. The flat band voltage shift to a more negative value with ideal value indicates the presence of positive fixed oxide charges. The net oxide charge presented in the sample and its number density is calculated as $N_{eff} = 1.23 \times 10^{10}$, which is in the limit of good quality oxide layer reported for native SiO_2 layers.

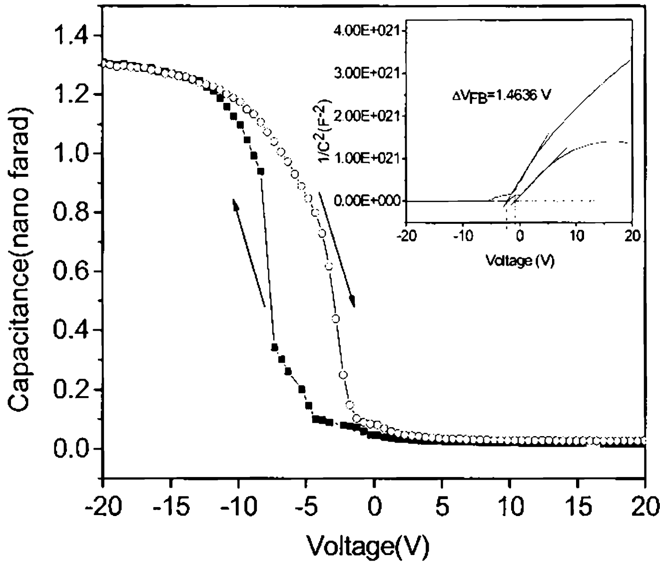

Figure 6.12: C-V hysteresis curve. Inset shows the shift in flat band voltage.

Figure 6.12 shows CV hysteresis curve and a shift in V_{FB} is observed. By measuring the shift we calculated the trapped oxide charges present in the sample (Q_{ot}) using the equation 6.15 [21] and obtained a value of 1.93×10^{-9} C.

$$Q_{ot} = -\Delta V_{FB} \times C_{ox} \tag{6.15}$$

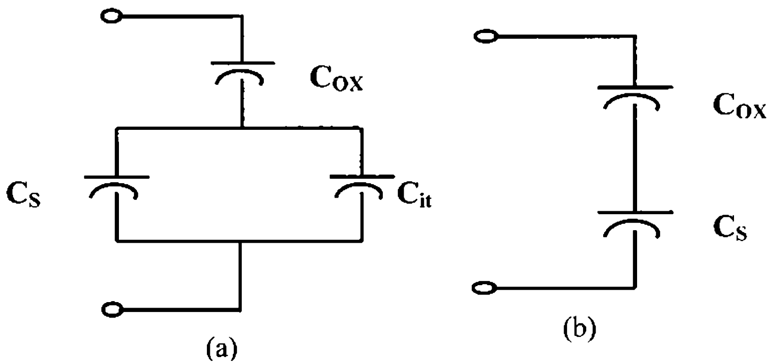

Figure 6.13:(a) Low frequency equivalent circuit of the MOS capacitor, (b) High frequency equivalent circuit of the MOS capacitor [1].

Figure 6.13(a) & (b) show the low and high frequency equivalent circuit of the MOS capacitor [1]. Where C_{OX}-oxide capacitance, C_S-silicon surface capacitance and C_{it}-interface trap capacitance. At lower frequencies, the interface traps respond to ac voltage change and yield an excess frequency dependent capacitance (C_{it}). In high frequency region since the interface traps cannot follow the ac signal, the contribution of interface trap capacitance to the total capacitance is negligibly small [1,11,12].

Figure 6.14 depicts the C-V and G/ω-V characteristics for $Al/Al_2O_3/p\text{-}Si$ structure at different frequencies. The overall behavior is indeed that of an MOS device, with distinct regions of accumulation, depletion and inversion. As can be seen in the figure the values of capacitance and conductance are dependent on the bias voltage and frequency. The measured values of C and G/ω at accumulation and depletion

region decrease with increasing frequency. This is an indication of the presence of interface states (N_{ss}) localized at semiconductor/oxide interface. The capacitance of such an inhomogeneous charge layer at the semiconductor/oxide interface will contribute an additional capacitance C_{it} with the oxide capacitance causing frequency dispersion [1].

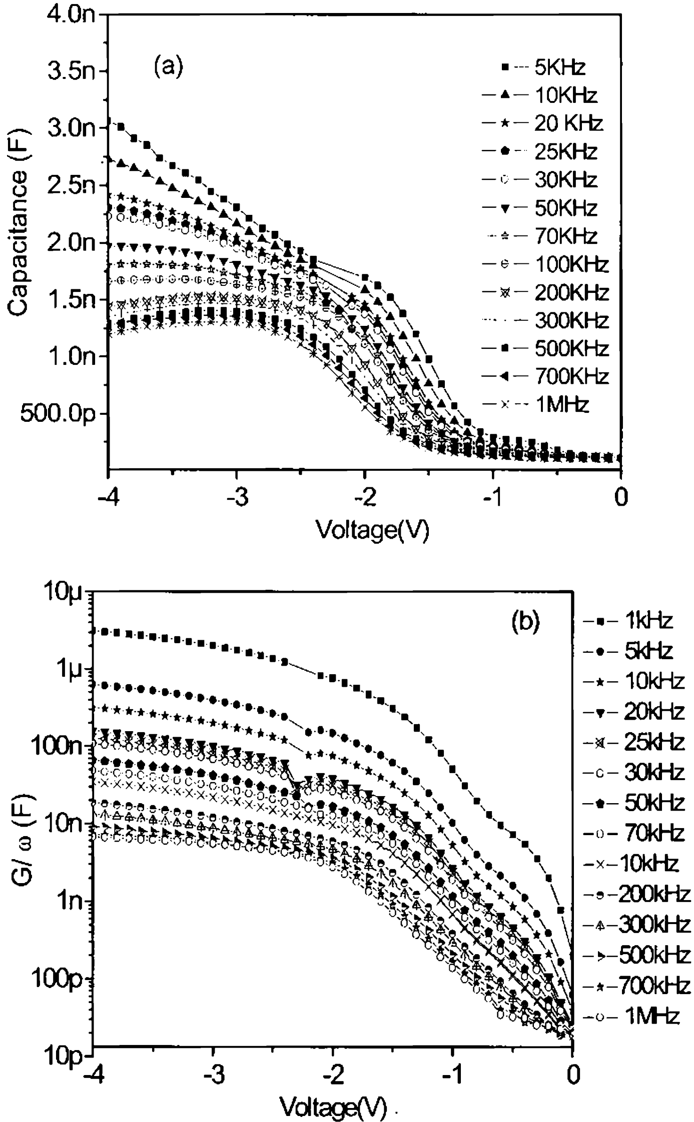

Figure 6.14: The frequency dependence of (a) C-V, (b) (G/ω)-V characteristics of Al/Al_2O_3/ p-Si MOS structure at room temperature.

6.7.2 Effect of frequency on series resistance

At a given frequency, most of the errors in the *C–V* and *G/ω–V* characteristics due to series resistance (R_s) occur in the strong accumulation region and a portion of the depletion region. The error can be minimized by measuring the R_s and applying a correction to the measured *C* and *G/ω* values before the desired information is extracted [1]. When the MOS structure is biased into strong accumulation, the frequency-dependent properties of MOS devices can be described via the complex impedance and the series resistance is the real part of the complex impedance as [1, 12].

$$R_S = \frac{G_m}{G_m^2 + (\omega^2 C_m^2)} \tag{6.16}$$

where C_m and G_m are the measured capacitance and conductance, The capacitance of the oxide layer (C_{ox}) is obtained as

$$C_{ox} = C_m[1 + ({}^{G_m}/_{\omega} C_m)^2] \tag{6.17}$$

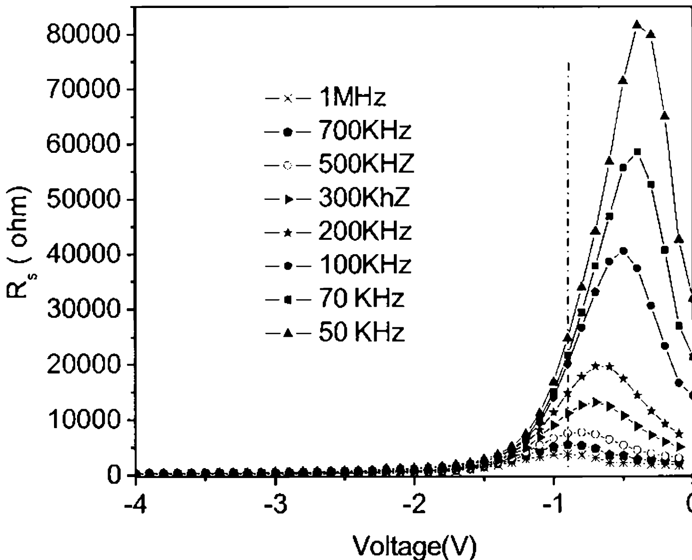

Figure 6.15: Variation of R_s of Al/Al_2O_3/p –Si structure as a function of the bias voltage at varies frequencies.

Figure 6.15 shows the variation of R_s as a function of bias voltage in the frequency range of 50 kHz to 1MHz. From the figure it is observed that Rs shows a peak value and position of Rs peak shift towards negative bias voltage from -0.4V to-0.9V when frequency increases from 50 kHz to 1MHz. It can also be observed that as frequency increases peak value decreases and almost disappear at high frequencies (>500 kHz). Such behavior of R_s is attributed to the particular distribution of localized interface states (N_{ss}) at Si/Al_2O_3 interface and the Al_2O_3 layer at the Al/p-Si interface. This type of behavior is reported in the case of Al/TiO_2/p-Si structures also [12,14].

6.7.3 Frequency dependence of dielectric properties

Dielectric constant (ε), dielectric loss (ε ''), loss tangent (tanδ) and ac electrical conductivity (σ_{ac}) were calculated from the values of capacitance and conductance measurements for Al/Al_2O_3/p-Si (MOS) structure in the frequency range of 1kHz–1MHz, at room temperature. The complex permittivity can be written [17,18] as

$$\varepsilon^* = \varepsilon' - i\varepsilon'' \tag{6.18}$$

where ε' and ε'' are the real and the imaginary parts of complex permittivity, and i is the imaginary root of -1. The complex permittivity formalism has been employed to describe the electrical and dielectric properties. In this the following relation:

$$\varepsilon^* = \frac{Y^*}{j\omega C_0} = \frac{C}{C_0} - i\frac{G}{\omega C_0} \tag{6.19}$$

where, C and G are the measured capacitance and conductance of the dielectric material , Y*-admittance and ω-angular frequency (ω =2πf) of the applied electric field [18]. The real part of the complex permittivity, the dielectric constant (ε'), at the various frequencies is calculated using the measured capacitance values at the strong accumulation region from the relation [15,16]:

$$\varepsilon' = \frac{C}{C_0} = \frac{Cd_{ox}}{\varepsilon_0 A} \quad (6.20)$$

where C_o-capacitance of the empty capacitor, A -electrode contact area, d_{ox} - oxide layer thickness and ε_0- permittivity of free space (ε_0=8.85×10^{-14} F/cm). In strong accumulation region, the maximum capacitance of the MOS structure corresponds to oxide capacitance (C_{ox}). The imaginary part of the complex permittivity-the dielectric loss (ε") at various frequencies is calculated using the measured conductance values from the relation,

$$\varepsilon'' = \frac{G}{\omega C_0} = \frac{Gd_{ox}}{\varepsilon_0 \omega A} \quad (6.21)$$

The loss tangent (tan δ) can be expressed as follows [12,17,16].

$$tan\delta = \frac{\varepsilon''}{\varepsilon'} \quad (6.22)$$

The ac electrical conductivity (σ_{ac}) of the dielectric material is be given by the following equation [12,17,18,19].

$$\sigma_{ac} = \omega C \left(\frac{d_{ox}}{A}\right) tan\delta = \varepsilon'' \omega \varepsilon_0 \quad (6.23)$$

The frequency dependencies of the ε', ε" and tan δ of $Al/Al_2O_3/p\text{-}Si$ structure vs. applied gate voltages are presented in Figure 6.16 a, b and c respectively. The values of ε', ε " and tan δ calculated from the measured capacitance and conductance were found to be strong functions of applied voltage especially at low frequencies. Also, it is evident from Figure 6.16 that the values of ε" and tan δ are almost independent of voltage at high frequencies. In principle, at low frequencies, all the four types of polarization processes, i.e., the electronic, ionic, dipolar, and interfacial or surface polarization contribute to the values of ε' and tanδ [3,22,23].

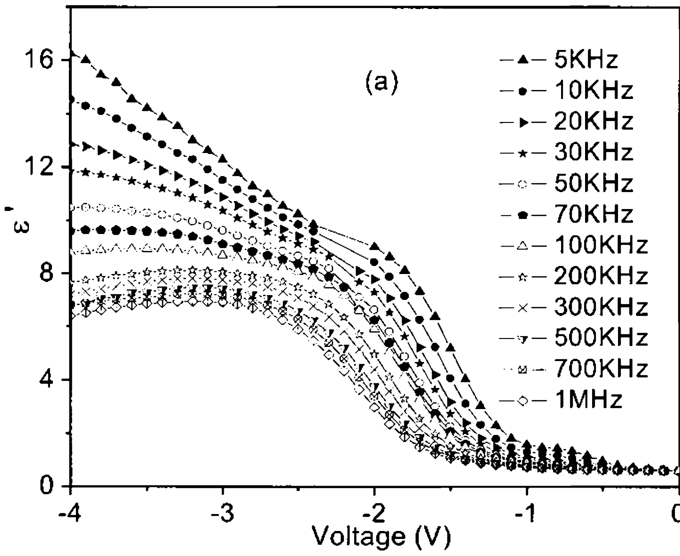

Figure 6.16(a): The frequency dependence on dielectric constant of $Al/Al_2O_3/p\text{-}Si$ structure at room temperature.

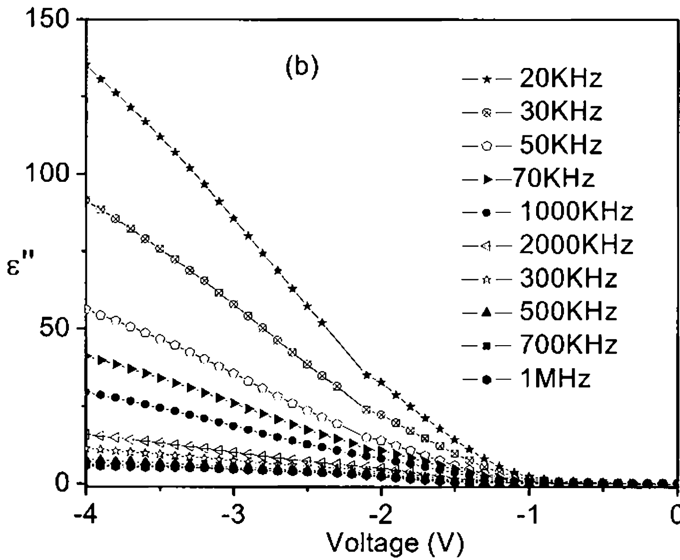

Figure 6.16 (b): The frequency dependence on dielectric loss of $Al/Al_2O_3/p\text{-}Si$ structure at room temperature.

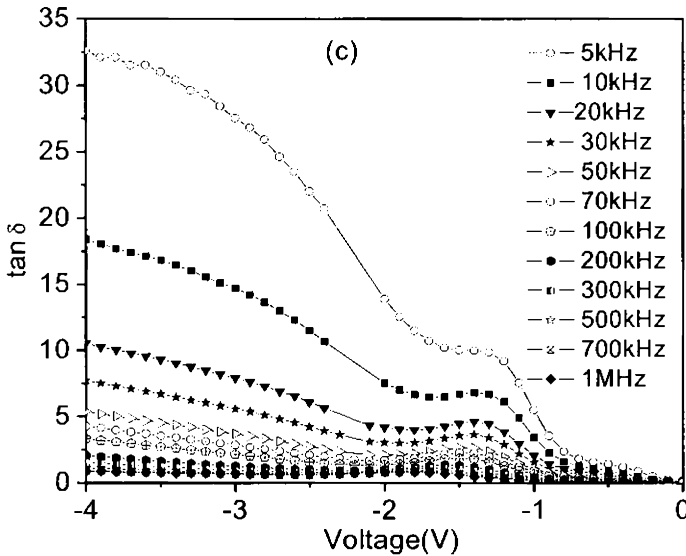

Figure 6.16 (C): The frequency dependence on tangent loss of $Al/Al_2O_3/p\text{-}Si$ structure at room temperature.

At accumulation region the values of ε' and ε" were found as 9.85 & 58.03, 8.19 & 13.08 and 5.85 & 3.81 at 10 kHz, 100 kHz and 1 MHz respectively. On increasing frequency, the contributions of the interfacial, dipolar or the ionic polarization become ineffective leaving behind only the electronic part. As it can be seen from these figures ε', ε" and tanδ decrease as the frequency is increased. It is explained by the fact that as the frequency is raised, the interfacial dipoles have less time to orient themselves in the direction of the alternating field [14,24,25]. In high frequency range, the values of ε' become closer to the values of ε". This behavior of ε' and ε" may be due to the inability of interface states to follow the ac signal at such frequencies. The lifetime of interface trapped charges (τ) are much larger than 1/ω at very high frequencies (ω). Similar behavior is observed in several dielectric materials [1, 12].

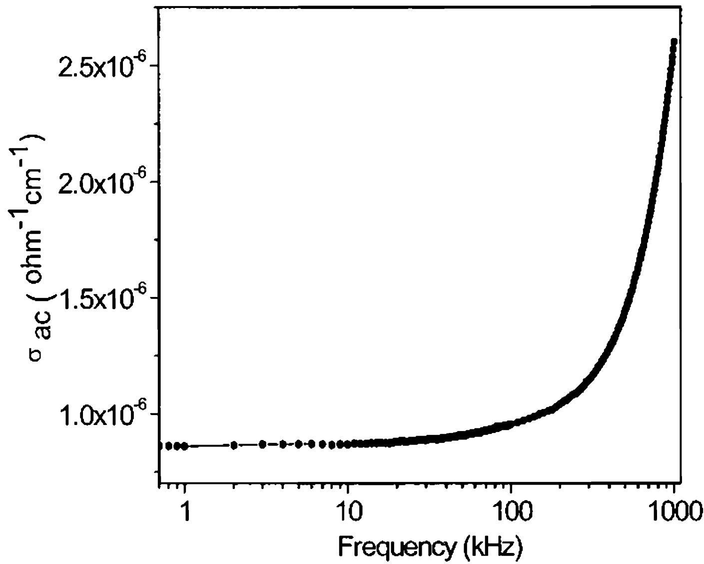

Figure 6.17: The frequency dependence of ac conductivity of $Al/Al_2O_3/p\text{-}Si$ structure at room temperature

Figure 6.17 shows the dependence of ac electrical conductivity (σ_{ac}) on frequency [20,26-32]. σ_{ac} is independent of frequency up to about 100kHZ and thereafter increases sharply. σ_{ac} depends on dielectric loss according to Equation 6.23. As observed in figure 6.16(b) dielectric loss decreases with increasing frequency and this explains the increase in σ_{ac} with frequency. This result is in agreement with the literature [20].

6.7.4 Temperature dependence of capacitance, conductance and dielectric properties

Figure 6.18(a) and (b) show the temperature dependant C –V and G/ω –V characteristic of $Al/Al_2O_3/p\text{-}Si$ MOS capacitor at 1MHz frequency. Comparing with the ideal characteristics the experimentally obtained one has some flatband shift along the voltage axis. As temperature increases shift in voltage axis decreases and move closer to ideal value. We can observe in the figure that the depletion regions of all curves are nearly parallel, without any stretch out. This is because at 1MHz frequency the interface charges which cause stretch out have already ceased to contributing to the total capacitance.

Hence as temperature varies from 300 to 430k the change in any of the charges (Q_f, Q_M or Q_{ot}) or combination of these only may cause shift in flat band voltage.

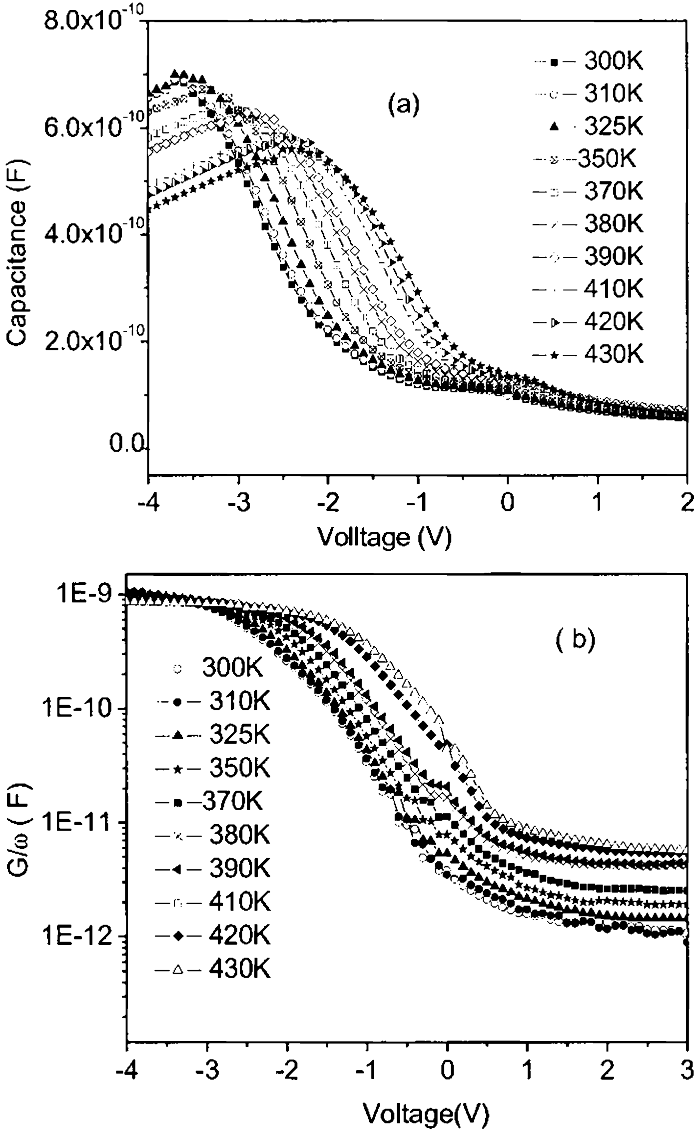

Figure 6.18: Temperature dependent (a) C-V, (b) G-V characteristics of $Al/Al_2O_3/Si$ capacitor at 1MHz.

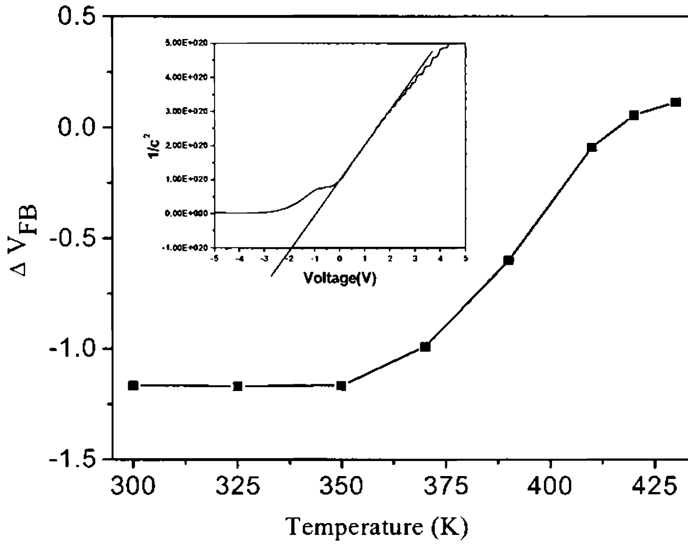

Figure 6.19: Flat band voltage shift vs. temperature of Al/Al_2O_3/p-Si structure, Inset of Figure shows the Flat band voltage of Al/Al_2O_3/p-Si MOS structure at 300K.

In Figure 6.19 we have found that ΔV_{FB} decreases as temperature rises. This means the C-V curve shifts towards right side along the voltage axis (Figure 6.18(a)). Hence at any particular measurement voltage in the depletion region, the measured capacitance will increase with increase in temperature. At low frequencies the variation will be more because of the effect of interface trapped charge on capacitance. It implies that charges in the interface traps get de trapped at higher temperature, which thus contribute to conductance G. The low frequency curve in Figure 6.22(b) supports this conclusion.

Flat band voltage for each temperature was experimentally calculated from C-V curve. The shift in Flat band (ΔV_{FB}) from ideal value for each temperature was plotted against temperature as shown in Figure 6.19. Inset of Figure 6.19 shows flat band voltage of the fabricated capacitor at 300K. As temperature increases flat band shift decreases. This may be due to the reduction of the total oxide charge density and the interface-trap density at higher temperature [1].

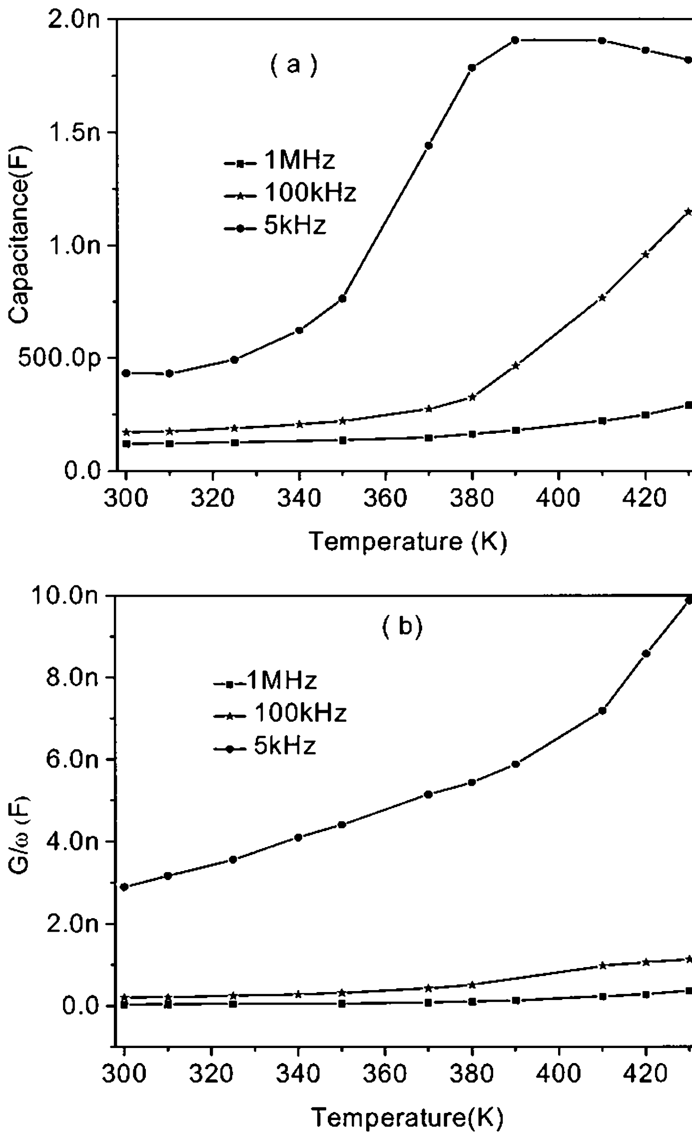

Figure 6.20: The temperature dependence of (a) capacitance, (b) conductance (G/ω) of Al/Al_2O_3/p-Si MOS structure at different frequencies (5kHz, 100kHz, 1 MHz).

Figure 6.20(a) and (b) shows the measured C–T and G/ω–T characteristics of the Al/Al_2O_3/P-Si MOS structure at various frequencies

(5kHz, 100kHz, 1MHz) in depletion region. It is clear that the C–T and Gm/ω–T curves are quite sensitive to frequency and temperatures especially at low frequency and high temperature. The values of C and G/ω increase with increasing temperature.

The results of the temperature dependences of ε', ε" and tan δ for the $Al/Al_2O_3/p\text{-}Si$ are plotted in the Figure 6.21(a),(b) and (c) in the temperature range of 300 to 430K and at various frequencies (5kHz, 100kHz and 1MHz). At low frequency (5 kHz), on increasing the temperature from 300 to 390K, the ε' value increases rapidly from 2.3 to as large as 10.17. The tanδ value decreases from 7.3 at 300K to 3 at 390K and then increases with increasing temperature. At high frequencies (100 kHz, 1 MHz) it has been observed that the variation of ε' and ε" is negligible up to 390K and then increases with temperature. Tanδ is almost independent of temperature at high frequencies.

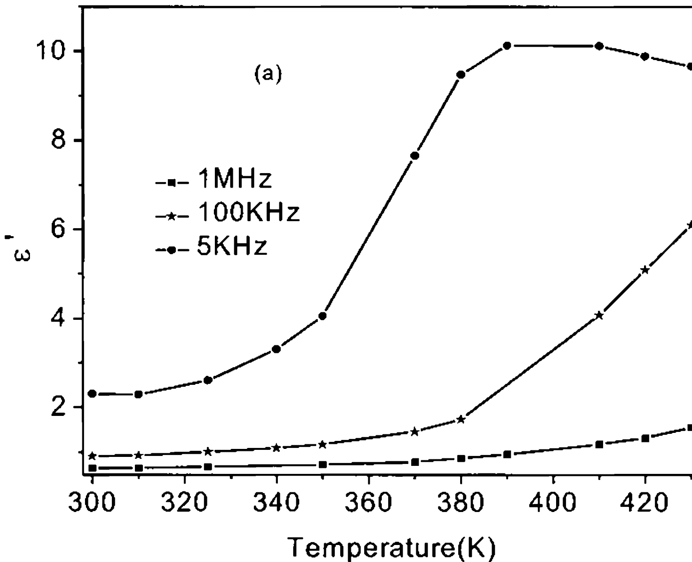

Figure 6.21: Temperature dependence of dielectric properties (a) dielectric constant (ε').

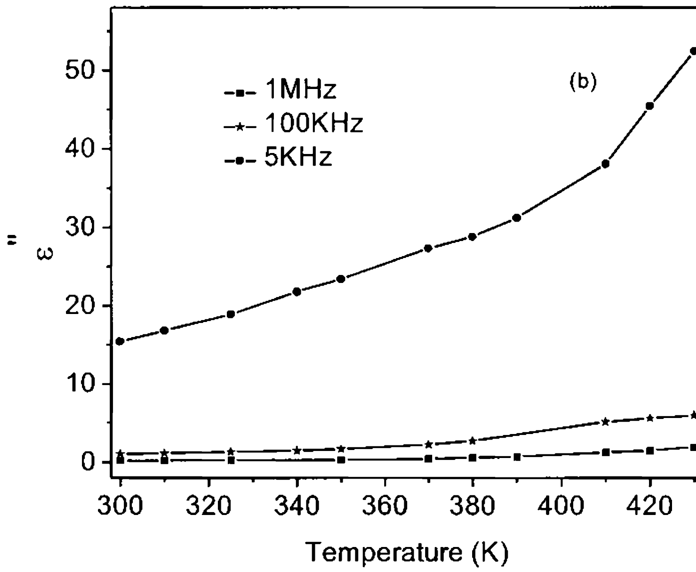

Figure 6.21: Temperature dependence of dielectric properties (b) dielectric loss (ε")

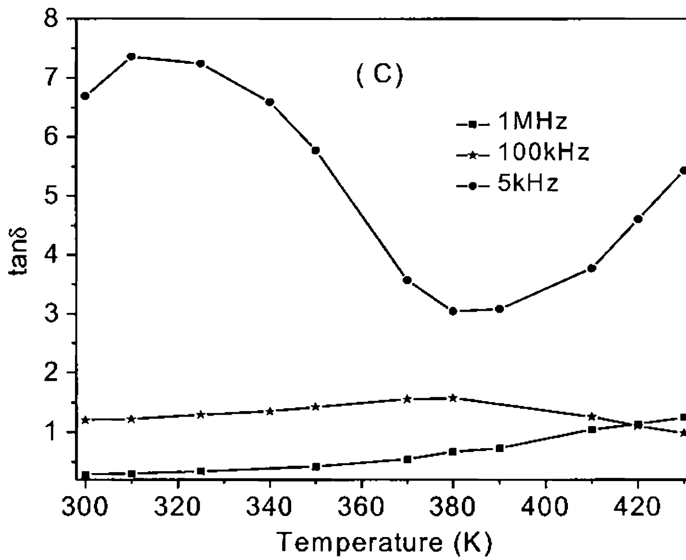

Figure 6.21: (c) Temperature dependence of dielectric loss tangent (tan δ).

The explanation of Figure 6.21(a) can be same as that of Figure 6.20(a). Here as capacitance C varies in certain way, naturally ε' will follow the curve of C. By increasing temperature, the number of charge carriers increase and thus produces further space charge polarization and hence leads to a rapid increase in the capacitance and hence dielectric constant. Ofcourse, both types of charge carriers n and p contribute to the polarization. However, the n-type contribution is negligible, where the dominant charge carriers are holes [18,20]. This increase in carrier concentrations is verified by conductance measurement and results are shown in Figure 6.22 b.

Furthermore, the increase in temperature induce an expansion of molecules which causes some increase in the electronic polarization [12,33–35]. The temperature causes a loosening of the rigid structure and hence results in an increase in dipole orientation and an increase in ε', ε" and tanδ. Since ε" proportional to G it follows the same nature of G. These results show that this MOS structure possess better dielectric properties at temperatures higher than room temperature.

6.7.5 Effect of temperature on series resistance

Frequency and temperature dependence of series resistance can be obtained from the measurements of C–T–f and G/ω–T–f data plotted in Figure 6.22 (a) and is clear that the series resistance has an inverse relation with frequency and temperature. The major parameters which affect series resistance are the presence of interface states and its particular distribution of N_{ss}. At high frequencies the interface trapped charges cannot follow the ac signal and consequently cannot contribute to the total capacitance and conductance. Similarly at high temperature the contribution of majority carriers and charges released from the interface states cause the decrease in R_s values. From figure 6.22(a) it is clear that at high frequency (1MHz) series resistance is almost independent of temperature. This implies trapping of charges at low temperature get reflected on low frequency R_s values.

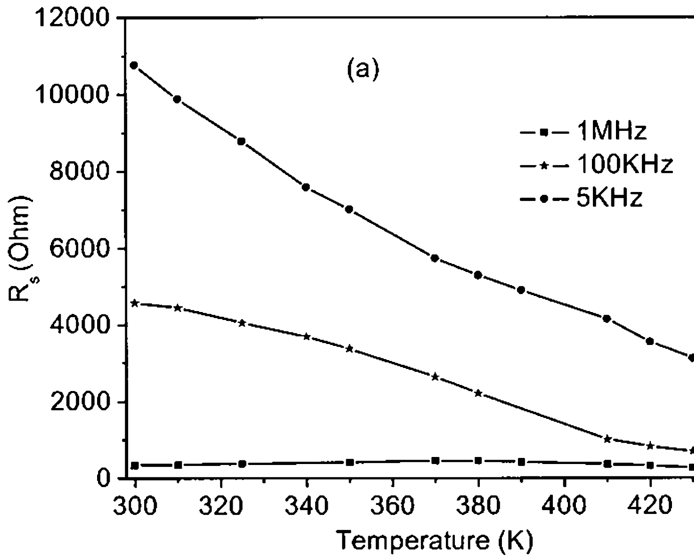

Figure 6.22(a): Variation of series resistance with temperature of Al/Al_2O_3/p-Si MOS structure at different frequencies (5kHz, 100kHz, 1MHz).

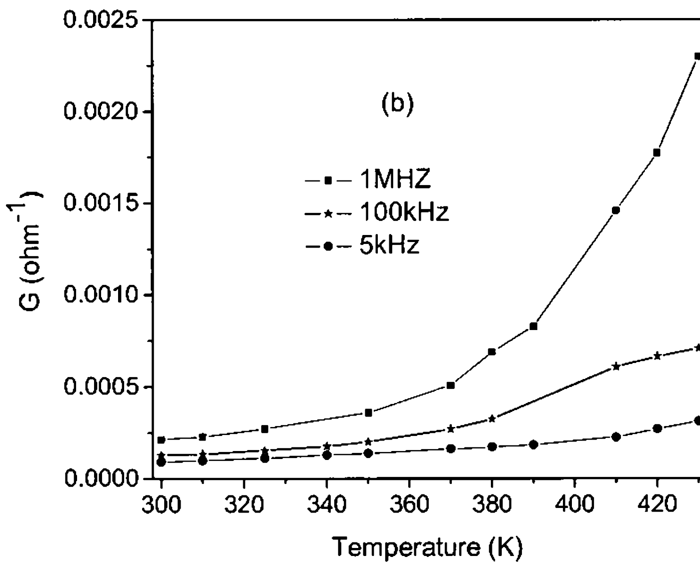

Figure 6.22 (b): Variation of conductance with temperature of Al/Al_2O_3/p-Si MOS structure at different frequencies (5kHz, 100kHz, 1MHz).

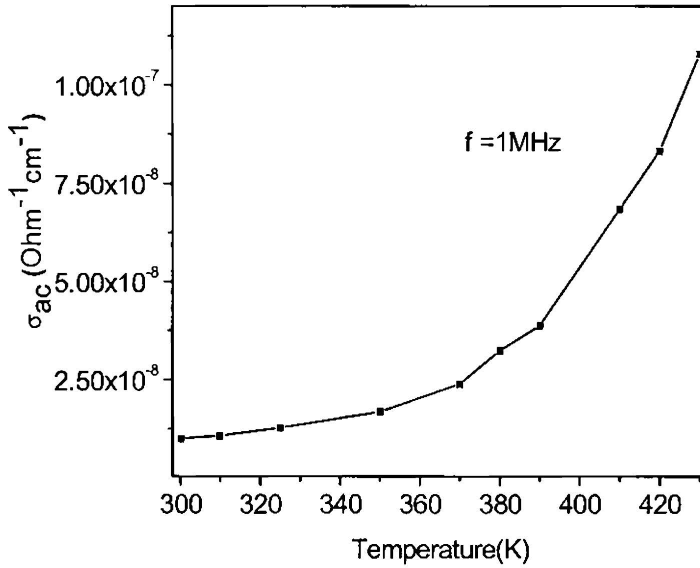

Figure 6.23: Temperature dependence of ac conductivity at frequency of 1MHz.

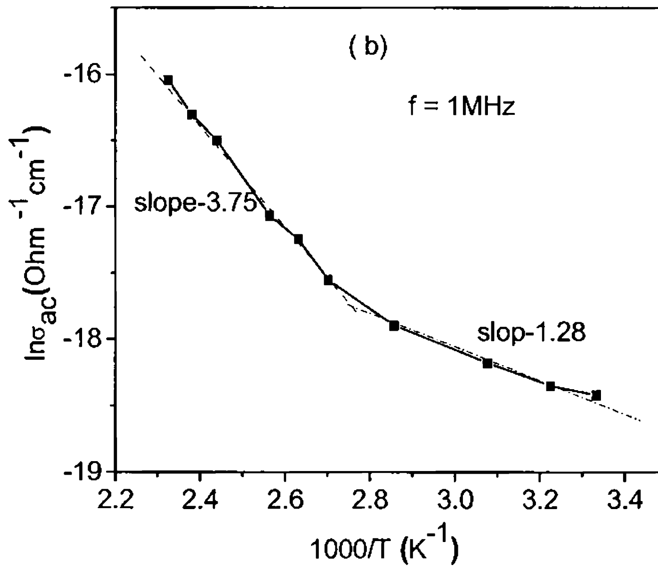

Figure 6.24: Arrhenius plot of $Al/Al_2O_3/p$-Si MOS structure at a frequency of 1MHz

Figure 6.23 & 6.24 show the temperature dependence of ac conductivity at a frequency of 1MHz. According to literature report [20,36], the increase in the electrical conductivity at low temperature is attributed to the impurities, which reside at the grain boundaries of Al_2O_3. These impurity levels lie close below the bottom of the conduction band and thus it has small activation energy.

A linear relationship between the total conductivity and the inverse temperature could be written as

$$\sigma_{ac} = \sigma_0 \exp(-E_a/kT) \tag{6.22}$$

By analyzing the temperature dependence of ac conductivity, the activation energy can be determined from the slope of Arrhenius plot (σ_{ac} vs.1000/T) [20,36-39]. From Figure 6.24 it is clear that the ac conductivity begins to change rapidly above 380K. From Arrhenius plot we get activation energy values as 110.6meV at temperature <390K and 321meV at temperature >390K respectively.

6.7.6 Current –Voltage (I-V) analysis

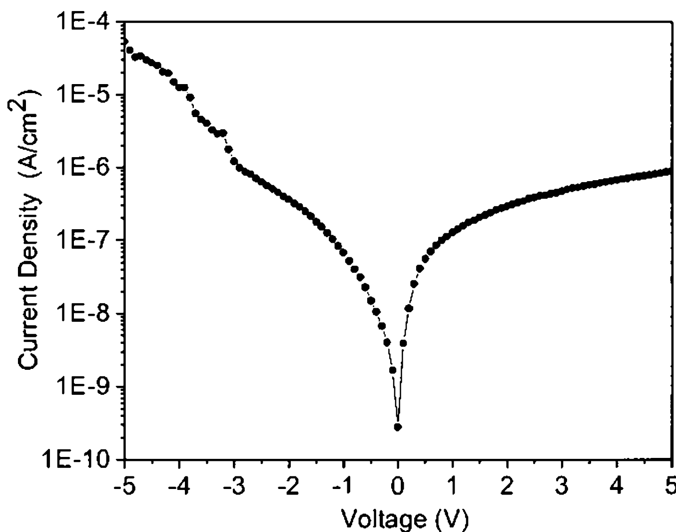

Figure 6.25: J-V Characteristics of $Al/Al_2O_3/p\text{-}Si$ MOS capacitor

Figure 6.25 shows J-V the (current density - voltage) characteristics of $Al/Al_2O_3/p\text{-}Si$ capacitor with a physical thickness of 24nm measured using a Keithley 485 pico ammeter and an ALSPC-02 data acquisition card. In negative bias condition (accumulation) the gate current is mainly conducted by the electron injected from the metal gate to the conduction band and consequently increases with increasing gate voltage. The current level in the negative bias condition depends on the oxide thickness, which increases with decreasing oxide thickness.

In substrate injection region (inversion), conduction is basically by the minority carrier generation from back contact, interface states and bulk traps [41,42]. At room temperature current component due to this minority carrier diffusion from back contact can be neglected, while it dominates at higher temperature. Thus the gate current in depletion region at room temperature is mainly due to by the minority carrier generation from the interface states and bulk trap. The amount of charge carriers from interface states should be invariant under deep depletion. Therefore gate current shows a nearly saturation tendency under deep depletion [39-41].

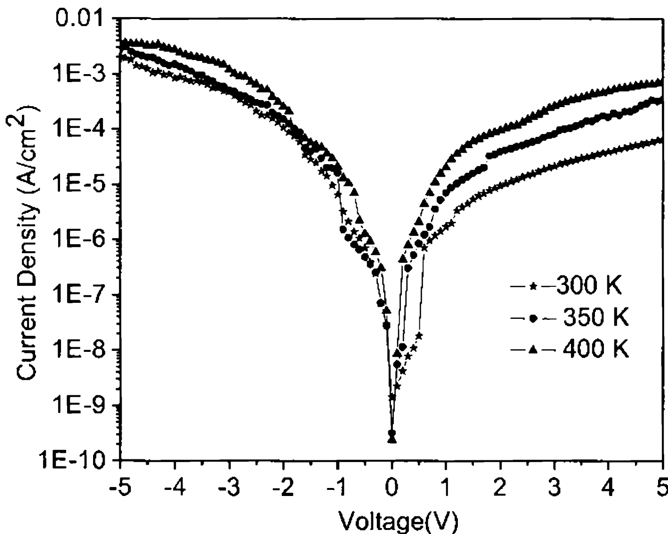

Figure 6.26: Temperature dependent J-V Characteristics

The leakage current densities were obtained in the order of 10^{-6} A/cm^2 at an applied gate voltage of 1V corresponding to a resistivity of 1.5× 10^{13} Ohm-cm. Temperature dependent I-V were studied (Figure 6.26) and it was found that as temperature was increased leakage current also increased.

From J-V characteristics the dc conductivity was extracted (Figure 6.27). It is clear that as temperature increases dc conductivity increases.

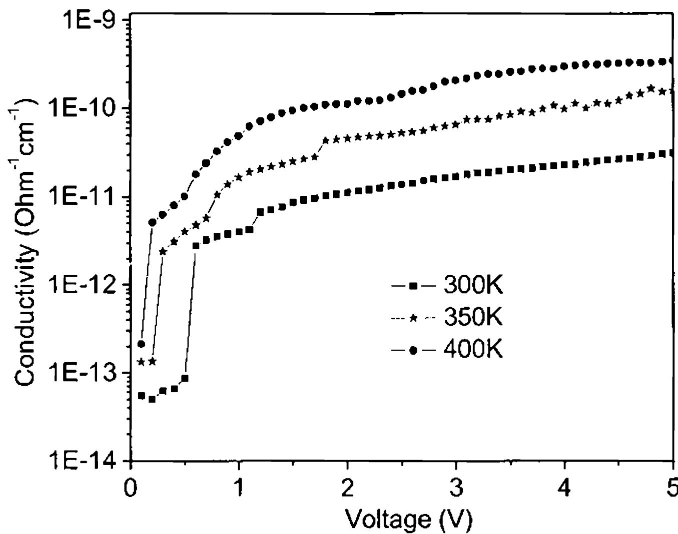

Figure 6.27: Temperature dependent dc conductivity

Figure 6.28 is J-E plot of Al_2O_3film having 24nm thickness and shows very low current density in the order of 10^{-7}A/cm^2 at low applied fields. This current is attributed to a combination of leakage current and charging current due to capacitive charging. The value of current density is lower at lower field and saturated at a field of 0.5 MV/cm to 3MV/cm and then increased. This behavior is observed in the case of SiO_2 thin film also. This may be due to phonon assisted tunneling in neutral traps or series resistance in measurement structure. The sudden increase in current at low field may be due to the breakdown at defects or weak spot in the dielectric and followed by self healing. It is possible that localized current surges evaporated small regions of the Al metal contact from the surface thus preventing further conduction [40,42]. Thin Al_2O_3 films exhibit low stress

induced leakage current effect. Very good transistor properties were reported for films having low stress induced effect. Breakdown is observed at a field of 3.8 MV/cm, which is higher than the reported value of sapphire (0.5 MV/cm) [40].

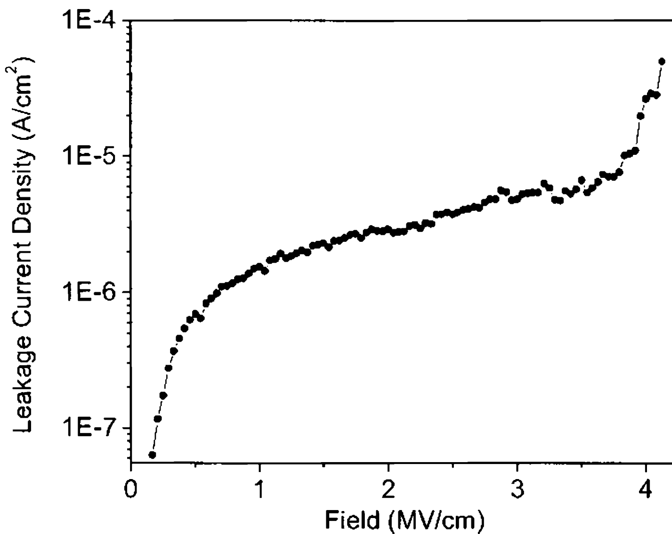

Figure 6.28: J-E characteristics of Al/Al_2O_3/p-Si MOS capacitor

6.8 Conclusions

MOS capacitors were fabricated successfully using nano layers of Al_2O_3 as dielectric, which is deposited by Atomic Layer Deposition. Frequency and temperature dependence of electrical and dielectric properties of Al/Al_2O_3/p-Si (MOS) capacitor have been studied in detail in the wide range of frequencies (5kHz to 1MHz) and temperature (300–430K) respectively. It was observed that the values of capacitance (C) and conductance (G/ω) decrease with increasing frequency and decreasing temperature. Experimental results verified that the frequency, temperature and bias voltage dependence of ε', ε'', and tanδ. The ac conductivity increases with increasing frequency and temperature for each bias voltage. The increase in capacitance with temperature at low frequency can be attributed to a shift in flat band voltage and effects of interface trap charges

present in the oxide material. The observed high values of ε' and ε" at low frequencies are attributed to flat band voltage shift and conductivity which is directly related to the increase in the mobility of localized charge carriers at interface states. Also interface traps can easily follow the ac signal at low frequencies and yield an excess capacitance and conductance. Series resistance of the structure decreases with increasing frequency and temperature. Thus we can draw a conclusion that the electrical and dielectric properties of Al/Al_2O_3/p-Si structure depend on the quality of the oxide layer, the density of interface traps and series resistance of the structure. These three are closely related to applied gate voltage, frequency and temperature.

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7

Formation of Alumina Nanoparticles in a Cold Wall Atomic Layer Deposition System and their Characterization

An explanation for the possible mechanism of formation of alumina nanoparticles in Atomic Layer Deposition process of alumina using Trimethyl Aluminum (TMA) and water in a cold wall ALD chamber based on the physisorption of TMA and surface energy of alumina thin films is presented here. Characterizations of synthesized particles are also presented.

7.1 Introduction

As outlined in the previous chapters Atomic Layer Deposition is a cyclic process with a sequence of self terminating process steps and films grow on any substrate topology [1-5]. The intrinsic surface control mechanism of ALD process is based on the saturation of an individual, sequentially-performed surface reaction between the substrate and precursor molecules. Most metal reactants used in ALD fulfill the criteria of self termination and adsorption in a monolayer. In the reaction of metal reactants (ML_n) with a solid oxide material, however, $MO_{n/2}$ particles can form in a single saturating reaction of metal reactant [6-12] and so multilayer formation occurs. These unexplained formation of nanoparticles of metal oxides in the chamber during the ALD of binary oxides for high-k gate applications was occasionally reported in the literature[6,7]. Metal oxide particles were formed during the reaction of metal precursor with oxide substrate used for various applications. In this present work we report the formation of alumina nanoparticles at the cold walls of the ALD chamber during the deposition of alumina films by atomic layer deposition. Trimethyl aluminum (TMA) and water were used as precursors. Attempts were made to explain the reaction mechanism which controls the formation of alumina nano particles. Detailed characterizations of these alumina nano particles

were also done. Detailed description of chemisorption mechanisms involved during TMA exposure on the substrate in done at chapter 4.

7.2 Formation of metal oxide particles in atomic layer deposition: A brief review

The first report of $MO_{n/2}$ particle formation during CVD was reported by Kooyman et al. in 1992 [6]. They observed TiO_2 particles after the reaction of $TiCl_4$ with silica crystals. The particles were 0.2-0.3μm in size and were chemically anchored to silicon substrate. In ALD investigations, $MO_{n/2}$ particle formation during ALD was first reported by Haukke *et al.* in 1993 [7]. They also observed TiO_2 particles after the chemisorption of $TiCl_4$ on porous high surface area silica. Haukke *et.al* examined particle formation in detail and found that TiO_2 particles were thin plate and with maximum dimensions of 2μm. These findings were in accord with the reports by Kooyman [6]. These authors concluded that TiO_2 formation is saturating and limited by the number of hydroxyl groups on the silicon substrate, and found that size and crystallinity of particles depend on process conditions, like reaction temperature and nature of substrates. Ritala *et al.* also reported unexpected observation of particles when they investigated the growth of TiO_2 on the flat oxide substrates by the $TiCl_4$/ H_2O ALD process [13,14].

In 1996 Kytokivi *et al.* reported the formation of ZrO_2 particles when they investigated the $ZrCl_4$ chemisorption on porous high surface area silica and on alumina [9]. ZrO_2 particles were considerably smaller, with dimensions in the order of 10 nm [10]. Kytokivi *et. al.* suggested that the ZrO_2 particles might be from the formation and decomposition of hydroxylchloride $Zr(OH)_mCl_{4-m}$ or oxychloride $ZrOCl_2$ intermediates. Kytokivi and Haukka showed by infrared measurements that TiO_2 and ZrO_2 particles are bonded to silica substrate through Si-O-Ti and Si-O-Zr bonds respectively [11].

In 2004 Elam *et al.* and Graugnard *et al.* again reported the formation of TiO_2 [15-17]. In 2005 Rikka L. Puurunen published a review on the formation of Metal Oxide particles in Atomic Layer Deposition during the chemisorption of metal chlorides [9]. She reviewed the experimental

results and suggested a mechanism for metal oxide particle formation and proposed a new mechanism based on Ligand Exchange reaction typical for ALD with hydroxyl and chlorine groups as reactive sites. None of the mechanism suggested so far can fully account for the experimental observations of the metal oxide particle formation. In the present work we try to explain the possible mechanism of formation of alumina nanoparticles in the cold wall ALD chamber during the Atomic Layer Deposition, based on the physisorption of TMA and surface energy of alumina thin films [18].

7.3 Experimental

Alumina nano particles were observed to grow simultaneously along with the alumina films under certain experimental conditions in our home made Atomic Layer Deposition system. Later these particles were grown purposefully to study their formation conditions. They were also subjected to structural and morphological characterization. A detailed description of the experimental setup is given in chapter 3. TMA (Trimethylaluminum: Sigma-Aldrich, 2.0 M solution in Toluene) and water were used as precursors for aluminum oxide deposition. Initially the precursors were loaded in stainless steel bubblers in vacuum and were introduced alternately to the hot zone of the chamber with an inert carrier gas (Nitrogen, 99.999 %). Between each precursor exposure a purge gas was pulsed through the deposition chamber in order to remove unreacted precursors and reaction by products. The flow rates of precursors and purge gas were measured with Mass Flow Meters (Bronkhorst). The order and typical time of the cycles used in these experiments were (i) TMA-3 seconds (ii) purge-15 seconds, (iii) water-2 seconds and (iv) purge-15 seconds. Nitrogen was used as the carrier gas at a rate of 250 sccm. The experiment was repeated by varying the conditions like chamber pressures, temperature and exposure times. The chamber pressure was varied between 0.15 mbar to 0.45mbar. Temperature of the hot zone was varied from room temperature to 300^0C. The chamber outer walls were water cooled. It was observed that the alumina powder gets deposited on the cooled surfaces of the chamber when the hot zone was at a higher

temperature and the deposition occurs everywhere inside the chamber when the hot zone was at room temperature.

Structural characterizations of the as prepared and post annealed Al_2O_3 samples were performed using X-ray diffraction (Bruker AXS D8 Advanced, Source: Cu- Kα- 1.5414Å). The powder morphology was studied using Scanning Electron Microscopy (SEM- JEOL JSM6390LV) and HRTEM (JEOL3010 operated at 200keV). The samples were also subjected to Selective Area Electron Diffraction (SAED). The chemical compositions of the as prepared samples were determined by Energy Dispersive Analysis through X-ray spectroscopy (EDS -JEOL JED 2300). The FTIR spectra were recorded on Thermo Nicolet Avatar 370. The samples were pelletized at $7x10^4$N and the dielectric studies were carried out using an LCR bridge (Fluke PM 6306).

7. 4 Results and discussion

There are two types of adsorption mechanisms- physical sorption (physisorption) and chemical sorption (chemisorption). Physisorption is due to weak Van der Waals forces (maximum value of heat of physisorption is taken as, 8kcal/mol=0.347eV/molecule) with minimum changes in the adsorbate, whereas chemisorption involves much more energy (heat of chemisorption is up to 250 kcal/mol) [20,21] and making and breaking of bonds. Hence only one layer is adsorbed in the case of chemisorption and the adsorbate remains on the adsorbed site (site specific), where as in physorption this restriction is not there. Physisorption generally occurs at low temperature areas of the chamber since the energy involved in this process is much smaller.

In ALD, the required adsorption mechanism is irreversible chemisorption to satisfy the condition of self termination of reaction [22]. Therefore it is safe to believe that at the water cooled walls of the reaction chamber (~300K) TMA is physisorbed rather than chemisorbed. This is aided by the fact that stainless steel surface of the chamber walls lack the OH surface species required for the easy chemisorption of TMA molecules. Since the physisorption is a reversible mechanism, some of the TMA may be

reemitted during the subsequent pumping and purging. But it is possible that some are retained on the walls. These TMA molecules react with the water molecules which enter the chamber in the next pulse and form alumina molecules. The reaction by products is removed from the chamber in the subsequent argon purging. These newly formed aluminum acts as substrate for further cycles.

How nanoparticles are formed instead of a nano film? The surface formation energy of alumina has a comparatively high value of 16.23 - 17.48 eV/nm^2 [1,23, 24]. From Ref. [22] Figure 22 we can find out the maximum number of alumina molecules per nm^2 area of silica substrate as 4.8. Assuming that (i) in the present case also this is the maximum possible number and (ii) the heat of physisorption is same as the energy of physisorption [20], the total energy associated with physisorption of 4.8 molecules per nm^2 area is $0.347eV \times 4.8 = 1.67\ eV/nm^2$. We can see that this is much smaller than the surface formation energy of alumina. In other words, to form 1 nm^2 surface area of alumina film, it requires minimum 16.23 eV, where as physisorption can provide only 1.67 eV energy to hold the film to the substrate. Hence the newly forming film will try to reduce the surface area by coalescing and assuming spherical shape. This is aided by the mobility of physisorbed molecules on the surface of the substrate. The spherical particles so formed will act as substrates for the subsequent cycles of deposition. It has to be noted that at the hot zone, since chemisorption takes place, which involves energies up to 10eV per molecule and since chemisorbed molecules are bound to the point where they are adsorbed, this curling of the film does not happen. This explains the mechanism of nano particle or nano rod formation in the cold regions of ALD chamber.

It is important to note here that there are reports of alumina films prepared by ALD at a substrate temperature of 33°C [25] and absence of any effect of substrate temperature on 'growth per cycle of alumina films [22]. But a literature survey reveals that most of the work in this field is done at a substrate temperature of 170°C or more to get good quality alumina films [26-32]. Our experiments also support this observation [Table 5.2]. The films which were prepared at 33^0C show degradation in all its electrical and

optical properties. During deposition long purge and exposure time is also needed. We have repeated the experiment by simply switching off the heater, keeping all other experimental conditions same. It was observed that particles were formed everywhere inside the chamber which was at a temperature of 27°C, without forming any detectable film on the substrate. Particles were formed even with longer purge durations after water pulses. This eliminates the possibility of TMA reacting with residual water vapour which may be present in the chamber. From these it is clear that particle formation can occur in a cold wall ALD system even with optimized process parameters with sufficiently long deposition durations.

7. 5 Characterization of Alumina particles

7. 5.1 Structural characterization

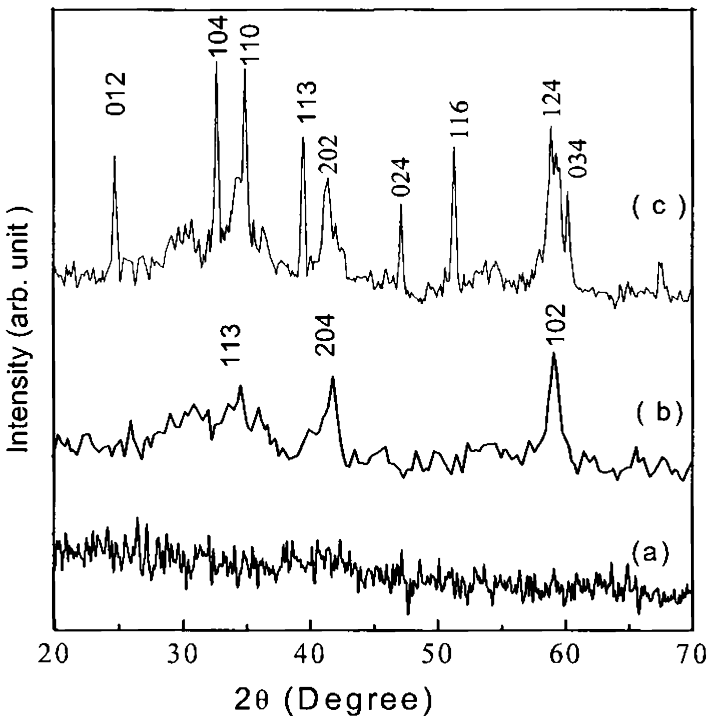

Figure7.1: X-ray diffraction patterns of Alumina powder samples-(a) as prepared, (b) 900°C and (c) 1200°C annealed.

The structural characterization of the powder was done using XRD. Figure 7.1 shows the XRD pattern of as prepared Al_2O_3 powder and annealed samples. Amorphous nature of the as prepared sample is evident from the pattern. The 900^0 C and 1200^0C annealed samples show weak Bragg peaks of $\acute{\eta}$-Al_2O_3 and α-Al_2O_3 respectively. The broad hump in 900^0C annealed samples indicates that the powder is not completely crystalline. Comparison of these values with JCPDS files [33] clearly shows that the annealed samples are indeed η and α polymorphs of alumina. The α phase samples were the most stable phase of alumina. The crystal size calculated using Debye-Scherer formula for 900°C annealed samples is 19.5nm whereas that for samples annealed at 1200^0C is between 34.2nm to 43.07nm.

7.5.2 Compositional analysis

Chemical compositions of the prepared powder samples were identified using EDS measurement. From Table 7.1 it is clear that the O/Al ratio of the annealed samples is less than that of as prepared samples which is in amorphous state.

Table 1: Comparison of EDS data of as prepared and annealed Al_2O_3

	Element	Wt%	At%	O/Al
Alumina powder as	O	43.93	56.92	
prepared	Al	56.07	43.08	1.32
Alumina powder	O	42.39	55.38	
annealed at 900^0 C.	Al	57.61	44.62	1.24
Alumina powder	O	36.25	48.95	
annealed at 1200^0 C.	Al	63.75	51.05	0.96

7.5.3 Surface morphology

Powder morphology of the samples was analyzed using SEM. Figure 7.2 shows the SEM photograph of as prepared, 900°C and 1200°C annealed alumina powders. As the sample is annealed, the powder agglomerates. Further increase in annealing temperature showed an enhancement in the cluster formation.

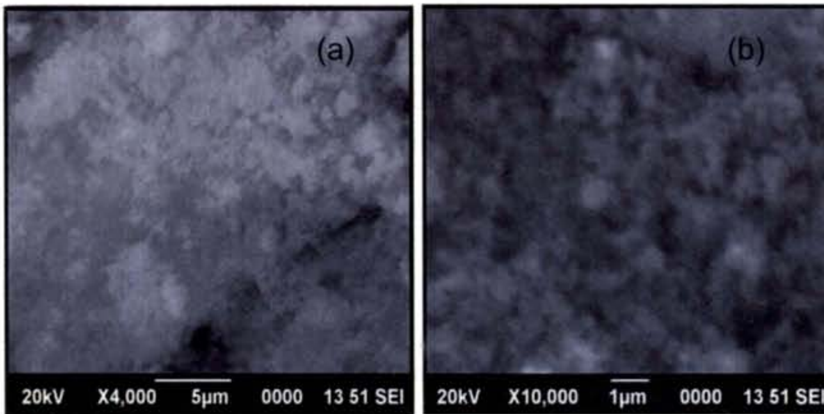

Figure 7.2: SEM images of the alumina powder: (a) as prepared (b) as prepared sample at higher magnification.

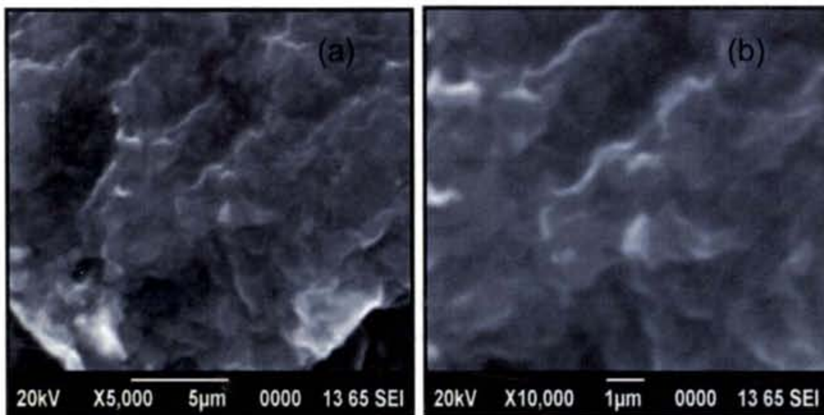

Figure 7.2: SEM images of the alumina powder: (a) 900°C annealed (b) 900°C annealed at higher magnification.

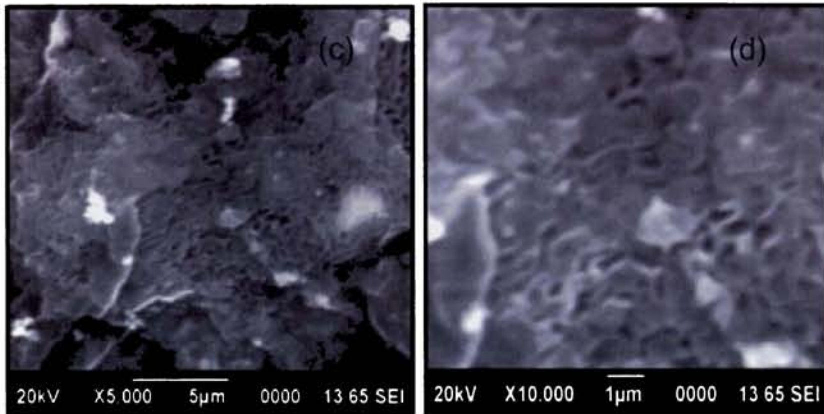

Figure 7.2: SEM images of the alumina powder (c) 1200°C annealed (d) 1200 C annealed sample at higher magnification.

Surface morphology of the prepared samples were analyzed using HRTEM. Figure 7.3 shows the HRTEM images of the as prepared and 1200°C annealed samples. It is evident from various HRTEM images of as prepared and annealed samples that most of the annealed particles are in the range ~35-45nm in size whereas as prepared samples are smaller.

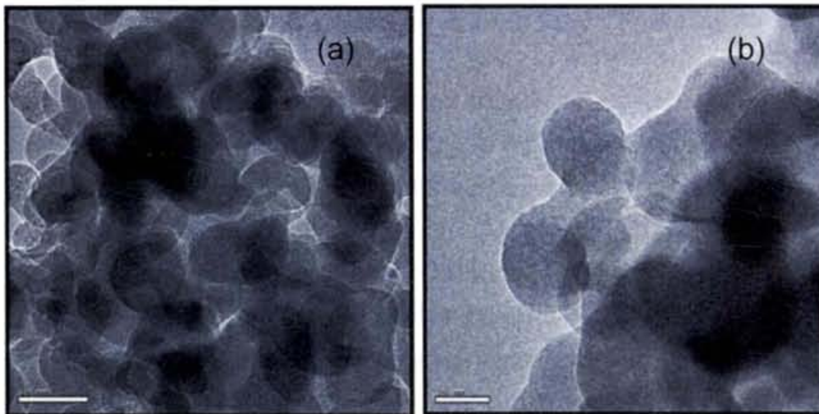

Figure7.3: HRTEM images of alumina Nanoparticles (a) as prepared sample (50nm scale) (b) as prepared sample (20nm scale).

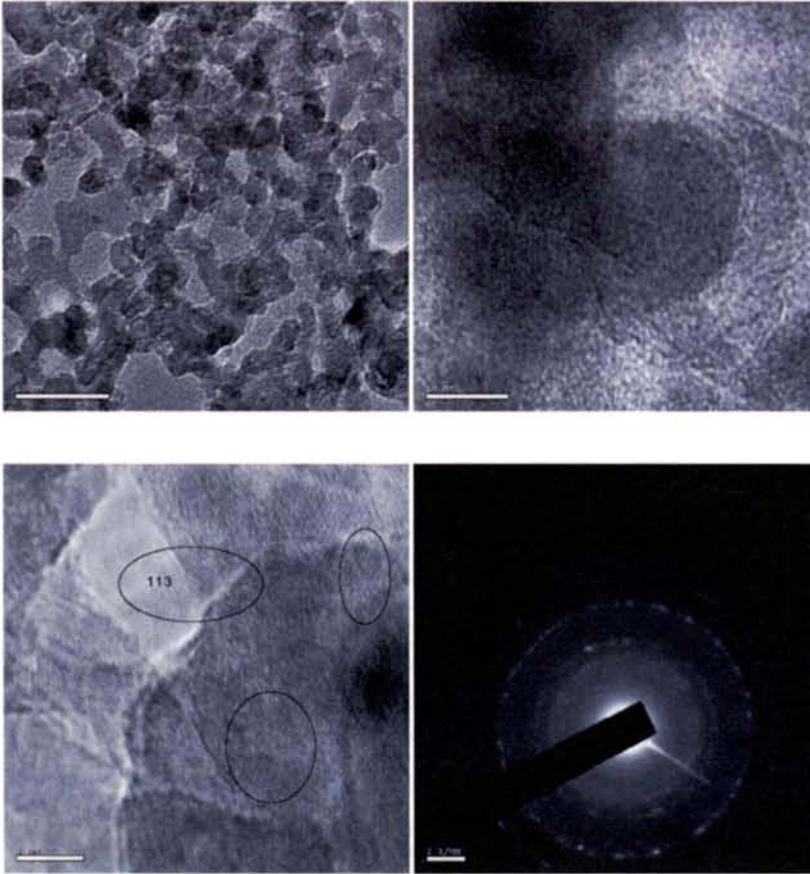

Figure7.3: HRTEM images of alumina nanoparticles; (c) annealed at 1200°C (50nm scale), (d) annealed at 1200°C (10nm scale), (e) annealed at 1200°C (5nm scale) shows crystal planes, (f) SAED of 1200°C annealed sample.

This increase in particle size is due to the agglomeration of particles at higher temperature. Figure 3(f) shows SAED pattern of sample annealed at 1200^0C. The more or less circular pattern instead of clear cut points in SAED, confirms the nano crystalline nature of the samples [1]. The d values and planes calculated from this is tabulated in Table 7.2 which match well with results from the powder XRD. The good agreement between the reported and experimental'd' values is a conclusive proof that the nano

particles formed are indeed α-alumina. This result in agreement with x-ray diffraction studies of 1200°C samples in the above section.

Table 7. 2: Comparison of reported and experimental'd' values and planes from SAED data. (*From JCPDS 1998)

*'d' reported**	*'d' expt.*	*hkl*
2.5520	2.556	104
2.0850	2.084	113
1.4044	1.461	---
1.1898	1.189	220
1.0988	1.095	0210

The as prepared alumina nano powder was pelletized at $7x10^4$N and annealed at 200^0C for 3 hours. The diameter and thickness of the pellets were 6mm and 2mm respectively. Aluminum electrodes were vacuum deposited onto both flat sides of the pellets and were subjected to dielectric measurements. The dielectric constant obtained was 9.08 at 1 MHz and was found to be in agreement with the reported values [34-36].

7.5.4 FTIR Analysis

Figure 7.4 (a) and (b) show the FTIR spectra of as prepared and annealed Al_2O_3 powder material. Amorphous nano alumina powder shows a broad peak in the range of 500-900cm^{-1}. This is due to Al-O stretching mode (750-850 cm^{-1}) and O-Al-O bending mode (650-700cm^{-1}) [37]. There is a broad peak between 3000cm^{-1} and 3700cm^{-1} which indicates OH stretching region. The peak at 1633.01 which can be considered as the H-O-H scissor mode [38] are the peak at 3438.15 can be due to water molecule. Annealed sample has multiple peaks in the range 500-900 cm^{-1}, which confirms the crystalline nature [39].

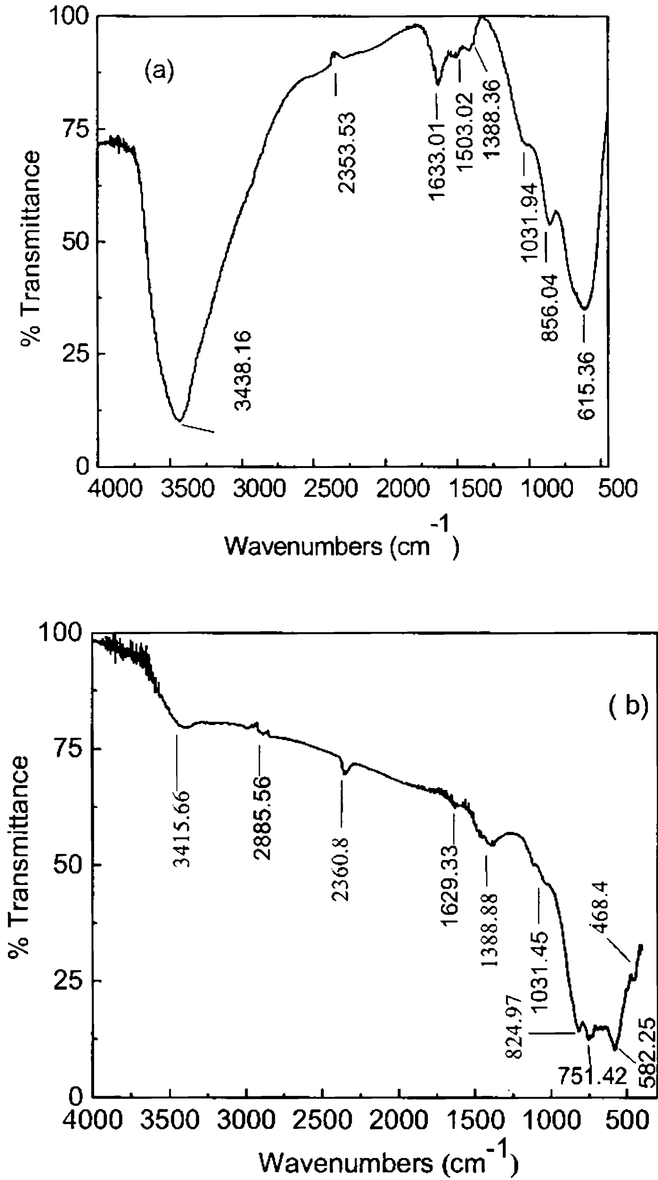

Figure 7.4: FTIR spectra of Alumina powder material. (a) As prepared sample. (b) Sample annealed at 1200^0C.

Stretching vibrations of Al-O and OH are observed at 582.25cm^{-1} and 3415.66 cm^{-1} respectively. The lack of H-O-H scissor mode in annealed

sample indicates that OH stretching mode at 3415.66 cm^{-1} corresponds to hydroxyl species. CH bending vibrations of CH_3 are present at 1388.88 cm^{-1} in the annealed sample.

7. 6 Conclusions

Nano alumina particles of size ranging from 20-45nm were observed at the cold walls of our home made cold wall type Atomic Layer Deposition system during the deposition of alumina thin films using TMA and Water as precursors. An explanation is given for this phenomena based on the physisorption of TMA on the cold walls of the ALD chamber. It was shown here that since the surface energy of alumina is larger than the physisorption energy, the newly forming film will try to reduce the surface area and assume spherical shape whenever physisorption take place. Structural characterizations of as prepared and annealed particles were done by various characterization tools. In prepared state the particles are amorphous in nature and become crystalline after annealing. Crystal size as calculated using Debye-Scherrer formula was 19-44nm range and that found from HRTEM images was in the range 20-45 nm. The dielectric constant of the pelletized sample was found to be 9.08 at 1MHz which matches well with the reported values.

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8

Summary and Scope for Further Study

1. Summary

The ever-increasing demand for functionality and speed for semiconductor applications requires enhanced performance, which is achieved by the continuous miniaturization of CMOS dimensions. Because of this miniaturization, several parameters, such as the dielectric thickness, come within reach of their physical limit. As the required oxide thickness approaches the sub-1 nm range, SiO_2 become unsuitable as a gate dielectric because its limited physical thickness results in excessive leakage current through the gate stack, affecting the long-term reliability of the device. This leakage issue is solved in the 45 nm technology node by the integration of high-k based gate dielectrics, as their higher k-value allows a physically thicker layer while targeting the same capacitance and Equivalent Oxide Thickness (EOT). Moreover, Intel announced that Atomic Layer Deposition (ALD) would be applied to grow these materials on the Si substrate. ALD is based on the sequential use of self-limiting surface reactions of a metallic and oxidizing precursor. This self-limiting feature allows control of material growth and properties at the atomic level, which makes ALD well-suited for the deposition of highly uniform and conformal layers in CMOS devices, even if these have challenging 3D topologies with high aspect-ratios.

In 2007, Intel announced the integration of high-k based gate dielectrics, grown by Atomic Layer Deposition (ALD), in the 45 nm technology node. This announcement indicates the importance of ALD and high-k-based materials, and therefore justifies the PhD research that has been done since 2006. During this research, we intended to gain fundamental knowledge on the ALD growth behavior of dielectric materials on semiconductor surfaces. We focused on three main topics: (i) The development of Atomic layer Deposition facility

(Chapter 3), (ii) The Surface chemistry and growth mechanism involved during the ALD of TMA and water (Chapter4). (iii) The deposition and characterization of Al_2O_3, the high-k material on silicon substrate for the various gate oxide applications.

We indigenously designed and fabricated a compact and inexpensive automated Atomic Layer Deposition system. The system has the capability to work in thermal as well as plasma mode. System parameters like precursor delivery parameters (flow rate, pulse time, pulse order and delay), chamber and precursor line pressure and Temperature (substrate temperature and precursor line temperature) were optimized in order to prepare films in ALD mode. The feasibility of the developed system were studied by depositing different materials including Al_2O_3, ZrO_2 and ZnO over different substrates (Silicon, glass and quartz).

Atomic Layer Deposition is a modified form of CVD. The mechanisms which underlie in ALD of several materials are not yet sufficiently understood. To understand the detailed growth mechanism and surface chemistry, we proposed a detailed chemisorption mechanism for the ALD of TMA and water. The most probable chemisorption mechanism taking place is suggested as the combination of complete ligand exchange and complete dissociation (CLE+CD). CLE dominates at higher OH concentrations, while CD dominates at lower OH concentrations. We theoretically calculated the maximum number of methyl groups that can be adsorbed per nm^2 area of Si surface as 6.25. Al concentration for different OH values were calculated which are in good agreement with experimentally reported data. We also calculated the growth per cycle for different OH concentrations, and calculated values are in agreement with experimentally reported values and our own experimental values.

Nano layers of Aluminum oxide were deposited over silicon substrates by ALD using TMA and water as precursors. The deposition parameters were optimized in order to obtain device quality Al_2O_3 films. The growth per cycle was calculated and obtained a value of 1.17Å/cycle. Stoichiometric composition

of the deposited films were measured using XPS and EDAX and obtained a value of 1.4. Deposited layers have a dielectric constant of 9.7 and a refractive index of 1.645. The amorphous nature of the films were verified by GXRD. Transparency of the deposited film over glass substrate was above 90%.

MOS capacitors were fabricated using ALD Al_2O_3 as dielectric layer. Electrical characterization of MOS capacitors was done by high frequency C-V analysis. The number density of fixed oxide charges present in our sample is in the order of 10^{10} which is in the limit of good quality oxide. The nature of fixed oxide charge is positive. The effect of frequency, gate voltage and temperature dependence of electrical and dielectric properties were studied in detail. It was observed that the values of capacitance (C) and conductance (G) decrease with increasing frequency and decreasing temperature. The ac conductivity increases with increasing frequency and temperature for each bias voltage. The increase in capacitance with temperature at low frequency can be attributed to a shift in flat band voltage and effects of interface trap charges present in the oxide material. The observed high values of ε' and ε'' at low frequencies are attributed to flat band voltage shift and conductivity which is directly related to the increase in the mobility of localized charge carriers at interface states. Also interface traps can easily follow the ac signal at low frequencies and yield an excess capacitance and conductance. Series resistance of the structure decreases with increasing frequency and temperature. Thus we can draw a conclusion that the electrical and dielectric properties of $Al/Al_2O_3/p\text{-}Si$ structure depend on the quality of the oxide layer (effective oxide charges and trapped charges), the density of interface traps and series resistance of the structure.

Nano alumina particles were formed at the walls of the Cold wall type ALD system during the deposition of alumina thin films using TMA and water. These samples were characterized using XRD, SEM,EDS, TEM and FTIR. An explanation for this phenomenon is also given.

2. Scope for further study

ALD has currently acquired the status of state-of-the-art and most preferred deposition technique, for producing nano layers of various materials of technological importance. This technique can be adapted to different situations where precision in thickness and perfection in structures are required, especially in the microelectronic scenario.

There is large scope for the modification and fine tuning of the ALD system hardware itself to suit different applications. Other than that some of the areas of interest regarding the ALD deposited high-k materials are listed below.

- Low temperature Plasma Enhanced Atomic Layer Deposition of Aluminum Oxide films over plastic substrate for flexible applications.
- Atomic Layer deposition of second generation high-k materials and nanolaminates is a very promising area of study.
- Investigations on the possibility of ALD deposited Al_2O_3 film used as a passivation layer in silicon solar cells. This may demonstrate the large potential of Atomic Layer Deposited Al_2O_3 films for future high-efficiency silicon solar cells.

Appendix A

Abbreviations used in the thesis

ALD	*Atomic Layer Deposition*
3D	*Three Dimension*
AFM	*Atomic Force Microscopy*
ALE	*Atomic Layer Epitaxy*
AS	*Association*
CD	*Complete Dissociation*
CDLE	*Complete Dissociation by Ligand Exchange*
CLE	*Complete ligand Exchange*
CMOS	*Complementary Metal Oxide Semiconductors*
C-V	*Capacitance Voltage*
CVD	*Chemical Vapour Deposition*
D_{it}	*Interface trap density*
DRAM	*Dynamic Random Access Memory*
EDAX	*Energy Dispersive X-ray spectroscopy*
EDS	*Energy dispersive spectrometer*
E_F	*Fermi level*
EOT	*Equivalent Oxide Thickness*
FESEM	*Field Emission Scanning Electron Microscopy*
FTIR	*Fourier Transform Infrared Spectroscopy*
GPC	*Growth Per Cycle*
GXRD	*Glancing Angle X-ray Diffraction*
HF	*High Frequency*
IC	*Integrated Circuit*
ITRS	*International Technological Road Map for Semiconductors*
I-V	*Current -Voltage*
MBE	*Molecular Beam Epitaxy*
ML	*Monolayer*

MOSFET	*Metal Oxide Semiconductor Filed Effect Transistor*
nm	*Nanometer*
PDA	*Post deposition Annealing*
PEALD	*Plasma Enhanced Atomic Layer Deposition*
PLD	*Pulsed Laser Deposition*
PLE	*Partial Ligand Exchange*
PVD	*Physical Vapour Deposition*
QCM	*Quartz Crystal Monitor*
QMS	*Quadrupole Mass Spectrometry*
RT	*Room Temperature*
RTA	*Rapid Thermal Annealing*
SD	*Simple Dissociation*
SEM	*Scanning Electron Microscopy*
sSOI	*strained Silicon-On-Insulator*
TEM	*Transmission Electron Microscopy*
TFEL	*Thin Film Electroluminescent*
TMA	*Tri Methyl Aluminum*
VDR	*Van der Waals Radius*
VLSI	*very large scale integrated circuits*
XPS	*X-ray Photoelectron Spectroscopy*
XRD	*X-ray Diffraction*

Appendix B

Symbols used in the thesis

ε_0	*Permittivity of free space*
ΔE_c	*Conduction band offset*
ΔE_v	*Valence band offset*
ΔV_{FB}	*Flat band voltage shift*
Al	*Aluminum*
Al_2O_3	*Aluminum Oxide*
C	*Capacitance*
C_{it}	*Interface trap capacitance*
C_{ox}	*Oxide capacitance*
C_s	*Silicon surface capacitance*
D_{it}	*Interface states density*
E	*Electric field*
e	*Elementary electronic charge*
E_c	*Conduction band edge*
E_F	*Fermi level*
E_g	*Band gap*
E_i	*Intrinsic Fermi level*
E_V	*Valance band edge*
G	*Conductance*
I	*Current*
J	*Current density*
k	*Dielectric constant*
N_{SS}	*Interface trap density*
Q_{eff}	*Effective oxide charge*
Q_f	*Fixed oxide charge*
Q_{it}	*Interface trapped charge*
Q_m	*Mobile ionic charge*
Q_{ot}	*Oxide trapped charge*
$\tan\delta$	*Loss tangent*
t_{ox}	*Thickness of oxide layer*

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V	*Voltage*
V_{FB}	*Flat band voltage*
V_G	*Applied Gate voltage*
ε'	*Dielectric constant*
ε''	*Dielectric loss*
σ_{ac}	*Ac conductivity*
φ_m	*Metal work function*
φ_s	*Semiconductor work function*
χ	*Electron affinity of the semiconductor*
χ_i	*Electron affinity of the insulator*
Ψ_B	*Bulk potential*
Ψ_s	*Surface potential*
ω	*Angular frequency*
β	*Full wave half maximum*