CASCADED SIGMA DELTA MODULATOR ARCHITECTURES FOR WIDEBAND ADCs

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THESIS CERTIFICATE

This is to certify that the thesis entitled "**CASCADED SIGMA DELTA MODULATOR ARCHITECTURES FOR WIDEBAND ADCs**" submitted by Mr**. Rijo Sebastian** to the Cochin University of Science and Technology, Kochi for the award of the degree of Doctor of Philosophy is a bonafide record of research work carried out by him under our supervision and guidance at the Division of Electronics Engineering, School of Engineering, Cochin University of Science and Technology. The contents of this thesis, in full or in parts, have not been submitted to any other University or Institute for the award of any degree or diploma.

We further certify that the corrections and modifications suggested by the audience during the pre-synopsis seminar and recommended by the Doctoral Committee of Mr**. Rijo Sebastian** are incorporated in the thesis.

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DECLARATION

I hereby declare that the work presented in the thesis entitled "**CASCADED SIGMA DELTA MODULATOR ARCHITECTURES FOR WIDEBAND ADCs**" is based on the original research work carried out by me under the supervision and guidance of **Dr. Babita Roslind Jose**, Associate Professor and **Dr. Shahana T.K.**, Professor, Division of Electronics Engineering, School of Engineering, Cochin University of Science and Technology, for the award of degree of Doctor of Philosophy with Cochin University of Science and Technology. I further declare that the contents of this thesis, in full or in parts, have not been submitted to any other University or Institute for the award of any degree or diploma.

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ABSTRACT

Among the different Analog to Digital Converter (ADC) architectures, Sigma Delta ($\Sigma\Delta$) ADC provides the highest resolution in low to medium bandwidths. $\Sigma\Delta$ ADCs sacrifices the speed to achieve accuracy. It uses relatively simple circuit elements to achieve higher conversion accuracy, and its accuracy and linearity are not as sensitive to the mismatch effects as seen in other types of ADC.

Low power, hardware efficient ADCs that can provide high resolution are preferred in wideband applications. A method to enhance the resolution in a cascaded $\Sigma\Delta$ modulator by adopting the analog inter-stage feedback paths between the stages is presented. This technique can be extended to Multi Stage Noise Shaping (MASH) and Sturdy MASH (SMASH) structures for improving the Signal to Noise Ratio (SNR). The inter-stage feedback paths in cascaded $\Sigma\Delta$ architecture contributes an enhancement in the order of noise shaping at the expense of a few delay blocks only and without affecting the digital cancellation logic. The higher order noise shaping achievement without any increase in the number of active blocks makes this architecture low power and hardware efficient.

An improved low-distortion MASH/SMASH $\Sigma\Delta$ modulator architecture along with resonation provides sufficient dynamic range (DR) for wideband operation. The easiest method to attain a further increase in Signal to Noise plus Distortion Ratio (SNDR) in higher order modulators utilized in wideband applications is to optimally place a pair of complex-conjugate zeros of the Noise Transfer Function (NTF) from dc to the signal bandwidth. The in-band quantization noise gets minimized by these shifting of zeros from dc to a frequency within the signal band. The improved low-distortion architecture eliminates the feedforward adder before the quantizer in the

first stage of MASH/SMASH structure and makes it hardware efficient. The shifted loop delay techniques incorporated in the improved low-distortion architecture helps to relax the signal processing timing issues in the critical path of the modulator.

The major challenges associated with the design of higher order $\Sigma\Delta$ modulators are loop stability issues due to its inherent non-linearity, integrator associated non-idealities, optimization of the integrator scaling coefficients and low operating bandwidth due to the accumulation of samples. An excellent alternative in the class of oversampling and noise shaping converters that can mitigate these problems associated with $\Sigma\Delta$ modulator, is the Differential Quantizer based Error Feedback Modulator (DQEFM) architecture. The design and simulation of a lowpass MASH DQEFM architecture is presented. The lower operating frequency and better performance of the proposed modulator in terms of hardware complexity and power makes it suitable for data conversion in 4G wireless standards. The performance of the proposed modulator has also been evaluated through circuit level simulations using HSPICE.

Finally, a novel bandpass DQEFM (BP DQEFM) architecture and its cascaded implementation are presented. The mathematical analysis and simulation results indicate the resemblance of the proposed BP DQEFM with the conventional $\Sigma\Delta$M. The circuit level simulations of a second order BP DQEFM for digital radio application indicate its better performance in terms of hardware complexity and power. The cascaded BP DQEFM architecture has been made re-configurable for data conversion operation in Global System for Mobile communications (GSM)/Wideband Code Division Multiple Access (WCDMA) standards. The circuit level simulations of the proposed MASH BP DQEFM has been performed for a bandwidth of 200 kHz for GSM and bandwidth of 5 MHz for WCDMA.

KEYWORDS: Analog-to-digital converters; Sigma delta modulators; MASH; Sturdy MASH; Cascaded sigma delta modulators; Differential Quantizer.

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ABBREVIATIONS

2G	Second Generation
3G	Third Generation
4G	Fourth Generation
5G	Fifth Generation
ADC	Analog-to-Digital Converter
BW	Bandwidth
CIFF	Cascade of Integrators in Feedforward
CMOS	Complementary Metal Oxide Semicondcutor
CT	Continuous Time
DAC	Digital to Analog Converter
DEM	Dynamic Element Matching
DNC	Delay based Noise Cancellation
DSP	Digital Signal Processing
DT	Discrete Time
DQ	Differential Quantizer
ECG	Electrocardiogram
EFM	Error Feedback Modulator
ELD	Excess Loop Delay
ENOB	Effective Number of Bits
ERBW	Effective Resolution BandWidth
FFT	Fast Fourier Transform
GBW	Gain Bandwidth
GSM	Global System for Mobile communications
GSPS	Giga Samples Per Second

IC	Integrated Circuits
LSB	Least Significant Bit
LTE	Long Term Evolution
MASH	Multi-Stage Noise Shaping
MSPS	Million Samples per Second
MIMO	Multiple-Input Multiple-Output
NRZ	Non Return to Zero
NTF	Noise Transfer Function
OL	Overloading Level
op-amp	Operational Amplifier
OSR	Oversampling Ratio
OTA	Operational Transconductance Amplifier
PSD	Power Spectral Density
RF	Radio Frequency
SC	Switched Capacitor
SDR	Software Defined Ratio
SFDR	Spurious Free Dynamic Range
SMASH	Sturdy Multistage Noise Shaping
SNDR	Signal to Noise-plus-Distortion Ratio
SNR	Signal to Noise Ratio
SNRp	Peak Signal to Noise Ratio
SR	Slew Rate
STF	Signal Transfer Function
TI	Time Interleaved
VLSI	Very Large Scale Integration
WLAN	Wireless Local Area Network
WCDMA	Wideband Code Division Multiple Access

NOTATIONS

C	Capacitance
C_f	Feedback capacitance
dB	Decibel
$dBFS$	Decibels relative to full scale
Δ	Quantization step size
E	Quantization error
FoM_w	Walden figure of merit
F_s	Sampling frequency
g_m	Transconductance
k	Boltzmann's constant
k_i'	Feedforward coefficients
N	Number of paths of the modulator
n	Nano
p	Pico
P_{diss}	Power Dissipated
ϕ	Clock rate
S/H	Sample and hold
$\Sigma\Delta$	Sigma delta
T	Temperature
T_s	Sampling time
μ	Micro (10^{-6})
V	Volts

CHAPTER 1

INTRODUCTION

Nowadays, digital technology has permeating all aspects of life. This can be attributed to the great advancements occurring in the digital computing and signal processing fields. Analog to Digital Converter (ADC) act as an interface between the analog and digital world, and it translates the analog signals into digital form. ADCs are used in a variety of fields and the application of ADCs include broadband telecommunication systems, precision industrial measurements and process control, ultra wideband communication systems, Software Defined Radio (SDR), data acquisition systems, consumer electronics and medical devices.

Modern communication systems often require high speed, low to moderate resolution ADCs with low power consumption (Qureshi *et al.*, 2017). The necessity of the conversion accuracy of ADC becomes extremely important in certain fields like medical imaging (Fan *et al.*, 2018), medical devices (DUrbino *et al.*, 2018) and measuring instruments (Frick *et al.*, 2016). The performance of ADC limit the performance of digital signal processing in a radio receiver system. Since the performance of different types of ADC architecture vary greatly, the designer has to carefully choose the right ADC for a particular application. ADCs are generally divided into two categories: Nyquist rate converters, which include Flash ADC, Pipeline ADC, Successive Approximation Register (SAR) ADC, and the other type is oversampling ADC, mainly the Sigma Delta ($\Sigma\Delta$) ADC.

1.1 Motivation

In modern wireless communication system design, the current trend is to move the analog-to-digital interface as close to the receiving antenna. The position of ADC in a radio receiver system plays a vital role in the overall performance, power consumption, cost and complexity. The modern receiver systems are capable of implementing many analog functions into the digital domain, as the ADC operation moves closer to the antenna side. Such ADCs, operating at radio frequency (RF) or intermediate frequency (IF), require very stringent performance specifications. ADCs used in broadband scenarios often require wide dynamic range (DR).

The rapid progress in VLSI technology along with the architectural advances have accelerated the development of portable and low power wireless broadband communication devices which can manage higher data rates. In recent years, most of the wireless communication systems make use of a direct conversion or zero-intermediate frequency demodulation scheme for down converting the radio frequency (RF) signal into baseband signal. In a direct conversion receiver system, the received signal is processed at the baseband rather than at some high IF (Abidi, 1995). Various fourth generation (4G) wireless communication standards such as Long Term Evolution (LTE), LTE-Advanced (LTE-A), LTE Advanced Pro (LTE-A Pro) are capable of providing data rates up to several hundred Mbps or even 1Gbps (Ghosh *et al.*, 2010). LTE technology manages higher data rates and provides simultaneous services to large number of users. The LTE release-8 supports six different bandwidths ranging from 1.4 MHz to 20 MHz. Among these, 5 MHz and 10 MHz are the most commonly used bandwidths. The LTE-Advanced can handle higher capacity through techniques like Carrier Aggregation (CA), enhanced use of multi-antenna techniques and support for Relay Nodes (RN). The LTE-A can operate with a maximum bandwidth of 100 MHz through carrier aggregation (Ghosh *et al.*, 2010). These 4G wireless standards demand the requirement of an ADC that can perform efficiently in higher bandwidths.

The increasing demand for high speed and high data rate mobile devices accelerated the deployment of fifth generation (5G) mobile communication systems. In order to manage huge data users, the 5G wireless systems make use of millimeter-wave (mmWave) frequency bands (Barati *et al.*, 2015) to attain large bandwidth. The advanced massive multiple-input multiple-output (MIMO) systems developed for next generation wireless systems are capable of providing high speed data rates. The overall power consumption of the transceiver is a key design parameter and the main challenge is the design and implementation of a high resolution, low power, wideband ADC operating with several GS/s required for the digitization in 5G wireless systems.

The demand for single-chip solution for multi-standard requirements in wireless systems necessitates ADCs which are re-configurable. In recent years, the observed trend has been towards the convergence of many standards of operation into a single mobile device, such as a smart phone. The convergence of various wireless communication standards like Global System for Mobile Communication (GSM), Wideband Code Division Multiple Access (WCDMA), Long Term Evolution (LTE) standards into a single mobile receiver makes it low power, small size and light in weight. The design of an efficient data converter that can handle the signal bandwidth associated with each wireless standard ranging from second generation (2G) to fifth generation (5G) will be a challenging task.

The scaling down of the CMOS technology improves chip density, reduces power consumption and increases the operating speed. In order to attain the benefits of scaling of CMOS technology, there is a persistent effort needed in developing ADCs that are compatible with low power, high speed digital circuits. Over the past several decades several architectural improvements occurred in the history of $\Sigma\Delta$ ADC and these developments makes it low power, high precision and hardware efficient. Initially $\Sigma\Delta$ ADCs were intended for the conversion of low to medium bandwidth applications, but the architectural advancements and the process technology scaling

helped this converter to emerge as a new category of converter named wideband ΣΔ ADC. ΣΔ ADCs are best suited for data conversion in low power wideband applications because of its robustness to non-idealities associated with analog circuit elements (Babita *et al.*, 2007). ΣΔ ADC consists of a ΣΔ modulator part and a digital decimation filter. The oversampling and noise shaping techniques helps the ΣΔM to achieve higher resolution (Schreier and Temes, 2005). An attractive solution to overcome the stability issues prevalent in single loop ΣΔ structure is to cascade many stable single loop ΣΔ modulators. The thesis explores the different discrete time (DT) cascaded ΣΔ modulator architectures for wideband applications.

1.1.1 Research Focus

The thesis focus on the design, analysis, modelling and simulation of advanced and more sophisticated cascaded ΣΔ modulators for wideband applications. Several effective methods are presented in the thesis to enhance the resolution of cascaded ΣΔ modulators as well as to make it low power and hardware efficient. The thesis also aims to introduce a novel bandpass Differential Quantizer based Error Feedback Modulator (DQEFM) Architecture.

1.2 Author's Contributions

The thesis initially proposes a MASH/SMASH ΣΔ architecture that attains a higher order noise shaping than the order of modulator using analog inter-stage feedback paths. An improved low-distortion MASH/SMASH ΣΔ modulator architecture that attains an enhancement in the resolution through techniques like resonation and NTF zero optimization have been designed and simulated. The mathematical analysis and circuit level simulation performed for a lowpass MASH DQEFM architecture shows that it is suitable for data conversion operation in 4G radios. A novel bandpass DQEFM (BP DQEFM) architecture and its cascaded implementation are designed

and simulated. The re-configurable MASH BP DQEFM performs data conversion operation for two wireless standards. This is followed by few suggestions for future work. The thesis is based on the following papers. [**C** represents International Conferences and **J** represents International Journals]

C1. Rijo Sebastian, Jos Prakash, Babita Roslind Jose, Shahana T.K, "A multi-mode MASH $\Sigma\Delta$ modulator for low power wideband applications", Sixth International Symposium on Embedded Computing and System Design (ISED), held at IIT, Patna, IEEE Xplore, pp. 87-90, December 2016, DOI: 10.1109/ISED.2016.7977060.
An extended version of **C1** has been published as
J1. Rijo Sebastian, Jos Prakash, Babita Roslind Jose, Shahana T.K "Multi-Stage Noise Shaping $\Sigma\Delta$ Modulator with Enhanced Noise Shaping for Low Power Wideband Applications", Journal of Low Power Electronics, Vol. 13, no. 4, pp.661-668(8), December 2017.

Author's Contribution: An effective method to enhance the resolution of cascaded $\Sigma\Delta$ modulators by utilizing analog inter-stage feedback paths is presented in this paper. A traditional feedforward MASH $\Sigma\Delta$ modulator along with this inter-stage feedback technique makes the modulator suitable for multi-mode operation. This re-configurable MASH 2-1 $\Sigma\Delta$ modulator achieves third, fourth and fifth order noise transfer function (NTF) in three different modes of operation. The mathematical analysis and behavioral simulations results obtained using MATLAB/SIMULINK prove the fitness of this architecture. The non-ideality analysis of the modulator and the circuit level feasibility of the proposed modulator using switched capacitor circuits is also presented.

J2. Rijo Sebastian, Babita Roslind Jose, Shahana T.K, Jimson Mathew, "A Low-distortion Hardware Efficient MASH $\Sigma\Delta$ Modulator with Enhanced Noise Shaping", Smart Science (Taylor and Francis), Vol. 6, Issue 2, pp.158-172, 2018, https://doi.org/ 10.1080/23080477.2017.1417962.

Author's Contribution: This paper presents an improved MASH $\Sigma\Delta$ modulator

architecture that can attain an enhanced noise shaping through resonation and noise transfer function (NTF) optimization. The elimination of the feedforward adder before the quantizer in the first stage and enhanced noise shaping without any increase in the number of active blocks makes this architecture hardware efficient. The shifted loop delay techniques introduced in this architecture helps to relax the signal processing timing issues in digital to analog conversion and dynamic element matching process. The low-distortion architecture utilized in both stages of MASH structure reduces the integrator associated non-idealities. The behavioral simulations and mathematical analysis performed for this architecture confirm the effectiveness of this proposed modulator.

C2. Rijo Sebastian, Jos Prakash, Babita Roslind Jose, Shahana T.K, Jimson Mathew "A lowpass MASH DQEFM for 4G wireless receivers", 7^{th} International Conference on Smart Computing and Communications (ICSCC 2019), held at Curtin University, Malaysia, during 28-30 June 2019.

Author's Contribution: The design and simulation of a lowpass MASH Differential Quantizer based Error Feedback Modulator (DQEFM) architecture suitable for data conversion in 4G wireless receivers is presented in this paper. The performance of the proposed modulator has been evaluated through circuit-level simulations using HSPICE. The power and Figure of Merit (FoM) obtained for this proposed LP MASH DQEFM architecture shows better performance when compared with the state-of-the-art $\Sigma\Delta$ architectures.

J3. Rijo Sebastian, Jos Prakash, Babita Roslind Jose, Jimson Mathew, "A Differentially Quantized Bandpass Error Feedback Modulator for ADCs in Digital Radio", Circuits, Systems, Signal Processing, Springer, Vol. 37, Issue 10, pp.41814199, October 2018, https://doi.org/10.1007/s00034-018-0782-z.

Author's Contribution: A novel differentially quantized bandpass (BP) analog-to-digital conversion technique for digital radio application is described in this paper. The BP DQEFM structure could replace the conventional bandpass modulator archi-

tecture and the integrator associated non-idealities, loop stability issues and optimization of the integrator scaling coefficients are no more a concern in BP DQEFM architecture. Behavioral-level simulation results demonstrate the mathematical equivalence of the BP DQEFM with the traditional BP $\Sigma\Delta$ modulator technique and confirm its novelty, theoretical stability. The circuit level simulation of the modulator has been performed using HSPICE. The low power operation of BP DQEFM is verified when simulated with a 45 nm CMOS technology using a supply voltage of 1 V.

J4. Rijo Sebastian, Jos Prakash, Babita Roslind Jose, Shahana T.K., Jimson Mathew, "A Re-configurable MASH 2-2 bandpass DQEFM for Multi-standard Applications", International Journal of Electronics- Taylor & Francis, vol. 106, issue. 10, pp 1498-1513, April 2019, https://doi.org/10.10 80/00207217.2019.1600737.

Author's Contribution: The design, analysis and implementation of a MASH BP modulator that employs a DQEFM structure is presented in this paper. The re-configurability, reduction of power-hungry active blocks and reduced sensitivity to circuit non-idealities makes this proposed bandpass modulator a suitable candidate for a digital intermediate frequency (IF) receiver system. The mathematical analysis and simulation results indicate the resemblance of the proposed modulator with the conventional $\Sigma\Delta$ modulator. The circuit level simulations shows better performance of the proposed modulator in terms of hardware complexity and power. The proposed cascaded modulator has been made re-configurable for Global System for Mobile communications (GSM) and Wideband Code Division Multiple Access (WCDMA) standards. The circuit level simulation of the proposed bandpass architecture were performed and the FoM is compared with the state-of-the-art BP $\Sigma\Delta$ architectures.

1.2.1 Contributions not Included in the Thesis

C3. Rijo Sebastian, Babita Roslind Jose, Shahana T.K., Jimson Mathew, "GA based Optimization of Second Order $\Sigma\Delta$ Modulator for Digital Hearing Aid Ap-

plications", Fourth International Conference on Ecofriendly Computing and Communication Systems (ICECCS), National Institute of Technology, Kurukshetra, 7-8 December 2015, Elsevier Procedia Computer Science, vol. 70, 2015, pp. 274 281, doi: 10.1016/j.procs. 2015.10.088.

Author's Contribution: This paper describes the design and simulation of a $\Sigma\Delta$ architecture that can be used in digital hearing aid applications. A second order feedforward $\Sigma\Delta$ Modulator considering all the non-ideal effects, was chosen for the hearing aid application. The loop coefficients of this architecture are optimized using Genetic Algorithm. The architecture together with optimized coefficients achieves SNDR and a dynamic range above 90 dB. A lower sampling frequency and a low order modulator makes this architecture less complex and power efficient.

C4. Rijo Sebastian, Babita Roslind Jose, Shahana T.K., Jimson Mathew, "An Optimized High Resolution $\Sigma\Delta$ Modulator for Digital Hearing Aid Applications", IEEE International Workshop on Recent Advances in Computing and Communications (IWACC-2015), September 2015, pp. 144-147, ISBN-93-392-2412-4.

Author's Contribution: This paper describes the design and simulation of a multibit $\Sigma\Delta$ modulator architecture that can be used in digital hearing aid applications. A low-distortion second order $\Sigma\Delta$ modulator was chosen for getting low power operation. The various non-ideal effects occurring in $\Sigma\Delta$ implementation were modelled and simulated using MATLAB/SIMULINK. The coefficients used in this architecture were optimized using Genetic Algorithm. The architecture together with optimized coefficient values improves the SNR and dynamic range.

1.3 Thesis Outline

Chapter 2 presents a detailed review of literatures and background information. The thesis commences with the ADC fundamentals, types, and an overview of the $\Sigma\Delta$ Modulator, which is the integral part of $\Sigma\Delta$ ADC. The concepts of $\Sigma\Delta$ Modulator,

main classification of $\Sigma\Delta$ architectures and various important works that has been published in the literature are also discussed in the beginning of the thesis. The thesis focuses on the architectural level exploration of various discrete time cascaded $\Sigma\Delta$ Modulators to be used in wideband applications.

Chapter 3 presents a method to enhance the resolution of cascaded $\Sigma\Delta$ modulators intended for wideband applications. Analog feedback paths are introduced between the cascaded stages. This inter-stage feedback path contributes to an increase in the order of noise shaping, which in turn enhances the resolution of the modulator. This technique can be adopted for Multi stAge noise SHaping (MASH) and Sturdy MASH (SMASH) structures for improving the Signal to Noise Ratio (SNR). Mathematical analysis and behavioral simulation results obtained for both MASH and SMASH architectures prove the fitness of these architectures.

An improved low-distortion MASH/SMASH $\Sigma\Delta$ modulator architecture that attains an enhancement in the resolution through techniques like resonation and NTF zero optimization are presented in **Chapter 4**. The improved low-distortion architecture eliminates the feedforward adder before the quantizer in the first stage of MASH/ SMASH structure. The enhancement in noise shaping is achieved without any additional active components makes this architecture hardware efficient. The shifted loop delay techniques utilized in this architecture helps to relax the signal processing timing issues in the critical path of the modulator. The utilization of low-distortion architecture, selection of low OSR, fewer number of active blocks and achievement of fourth order noise shaping makes this modulator suitable for low power wideband applications.

In **Chapter 5**, the design and simulation of a lowpass MASH Differential Quantizer based Error Feedback Modulator (DQEFM) architecture is presented. The DQEFM structure has been incorporated for obtaining benefits like relaxed op-amp requirements and reduced sensitivity to mismatch effects. The lower operating frequency and better performance of the proposed modulator in terms of hardware complex-

ity and power makes it suitable for data conversion in 4G wireless receivers. The performance of the proposed modulator has also been evaluated through circuit-level simulations using HSPICE.

Chapter 6 proposes a novel bandpass DQEFM (BP DQEFM) architecture and its cascaded implementation. The mathematical analysis and simulation results indicate the resemblance of the proposed BP DQEFM with the conventional $\Sigma\Delta$M. The circuit level simulations of the second order BP DQEFM for a digital radio application indicate the better performance of the proposed BP DQEFM in terms of hardware complexity and power. A re-configurable cascaded BP DQEFM architecture has been designed for data conversion operation in Global System for Mobile communications (GSM)/Wideband Code Division Multiple Access (WCDMA) applications. The circuit level simulations of the MASH BP DQEFM has been performed for a bandwidth of 200 kHz for GSM and bandwidth of 5 MHz for WCDMA.

Chapter 7 provides the summary of the research work presented in this thesis.

CHAPTER 2

BACKGROUND AND LITERATURE REVIEW

2.1 Introduction

Analog to Digital Converter (ADC) is a device which transforms an analog signal to digital domain. This digital representation can be easily processed by a computer, transmitted or stored. ADCs are widely used in a variety of fields such as communication systems (Mirzaie *et al.*, 2018; Grzing *et al.*, 2013), consumer electronics (Morisson, 1995), industrial measurements (Bertl, 1994), software defined radio (SDR) (Tanaka *et al.*, 2011), medical equipments (D'Urbino *et al.*, 2017) etc. The performance of an ADC can be measured by parameters like resolution, accuracy and precision. The other desirable features needed for an ADC includes low power consumption, light in weight and high speed of operation.

2.2 ADC Fundamentals

ADC act as key element in modern electronic systems. It converts the continuous amplitude, continuous time analog signals into digital signals, which are discrete in amplitude and discrete in time (Maloberti, 2007). The fundamental operations associated with an analog to digital conversion are sampling, quantization and coding as shown in Figure 2.1 (Libin *et al.*, 2006). The first operation in an ADC is the

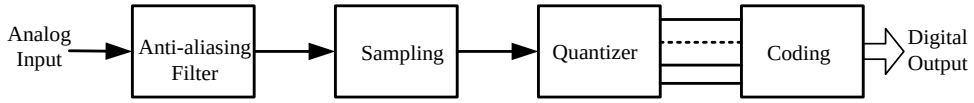


Figure 2.1: Block diagram of ADC

discretization of a continuously varying analog signal in time using Sample and Hold (S/H) circuits and the function of quantizer is to discretize the sampled signal in amplitude. The anti-aliasing filter removes the unwanted signals that may alias into the signal bandwidth and the coder provides a unique digital code to each quantized amplitude. An error is often associated with every quantization process, known by the name quantization error (e_q). It is defined as the discrepancy between the quantized and true value of the sampled data. The smaller the quantization error, better will be the resolution of the ADC. If V_{ref} is the full-scale amplitude of the analog signal and '*n*' is the number of bits assigned to each amplitude value, then the quantization step is given by $\Delta = V_{ref}/2^n$. The quantization error is bounded by the step size 'Δ', which is the least significant bit (LSB) of an ADC and the quantization error lies between $\pm\Delta/2$ (Norsworthy *et al.*, 1997).

$$\frac{-\Delta}{2} \leq e_q \leq \frac{+\Delta}{2} \tag{2.1}$$

Assuming the quantization error is uniformly distributed between $\pm\Delta/2$, the rms value of quantization noise is given in Equation 2.2,

$$e_q = \frac{\Delta}{\sqrt{12}} \tag{2.2}$$

The quantization error is dependent on the resolution of the ADC and it is often referred to as the quantization noise of an ADC. The quantization errors can often be seen as white noise. For Nyquist rate ADCs that performs sampling operation according to the Nyquist criteria, the quantization noise will be uniformly distributed within the band ranging from 0 (dc) to $F_s/2$ (where F_s is the sampling frequency) as shown in Figure 2.2. The quantizer is a non-linear device, the best way to do the analysis of a non-linear system is to make it linear and do the analysis. So the linear model of a quantizer is represented as shown in Figure 2.3. The quantizer is modelled as an additive noise source. For an *n*-bit ADC, the expression to find the peak signal

to noise ratio (SNR_p) for a sinusoidal input signal is given in Equation 2.3.

$$SNR_p = 6.02n + 1.76dB \tag{2.3}$$

The non-ideal effects, imperfections associated with manufacturing, design issues

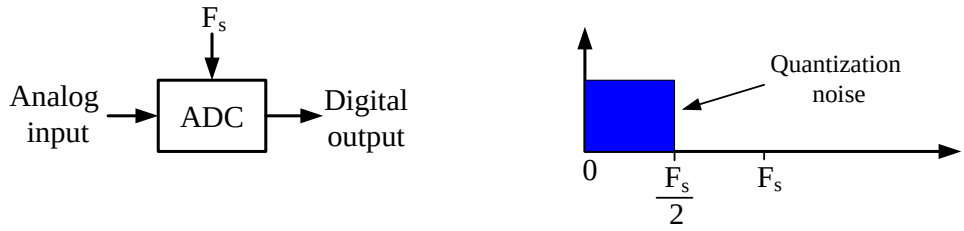


Figure 2.2: Nyquist rate ADC -distribution of quantization noise in frequency domain

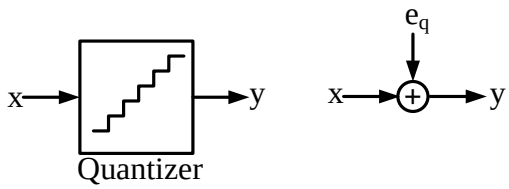


Figure 2.3: Linear model of a quantizer

etc will cause reduction in the theoretical resolution of ADC. The actual or effective number of bits (ENOB) can be calculated by the following expression

$$ENOB = \frac{SNR_{dB} - 1.76}{6.02} \tag{2.4}$$

2.3 Performance evaluation of ADCs

The performance of various ADC architectures are measured and compared usually with the following parameters.

- Resolution

- Signal to Noise Ratio (SNR)
- Signal to Noise and Distortion Ratio (SNDR)
- Spurious Free Dynamic Range (SFDR)
- Effective Number of Bits (ENOB)
- Effective Resolution Bandwidth (ERBW)
- Dynamic Range (DR)
- Power Dissipation and
- Total Harmonic Distortion (THD)

The resolution of an ADC is defined as the smallest incremental voltage that can be recognized and thus causes a change in the digital output. It is expressed as the number of bits output by the ADC. The SNR of a converter is defined as the ratio of signal power divided by the total noise integrated over the signal bandwidth. When the integrated noise power includes harmonic distortion, then we often speak of SNDR. The SFDR is the difference in power between the test signal and the largest nonsignal peak in the spectrum. The THD is the ratio between the power in all the harmonic components and the signal power. In oversampled systems only the harmonic power in the band of interest is included in the calculation. The most often used performance indicators are the SNR, SNDR, SFDR and THD.

The DR of the converter is defined as the maximum value of the linearly extrapolated SNR/SNDR-curves up to the full-scale value. The SNR performance of an ADC depends on the signal frequency 'f' with F_s as a parameter. SNR decreases as signal frequency increases. The value of 'f' at which the SNR decreases to 3 dB below the low frequency value is the effective resolution bandwidth (ERBW). ERBW implies the range of frequencies over which the converter may be used.

The accuracy and precision are the two important parameters denoting the quality of conversion. The performance parameters like resolution, power dissipation and rate of conversion associated with an analog to digital converter are usually considered

for finding the Figure of merit (FoM). FoM is a numerical quantity based on one or more characteristics of a system. It combines several performance metrics into a single number. The expression for two popular FoM found in the literature are as follows:

The figure of merit proposed by Walden (Walden, 1999), also denoted as FoM_w is given by,

$$FoM_w = \frac{P_d}{2^{ENOB}.F_s}[Joule/Conversion - step] \tag{2.5}$$

where P_d is the power dissipation, F_s is the sampling frequency and ENOB is the effective number of bits respectively.

The figure of merit proposed by Schreier, also denoted as FoM_s is given by,

$$FoM_s = SNDR + 10log\frac{F_s/2}{P_d}[dB] \tag{2.6}$$

Walden FoM describes the energy required for conversion and is preferred for low resolution converters while Schreier FoM works better for higher dynamic range designs.

2.4 ADC Performance Over Time

Over the past several decades, several architectural and immense technological improvements occurred in the history of ADC. The developments occurred through out these years makes it low power, high precision and hardware efficient. The performance of various ADCs found in the literature during the last 20 years (year 2000-2019) is shown in Figure 2.4. The FoM proposed by Walden is plotted against the Fs-nyq, which is the Nyquist sampling rate, equal to the sampling rate (Fs) divided by the oversampling ratio (OSR). Since the FoM is expressed in fJ/conversion-step, the ADCs with the lowest FoM_w consumes the least energy for the conversion. It can be seen from Figure 2.4 that there is a tremendous decrease in FoM_w value during the past 4 years.

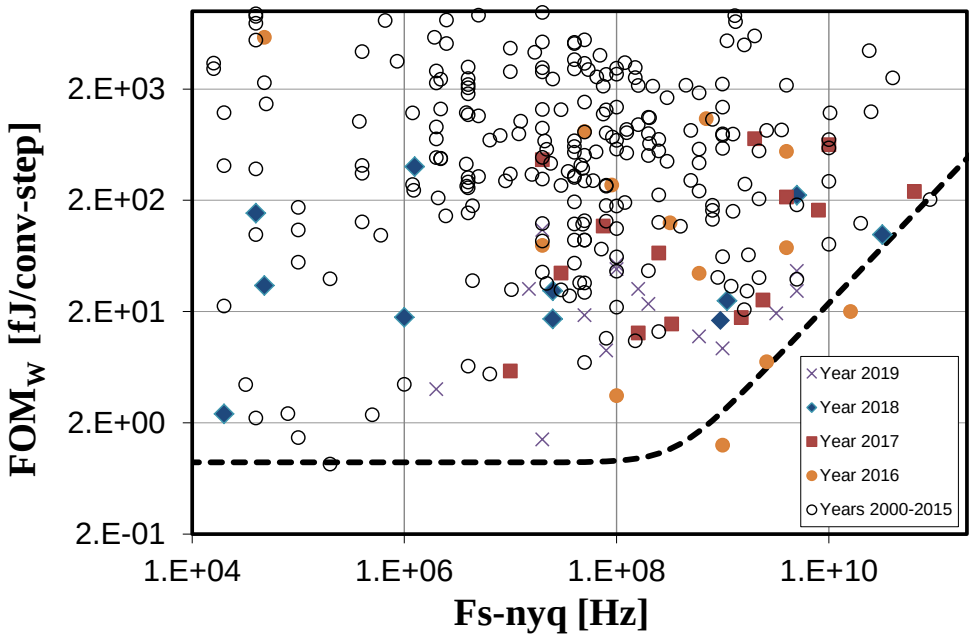


Figure 2.4: Walden's FoM vs Nyquist sampling rate of wide range of ADCs in research papers from 2000 to 2019

2.5 Classification of ADCs

ADCs are divided into two broad categories in general: Nyquist rate converters and Oversampling converters.

2.5.1 Nyquist Rate Converters

Nyquist rate converters operate at the minimum sampling frequency required to capture all the information about the entire input bandwidth. Nyquist rate converters are defined to be converters that sample the analog signal at the Nyquist rate. The sampling frequency, F_s=2F_b, where 2F_b is the Nyquist rate and F_b is the signal bandwidth. Nyquist rate converters are fast but their resolution is usually limited to 10 -12 bits. Three of the most popular Nyquist rate converters are

- Successive Approximation Register (SAR) ADC

- Flash ADC and
- Pipeline ADC

2.5.2 Oversampling Converters

In oversampling converters, the sampling frequency is much greater than the Nyquist rate of the input signal bandwidth. The sampling frequency in oversampling converters is, F_s = K.2F_b, where K is the oversampling ratio (OSR). The OSR is the ratio of sampling rate to the nyquist rate (K= F_s/2F_b). Oversampling reduces the inband quantization error, so that this converter can achieve higher resolution than Nyquist rate converters. The anti-alising filter (AAF) design is much relaxed in the case of oversampling ADCs. Two types of such ADCs are oversampling ADCs and Sigma Delta ($\Sigma\Delta$) ADCs. In addition to oversampling, $\Sigma\Delta$ ADC uses noise shaping concept to achieve higher resolution.

2.6 Sigma Delta ADC Architectures

The concept of sigma delta ($\Sigma\Delta$) modulation derived initially from pulse transmission techniques like pulse code modulation (PCM) and delta modulation (DM). The history of oversampled and noise shaped converters begins when C.C. Cutler of Bell laboratory filed a US patent in the year 1954 describing transmission systems employing quantization (Cutler, 1954). His objective was to transmit the oversampled and noise shaped signal without reducing the data rate. In the year 1961, C. B. Brahm introduced a second order oversampling noise shaping ADC through the US patent named feedback integrating system (Brahm, 1961). The term delta sigma was first introduced in the year 1962 by H. Inose et.al while illustrating an experimental telemetering system employing delta sigma modulation (Inose *et al.*, 1962). $\Sigma\Delta$ ADC is able to provide high quality analog to digital conversion with simple, inexpensive and low precision components (Candy, 1974). Initially, $\Sigma\Delta$ ADC was considered a

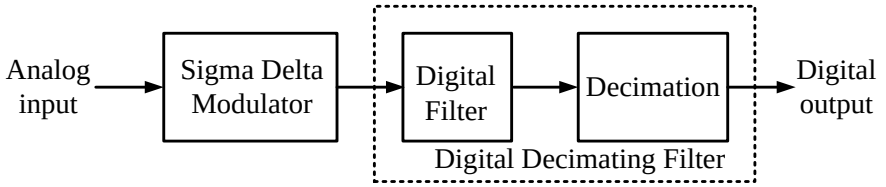


Figure 2.5: Block diagram of Sigma Delta ADC

converter of choice for low to medium bandwidth applications. The advent of CMOS technology and architectural improvements made $\Sigma\Delta$ ADC a suitable candidate for wideband applications.

Figure 2.5 shows the general block diagram of a $\Sigma\Delta$ ADC. It consists of a $\Sigma\Delta$ modulator part and a digital decimation filter. $\Sigma\Delta$ ADC is a mixed signal integrated circuit in which the modulator part is implemented in analog domain followed by the digital implementation of decimation filter. The digital lowpass filter is used to remove the quantization noise beyond the band of interest and the oversampled output data rate is made low through decimation process. The $\Sigma\Delta$ modulator is also implemented with simple electronic components like integrator, comparator, switch, voltage reference and analog summing circuit. The block diagram of a $\Sigma\Delta$ modulator is shown in Figure 2.6.

The basic principle of operation for a $\Sigma\Delta$ modulator is to enclose a simple quantizer in a feedback loop to shape the quantization noise such that most of the noise is shifted out of the band of interest, where it can later be suppressed by filtering. The output of $\Sigma\Delta$ modulator is a pulse density modulated waveform. The integrator acts

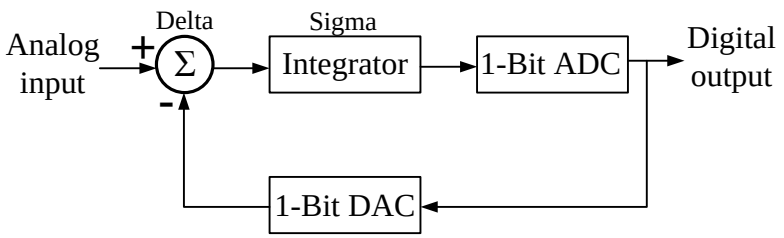


Figure 2.6: Block diagram of Sigma Delta Modulator

as a loop filter for lowpass ΣΔ modulator. The resonator functions as a loop filter for bandpass ΣΔ modulator.

2.6.1 Oversampling and Noise Shaping Concepts

ΣΔ modulator functions with two signal processing techniques namely, oversampling and noise shaping. ΣΔ modulator usually works with a high sampling frequency, samples at a rate very much higher than nyquist rate. The oversampling ratio (OSR) is usually denoted by 'K', expressed as K=F_s/2F_b, where F_b is the signal bandwidth. 'K' may take values ranging from 4 to 256. The concept of oversampling and how it improves resolution can be easily understood from the Figure 2.7. Consider an ADC, which is sampling at a rate KF_s. The factor K is generally referred to as the OSR. The rms value of the quantization noise remains the same ($\Delta/\sqrt{12}$), but the quantization noise is now distributed over a wider range from 0 to KF_s/2. The output of the modulator is given to a digital low pass filter, which removes the quantization noise beyond F_s/2, but it does not affect the signal content and the inband quantization noise also get reduced because of oversampling. Thus the inband noise power decreases and the SNR and ENOB are improved. A major advantage of ΣΔ ADC is that high resolution analog to digital conversion is achieved with a low resolution ADC. It should also be noted that oversampling relaxes the requirements on the analog anti-aliasing filter. This is another significant advantage of ΣΔ ADC.

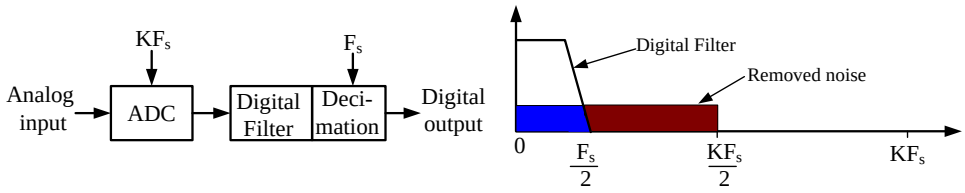


Figure 2.7: ADC-oversampling, digital filter and decimation

The ΣΔ modulator shown in Figure 2.8 performs the sampling operation at a rate KF_s and the oversampling process distributes the entire quantization noise over a

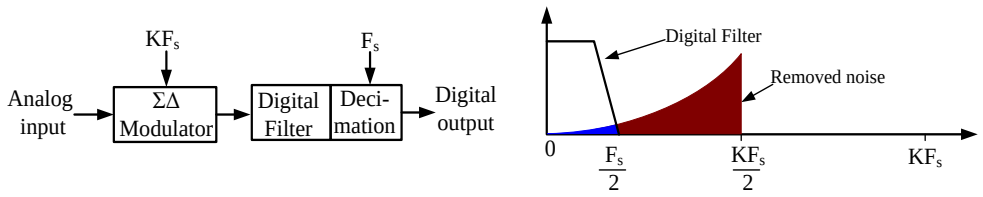


Figure 2.8: ΣΔ ADC-oversampling, noise shaping, digital filter and decimation

range from 0 to KF_s/2. The noise shaping property of the ΣΔ loop shifts the inband quantization noise to out of band, which can be seen in Figure 2.8. The analog loop filter in ΣΔ modulator has a lowpass effect on the signal and highpass effect on the quantization noise. The output of the ΣΔ modulator is applied to a digital filtering, which eliminates the shaped quantization noise beyond F_s/2. The decimation process reduces the output data rate back to the nyquist rate. The quantization noise in the band of interest in the oversampled and noise shaped converter is further reduced when compared against a converter that works with oversampling principle alone.

2.7 Taxonomy of ΣΔ Modulators

The following sections describe the main classifications and the architectural advancements occurred in the history of ΣΔ modulator.

2.7.1 Discrete time, Continuous time and hybrid ΣΔ Modulators

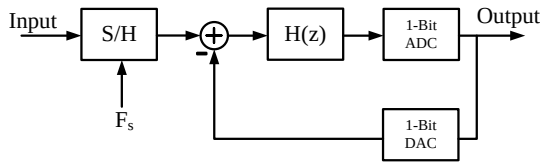
Depending on the circuit nature of analog loop filter, ΣΔM are classified into Discrete Time (DT) and Continuous Time (CT) ΣΔM. The block diagram of DT and CT ΣΔM is shown in Figure 2.9. The following are the main differences between discrete time ΣΔ modulator (DT ΣΔM) and continuous time ΣΔ modulator (CT ΣΔM):

- A DT ΣΔM uses DT integrators rather than CT integrators. The DT implementation of ΣΔM is usually done with Switched Capacitor (SC) circuits, where as CT ΣΔM employs continuous time circuits, often Resistor Capacitor (RC) or Transconductance-Capacitor (Gm-C) integrators.

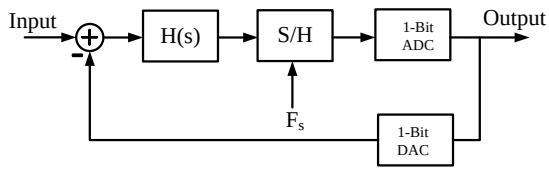
- The sampling operation in DT ΣΔM occurs at the input of ADC, where as in CT operation the sampling operation takes place at the output of the loop filter, before the quantizer.

- CT ΣΔM have implicit anti-aliasing property (Keller *et al.*, 2007) and they operate at high frequency with relatively low power. Even though CT implementation offer these features, they are very sensitive towards circuit non-idealities like circuit mismatch, Excess Loop Delay (ELD) and clock jitter (Ortmanns and Gerfers, 2006). The majority of ΣΔMs are implemented with DT circuits because they offer high precision and accuracy.

The loop filter coefficients can be varied easily by adjusting the capacitor ratios in DT implementation. The use of source-follower-based integrators in the DT implemen-



(a) Discrete time ΣΔM



(b) Continuous time ΣΔM

Figure 2.9: ΣΔ Modulator (a) Discrete time (b) Continuous time

tation of a sturdy multi-stage noise shaping (SMASH) $\Sigma\Delta$M increases the speed of operation (Kwak *et al.*, 2018). Improvement in SNDR can be obtained by optimizing the NTF, which is having a high pass filter characteristics (Kidambi, 2019). One method to reduce power consumption and to achieve power effectiveness is to realize the SC integrator function with low gain amplifier and passive SC circuits (Hussain *et al.*, 2017). The concept of multi-rate op-amp sharing scheme (Qi *et al.*, 2017) in the DT MASH modulator implementation enhances the resolution and helps in optimizing the power efficiency in active blocks. Multi-path architectures with cross coupling (Feng *et al.*, 2018; Fiore *et al.*, 2006) in DT implementation offers several advantages like low power consumption, high sampling rate and high SNR value.

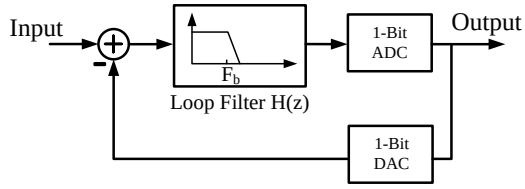
The CT implementation is extended to both lowpass and bandpass $\Sigma\Delta$Ms. The low power operation, higher operating frequency along with anti-aliasing feature makes this CT $\Sigma\Delta$Ms appropriate for applications such as medical equipments like ultrasound (Kaald *et al.*, 2017), communication devices (Zhang *et al.*, 2017), instrumentation (Huang *et al.*, 2016) etc. CT $\Sigma\Delta$Ms suffer from Excess Loop Delay (ELD) (Cherry and Snelgrove, 1999*b*) and many methods were suggested in the literature how to compensate for this ELD effects (Gao *et al.*, 1997; Pavan, 2008). The performance of CT $\Sigma\Delta$M is also limited by clock jitter and quantizer metastability (Cherry and Snelgrove, 1999*a*).

The hybrid $\Sigma\Delta$M is a combination of both DT $\Sigma\Delta$M and CT $\Sigma\Delta$M, in which some parts of modulator are implemented using DT circuits and remaining parts with CT circuits. In hybrid $\Sigma\Delta$M, the front-end stage is usually implemented with CT circuits, and the remaining back-end stages are realized using switched-capacitor circuits (Garcia-Sanchez and de la Rosa, 2012). This offers advantages such as low power consumption (Kulchycki *et al.*, 2008), reduced sensitivity to circuit non-ideal effects, fast operation and embedded anti-aliasing filter (Keller *et al.*, 2007).

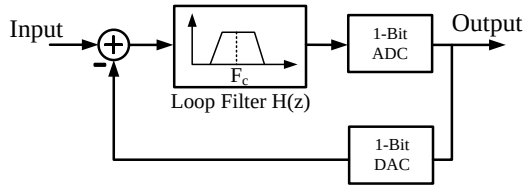
2.7.2 Lowpass and Bandpass ΣΔ Modulators

The main classsification of ΣΔM based on the nature of signals being handled is the lowpass and bandpass ΣΔM. The passband of lowpass (LP) ΣΔM is around DC, where as for the bandpass (BP) ΣΔM it is not near DC. Figure 2.10 shows the LP and BP ΣΔM. The loop filter of lowpass ΣΔM is built with integrators and resonators are used for building the bandpass loop filter.

LP ΣΔM can be built with DT (Silva *et al.*, 2001) or CT (Ke *et al.*, 2010; Baltolu *et al.*, 2018) circuits. LP ΣΔ ADC is able to provide the highest resolution among other ADCs especially in low to medium bandwidth applications. LP ΣΔ ADCs are widely used in audio bands(Shim *et al.*, 2014; Felding *et al.*, 2016; Baltolu *et al.*, 2018). Recently, LP ΣΔM are getting increased attention in low power wideband applications (A.Hamoui and Martin, 2004; Lee *et al.*, 2009). LP ΣΔM used for conversion up to a 20 MHz signal bandwidth have been reported in the literature (Ke *et al.*, 2010; Christen and Huang, 2010; Li *et al.*, 2013). LP ΣΔ ADC also can be implemented using only oscillators and digital circuitry, without operational amplifiers nor other highly linear circuits (Cardes *et al.*, 2018). The re-configurabile LP ΣΔM are extensively used for handling multiple wireless communication standards (Chris-



(a) Lowpass ΣΔM



(b) Bandpass ΣΔM

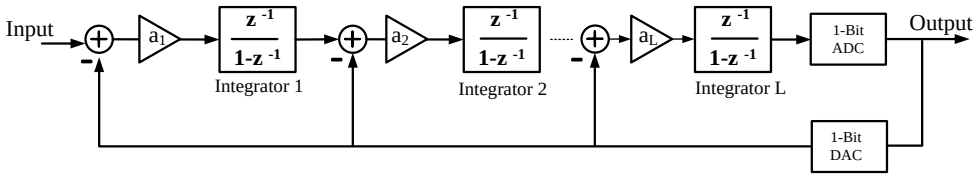
Figure 2.10: ΣΔM (a) Lowpass (b) Bandpass

ten and Huang, 2010; Bettini *et al.*, 2015). The local and global resonation strategies implemented with inter-stage feedback paths and NTF optimization are helpful for attaining an enhanced resolution in low power broadband applications (A.Morgado *et al.*, 2008; Beheshte and Yavari, 2017)

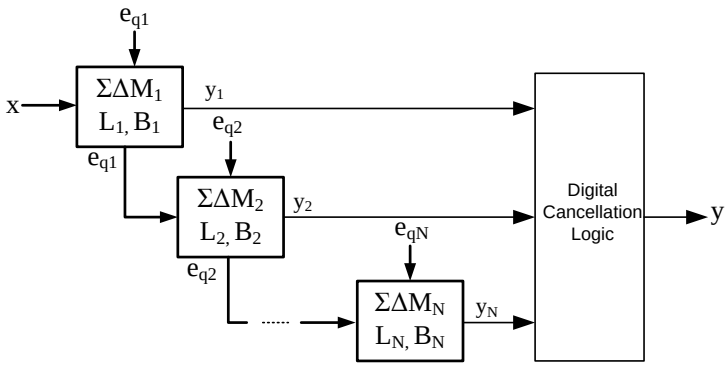
The $\Sigma\Delta$ modulation technique initially used for low frequency signals has also been extended to digitize relatively narrowband signals and the first bandpass (BP) version of $\Sigma\Delta$ modulation was proposed by Schreier and Snelgrove (Schreier and Snelgrove, 1989). In bandpass $\Sigma\Delta$M, the quantization noise has to be small only in the band of interest, oversampling reduces the quantization noise within the band and noise shaping further reduces noise within the band. The bandpass $\Sigma\Delta$M (BP $\Sigma\Delta$M) is capable to provide high resolution at higher frequencies for a bandlimited input, and finds application mainly in digital radio receivers (Keady and Lyden, 1998). The noise shaped out-of-band signals in BP $\Sigma\Delta$M can effectively be attenuated by a post digital BP filter. Thus BP $\Sigma\Delta$ ADCs offer high resolution conversion of a narrow frequency band and strong rejection of out-of-band signals (Keady and Lyden, 1995). A remarkable feature of BP $\Sigma\Delta$M is its ability to handle multi-standard signal bandwidths in different modes through re-configurability (Ho *et al.*, 2011). A wide tuning range can be attained by adopting a time-interleaving scheme for BP $\Sigma\Delta$M (Jiang *et al.*, 2017).

2.7.3 Single Loop and Cascaded $\Sigma\Delta$ Modulators

The simplest form of a $\Sigma\Delta$M is a single-stage structure consisting of a loop filter, quantizer and a feedback path employing a DAC. An L^{th} order single loop $\Sigma\Delta$M is shown in Figure 2.11(a). Generally, an L^{th} order $\Sigma\Delta$M contains 'L'number of integrators and the noise transfer function (NTF) is expressed as $NTF(z) = (1 - z^{-1})^L$. When the order of modulator goes beyond two in a traditional single loop structure, it is at a greater risk of instability due to the delays associated with the multiple feedback paths. The loop coefficients incorporated for better stability also



(a) L^{th} order Single loop ΣΔM



(b) L^{th} order Cascaded ΣΔM

Figure 2.11: Block diagram of (a) Single loop ΣΔM (b) Cascaded ΣΔM

needs to be optimized in a single loop structure, which limits the gain of integrators and ultimately the resolution of the modulator. Stability is an important concern while designing higher order single loop modulators, increasing the modulator's NTFs out-of-band gain enhances its resolution at the cost of degradation of its stability (Yavari and Shoaei, 2004).

The single loop ΣΔM can utilize either single-bit or multi-bit quantizer (Meng *et al.*, 2014). Multi-bit quanizer in the loop offers better stability and enhanced resolution. Some cascaded ΣΔM found in literature incorporates a single-bit quantizer in the first stage and a multi-bit quantizer in the second stage (Chiang *et al.*, 2002), thus minimizing the DAC mismatch effects associated with the first stage. The two popular topologies used in single-loop structure are feedback (FB) and feedforward (FF) topology (Silva *et al.*, 2001).

An attractive solution to overcome the stability issues prevalent in single loop structure is to cascade many stable single loop modulators. The cascaded or MASH ΣΔ

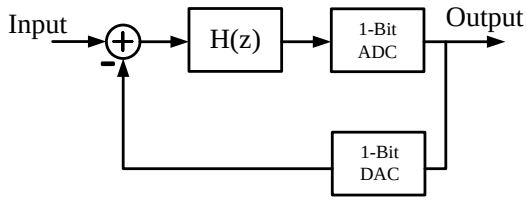
structure uses a combination of several low order modulators to achieve the required modulator order without any stability issues. Figure 2.11(b) shows an L^{th} order cascaded $\Sigma\Delta$M. In cascaded/MASH architecture, the quantization noise of the each modulator is extracted and provided as an input to the subsequent stage. The digital output of all stages of cascaded structure is given to the Digital Cancellation Logic (DCL). An appropriate digital noise cancellation logic cancels the quantization noise of all previous stages except the last stage. The last stage quantization noise is shaped by an NTF of order equal to the sum of all the orders. The cascaded structure provides the advantages like inherent stability, higher dynamic range and higher overload input level when compared with the single loop approach. The MASH structure contains analog and digital circuits. Mismatch between the analog and digital filters may lead to quantization error leakage, which in turn causes a reduction in SNR value. This need for matching between the analog and digital filters in MASH structure necessitate high accuracy active elements. The cascaded or MASH structure need high DC gain operational amplifiers (op-amps) for the implementation of integrators to avoid the quantization noise leakage.

The Sturdy MASH (SMASH) (Maghari *et al.*, 2006) architecture is similar in operation when compared with MASH, but it doesn't require digital noise cancellation filters. The matching between analog and digital elements is no more a concern in SMASH modulators. In SMASH structure, the second stage output is directly subtracted inside the first stage loop in the digital domain. This will provide an additional noise shaping for the first stage quantization noise.

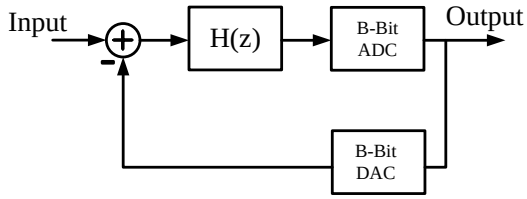
2.7.4 Single-bit and Multi-bit Quantizer in $\Sigma\Delta$ Modulator Loop

$\Sigma\Delta$M can use a single-bit or multi-bit quantizer in the loop as shown in Figure 2.12. The intrinsic linearity of the single-bit quantizer and a single-bit Digital to Analog Converter (DAC) motivated many researchers to design a $\Sigma\Delta$M with 1-bit quantizer. By employing a multi-bit quantizer, the SNR attained by a $\Sigma\Delta$M can be increased

significantly. The SNR value increases by 6 dB for each additional bit in the quantizer. The loop coefficients or scaling coefficients introduced to stabilize the $\Sigma\Delta$M loop, degrades the SNR. The larger the loop coefficients, greater is the risk to get instability in the case of single-bit $\Sigma\Delta$M. The loop coefficient values can be enlarged and the loop stability also improves by employing a multi-bit quantizer in the $\Sigma\Delta$ loop. The use of multi-bit quantizer demands a multi-bit DAC, where the linearity of the converter depends on the linearity of the multi-bit DAC in the feedback loop (Libin *et al.*, 2006). The output of DAC in the feedback loop is directly connected to the input, so any non-linearity associated with the multi-bit DAC cannot be distinguished from the input signal. The DAC mismatch errors in the feedback loop cause distortion (Park *et al.*, 2003), which affect the performance of the modulator. The linearity of multi-bit DAC in the feedback path can be increased by methods such as Dynamic Element Matching (DEM)(Jensen and Jensen, 1999), digital correction (Fornasari *et al.*, 2005) and digital correction technique combined with Data Weighted Averaging (DWA) algorithm (Pakniat and Yavari, 2010). ADCs designed for wideband applications have limitations in choosing a higher value for oversampling ratio (OSR) due to technology constraints. An effective solution to increase



(a) Single-bit $\Sigma\Delta$M



(b) Multi-bit $\Sigma\Delta$M

Figure 2.12: $\Sigma\Delta$M (a) Single-bit (b) Multi-bit

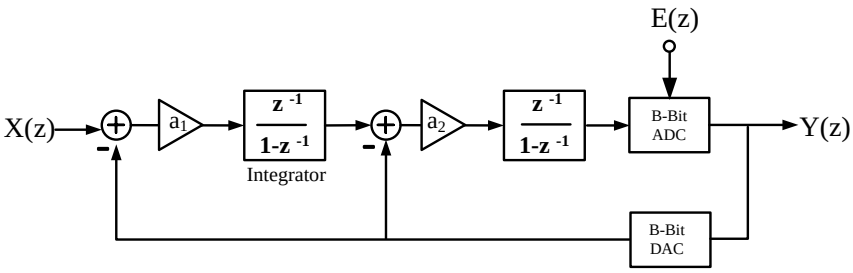
the resolution in wideband scenario is to employ a multi-bit quantizer (Bettini *et al.*, 2015; Li *et al.*, 2013; Kwak *et al.*, 2018) along with a suitable DAC linearization technique.

2.7.5 Feedback and Feedforward Topologies in $\Sigma\Delta$ Modulators

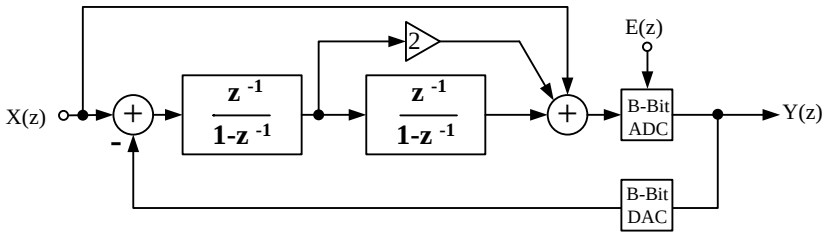
The two main topologies used for $\Sigma\Delta$M implementation are the feedback (FB) and feedforward (FF) topology. Figure 2.13(a) and 2.13(b) shows a second order $\Sigma\Delta$M with FB and FF topology respectively.

In FB topology, the integrator output contains a significant amount of input signal and shaped quantization noise, this makes the integrator output swing more, which inturn increases the power consumption of the modulator. The cascade of integrators with distributed feedback (CIFB)(Schreier and Temes, 2005) act as a building block of other complex structures, to realize single loop topologies. Eventhough, the integrator output swing and the number of feedback DACs are more in FB topology, it is having advantages like the timing requirements are not critical. If we employ a single-bit modulator, the complexities of the feedback DACs are greatly reduced. Therefore, CIFB is still an alternate method in recent designs (Yaghoubi *et al.*, 2016; Zanbaghi *et al.*, 2012). The output of last integrator is given as the input to the quantizer in CIFB topology, so no separate adder is required at the input of quantizer. In the case of non-idealities, FF architecture performs better than FB topology. The CIFB modulator with direct input feedforward path (Liu *et al.*, 2012) is an attractive solution to overcome the limitations associated with CIFB topology.

In FF topology, there is a direct FF path from input to the internal quantizer. So the loop filter contains no longer the input signal but only the shaped quantization noise. Since the loop filter process only the quantization noise, its linearity requirement can be significantly relaxed (Shen *et al.*, 2010). Another advantage is the reduced integrator output swing, which reduces the modulator power consumption. The signal



(a) Feedback ΣΔM



(b) Feedforward ΣΔM

Figure 2.13: ΣΔM (a) Feedback topology (b) Feedforward topology

transfer function (STF) is unity for FF topology, but it requires an analog FF adder at the input of quantizer. The sensitivity to op-amp nonlinearities are less in FF topology, so this topology is also known by the name low-distortion topology (Silva *et al.*, 2001). In addition to reduced sensitivity to opamp nonlinearities, the low-distortion topology has the following advantages (Silva *et al.*, 2004):

- Lower area and power consumption in multibit implementations
- Improved input signal range
- Only one DAC in feedback path
- Simplified MASH architectures

The input-feedforward path imposes a timing constraint that complicates its implementation, especially for high-speed multi-bit modulators (Gharbiya and Johns, 2006). The shifted loop delays in low-distortion topology (Meng *et al.*, 2014) can relax the critical timing for quantization and DEM by shifting the loop delay from the last integrator to the feedback path.

2.7.6 Multi-standard $\Sigma\Delta$ Modulators

The demand for single-chip solution for multi-standard requirements in wireless systems necessitates ADCs which are reconfigurable. $\Sigma\Delta$M can be made re-configurable so that the same modulator architecture can be used for different standards of operation. This multi-mode operation of the same modulator architecture reduces power and cost, at the expense of increased circuit complexity. In recent years, the observed trend has been towards the convergence of many standards of operation into a single mobile device, such as a smart phone. The convergence of various wireless communication standards like Global System for Mobile Communication (GSM), Wideband Code Division Multiple Access (WCDMA), Long Term Evolution (LTE) standards into a single receiver makes the receiver device size smaller and light in weight.

The majority of the multi-standard ADCs reported in the literature uses the $\Sigma\Delta$ Modulation scheme (Morgado *et al.*, 2007). The ADCs designed for the multi-standard purpose should be linear with low power consumption. Several Discrete Time (DT) and Continuous Time (CT) implementation of a re-configurable $\Sigma\Delta$ architecture with signal bandwidth ranging from 100 KHz to 20 MHz are reported in the literature (Burger and Huang, 2001; Christen and Huang, 2010; Bettini *et al.*, 2015; Grassi *et al.*, 2016). The re-configurability is implemented mainly in the architectural level inorder to achieve the required performance in each standard.

Today's fourth generation (4G) mobile devices have been providing backward compatibility with 3G and 2G technologies due to their popularity and predominence in the number of users. This demands a converter with wide bandwidths ranging from 100 KHz to 20 MHz inorder to accomodate many standards ranging from GSM (2G) to LTE-Advanced (LTE-A). Table 2.1 shows the performance of the various state-of-the-art multi-standard $\Sigma\Delta$M with DT and CT implementation. The multi-standard capabilty is extended to both LP and BP $\Sigma\Delta$Ms. Multi-standard architectures dealing with higher bandwidths often employ a multi-bit quantizer (Kwak *et al.*, 2018) in order to meet the dynamic range (DR) requirements in that particular standard.

A re-configurable quadrature BP ΣΔM with CT implementation is suitable for use in a low-IF global navigation satellite system receiver (Xu *et al.*, 2016). The dual mode of operation of this BP modulator supports both narrowband of 5 MHz bandwidth and wideband of 20 MHz bandwidth. High resolution re-configurable ΣΔ ADCs finds application in radio frequency (RF) pulse transmission in Magnetic Resonance Imaging (MRI) scanners, with real-time resolution control and targeting a specific tissue precisely (Qazi *et al.*, 2017).

2.7.7 Error Feedback Modulators

In cascaded ΣΔM, the quantization error of the first stage is extracted and it is provided as an input to the following stage. The error extraction is performed by an analog subtraction between the input and output of the quantizer. The quantization error of second stage can be introduced into the first stage by an additional path inorder to optimize a pair of complex conjugate zeros in the overall NTF (Sanchez-Renedo *et al.*, 2006). The Error Feedback Modulators (EFMs) has been widely utilized for the implementation of highly efficient Digital-to-Analog Converters (DACs)(Norsworthy *et al.*, 1997). The newly introduced differential quantizer based error feedback modulator (DQEFM) (Prakash *et al.*, 2018) also belongs to the category of noise shaping data converters. DQEFM replaces the integrator with a differential quantizer to achieve noise-shaping characteristics. Thus, integrator associated non-idealities, loop-stability issues, and optimization of the integrator scaling coefficients is no more a concern in DQEFM. The error feedback structure or noise coupling is an effective technique that can be used to enhance the order of noiseshaping, without much increase in the power consumption (Lee *et al.*, 2009, 2008).

Table 2.1: Multi-standard ΣΔ ADCs Benchmark

Work	Type	Standard	Bandwidth (MHz)	Sampling Freq.(MHz)	Architecture	Quantizer	CMOS Process (nm)	Power (mW)	FoM (dB)
(Sauerbrey *et al.*, 2018)	CT	GSM	0.24	153.7	3^{rd} order ΣΔ	4 bit	28	4	174
		LTE	27	1230	3^{rd} order ΣΔ	4 bit	28	10.31	171
(Prakash *et al.*, 2017)	DT	WLAN	22	220	4^{th} order ΣΔ	2 bit-1bit	45	1.93	168
		WiMAX	28	224	4^{th} order ΣΔ	2 bit-1 bit	45	1.93	158
(Bettini *et al.*, 2015)	DT	EDGE	0.1	26	3^{rd} order ΣΔ	1.5 bit	130	3.4	162
		UMTS	1.92	61.44	3^{rd} order ΣΔ	3.5 bit	130	6.8	163
		LTE	10	240	3^{rd} order ΣΔ	3.5 bit	130	22.4	160
		LTE-A	20	400	3^{rd} order ΣΔ	3.5 bit	130	44	154
(Li *et al.*, 2013)	CT	LTE	10	400	3^{rd} order ΣΔ	5 bit	130	14.7	157
		LTE-A	20	640	3^{rd} order ΣΔ	5 bit	130	21	150
(Morgado *et al.*, 2010)	DT	GSM	0.1	40	2^{nd} order ΣΔ	1.5 bit	90	4.6	148
		GPS	1	120	2^{nd} order ΣΔ	1.5 bit	90	6.2	148
		WiMAX	10	240	Cascade 2-2 ΣΔ	1.5 bit-1.5 bit	90	11	138
(Christen and Huang, 2010)	DT	UMTS	1.92	61.44	3^{rd} order ΣΔ	1.5 bit	130	5.2	162
		LTE-A	20	400	3^{rd} order ΣΔ	3.5 bit	130	34.7	158
(Crombez *et al.*, 2010)	CT	UMTS	1.92	245.8	3^{rd} order ΣΔ	1 bit	90	6.4	162
		WLAN	10	640	3^{rd} order ΣΔ	1 bit	90	6.8	159

2.8 Performance Comparison of Various ΣΔ Modulators

The performance of various ΣΔ Modulators reported during the past decade are shown in Figure 2.14. The dynamic range (DR) expressed in bits is plotted against bandwidth of the modulator. The majority of the ΣΔ Modulators achieves a resolution in the range 8-18 bits. It can be seen from the figure that CT ΣΔ Modulators are dominating in the wideband region. DT ΣΔ Modulators are also showing an excellent performance upto a bandwidth of 20 MHz. The multi-bit ΣΔ design offer a higher resolution. The energy efficiency of different ΣΔ architectures are evaluated against bandwidth of operation and are plotted in Figure 2.15. CT ΣΔ architectures have the least FoM_w in the wideband region. The observed trend in DR (bits) for the various BP ΣΔ Modulators reported during the last decade is represented in Figure 2.16. The attained resolution for BP ΣΔ architectures is relatively low in the broadband region. CT BP ΣΔ architectures shows an excellent performance for the bandwidths above 10 MHz.

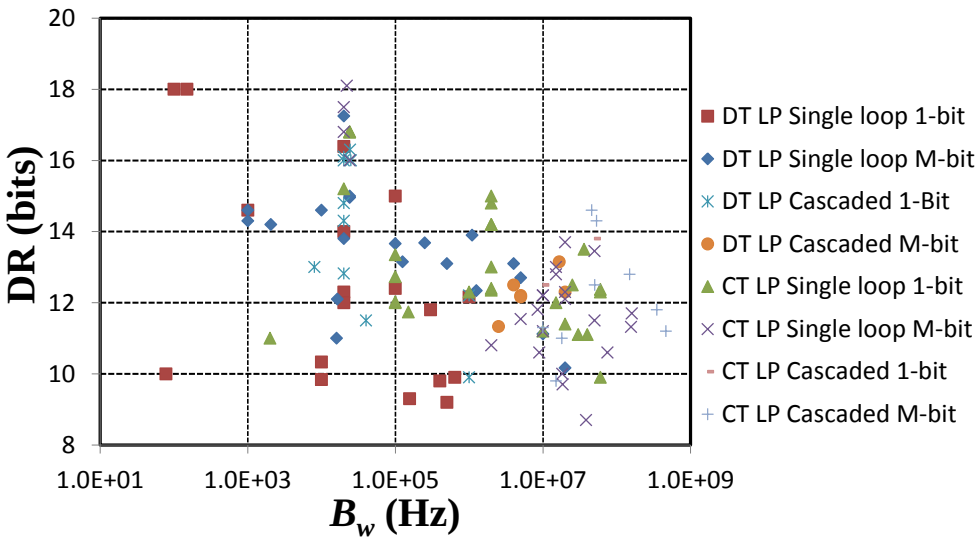


Figure 2.14: Trend in DR (bits) for the various LP ΣΔ Modulators reported during the past decade

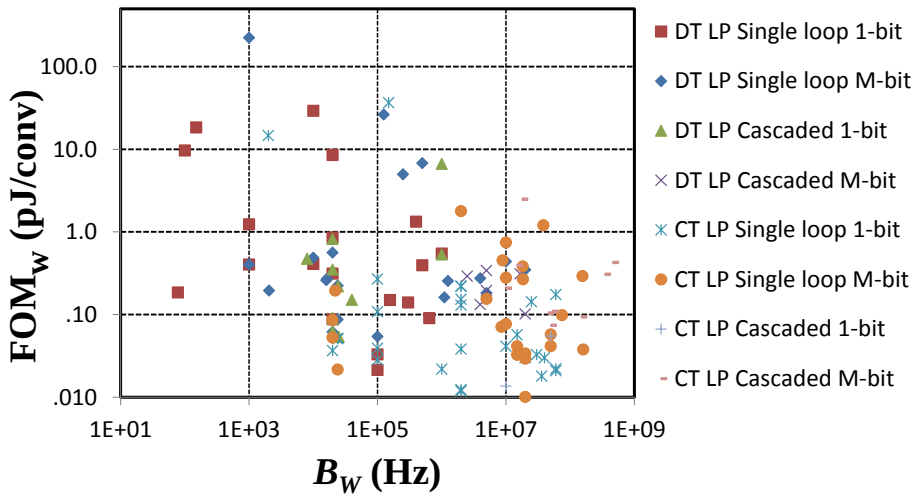


Figure 2.15: FoM_w vs BW for the various $\Sigma\Delta$ architectures reported during the past decade

2.9 Wideband $\Sigma\Delta$ ADCs

The high performance and large data rate requirement of future communication systems can be satisfied only by increasing the input signal bandwidth. $\Sigma\Delta$ ADCs were

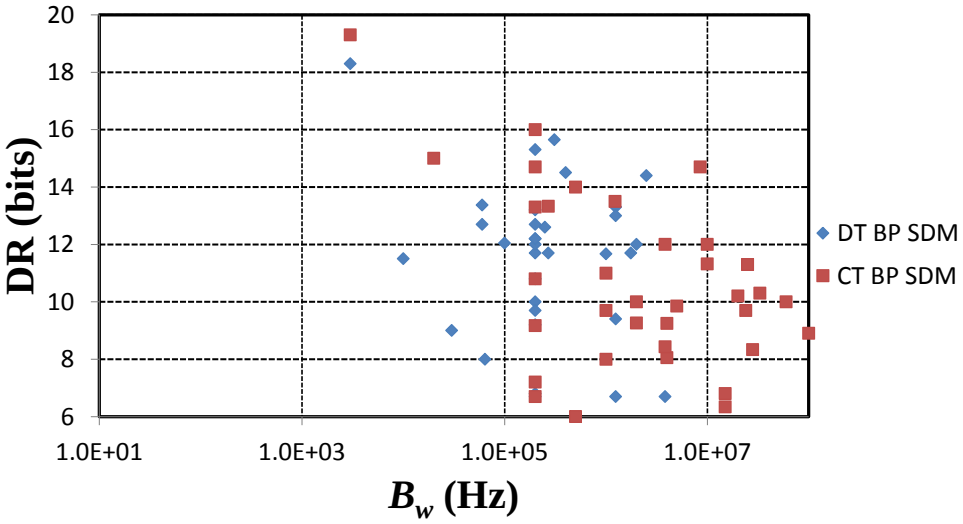


Figure 2.16: Observed trend in DR (bits) for the various BP $\Sigma\Delta$ Modulators reported during the past decade

considered the conversion of choice for low to medium bandwidth applications, but the architectural advancements and technology scaling contributed this converter to emerge as a new category of converter named wideband $\Sigma\Delta$ ADC.

The ADCs operating in wideband applications often require a larger dynamic range (DR). High performance, low power CT $\Sigma\Delta$ ADCs have been widely used in wideband applications, where high resolution at medium conversion speed is required. The lowpass (LP) and bandpass (BP) $\Sigma\Delta$ modulators are utilized in realizing a wideband $\Sigma\Delta$ ADC. In the case of DT $\Sigma\Delta$M the commonly used methods to meet the wide dynamic range (DR) required for wideband applications are increasing the order of the loop filter and employing a multibit quantizer. Another way to achieve a higher Signal to Noise Ratio (SNR), is by increasing the operating frequency, but that is restricted because of technology limitations.

The recent advancement in CMOS scaling technology has significantly improved the speed of transistors, but the sampling frequency is still the main limiting factor of the bandwidth of $\Sigma\Delta$Ms (Maghari and Moon, 2014). A higher sampling frequency also results in an increased power consumption (Shettigar and Pavan, 2012). This is the reason why a low oversampling ratio (OSR) is preferred for wideband $\Sigma\Delta$ ADC. As we increase the order of modulator the resolution improves, however when the order of modulator goes beyond two in a traditional single loop structure, it is at a greater risk of instability. The stability issues prevailing in single stage higher order modulators can be eliminated by cascaded or multi-stage noise shaping (MASH) topology. The cascaded or MASH $\Sigma\Delta$ structure combines many stable first or second order $\Sigma\Delta$ modulators to achieve the required modulator order and ensures stability (Maloberti, 2007).

2.10 Chapter Summary

This chapter describes the ADC fundamentals, ADC performance over time and $\Sigma\Delta$ ADC. The basics of $\Sigma\Delta$ modulator operation, the architectural improvements taken place in the history of $\Sigma\Delta$ modulator, and the major findings reported in the literature related to $\Sigma\Delta$ modulator implementation are also presented. The thesis explores the different DT cascaded $\Sigma\Delta$ modulator architectures for wideband applications. Several techniques are also introduced inorder to enhance resolution with limited hardware and power, especially for use in wideband ADCs.

CHAPTER 3

CASCADED $\Sigma\Delta$ ARCHITECTURES WITH IMPROVED RESOLUTION

An effective method to enhance the resolution of cascaded $\Sigma\Delta$ modulators by introducing analog feedback paths between the cascaded stages is presented in this chapter. This inter-stage feedback path contribute to an increase in the order of noise shaping, which in turn enhances the resolution of the modulator. This technique can be adopted for Multi stAge noise SHaping (MASH) and Sturdy MASH (SMASH) structures for improving the Signal to Noise Ratio (SNR). The MASH/SMASH 2-1 $\Sigma\Delta$ modulator can attain fourth and fifth order noise shaping by employing suitable analog feedback paths between the two stages, without affecting the digital cancellation logic. A low oversampling ratio, utilization of low-distortion architecture, reduction in the number of active blocks and noise shaping enhancement makes these architectures attractive for low power wideband applications. The response of the MASH and SMASH architecture to various non-ideal effects are also studied with the help of MATLAB simulations. Mathematical analysis and behavioral simulation results obtained for both MASH and SMASH architectures prove the fitness of these architectures.

The chapter is organized as follows. Section 3.1 discusses the traditional MASH $\Sigma\Delta$ architecture and a method to improve the order of noise shaping in MASH modulators by the use of analog inter-stage paths between the cascaded stages. A MASH 2-1 $\Sigma\Delta$ modulator capable of achieving fourth and fifth order of noise shaping are also described here. Section 3.2 describes the conventional SMASH architecture. The resolution enhancement techniques through analog inter-stage paths between the cascaded stages are also extended to the SMASH 2-1 $\Sigma\Delta$ modulator to achieve fourth

and fifth order of noise shaping. Section 3.3 illustrates the behavioral level simulatons performed for the modified MASH and SMASH architectures. Finally, Section 3.4 portrays the inferences from this chapter.

3.1 MASH $\Sigma\Delta$ Modulator Architecture

The single stage higher order $\Sigma\Delta$ modulator architectures have stability issues when the order of modulator goes beyond two. The MASH structure is a useful candidate to alleviate these stability problems by cascading several low order modulators which are individually stable. The cascaded structure provides the advantages like inherent stability, higher dynamic range and higher overload input level when compared with the single loop approach.

The block diagram of a traditional two stage cascaded $\Sigma\Delta$ architecture is shown in Figure 3.1 (Schreier and Temes, 2005). In MASH architecture, the quantization noise of the first stage modulator is extracted and provided as an input to the subsequent stage. The digital output of first and second stage of MASH structure is given to the Digital Cancellation Logic (DCL). An appropriate digital noise cancellation logic cancels the quantization noise of all previous stages except the last stage. The last stage quantization noise is shaped by a Noise Transfer Function (NTF) of order equal to the sum of all the orders. The L_{si} and L_{ni} in Figure 3.1 denote the signal and noise loop filters of the i^{th} stage. $H_1(z)$ and $H_2(z)$ are the digital filters. STF and NTF are the signal transfer function and the noise transfer function respectively.

The output of first stage modulator is given by

$$Y_1(z) = X(z)STF_1(z) + E_1(z)NTF_1(z) \tag{3.1}$$

where

$$STF_1(z) = \frac{L_{s1}(z)}{1 + L_{n1}(z)}$$

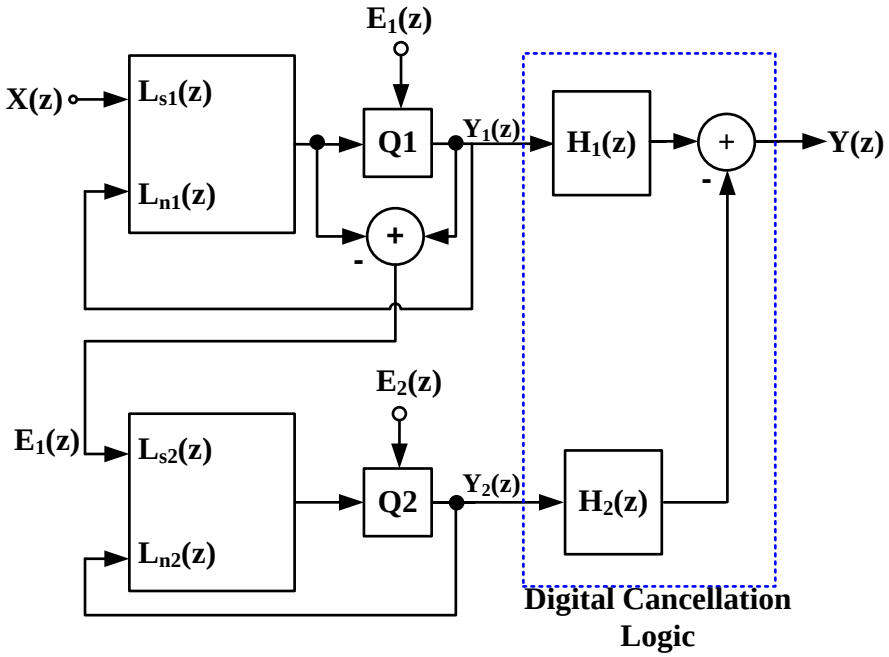


Figure 3.1: Block diagram of the traditional 2 stage MASH ΣΔ Modulator Architecture

and

$$NTF_1(z) = \frac{1}{1 + L_{n1}(z)}$$

Similarly the output of second stage modulator is given by

$$Y_2(z) = E_1(z)STF_2(z) + E_2(z)NTF_2(z) \tag{3.2}$$

where

$$STF_2(z) = \frac{L_{s2}(z)}{1 + L_{n2}(z)}$$

and

$$NTF_2(z) = \frac{1}{1 + L_{n2}(z)}$$

The MASH modulator output is expressed as

$$Y(z) = Y_1(z)H_1(z) - Y_2(z)H_2(z) \tag{3.3}$$

i.e.

$$\begin{aligned} Y(z) = [X(z)STF_1(z) + E_1(z)NTF_1(z)]H_1(z) \\ - [E_1(z)STF_2(z) + E_2(z)NTF_2(z)]H_2(z) \end{aligned} \tag{3.4}$$

If we choose $H_1(z) = STF_2(z)$ and $H_2(z) = NTF_1(z)$ the quantization noise associated with the first stage is eliminated and the output is given by

$$Y(z) = X(z)STF_1(z)STF_2(z) - E_2(z)NTF_1(z)NTF_2(z) \tag{3.5}$$

where $X(z)$, $Y(z)$, and $E_2(z)$ are the input signal, output of the modulator and quantization noise of the second stage respectively. The $STF_i(z)$, $NTF_i(z)$, represents STF and NTF of the i^{th} stage MASH $\Sigma\Delta$M.

3.1.1 Traditional Feedforward MASH 2-1 $\Sigma\Delta$ Modulator Architecture with 3^{rd} Order Noise Shaping

The MASH 2-1 $\Sigma\Delta$ modulator consists of a second order modulator in the first stage and a first order modulator in the second stage (called a 2-1 modulator). A MASH 2-1 modulator employing a feedforward topology is shown in Figure 3.2. The quantization noise associated with the first stage is extracted and provided as an input to the subsequent stage. A suitable Digital Cancellation Logic (DCL) eliminates the quantization noise present in the first stage and the second stage quantization noise is shaped by a 3^{rd} order NTF. Q1 and Q2 represents the multi-bit quantizers utilized in the first and second stages of the MASH structure. The output of the MASH 2-1 $\Sigma\Delta$ modulator is expressed as

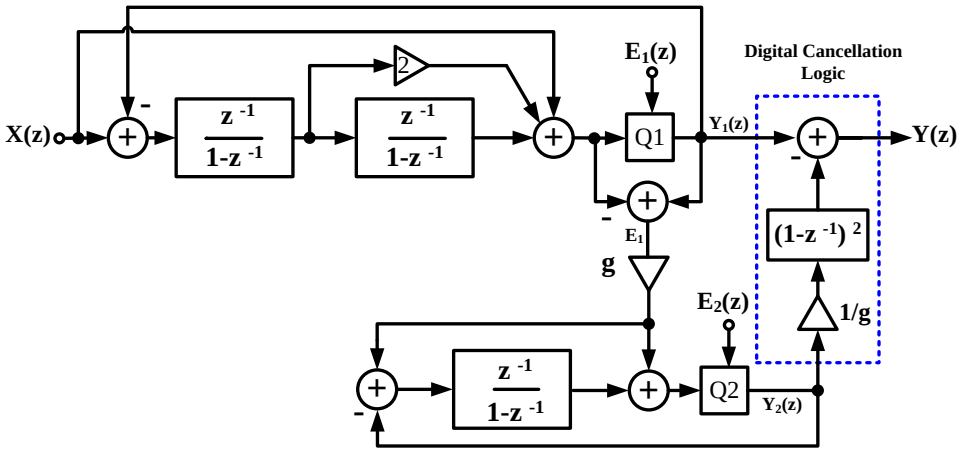


Figure 3.2: Traditional feedforward MASH 2-1 $\Sigma\Delta$ modulator with 3^{rd} order noise shaping

$$Y(z) = X(z) - \frac{1}{g}(1 - z^{-1})^3 E_2(z) \tag{3.6}$$

where $X(z)$, $Y(z)$, and $E_2(z)$ are the input signal, digital output of the modulator and quantization noise of the second stage respectively. The inter-stage gain is represented by 'g'. Equation (3.6) indicate that the quantization noise of the first stage, $E_1(z)$ has been eliminated completely and the second stage quantization noise is shaped by an NTF of order equal to three. A first-order modulator as the first stage of the MASH architecture will result in the presence of pattern noise and the so-called idle tones popping up in the output spectrum of the modulator. So we always prefer to choose a second order modulator as the first stage in a MASH/SMASH structure.

3.1.2 MASH 2-1 $\Sigma\Delta$ Architecture with Enhanced $(3+1)^{th}$ Order Noise Shaping

A MASH 2-1 $\Sigma\Delta$ modulator can achieve higher order noise shaping by using suitable analog inter-stage feedback paths between the cascaded stages as shown in Figure 3.3 (Khazaeili and Yavari, 2014). The analog feedback paths introduced between the

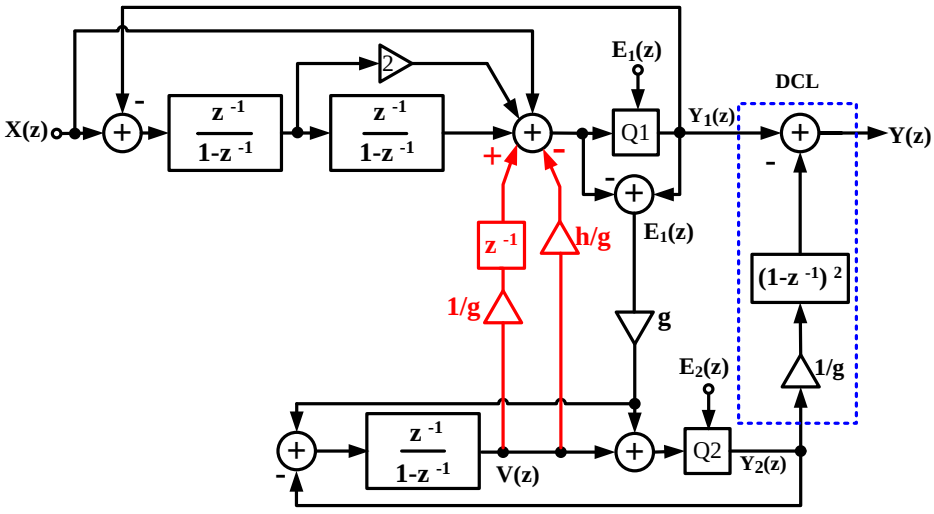


Figure 3.3: Traditional feedforward MASH 2-1 $\Sigma\Delta$ Modulator with $(3+1)^{th}$ order of noise shaping (Khazaeili and Yavari, 2014)

two stages of MASH structure inject a portion of second stage quantization noise to the adder in front of the first quantizer. However, the number of integrator blocks remain the same as that of conventional MASH 2-1 modulator and the DCL remains unaffected. The enhancement in the order of NTF can be verified mathematically. The output of the second stage modulator, $Y_2(z)$ is

$$Y_2(z) = gE_1(z) + E_2(z)(1 - z^{-1}) \tag{3.7}$$

The structure used in the second stage is a unity STF modulator, so $STF_2(z)$=1. The NTF associated with second stage is $NTF_2(z)$= $(1 - z^{-1})$. The output of the integrator in the second stage of MASH structure is represented by V(z)

$$V(z) = -\frac{z^{-1}}{1 - z^{-1}} NTF_2(z)E_2(z) \tag{3.8}$$

substituting $NTF_2(z)$= $(1 - z^{-1})$, we get

$$V(z) = -z^{-1}E_2(z) \tag{3.9}$$

The output of the first stage modulator is

$$Y_1(z) = X(z)+\frac{1}{g}V(z)z^{-1}(1-z^{-1})^2-\frac{h}{g}V(z)(1-z^{-1})^2+E_1(z)(1-z^{-1})^2 \quad (3.10)$$

substituting V(z) in equation (3.10) gives

$$Y_1(z) = X(z)-\frac{1}{g}z^{-2}(1-z^{-1})^2E_2(z)+\frac{h}{g}z^{-1}(1-z^{-1})^2E_2(z)+E_1(z)(1-z^{-1})^2 \quad (3.11)$$

The output of the MASH modulator is given by

$$Y(z) = Y_1(z) - \frac{1}{g}Y_2(z)(1-z^{-1})^2 \quad (3.12)$$

substituting $Y_1(z)$ and $Y_2(z)$, we get

$$Y(z) = X(z) - \frac{1}{g}E_2(z)(1-z^{-1})^2[1-(1+h)z^{-1}+z^{-2}] \quad (3.13)$$

In equation (3.13), if the value of '*h*' is chosen to be equal to 1, then

$$Y(z) = X(z) - \frac{1}{g}E_2(z)(1-z^{-1})^4 \quad (3.14)$$

Equation (3.14) affirms that, $E_1(z)$ has been eliminated and $E_2(z)$ is shaped by an NTF of order equal to four. The inter-stage feedback paths contributes to an increase in the order of noise shaping, which causes an enhancement in the resolution of the modulator. Any further improvement in SNR value can be achieved by optimizing the coefficient value '*h*'.

3.1.3 Proposed MASH 2-1 $\Sigma\Delta$ architecture with Enhanced $(3+2)^{th}$ Order Noise Shaping

A MASH 2-1 structure capable of achieving fifth order noise shaping using analog inter-stage feedback paths is depicted in Figure 3.4. The inter-stage feedback paths

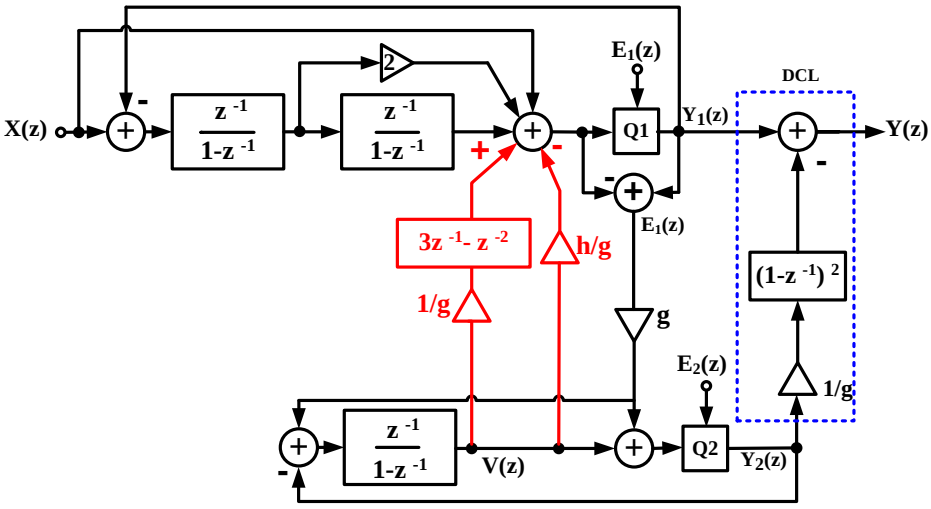


Figure 3.4: Proposed MASH 2-1 $\Sigma\Delta$ Modulator with $(3+2)^{th}$ order of noise shaping

have been modified for obtaining $(3+2)^{th}$ order noise shaping without affecting the DCL. The number of integrators required also remains the same when compared with the conventional MASH 2-1 modulator. The output of the integrator in the second stage of MASH structure is given by

$$V(z) = -\frac{z^{-1}}{1-z^{-1}} NTF_2(z) E_2(z) \tag{3.15}$$

where $NTF_2(z)$ is the NTF of the second stage of MASH modulator. Since the two stages employ the feedforward topology, the STF remains unity. The output of the first and second stage of the modulator is given by

$$Y_1(z) = X(z) + \frac{1}{g} V(z)(1-z^{-1})^2[3z^{-1} - z^{-2}] - \frac{h}{g} V(z)(1-z^{-1})^2 + E_1(z)(1-z^{-1})^2 \tag{3.16}$$

substituting V(z), we get

$$Y_1(z) = X(z) - \frac{1}{g}(1-z^{-1})^2[3z^{-2} - z^{-3} - hz^{-1}]E_2(z) + E_1(z)(1-z^{-1})^2 \tag{3.17}$$

$$Y_2(z) = gE_1(z) + E_2(z)(1 - z^{-1}) \tag{3.18}$$

$Y_1(z)$ and $Y_2(z)$ represents the output of the first and second stage of the MASH structure. The combined output $Y(z)$ is represented by

$$Y(z) = Y_1(z) - \frac{1}{g_{dig}}(1 - z^{-1})^2 Y_2(z) \tag{3.19}$$

A good matching between the analog and digital filters makes $g = g_{dig}$. The output of the MASH modulator is as follows

$$Y(z) = X(z) - \frac{1}{g}(1 - z^{-1})^2[1 - (1 + h)z^{-1} + 3z^{-2} - z^{-3}]E_2(z) \tag{3.20}$$

Substituting *h*=2 in equation (3.20) the modulator achieves fifth order noise shaping. That is,

$$Y(z) = X(z) - \frac{1}{g}(1 - z^{-1})^5 E_2(z) \tag{3.21}$$

In equation (3.21) the output $Y(z)$ contains the input signal and the shaped quantization noise of the second stage. The first stage quantization noise has been removed completely. A proper selection of the inter-stage gain (g) value, will further reduce the value of $E_2(z)$.

A major advantage of this proposed modulator is that, it requires only three integrators for obtaining a fifth order noise shaping at the expense of some delay blocks. Generally, for obtaining an N^{th} order noise shaping, the modulator requires 'N' number of integrators. This improved modulator saves two additional power hungry active integrator blocks which will ultimately result in lesser chip area and power. The DCL also remains unaffected by these new additional inter-stage paths. Increased circuit complexity and the requirement of additional passive components are the limitations of this approach. Meanwhile, passive implementation of the inter-stage paths and reduction in active blocks make this proposed modulator suitable for low power applications.

3.2 Sturdy MASH ΣΔ Modulator Architecture

The MASH structure contains analog and digital circuits. Mismatch between the analog and digital filters may lead to quantization error leakage, which in turn causes a reduction in SNR value. This need for matching between the analog and digital filters in MASH structure necessitate high accuracy active elements. The Sturdy MASH (SMASH) architecture is similar in operation when compared with MASH, but it doesn't require digital noise cancellation filters. The matching between analog and digital elements is no more a concern in SMASH modulators.

The block diagram of a two stage SMASH modulator is shown in Figure 3.5. The first stage noise is obtained by performing analog subtraction between the input and output of the quantizer, and the resulting error is fed to the next stage. In SMASH structure the second stage output is directly subtracted inside the first stage loop in the digital domain. This will provide an additional noise shaping for the first stage quantization noise. The mathematical analysis of the SMASH modulator shown in

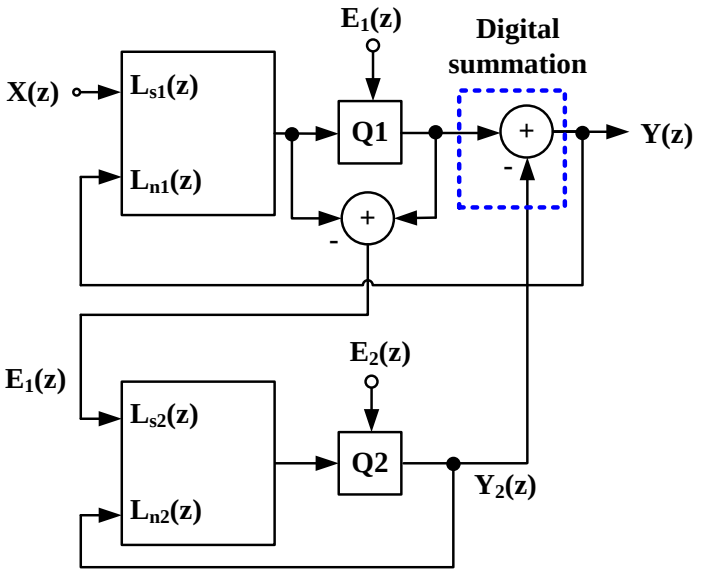


Figure 3.5: Block diagram of a traditional 2 stage SMASH ΣΔ modulator

Figure 3.5 is as follows

$$Y(z) = X(z)STF_1(z) + E_1(z)NTF_1(z) - Y_2(z)NTF_1(z) \tag{3.22}$$

where

$$STF_1(z) = \frac{L_{s1}(z)}{1 + L_{n1}(z)}$$

and

$$NTF_1(z) = \frac{1}{1 + L_{n1}(z)}$$

The output of second stage modulator is given by

$$Y_2(z) = E_1(z)STF_2(z) + E_2(z)NTF_2(z) \tag{3.23}$$

where

$$STF_2(z) = \frac{L_{s2}(z)}{1 + L_{n2}(z)}$$

and

$$NTF_2(z) = \frac{1}{1 + L_{n2}(z)}$$

The SMASH modulator output is expressed as

$$\begin{aligned} Y(z) = X(z)STF_1(z) + E_1(z)NTF_1(z)[1 - STF_2(z)] \\ - E_2(z)NTF_1(z)NTF_2(z) \end{aligned} \tag{3.24}$$

If $STF_2(z) = 1$, then equation (3.24) becomes

$$Y(z) = X(z)STF_1(z) - E_2(z)NTF_1(z)NTF_2(z) \tag{3.25}$$

where $X(z)$, $Y(z)$, and $E_2(z)$ are the input signal, output of the modulator and quantization noise of the second stage respectively. The $STF_i(z)$, $NTF_i(z)$, represents STF and NTF of the i^{th} stage SMASH $\Sigma\Delta$M.

3.2.1 Traditional Feedforward SMASH 2-1 $\Sigma\Delta$ modulator Architecture with 3^{rd} Order Noise Shaping

A feedforward topology is chosen for the SMASH 2-1 modulator described here, and it is represented in Figure 3.6. The output of the SMASH 2-1 $\Sigma\Delta$ modulator is expressed as

$$Y(z) = X(z) - \frac{1}{g}(1 - z^{-1})^3 E_2(z) \tag{3.26}$$

Equation (3.26) indicate that the quantization noise of the first stage, $E_1(z)$ is removed completely and the second stage quantization noise is shaped by an NTF of order three.

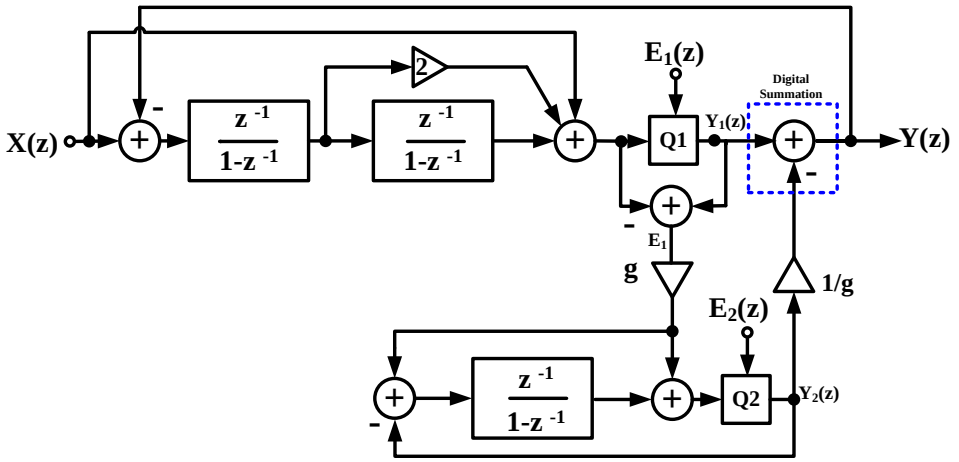


Figure 3.6: Traditional feedforward SMASH 2-1 $\Sigma\Delta$ modulator with 3^{rd} order noise shaping

3.2.2 Proposed SMASH 2-1 $\Sigma\Delta$ Architecture with Enhanced $(3+1)^{th}$ Order Noise Shaping

In Figure 3.7, the feedback paths are introduced between the two stages of SMASH structure in order to obtain a one order higher noise shaping than order of the modu-

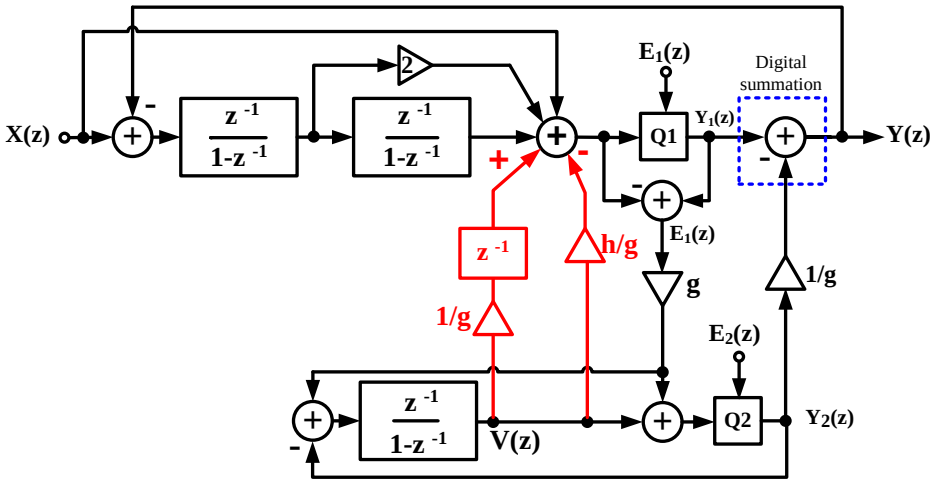


Figure 3.7: Proposed SMASH 2-1 $\Sigma\Delta$ Modulator with $(3+1)^{th}$ order noise shaping

lator. The output of the second stage modulator is

$$Y_2(z) = gE_1(z) + E_2(z)(1 - z^{-1}) \tag{3.27}$$

The output of the integrator in the second stage of SMASH structure is represented by V(z)

$$V(z) = -\frac{z^{-1}}{1 - z^{-1}} NTF_2(z)E_2(z) \tag{3.28}$$

substituting $NTF_2(z)$= $(1 - z^{-1})$, we get

$$V(z) = -z^{-1}E_2(z) \tag{3.29}$$

The output of the modulator is expressed mathematically as

$$Y(z) = X(z) + \frac{1}{g}V(z)z^{-1}(1 - z^{-1})^2 - \frac{h}{g}V(z)(1 - z^{-1})^2 + E_1(z)(1 - z^{-1})^2 - \frac{1}{g}Y_2(z)(1 - z^{-1})^2 \tag{3.30}$$

substituting $Y_2(z)$ in equation (3.30), we get

$$Y(z) = X(z) - \frac{1}{g}E_2(z)(1 - z^{-1})^2[1 - (1 + h)z^{-1} + z^{-2}] \tag{3.31}$$

In equation (3.31), if the value of '*h*' is chosen to be equal to 1, then

$$Y(z) = X(z) - \frac{1}{g}E_2(z)(1 - z^{-1})^4 \tag{3.32}$$

Equation (3.32) denotes the elimination of $E_1(z)$ and the fourth order shaping of the quantization noise $E_2(z)$.

3.2.3 Proposed SMASH 2-1 $\Sigma\Delta$ Architecture with Enhanced $(3 + 2)^{th}$ Order Noise Shaping

The SMASH 2-1 architecture has been modified to attain a $(3 + 2)^{th}$ order noise shaping and it is represented in Figure 3.8. The output of the integrator in the second stage of SMASH structure is given by

$$V(z) = -\frac{z^{-1}}{1 - z^{-1}}NTF_2(z)E_2(z) \tag{3.33}$$

where $NTF_2(z)$ is the noise transfer function of the second stage of the SMASH structure. Since the two stages employ the feedforward topology, the STF remains unity. The output of the SMASH modulator is given by

$$Y(z) = X(z) - \frac{1}{g}(1 - z^{-1})^3[3z^{-2} - z^{-3} - hz^{-1}]E_2(z) + E_1(z)(1 - z^{-1})^2 - \frac{1}{g}Y_2(z)(1 - z^{-1})^2 \tag{3.34}$$

$$Y_2(z) = gE_1(z) + E_2(z)(1 - z^{-1}) \tag{3.35}$$

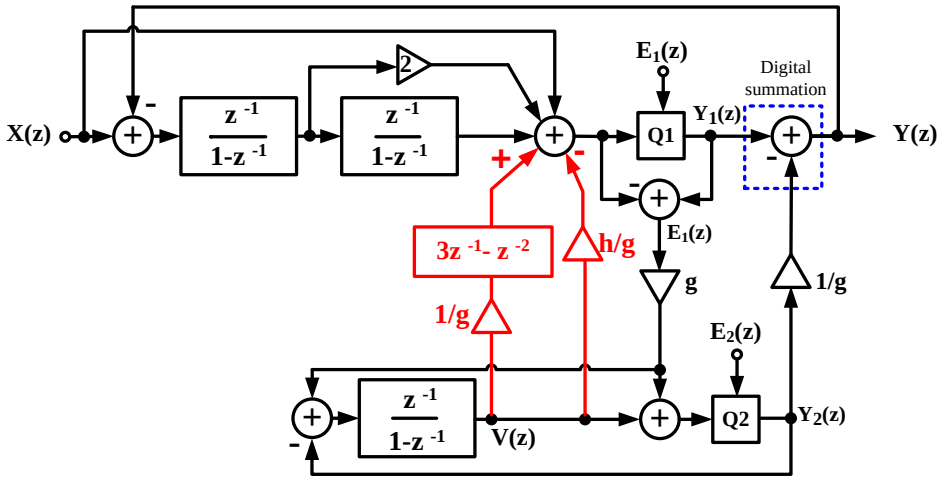


Figure 3.8: Proposed SMASH 2-1 $\Sigma\Delta$ Modulator with $(3+2)^{th}$ order noise shaping

$Y_2(z)$ represents the output of the second stage of the SMASH structure. The combined output $Y(z)$ is represented by

$$Y(z) = X(z) - \frac{1}{g}(1-z^{-1})^2[1-(1+h)z^{-1}+3z^{-2}-z^{-3}]E_2(z) \tag{3.36}$$

Substituting *h*=2 in equation (3.36) the modulator achieves fifth order noise shaping. That is,

$$Y(z) = X(z) - \frac{1}{g}(1-z^{-1})^5 E_2(z) \tag{3.37}$$

The first stage quantization noise has been removed and a proper selection of the inter stage gain 'g', will further reduce the value of $E_2(z)$.

3.3 Simulation Results of the Resolution Enhanced MASH and SMASH Architectures

The behavioral level simulations were conducted for the resolution enhanced MASH and SMASH architectures using MATLAB/SIMULINK. In order to have a uniformity in comparison, an OSR of 6, a bandwidth of 10 MHz, 4-bit quantizer in both

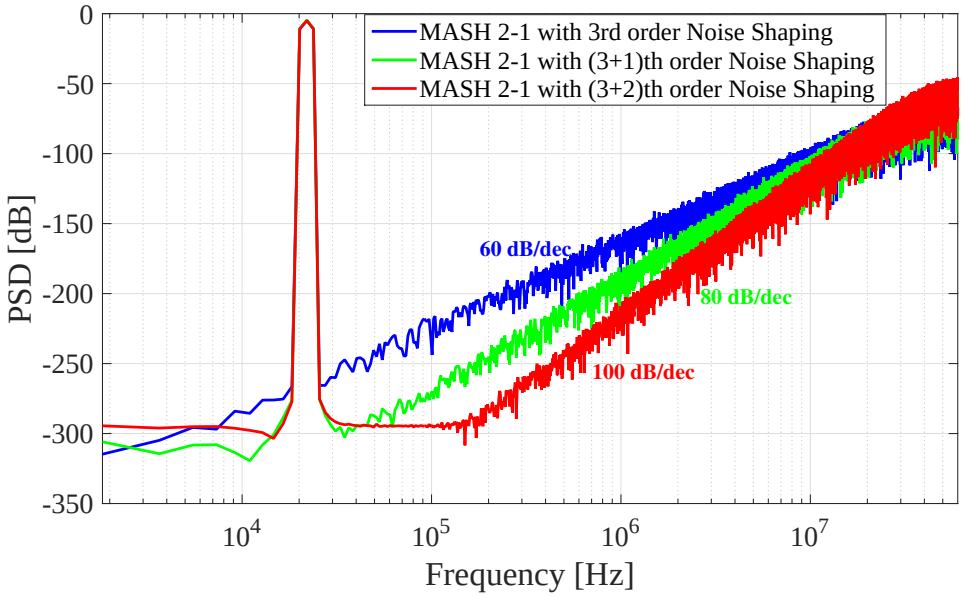


Figure 3.9: PSD comparison of MASH architectures in the increasing order of noise shaping

stages and sampling frequency (Fs) of 120 MHz were used for all the simulations. The inter-stage gain 'g' was chosen as 4. The power spectral densities (PSDs) of the resolution enhanced MASH and SMASH modulator against conventional architectures were simulated and compared as shown in Figure 3.9 and Figure 3.10. A slope of 60dB/decade, 80dB/decade and 100dB/decade were attained for third, fourth and fifth order of noise shaping respectively. The simulations performed with ideal components for MASH and SMASH architectures indicate a similar performance when their output spectra were compared.

Figure 3.11 and Figure 3.12 compares the SNR versus input amplitude curves for MASH and SMASH structures with different noise shaping capability. The peak SNR (SNR_p) value obtained for MASH/ SMASH structure with $(3+2)^{th}$ order noise shaping is 82.7 dB. An SNR_p of 77.5 dB and 70.6 dB were obtained for MASH/SMASH modulator with $(3+1)^{th}$ and 3^{rd} order noise shaping respectively. Thus, an SNR enhancement of 12 dB is achieved for proposed MASH/SMASH with $(3+2)^{th}$ order noise shaping when compared to traditional MASH/SMASH 2-1 ar-

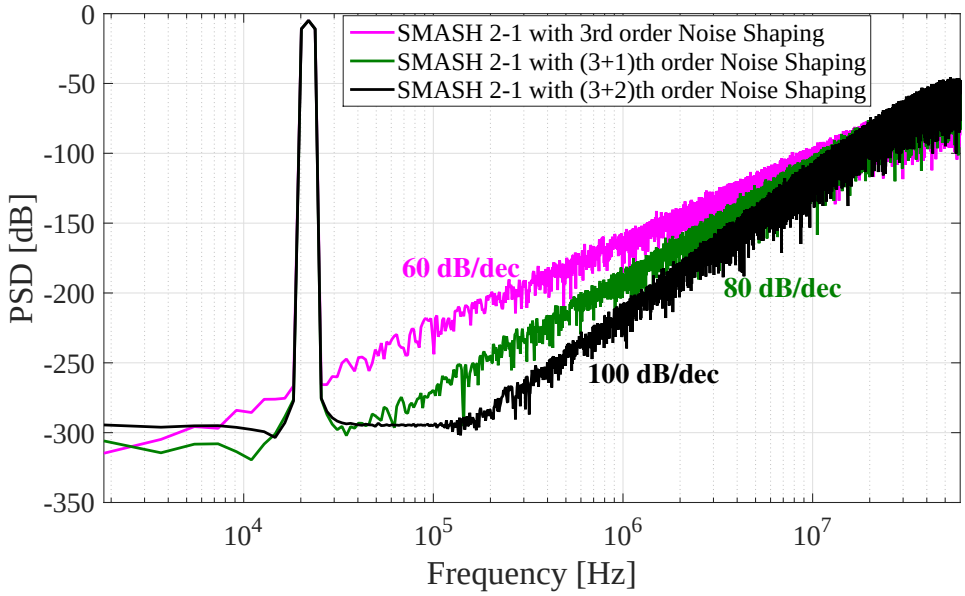


Figure 3.10: PSD comparison of SMASH architectures in the increasing order of noise shaping

chitecture. The inter-stage feedback demands the first quantizer to process a part of second stage quantization noise. So the overloading level (OL) of enhanced noise shaping architecture will be less when compared with the traditional MASH architecture. The proposed $(3+2)^{th}$ order noise shaping MASH and SMASH modulators have been simulated for all the non-ideal effects that usually occur in the hardware implementation of $\Sigma\Delta$ modulator. The various non-idealities like clock jitter, switch thermal noise, input referred op-amp noise, and the different operational amplifier non-idealities like the op-amp finite gain, slew rate, gain bandwidth were modeled and simulated using MATLAB/SIMULINK based on the models proposed in (Malcovati *et al.*, 2003). Table 3.1 describes the effect of different non-idealities on the MASH and SMASH modulators. The peak Signal to Noise and Distortion ratio ($SNDR_p$) value attained for MASH structure while considering all the non-idealities is 76.5 dB, where as SMASH attains an $SNDR_p$ of 78.4 dB. This indicates that the SMASH structure is less sensitive to different non-ideal effects. The PSD plot considering all the non-idealities for MASH and SMASH architectures with $(3+2)^{th}$

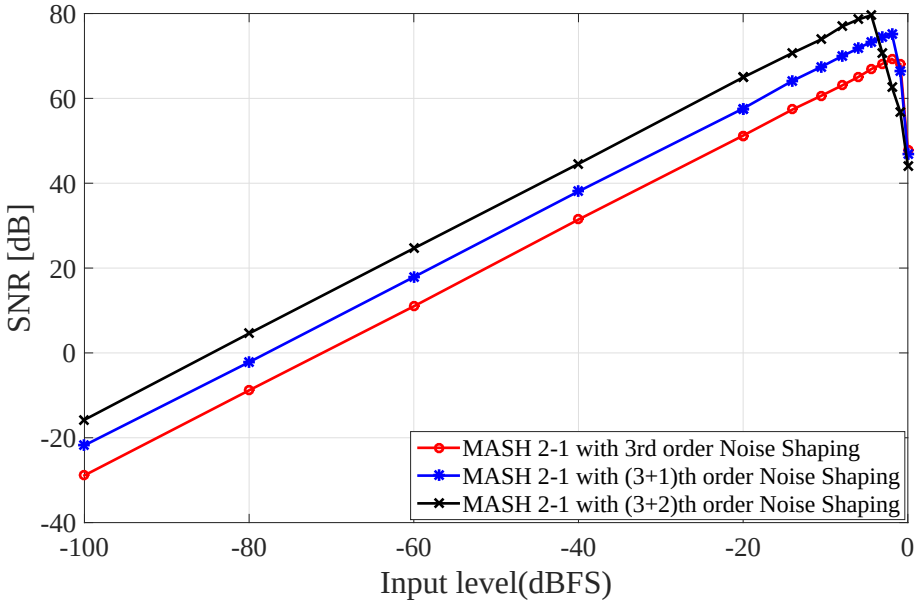


Figure 3.11: SNR versus input amplitude plot for MASH architectures in the increasing order of noise shaping

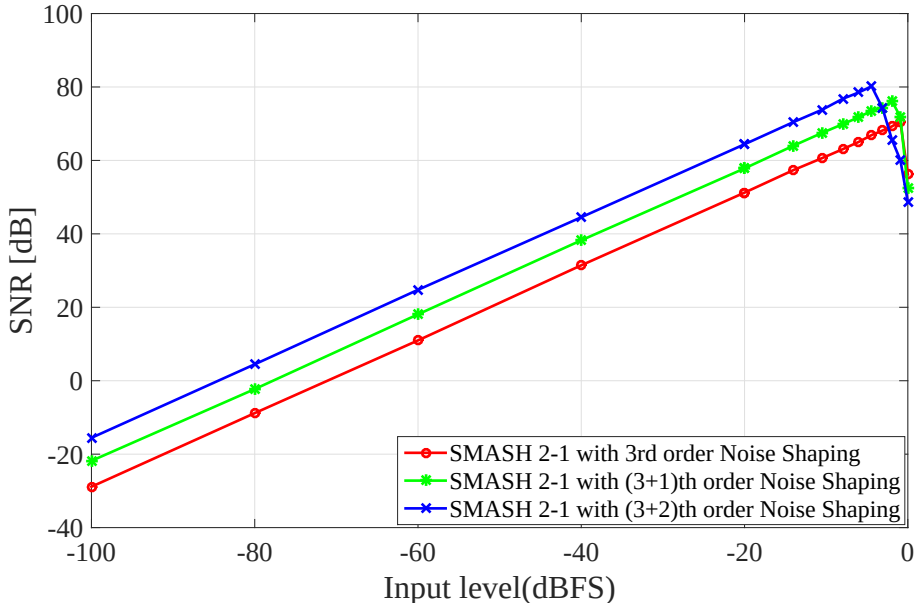


Figure 3.12: SNR versus input amplitude plot for SMASH architectures in the increasing order of noise shaping

Table 3.1: Non-ideality analysis of the proposed MASH/SMASH 2-1 ΣΔ Modulator with $(3+2)^{th}$ order noise shaping

Modulator Parameter	Parameter value	MASH 2-1 Modulator with $(3+2)^{th}$ order noise shaping $SNDR_{-4dBFS}$	SMASH 2-1 Modulator with $(3+2)^{th}$ order noise shaping $SNDR_{-4dBFS}$
Ideal modulator	-	82.7 dB	82.7 dB
Sampling Jitter	$\Delta\tau$ = 16 ns	80.6 dB	80.9 dB
Sampling capacitance	C_s = 1 pF	80.8 dB	80.8 dB
Input referred op-amp Noise	V_n = 73μVrms	79.1 dB	81.0 dB
Op-amp Finite Bandwidth	GBW = 250 MHz	81.3 dB	81.5 dB
Op-amp Finite Slew rate	SR = 200 V/μs	81.5 dB	81.5 dB
Saturation Voltage	Vmax = ±1 V	79.6 dB	80.0 dB
Op-amp Finite Gain	A_{dB} = 60 dB	81.3 dB	81.4 dB
Modulator simulated including all non-idealities	-	76.5 dB	78.4 dB

order noise shaping is shown in Figure 3.13. These non-idealities deviates the actual NTF from the ideal value. The variation in SNDR of the proposed modulator when different op-amp non-idealities were introduced are shown in Figure 3.14. The op-amp gain requirements for the SMASH structure are relaxed when compared with the MASH architecture. A gain of 30 dB is sufficient for the SMASH operation, where as a MASH architecture require a minimum of 60 dB as indicated by Figure 3.14 (a). The slew rate and gain bandwidth requirements for the MASH and SMASH are represented in Figure 3.14 (b) and Figure 3.14 (c). SMASH structure has better immunity towards op-amp non-ideal effects when compared with MASH architecture.

The SNDR value is also sensitive to the discrepancy between analog and digital co-

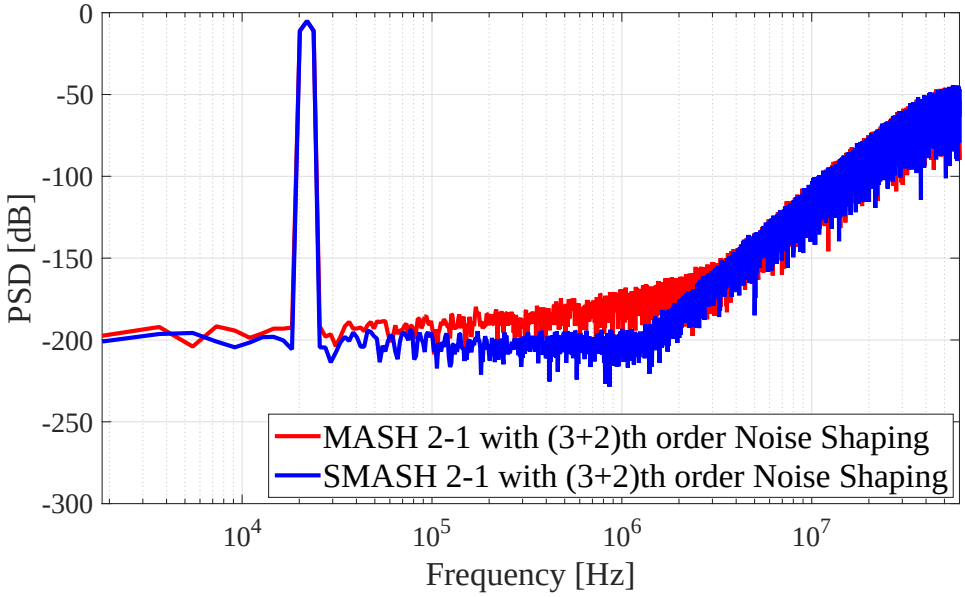
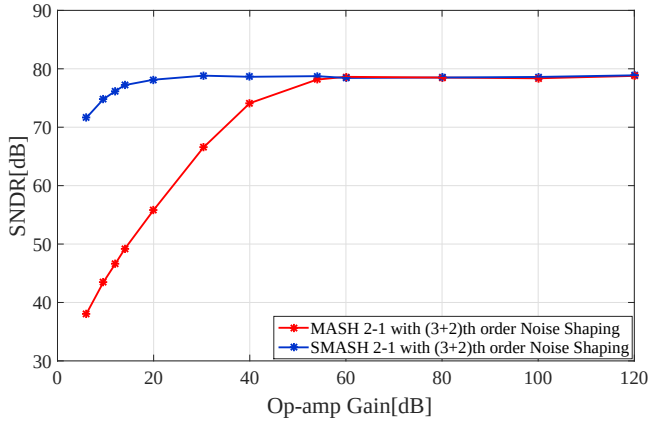


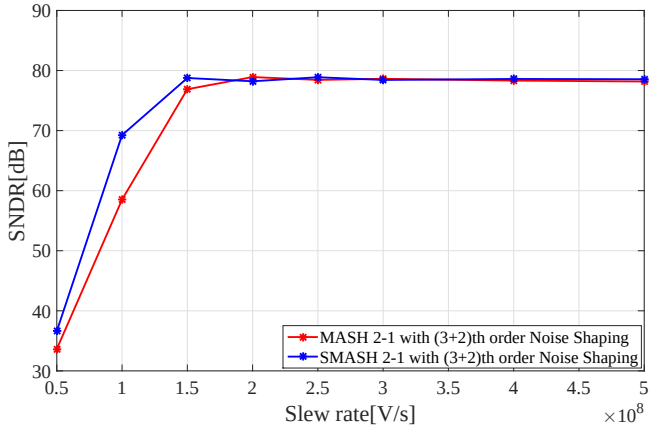
Figure 3.13: PSD plot considering all the non-ideal effects

efficients (Sohrabi and Yavarii, 2013). The mismatch between the analog coefficient (g), its digital estimate (g_{dig}) and its effect on the degradation in the SNDR value for the MASH structure is shown in Figure 3.15. A $\pm 5\%$ variation in analog and digital coefficient values leads to a degradation of 13 dB in SNDR. A comparison of the output swing of the three integrators used in MASH/SMASH 2-1 $\Sigma\Delta$ Modulator with $(3+2)^{th}$ order noise shaping is shown in Figure 3.16. The integrator output swing is also minimum because of the selection of low-distortion topology (Silva *et al.*, 2001).

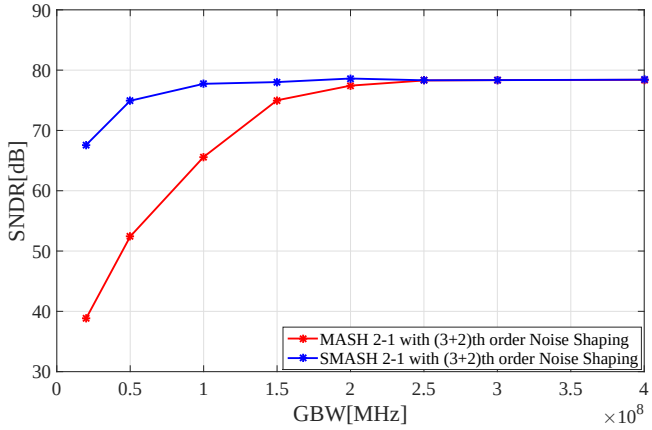
The proposed MASH/SMASH architecture with improved resolution is compared with the other state-of-the-art $\Sigma\Delta$ architectures and it is represented in Table 3.2. The proposed architectures shows a better performance when compared with other architectures. A major advantage of this enhanced noise shaping architecture is that, it requires only three integrators for generating third, fourth and fifth order noise shaping. The design of analog components are also relaxed by utilizing the low-distortion architecture in both the stages of modulator.



(a) SNDR vs Op-amp gain



(b) SNDR vs Slew rate



(c) SNDR vs GBW

Figure 3.14: SNDR variation with (a) Op-amp gain (b) Gain bandwidth (c) Slew rate for the MASH and SMASH 2-1 $\Sigma\Delta$ Modulator with $(3+2)^{th}$ order noise shaping

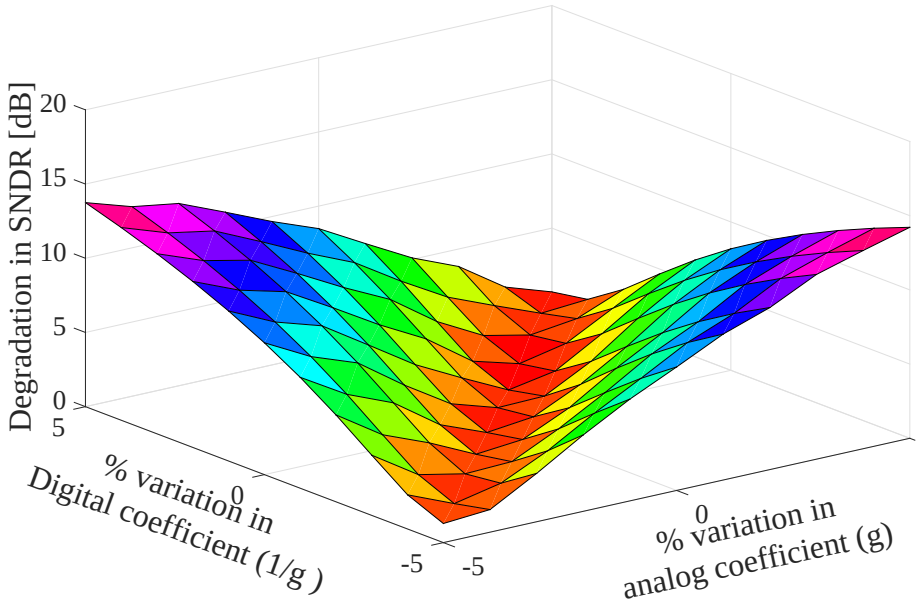


Figure 3.15: Degradation in SNDR versus mismatch between analog inter-stage gain 'g' and its digital estimate 'g_{dig}' for the MASH architecture

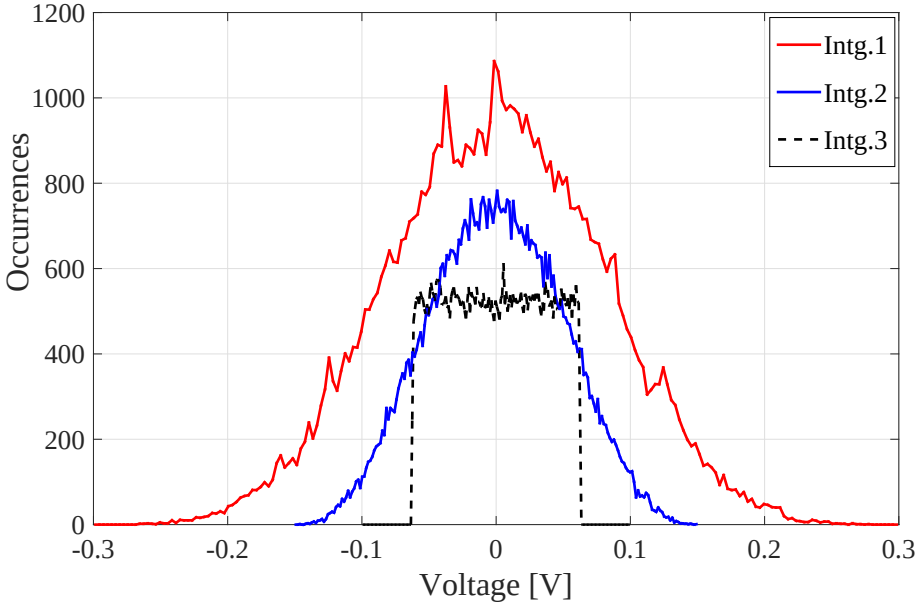


Figure 3.16: Output swing of the integrators in MASH/SMASH architecture with $(3+2)^{th}$ order noise shaping

Table 3.2: Performance comparison with other state-of-the-art $\Sigma\Delta$ modulators

Parameter	Proposed MASH	Khazaeili and Yavari (2014)	Conventional FF MASH	Proposed SMASH	Conventional FF SMASH
Architecture	MASH 2-1	MASH 2-1	MASH 2-1	SMASH 2-1	SMASH 2-1
Order of NTF	5	4	3	5	3
No. of Integrators	3	3	3	3	3
Bandwidth	10 MHz	10 MHz	10 MHz	10 MHz	10 MHz
OSR	6	6	6	6	6
Fs	120 MHz	120 MHz	120 MHz	120 MHz	120 MHz
SNR_p (dB)	82.7	77.5	70.6	82.7	70.6
$SNDR_p$ (dB)	76.5	74.6	69.1	78.4	70.0
ENOB (Bits)	12.41	12.09	11.18	12.73	11.33

3.4 Chapter Summary

A MASH/SMASH 2-1 $\Sigma\Delta$ modulator that can attain higher order noise shaping than the order of the modulator (determined by the number of integrators) using analog inter-stage feedback paths is presented in this chapter. The higher order noise shaping attainment is at the expense of extra delay blocks and without any increase in the number of active blocks. The inter-stage paths are introduced in such a way that the digital noise cancellation filter remains unaffected. The higher order noise shaping property of proposed architecture makes a reduction in the inband quantization noise, which in turn results in an enhancement in the resolution of the modulator. This MASH/SMASH architecture with inter-stage feedback paths can be used in multi-mode operation, where a single MASH 2-1 modulator can provide third, fourth and fifth order noise shaping in different modes. The simulation results shows that SMASH structure has a better immunity towards the circuit non-ideal effects when compared with the MASH architecture. An SNDR of value above 70 dB and low OSR makes these MASH/SMASH modulators suitable for low power and wide bandwidth applications.

CHAPTER 4

RESONATION BASED CASCADED $\Sigma\Delta$ ARCHITECTURES WITH SHIFTED LOOP DELAYS

An improved low-distortion MASH/SMASH $\Sigma\Delta$ modulator architecture that attains an enhancement in the resolution through techniques like resonation and NTF zero optimization are presented in this chapter. The improved low-distortion architecture eliminates the feedforward adder before the quantizer in the first stage of MASH/ SMASH structure. The enhancement in noise shaping is achieved without any additional active components, which makes this architecture hardware efficient. The shifted loop delay techniques utilized in this architecture helps to relax the signal processing timing issues in the critical path of the modulator. The low-distortion architecture in both stages of MASH structure causes a reduction in the integrator associated non-idealities. The utilization of low-distortion architecture, selection of low OSR, fewer number of adder and active blocks and achievement of fourth order noise shaping makes this modulator suitable for low power wideband applications. The behavioral simulations and mathematical analysis confirm the effectiveness of this proposed MASH/SMASH modulator.

The chapter is organized as follows. Section 4.1 reviews the concepts and limitations of the low-distortion topology and its improved version is suggested for $\Sigma\Delta$ modulator implementation. Section 4.2 presents the utilization of the improved low-distortion topology for the MASH 2-1 architecture. MASH 2-1 architecture with improved low-distortion topology and resonation techniques are demonstrated in Section 4.3. Section 4.4 and Section 4.5 illustrates the SMASH 2-1 architecture and the improved SMASH architecture with resonation capable of one order higher noise shaping. The simulation results of MASH and SMASH architectures are provided in

Section 4.6 . Finally, Section 4.7 portrays the inferences from this chapter.

4.1 Improved Low-distortion Architecture

The block diagram of the traditional low-distortion architecture is shown in Figure 4.1 (Silva *et al.*, 2001). In low-distortion topology with unity STF, the integrators process only the quantization noise. The reduced signal swing associated with the integrator blocks in low-distortion topology relaxes the op-amp design. The low-distortion topology demands an analog feedforward adder at the quantizer input, which is often implemented by a delay-free power-hungry active block. Thus, an N^{th}order low-distortion $\Sigma\Delta$M needs 'N + 1' active components. This block, also, restricts the conversion speed of the quantizer. To alleviate these issues, an improved low-distortion topology was introduced as shown in Figure 4.2 (Taghizadeh and Sadughi, 2015). The shifted loop delay technique moves the last integrator delay into the feedback path, that is used to resolve the timing issues present in the feedback path. To keep the low-distortion property for the $\Sigma\Delta$M, the adder block in front of the quantizer is shifted to the input of last integrator with an extra feedback path in modulator loop. The architecture is now a hybrid version of FB and FF topologies. The number of active blocks, which are needed to implement the improved low-distortion $\Sigma\Delta$M, is reduced by one.

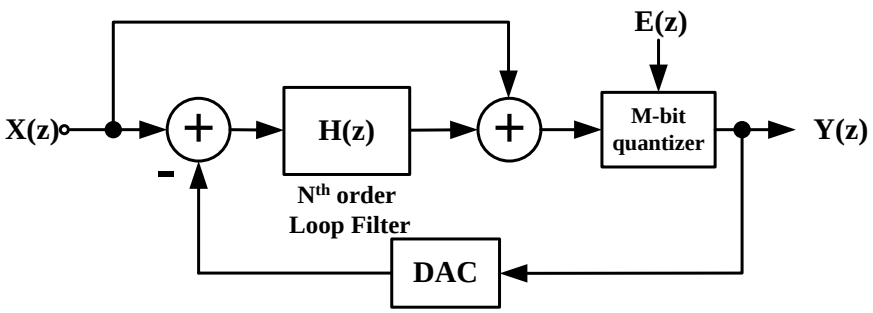


Figure 4.1: Traditional low-distortion architecture (Silva *et al.*, 2001)

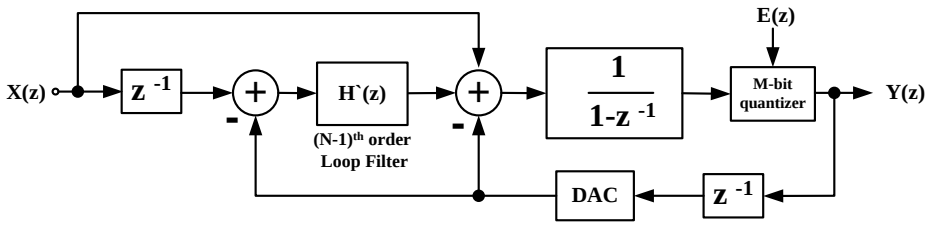


Figure 4.2: Improved low-distortion architecture (Taghizadeh and Sadughi, 2015)

4.2 Improved Low-distortion MASH 2-1 $\Sigma\Delta$ Architecture

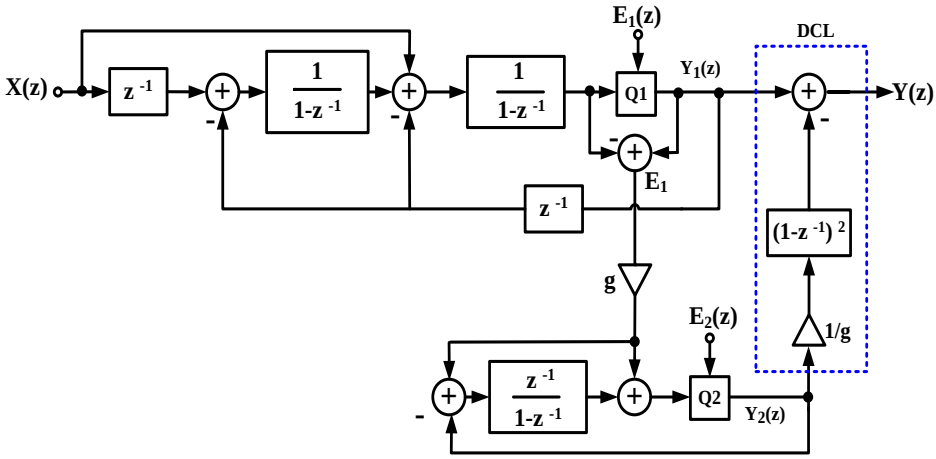


Figure 4.3: Improved low-distortion MASH 2-1 architecture

The MASH 2-1 $\Sigma\Delta$ modulator shown in Figure 4.3 utilizes an improved low-distortion topology in the first stage. This unity STF MASH modulator achieves a third order noise shaping. In this architecture, the adder block before the quantizer is shifted to the input of second integrator and an extra feedback path is inserted in the modulator loop. This saves one power hungry feedforward active adder usually required in multi-bit quantization. The output of the improved low-distortion MASH 2-1 modulator is expressed as

$$Y(z) = X(z) - \frac{1}{g}(1 - z^{-1})^3 E_2(z) \tag{4.1}$$

4.3 Proposed MASH 2-1 ΣΔ Architecture with Resonation

Several techniques have been proposed in the literature to enhance the noise shaping ability of modulator, especially in broadband applications with low OSR. Noise coupling techniques or error feedback modulator (Lee *et al.*, 2009; Prakash *et al.*, 2018), VCO-based quantizer (Straayer and Perrott, 2007), and resonation based structures (A.Morgado *et al.*, 2008; Beheshte and Yavari, 2017) are the commonly used techniques to enhance the order of NTF. The local resonation technique used in MASH structure enhances the resolution, but it affects the digital cancellation logic (A.Morgado *et al.*, 2008). In global resonation, a scaled version of last stage quantization noise is injected before the first quantizer with the help of inter-stage feedback paths (Beheshte and Yavari, 2017; Khazaeili and Yavari, 2014). The resonation techniques help to move the zeros of the NTF from dc to an optimal place in the signal band. The in-band quantization noise gets minimized by these shifting of zeros from dc to a frequency within the signal band (Schreier, 1993).

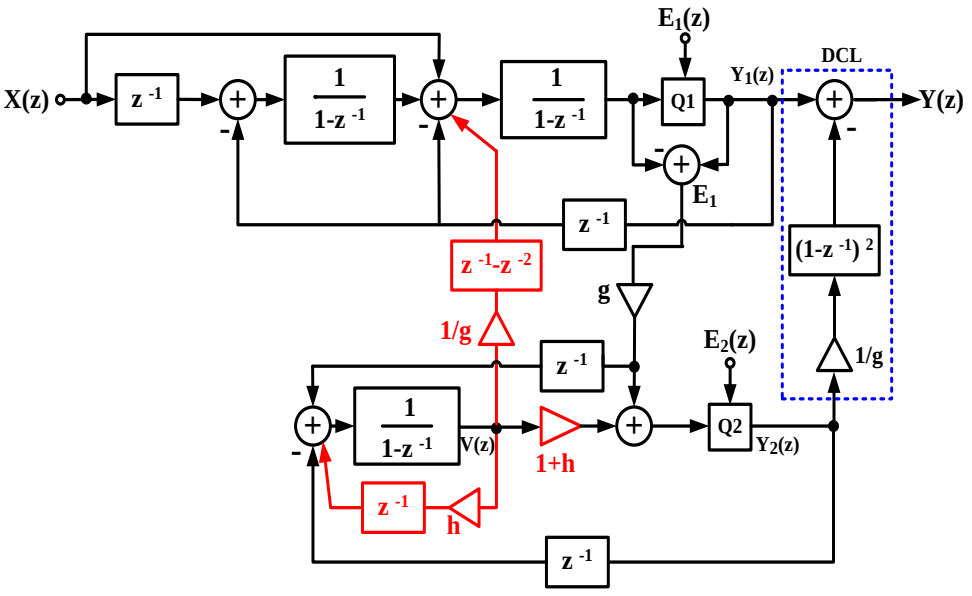


Figure 4.4: Proposed MASH 2-1 Modulator with resonation

Figure 4.4 shows the improved MASH 2-1 architecture with resonation. This third order modulator attains an enhanced fourth order noise shaping at the expense of few delay blocks. A portion of the second stage quantization noise injected into the first stage acts as a dither signal there. Moreover, the unity STF relaxes the analog circuit non-idealities. A shifted loop delay topology, introduces delay in the feedback path, which is used to relax the signal processing timing for Digital to Analog Conversion (DAC) and Dynamic Element Matching (DEM) techniques. The mathematical analysis of the proposed modulator shows, how a third order modulator can achieve a fourth order NTF using inter-stage feedback paths. The output of first and second stage of MASH structure is given by

$$Y_1(z) = X(z) + \frac{1}{g}z^{-1}(1-z^{-1})^2V(z) + E_1(z)(1-z^{-1})^2 \tag{4.2}$$

where $X(z)$,$Y_1(z)$, and $E_1(z)$ represents the input signal, output of the first stage and quantization noise of the first stage of MASH structure respectively. The inter-stage gain is represented by 'g'. V(z) is the output of the integrator in the second stage of MASH architecture.

$$Y_2(z) = [gE_1(z)z^{-1} - Y_2(z)z^{-1}]\frac{1+h}{1-z^{-1}(1+h)} + gE_1(z) + E_2(z) \tag{4.3}$$

The output and quantization noise of the second stage modulator are denoted by $Y_2(z)$, and $E_2(z)$ respectively.

The second stage of the proposed modulator shown in Figure 4.4 is simplified through block reduction methods and the resulting structure is shown in Figure 4.5. The integrator output in the second stage, V(z) is injected into the first stage through analog feedback paths. The V(z) signal is delayed and added at the input of last integrator in first stage. The signal V(z) can be obtained as

$$V(z) = \frac{1}{1-z^{-1}(1+h)}[gE_1(z)z^{-1} - Y_2(z)z^{-1}] \tag{4.4}$$

$$Y_2(z) = gE_1(z) + E_2(z)[1 - z^{-1}(1 + h)] \tag{4.5}$$

The NTF of the second stage modulator is

$$NTF_2(z) = 1 - z^{-1}(1 + h) \tag{4.6}$$

$$V(z) = -\frac{z^{-1}}{1 - z^{-1}(1 + h)} NTF_2(z)E_2(z) \tag{4.7}$$

$$V(z) = -z^{-1}E_2(z) \tag{4.8}$$

Substituting V(z) in equation (4.2), we get

$$Y_1(z) = X(z) - \frac{1}{g}z^{-2}(1 - z^{-1})^2E_2(z) + E_1(z)(1 - z^{-1})^2 \tag{4.9}$$

The overall output of the modulator is represented by Y(z)

$$Y(z) = Y_1(z) - \frac{1}{g_{dig}}(1 - z^{-1})^2Y_2(z) \tag{4.10}$$

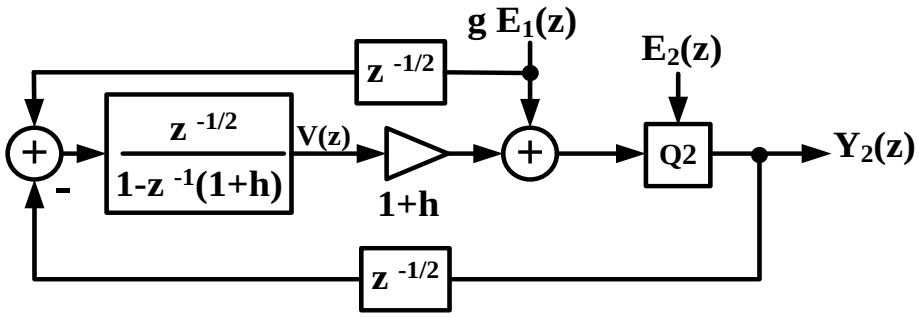


Figure 4.5: Simplified second stage of the proposed MASH Modulator

If there is good matching between analog and digital coefficients, then $g = g_{dig}$

$$Y(z) = X(z) - \frac{1}{g}(1 - z^{-1})^2[1 - z^{-1}(1 + h) + z^{-2}]E_2(z) \tag{4.11}$$

If the value of $h = 1$, then

$$Y(z) = X(z) - \frac{1}{g}(1 - z^{-1})^2[1 - 2z^{-1} + z^{-2}]E_2(z) \tag{4.12}$$

i.e.,

$$Y(z) = X(z) - \frac{1}{g}(1 - z^{-1})^4 E_2(z) \tag{4.13}$$

The output Y(z) contains the input signal and the shaped quantization noise of the second stage modulator. The first stage quantization noise has completely eliminated and the second stage noise is shaped by an NTF of order four.

4.3.1 Optimization of the NTF Zeros

The easiest method to have a further increase in SNDR, in higher order modulators utilized in wideband applications is to optimally place a pair of complex-conjugate zeros of the NTF from dc to a frequency f_0. The in-band quantization noise gets minimized by these shifting of zeros from dc to a frequency within the signal band. The reduction in in-band noise will ultimately result in a better SNDR value. In order to obtain an optimum value for 'h', lets examine an L^{th} order $\Sigma\Delta$ modulator. If $L \geq 2$, then the NTF can be represented by, $NTF(z) = (1-z^{-1})^{L-2}(1-\delta z^{-1}+z^{-2})$ (A.Hamoui and Martin, 2004)

Also $\delta \equiv 2cos\left(\frac{2\pi f_0}{f_s}\right)$, f_s is the signal bandwidth and f_0 is the frequency corresponding to the optimal place where the zeros are shifted from dc. The value of f_0 can be found by,

$$f_0 = \sqrt{\frac{2L-3}{2L-1}} f_{BW} \tag{4.14}$$

where 'L' is the order of NTF and f_{BW} is the signal bandwidth, the optimum value for the coefficient 'h' is

$$h = 2cos\left(\frac{2\pi f_0}{f_s}\right) - 1 \tag{4.15}$$

The value of 'h' corresponding to maximum SNDR can also be verified using behavioral simulations. Figure 4.6 shows the variation of SNDR with the coefficient 'h'. It also confirms that the maximum value of SNDR will be obtained, when 'h' hold the value 0.89. The pole-zero plot provides the location of the NTF zeros. Since the NTF is of order four in the proposed architecture, there are four zeros. Figure 4.7 shows the position of zeros, two zeros are located at dc and the shifted complex conjugate pair zeros are located at $0.945 \pm 0.327i$, which is within the signal band. By adjusting the value of a single coefficient 'h', we were able to optimize the NTF zeros.

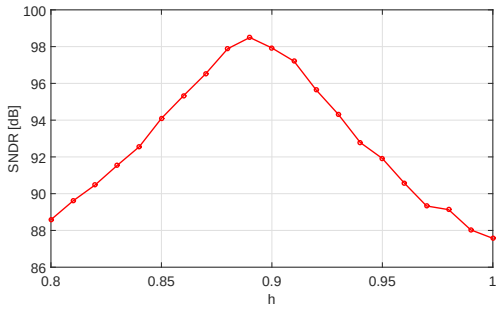


Figure 4.6: Variation of SNDR with coefficient 'h'

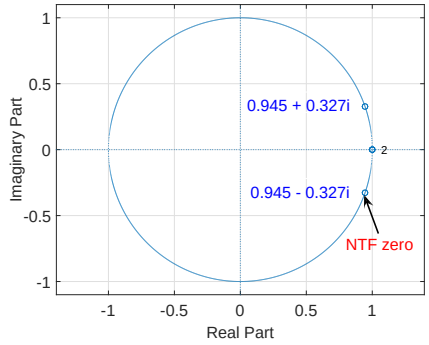


Figure 4.7: Location of the optimized NTF zeros

4.3.2 Shifted Loop Delays for Relaxed Timing

In the proposed MASH structure, the half clock period delay ($z^{-1/2}$) of the first integrator is shifted to the input signal and feedback paths as seen in Figure 4.8. The half delay in the feedback path helps to relax the speed requirement for DEM logic operation, which can be easily realized in transistor level by holding half phase. This modulator also shifts one loop delay (z^{-1}) from the second integrator of first

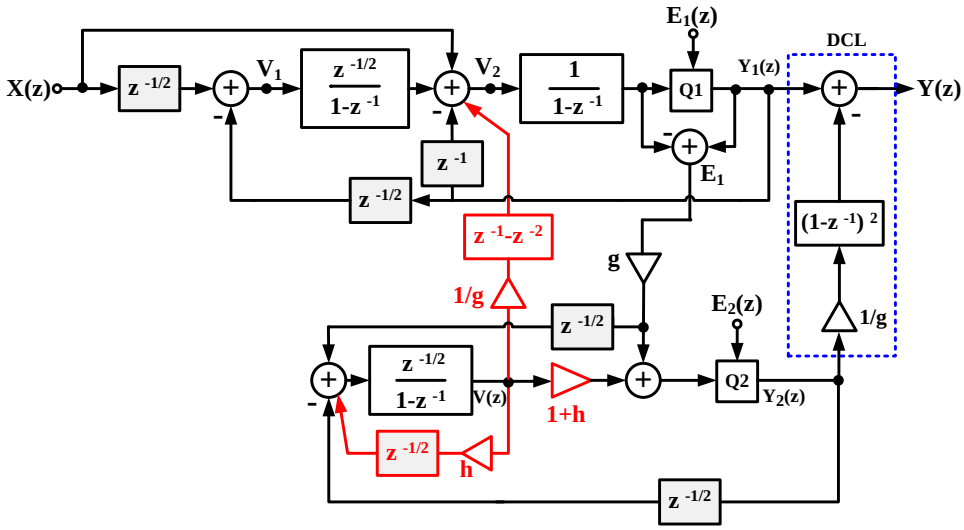


Figure 4.8: Shifted loop delays in the proposed MASH 2-1 Modulator with resonation

stage into the newly formed feedback branch to stabilize the loop. The delay in the input signal path helps to maintain the low-distortion property. Both stages of this architecture uses the shifted loop delay techniques.

4.4 Improved Low-distortion SMASH 2-1 $\Sigma\Delta$ Architecture

Figure 4.9 shows the improved low-distortion SMASH 2-1 architecture. The quantization noise of the first stage ($E_1(z)$) is extracted and it is provided as an input to the second stage of SMASH structure.The output of the second stage is digitally subtracted inside the first stage loop and the first stage quantization noise gets eliminated. The output (Y(z)) contains only the shaped quantization noise of the second stage. The output of the improved low-distortion SMASH 2-1 modulator is expressed as

$$Y(z) = X(z) - \frac{1}{g}(1 - z^{-1})^3 E_2(z) \tag{4.16}$$

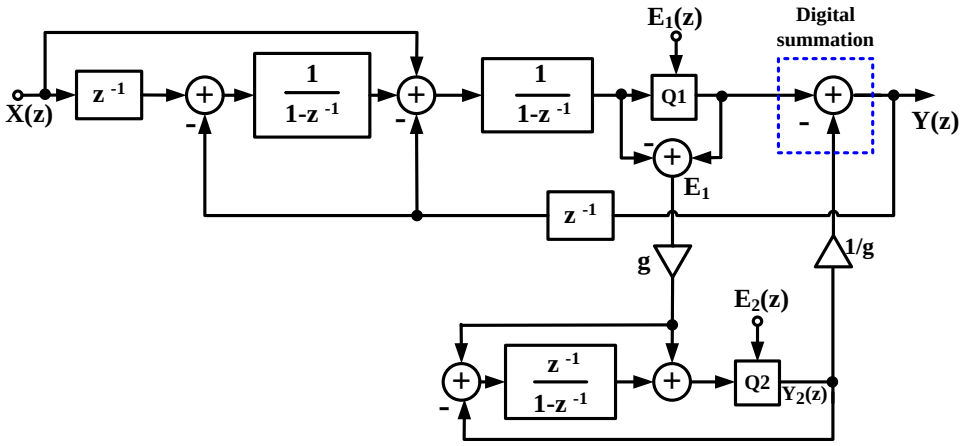


Figure 4.9: Improved low-distortion SMASH 2-1 architecture (Taghizadeh and Sadughi, 2015)

4.5 Proposed SMASH 2-1 ΣΔ Architecture with Resonation

Figure 4.10 shows the proposed improved low-distortion SMASH 2-1 architecture with resonation. The inter-stage feedback paths and the feedback path introduced

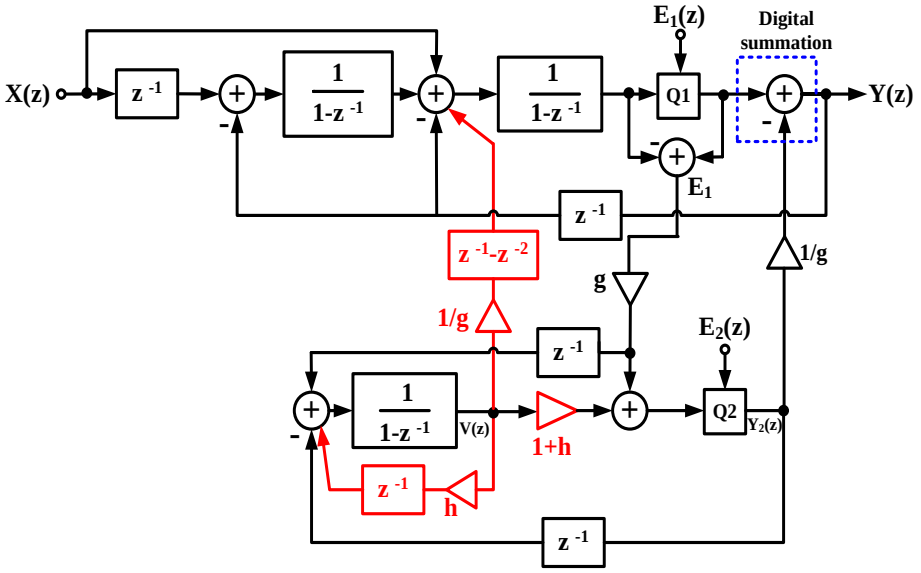


Figure 4.10: Proposed SMASH 2-1 ΣΔ architecture with resonation

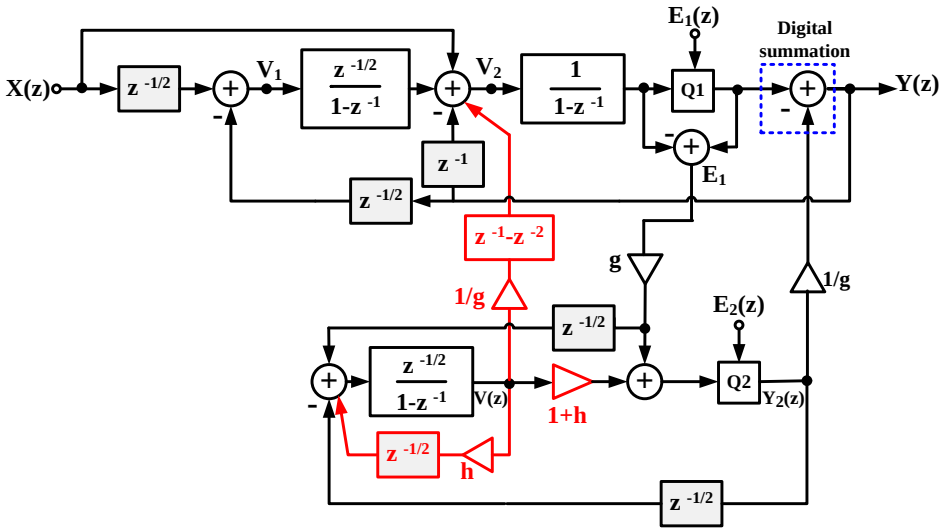


Figure 4.11: Shifted loop delays in the proposed SMASH 2-1 Modulator with resonation

between the output and input of the integrator in the second stage contributes for a reduction in the inband noise. An enhancement of one order higher noise shaping is achieved by this architecture. The output of the modulator is given by

$$Y(z) = X(z) - \frac{1}{g}E_2(z)(1 - z^{-1})^2[1 - (1 + h)z^{-1} + z^{-2}] \tag{4.17}$$

In equation (4.17), if the value of 'h' is chosen to be equal to 1, then

$$Y(z) = X(z) - \frac{1}{g}E_2(z)(1 - z^{-1})^4 \tag{4.18}$$

Equation (4.18) denotes the elimination of $E_1(z)$ and the fourth order shaping of the quantization noise $E_2(z)$.

The shifting of loop delays are also extended to SMASH structure, which in turn relaxes the timing issues in the critical path of modulator. Figure 4.11 shows the shifted loop delays in the proposed SMASH structure with resonation.

4.6 Simulation Results of the MASH and SMASH Architectures with Resonation

The behavioral simulations were conducted to evaluate the performance of the proposed MASH/SMASH architecture with resonation using MATLAB and SIMULINK. The OSR, bandwidth (BW) and sampling frequency (Fs) used in all the simulation were 8, 10 MHz and 160 MHz respectively. Four bit quantizers were used in both stages of the modulator with an inter-stage gain (g) of value 4. Figure 4.12 and Figure 4.13 depicts the PSD plot comparison between the proposed MASH/SMASH architecture and the conventional feedforward MASH/SMASH structure. We can observe a notch near 10 MHz for the proposed MASH/SMASH, which is lying inside the signal band [0, f_{BW}]. The optimal value of the coefficient 'h' places a pair of complex conjugate NTF zeros inside the signal bandwidth and it will leads to a reduction in in-band noise. This will contribute to a further increase in the resolution of the proposed MASH/SMASH structure. The PSDs of MASH and SMASH looks similar when simulations where conducted using MATLAB/SIMULINK with

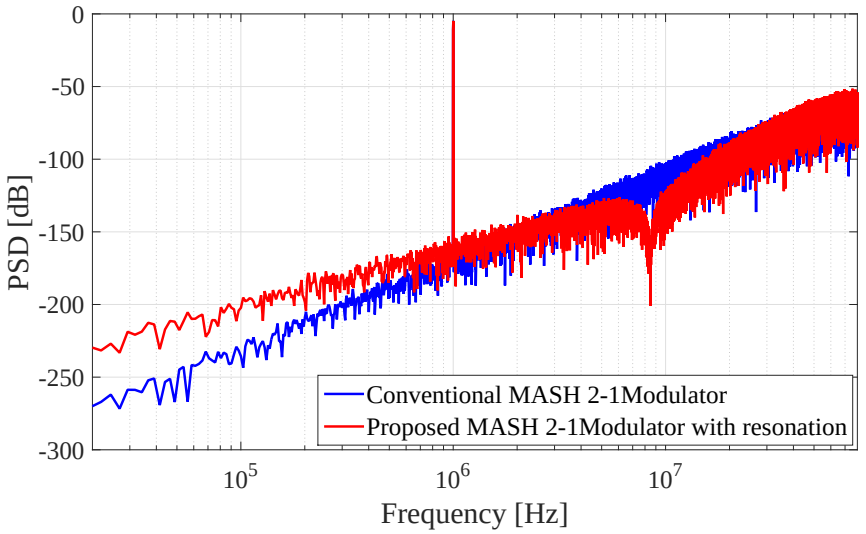


Figure 4.12: Output spectra of the conventional MASH 2-1 Modulator and MASH 2-1 Modulator with resonation (proposed)

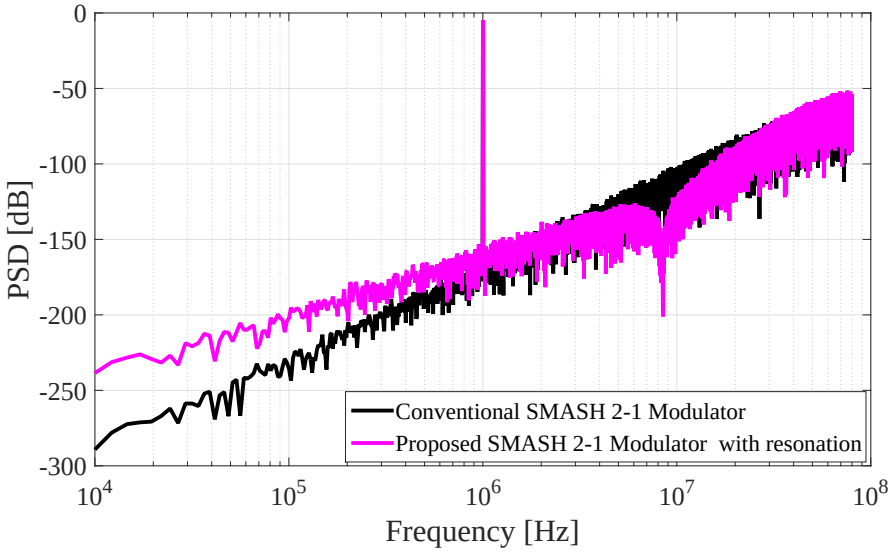


Figure 4.13: Output spectra of the conventional SMASH 2-1 Modulator and SMASH 2-1 Modulator with resonation (proposed)

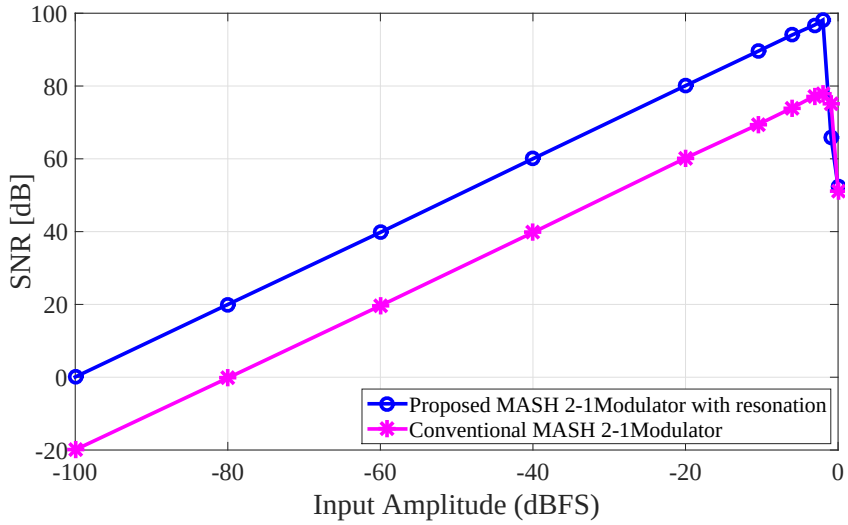


Figure 4.14: Variation of SNR against input signal amplitude for MASH architecture

ideal blocks. The proposed MASH/SMASH architecture along with the traditional MASH/SMASH architectures were simulated, and plotted the SNR against input amplitude swept from -100 dB to 0 dB as shown in Figure 4.14 and Figure 4.15. The PSDs of the node voltages V_1, V_2, V, Y_1, Y_2 and Y marked in Figure 4.8 and Figure 4.11 are depicted in Figure 4.16. The node V_1 is before the first integrator, its

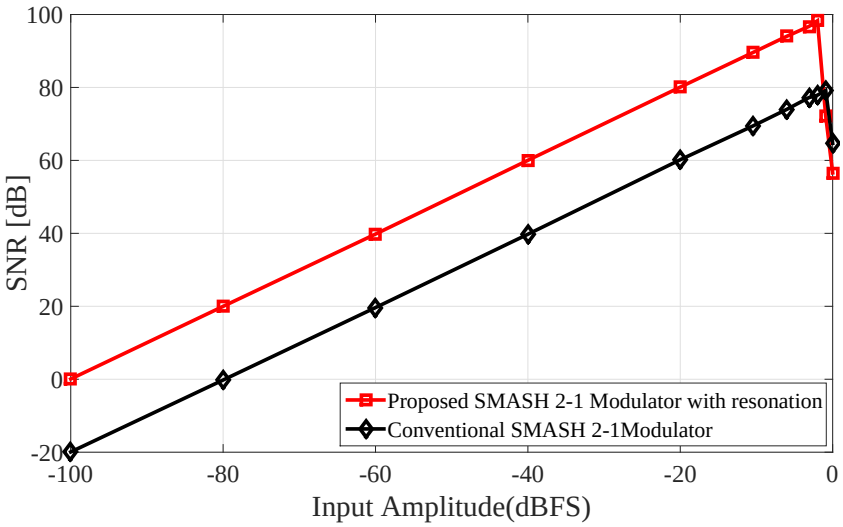
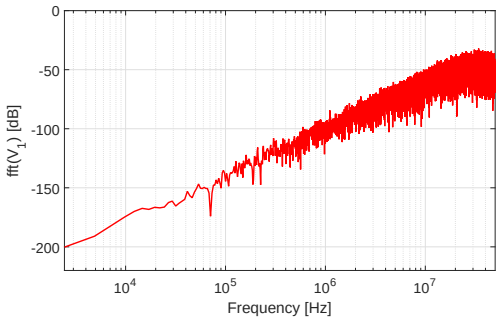


Figure 4.15: Variation of SNR against input signal amplitude for SMASH architecture

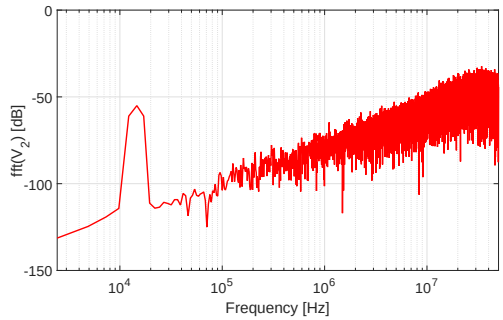
PSD plot indicates the absence of any signal component because of low-distortion topology. A comparison of the output swing of the three integrators in the proposed MASH/SMASH architecture is shown in Figure 4.17. The histogram output of the first integrator shows the presence of quantization error alone due to the swing suppression feature of the low-distortion topology. Since the feedforward input is directly added at the input of the second integrator, its output swing is more compared to other integrators.

4.6.1 Non-ideality Analysis

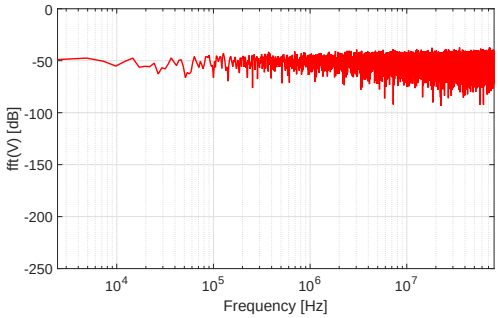
The analysis of the proposed MASH/SMASH modulator against different non-idealities like finite op-amp gain, finite slew rate and finite gainbandwidth (GBW) were performed based on the models proposed in (Malcovati *et al.*, 2003). In order to have a fair comparison in the result, all the structures were simulated for the same OSR, BW and Fs. Input amplitude of -2 dB with reference to the full-scale level is used to compare the SNDR. The variation in SNDR of the proposed architectures as a function of op-amp gain and GBW is shown in Figure 4.18. The minimum gain required for



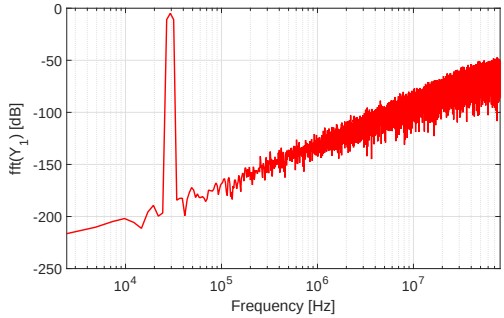
(a) Spectrum of V_1



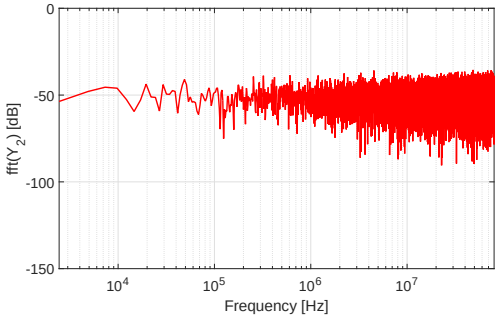
(b) Spectrum of V_2



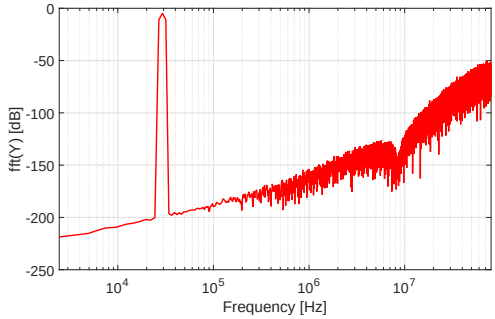
(c) Spectrum of V



(d) Spectrum of Y_1



(e) Spectrum of Y_2



(f) Final output spectrum, Y

Figure 4.16: Spectrum of the node voltages of the proposed MASH/SMASH modulator

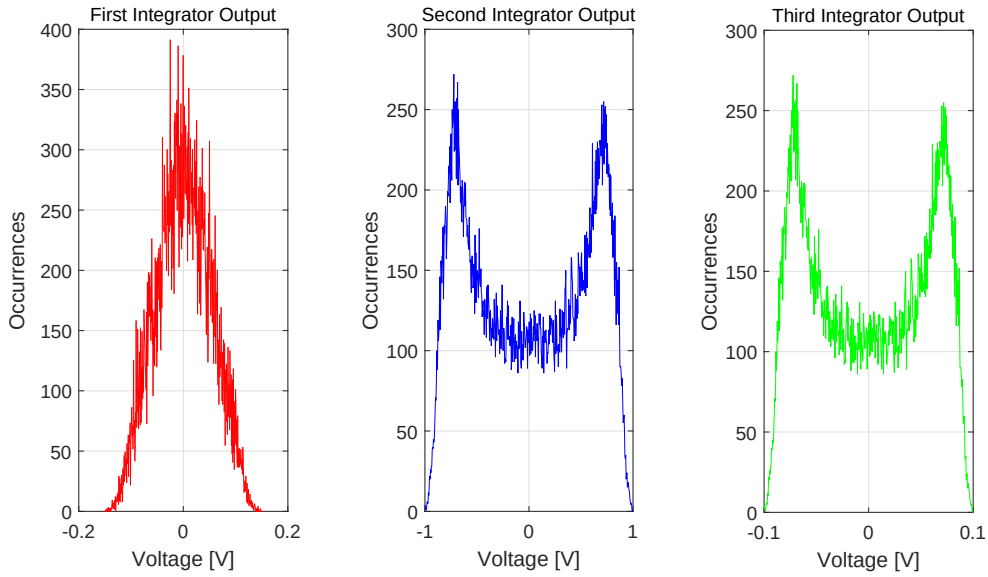
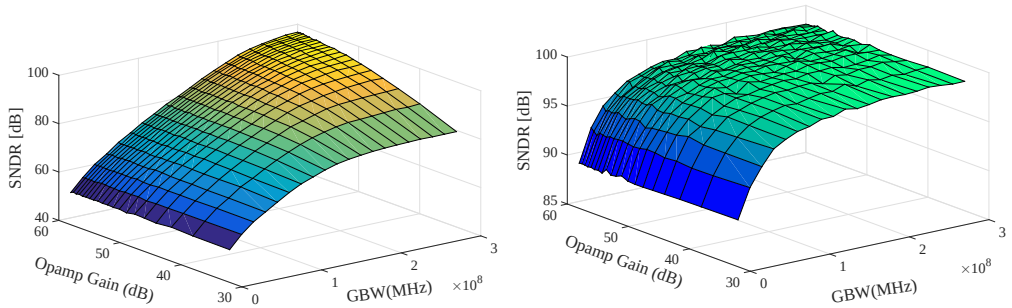


Figure 4.17: Output swing of the integrators in the proposed MASH/SMASH modulator

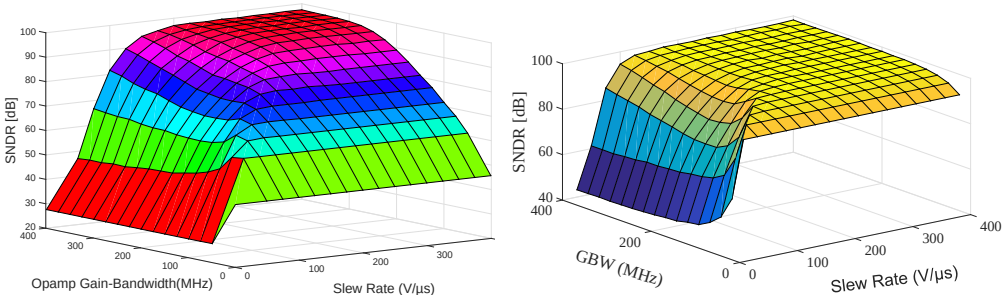


(a) MASH 2-1 with resonation

(b) SMASH 2-1 with resonation

Figure 4.18: SNDR variation of the proposed MASH/SMASH architecture as a function of Op-amp Gain and GBW

the op-amp in the proposed MASH modulator is 60 dB. The op-amp gain and GBW requirements are relaxed in the case of SMASH architecture. The variation in SNDR of the proposed architecture as a function of GBW and slew rate is shown in Figure 4.19.



(a) MASH 2-1 with resonation (b) SMASH 2-1 with resonation

Figure 4.19: SNDR variation of the proposed MASH/SMASH architecture as a function of GBW and Slew-rate

4.6.2 Matching Requirements in MASH Architecture

The matching between the analog and digital circuits is highly essential in MASH structures, otherwise it may lead to the leakage of quantization noise. A good matching between analog loop filter and digital noise cancellation filters often demand high gain operational amplifiers and accurate modulator coefficients. The SNDR value is sensitive to the disparity between digital and analog coefficients. The degradation in SNDR versus mismatch between the analog coefficient (g) and digital coefficient (g_{dig}) in the proposed architecture is shown in Figure 4.20. A $\pm 5\%$ variation in analog and digital coefficients leads to a degradation of 22 dB in SNDR.

The scaling coefficients are realized in circuit level by the ratio of sampling and integrating capacitances. The architecture proposed here is tested against the effect of capacitor mismatches by performing a Monte Carlo simulation of 1000 iterations. The degradation in the value of SNR due to mismatch in capacitor values can be analysed through this simulation. The simulations were conducted for the capacitor value C_G (corresponds to the inter-stage gain 'g') by assuming a mismatch of $\pm 1\%$ in the capacitor values. The capacitor values are randomly selected, gaussian distributed and the resulting SNR values are plotted. The histogram output based on Monte Carlo simulation are shown in Figures 4.21. The performance summary of the

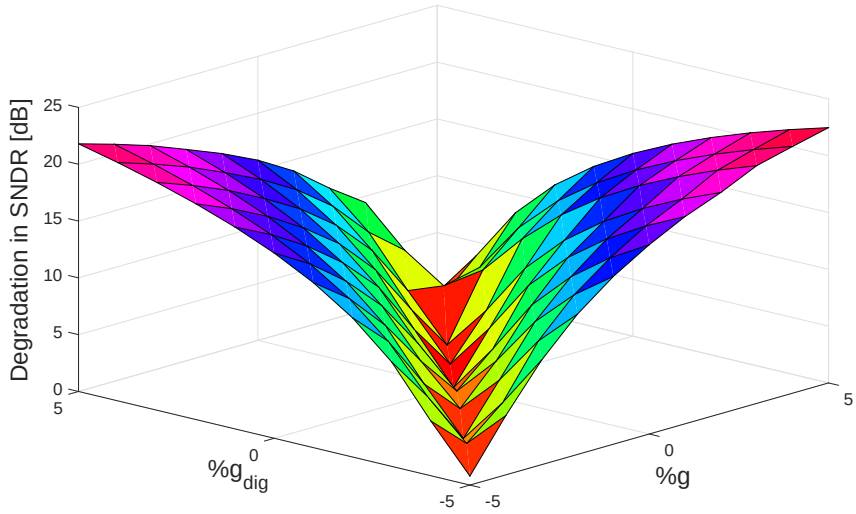
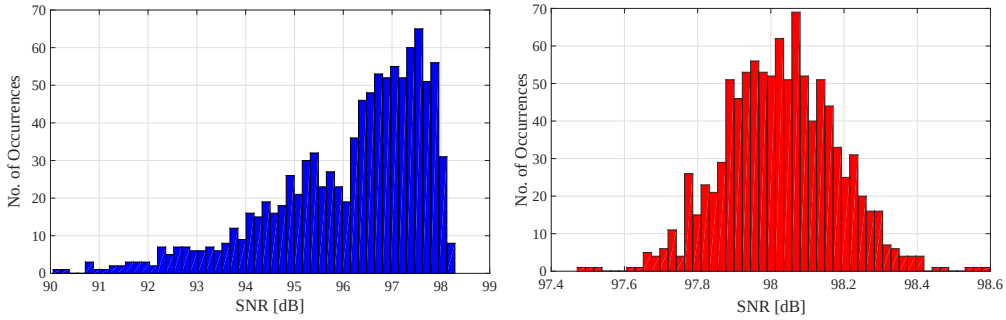


Figure 4.20: SNDR variation versus mismatch between analog inter-stage gain 'g'and its digital estimate 'g_{dig}'



(a) MASH 2-1 with resonation

(b) SMASH 2-1 with resonation

Figure 4.21: Monte Carlo simulations for Capacitor mismatch

proposed MASH/SMASH architecture with resonation is shown in Table 4.1. The proposed MASH and SMASH modulators achieves an SNR_p of value 98.5 dB and a dynamic range of 99 dB. The proposed MASH/SMASH structure attains a 20 dB increase in SNR and saves one feedforward adder, when compared with conventional feedforward MASH/SMASH modulator.

Table 4.1: Performance comparison of the proposed MASH/SMASH 2-1 modulator with the conventional MASH/SMASH 2-1 Modulator

Parameter	Proposed MASH 2-1	Conventional MASH 2-1	Proposed SMASH 2-1	Conventional SMASH 2-1
Fs	160 MHz	160 MHz	160 MHz	160 MHz
Bandwidth	10 MHz	10 MHz	10 MHz	10 MHz
OSR	8	8	8	8
SNR_p (dB)	98.5	78.2	98.5	78.2
DR	99	79	99	79
Order of NTF	4	3	4	3
No. of Integrators	3	3	3	3
No. of feedforward adder	1	2	1	2

4.7 Chapter Summary

A resonation based cascaded $\Sigma\Delta$ architecture that enhances the resolution with fewer active blocks is presented. The enhancement in the resolution is achieved through inter-stage paths and NTF zero optimization methods. The low-distortion architecture, reduction in active components and elimination of a power hungry adder helps this modulator to be used in low power applications. The shifted loop delay techniques solves the timing issues in the critical path of the modulator. The behavioral simulations, mathematical analysis and an SNDR and dynamic range of value above 90 dB prove the fitness of this modulator to be used in wideband applications.

CHAPTER 5

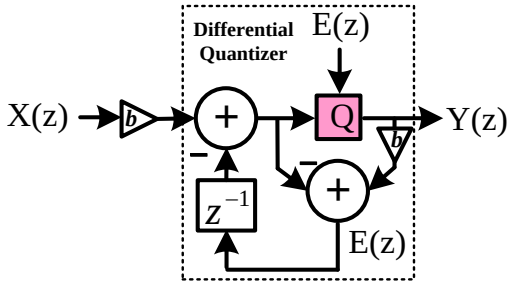
LOWPASS MASH DQEFM FOR 4G WIRELESS RECEIVERS

The design and simulation of a lowpass MASH Differential Quantizer based Error Feedback Modulator (DQEFM) architecture is presented in this chapter. The DQEFM structure has been incorporated for obtaining benefits like relaxed op-amp requirements and reduced sensitivity to mismatch effects. The lower operating frequency and better performance of the proposed modulator in terms of hardware complexity and power makes it suitable for data conversion in 4G wireless receivers. The performance of the proposed modulator has also been evaluated through circuit-level simulations using 45nm CMOS process.

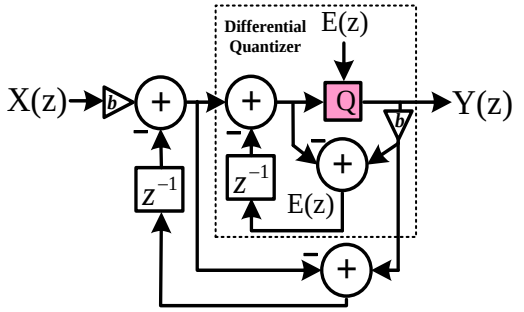
This chapter is structured as follows. Section 5.1 presents the lowpass DQEFM architecture and its mathematical representation. Section 5.2 describes the cascaded DQEFM structure intended for data conversion in wide bandwidths. Simulation results are provided in Section 5.3. The circuit-level simulation details are provided in Section 5.4. Finally, Section 5.5 concludes this chapter.

5.1 Lowpass Differential Quantizer based Error Feedback Modulator Architecture

The newly introduced differential quantizer based error feedback modulator (DQEFM) (Prakash *et al.*, 2018) also belongs to the category of noise shaping data converters. The first and second order lowpass DQEFM (LP DQEFM) architecture, is represented in Figure 5.1. The quantization error extracted by taking the difference between the input and output of the quantizer (so the name differential quantizer), is delayed by



(a) First order Lowpass DQEFM architecture



(b) Second order Lowpass DQEFM architecture

Figure 5.1: Lowpass DQEFM architecture (Prakash *et al.*, 2018)

one clock cycle before it is being fed back to the input of the modulator. The $X(z)$, $Y(z)$ and $E(z)$ represents input, output and the quantization error respectively. The mathematical representation of the first and second order LP DQEFM is given in equations (5.1) and (5.2) respectively. The value chosen for the scaling coefficient 'b'is unity while deriving these equations.

$$Y(z)_{LPDQM1} = X(z)_{LPDQM1} + (1 - z^{-1})E(z)_{LPDQM1} \tag{5.1}$$

$$Y(z)_{LPDQM2} = X(z)_{LPDQM2} + (1 - z^{-1})^2 E(z)_{LPDQM2} \tag{5.2}$$

The mathematical equations for DQEFM indicates that the STF is unity and the NTF is of highpass nature.

5.2 Cascaded Lowpass DQEFM Architecture

Higher order DQEFM structures are often needed to meet the large dynamic range (DR) requirement of data converters used in wideband application. The proposed cascaded LP DQEFM structure is intended for data conversion in fourth generation (4G) wireless standards. A fourth order LP DQEFM made by cascading two second order stable modulators, is chosen for the proposed 4G Long Term Evolution (LTE) standard. The block diagramatic representation of the fourth order MASH DQEFM modulator is shown in Figure 5.2. The detailed architecture of the MASH 2-2 DQEFM with error cancellation logic is illustrated in Figure 5.3. 3-bit quantizers utilized in each stage of the modulator provides better stability, enhances the resolution and relaxes the scaling coefficient values.

The mathematical analysis of the proposed LP MASH 2-2 DQEFM architecture is

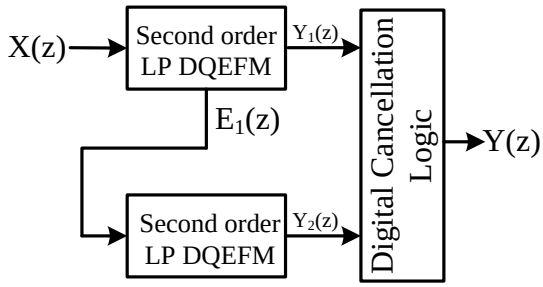


Figure 5.2: Block Diagram of the proposed Lowpass MASH 2-2 DQEFM

given by

$$Y_1(z)_{LPDQM2} = X(z)_{LPDQM2} + (1 - z^{-1})^2 E_1(z)_{LPDQM2} \tag{5.3}$$

$$Y_2(z)_{LPDQM2} = gE_1(z)_{LPDQM2} + (1 - z^{-1})^2 E_2(z)_{LPDQM2} \tag{5.4}$$

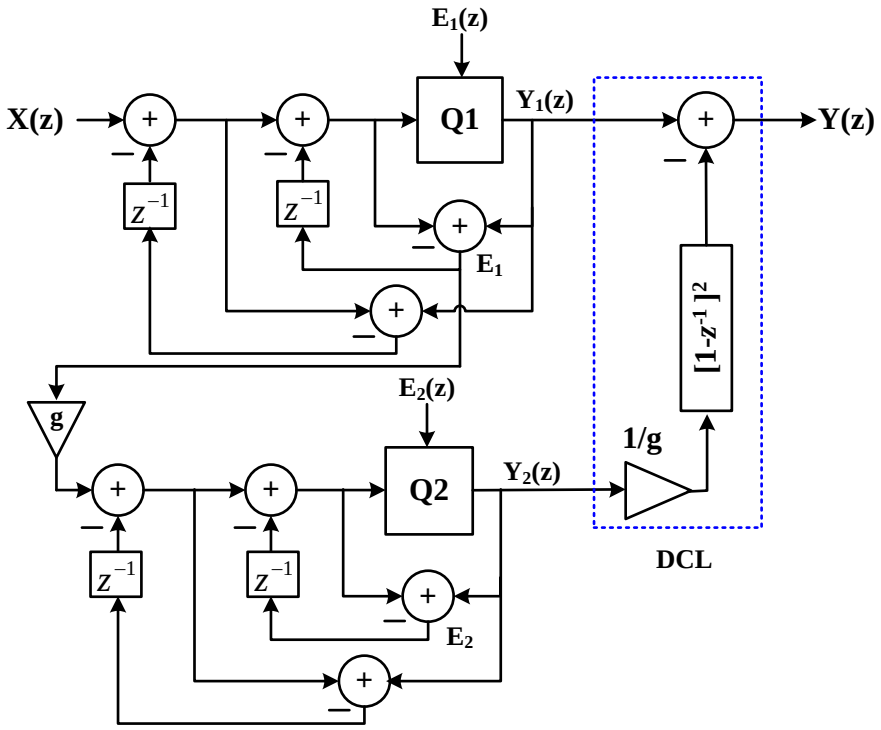


Figure 5.3: Proposed Lowpass MASH 2-2 DQEFM Architecture

where $X(z)_{LPDQM2}$, $Y_1(z)_{LPDQM2}$, and $E_1(z)_{LPDQM2}$ denotes the input signal, output of the first stage and quantization noise of the first stage of MASH modulator. The output of the second stage and quantization error associated with second stage quantizer are denoted by $Y_2(z)_{LPDQM2}$ and $E_2(z)_{LPDQM2}$ respectively. The gain between the stages is denoted by 'g' and the overall output of the proposed modulator is given by

$$Y(z)_{LPDQ22} = Y_1(z)_{LPDQM2} - \frac{1}{g}(1 - z^{-1})^2 Y_2(z)_{LPDQM2} \tag{5.5}$$

$$Y(z)_{LPDQ22} = X(z)_{LPDQ22} - \frac{1}{g}(1 - z^{-1})^4 E_2(z)_{LPDQ22} \tag{5.6}$$

where

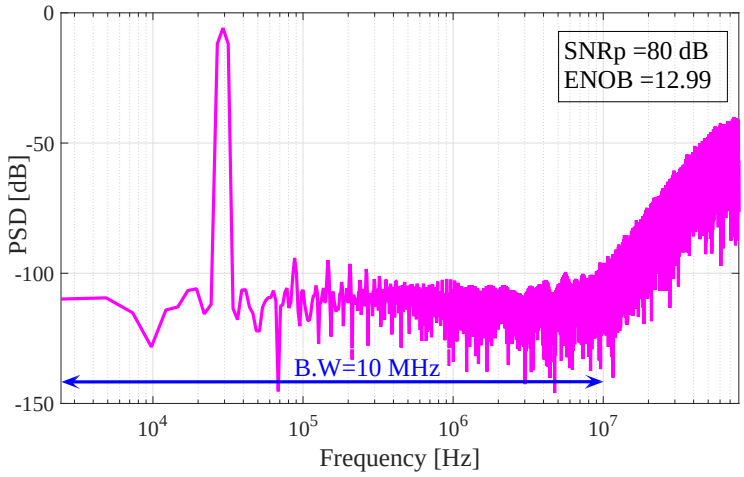
$$STF_{LPDQ22} = 1, \quad NTF_{LPDQ22} = (1 - z^{-1})^4 \tag{5.7}$$

Here STF_{LPDQ22}, NTF_{LPDQ22}, $X(z)_{LPDQ22}$, $E_2(z)_{LPDQ22}$ and $Y(z)_{LPDQ22}$ represents STF, NTF, input signal, quantization error of the second stage and the overall output of the MASH LP DQEFM respectively. The quantization error associated with the first stage, i.e. $E_1(z)$ has been completely eliminated by selecting an appropriate Digital Cancellation Logic (DCL) and the second stage quantization noise is shaped by a NTF of order equal to four.

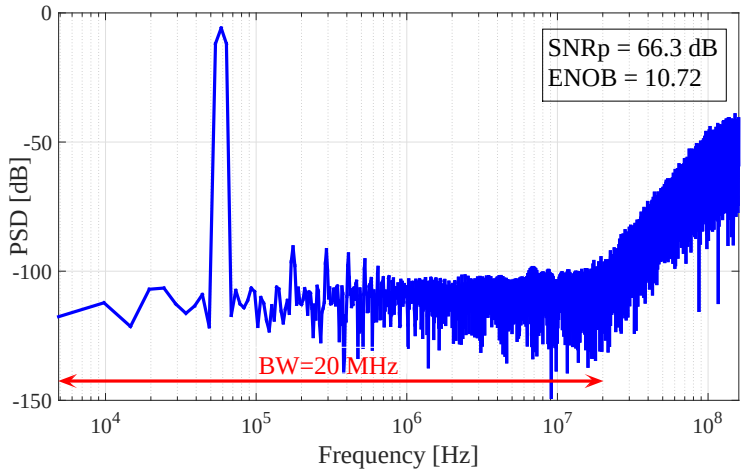
5.3 Simulation Results for LP MASH DQEFM Architecture

The proposed architecture has been simulated for the most commonly used bandwidths in LTE technology using MATLAB/SIMULINK and the output spectra are depicted in Figure 5.4(a) and Figure 5.4(b). The variation in SNR against different input amplitude for the proposed architecture is plotted in Figure 5.5. The error feedback structure contributes to an increase in the overload level (OL) value, which extends the dynamic range. The different op-amp non-ideal effects such as finite op-amp gain, finite gain bandwidth (GBW), finite slew rate and saturation voltages which limit the performance of the modulator were simulated and analysed using the models provided in (Malcovati *et al.*, 2003). The simulations were performed for the bandwidths 10 and 20 MHz. The effect due to each non-ideality on the SNDR is simulated and the resulting plots obtained for each non-ideality are depicted in Figure 5.6(a) to Figure 5.6(c). The op-amp requirements are relaxed in the case of proposed modulator as indicated by Figure 5.6(a). An op-amp with 40 dB gain is sufficient to attain the required SNDR in each mode and the GBW requirement for the modulator is around 400 MHz.

The performance of the MASH DQEFM is also limited by the mismatch between the



(a)



(b)

Figure 5.4: Output spectra in different LTE modes (a) 10 MHz BW (b) 20 MHz BW

analog and digital circuits. Since the different LTE modes uses the same hardware, the worst case analysis to find the effect of mismatch is the analysis of 20 MHz bandwidth. The decline in SNDR due to this mismatch effects are shown in Figure 5.7. A reduction of 6 dB in SNDR is noted when the analog inter-stage gain (g) and its corresponding digital estimate (g_{dig}) are varied $\pm 5\%$ for the proposed MASH DQEFM modulator. This indicates the less sensitivity of proposed MASH DQEFM structure towards mismatch effects. The performance summary of the proposed modulator obtained through behavioral level simulations for 10 MHz and 20 MHz LTE bandwidths

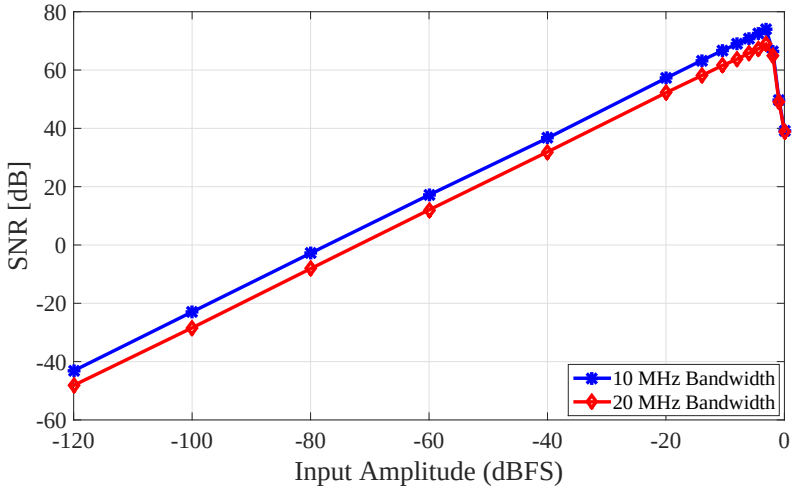
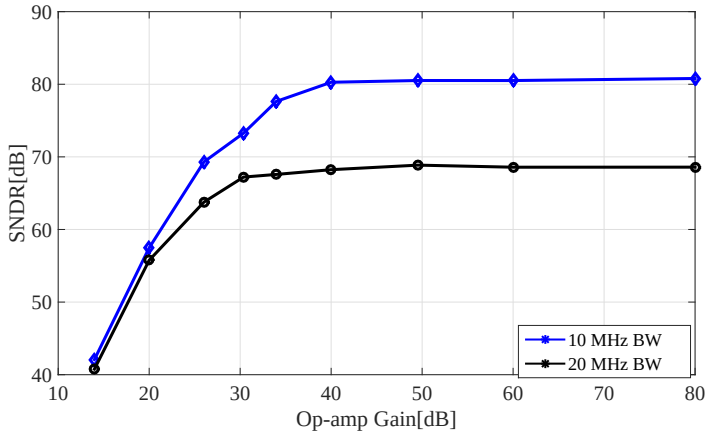


Figure 5.5: SNR variation with different input amplitude

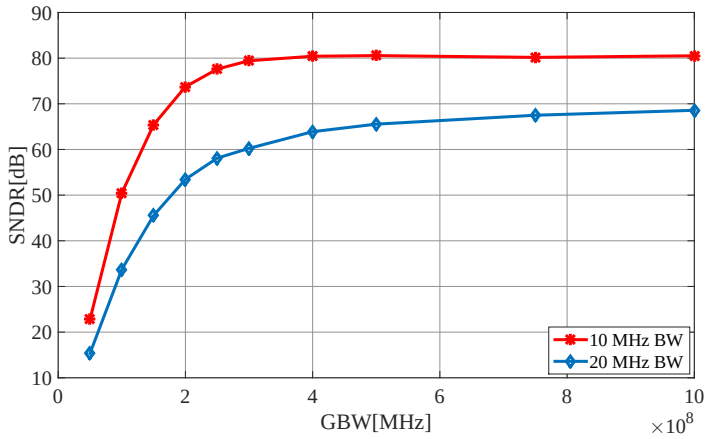
are described in Table 5.1. The proposed architecture attains a higher SNR value with low sampling frequency. The selection of low sampling frequency reduces the power consumption and also relaxes the requirements of analog circuit components.

Table 5.1: Performance Summary of the proposed LP MASH DQEFM in different LTE bandwidths

LTE Bandwidth	**10 MHz**	**20 MHz**
OSR	8	8
Fs [MHz]	160	320
No. of samples	65536	65536
Input frequency (Fin) KHz	29.3	58.8
SNRp [dB]	80	66.3
ENOB (bits)	12.99	10.72



(a)



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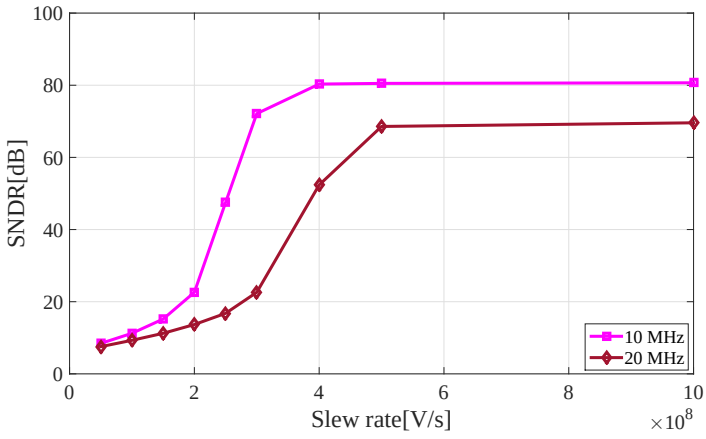


(c)

Figure 5.6: Variation of SNDR against different op-amp non-idealities (a) SNDR vs Op-amp gain (b) SNDR vs GBW (c) SNDR vs Slew rate

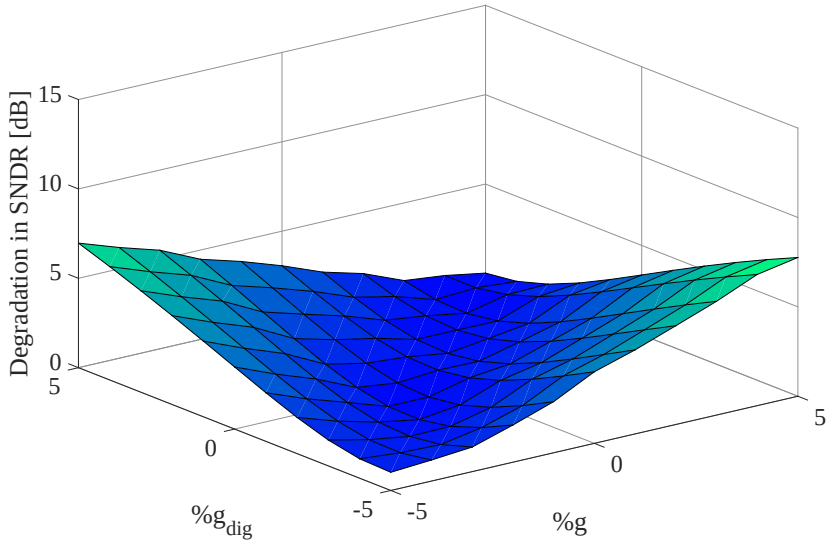


Figure 5.7: Degradation in SNDR versus mismatch between analog inter-stage gain 'g'and its digital estimate 'g_{dig}'

5.4 Circuit Level Simulation of the LP MASH DQEFM

The circuit level simulation of the proposed MASH DQEFM has been performed using HSPICE.

5.4.1 Switched Capacitor Implementation of the LP MASH DQEFM

The single ended switched capacitor (SC) implementation of the proposed LP MASH DQEFM using sample and hold (S/H) circuit is shown in Figure 5.8. The circuit is operated with two non-overlapping clocks ϕ_1 and ϕ_2.

5.4.2 The Operational Transconductance Amplifier (OTA)

The operational transconductance amplifier (OTA) used for the switched capacitor(SC) circuit implementation of the proposed modulator is a folded-cascode OTA with a class AB output buffer, which is shown in Figure 5.9 (Baker, 2008). The open loop

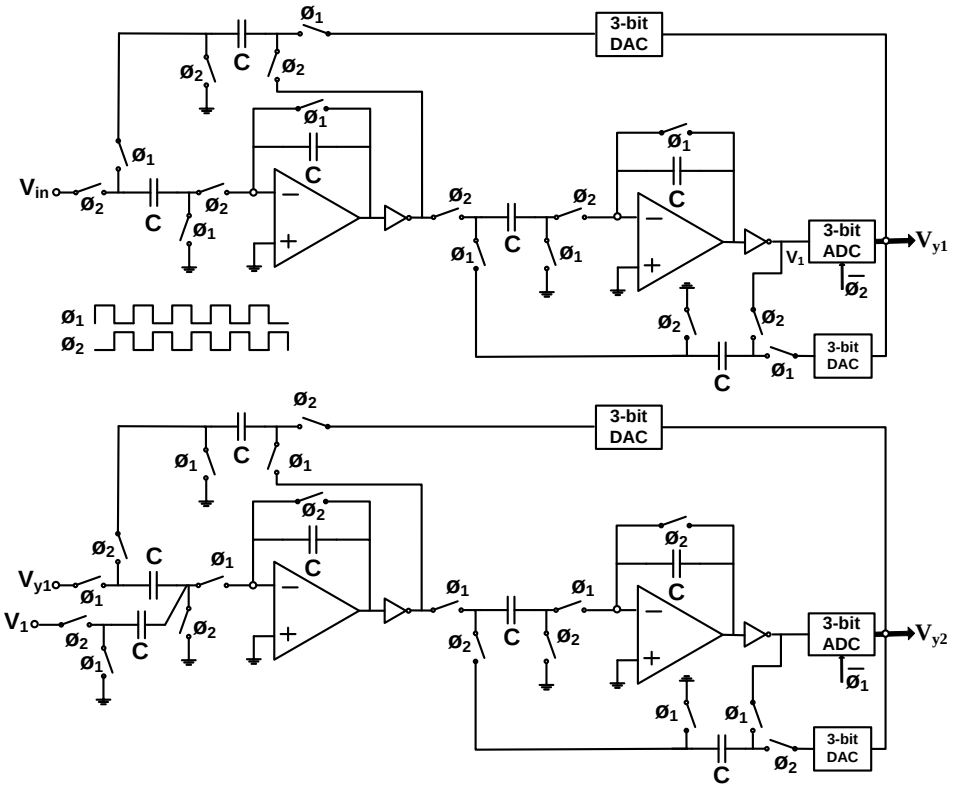


Figure 5.8: Single ended SC Circuit Implementation of LP MASH 2-2 DQEFM

gain and the phase response of this OTA are shown in Figure 5.10. It attains a gain of 53 dB, unity gain-bandwidth of 470 MHz, phase margin of 77 degree and has a settling time of 5 ns. To measure the settling time and slew rate for this OTA, a step input is applied at the input of OTA driving a 1pF capacitive load. This response is shown in Figure 5.11. As the load capacitance increases, slew rate of the OTA decreases, therefore slew rate is specified at a particular value of load capacitance. The detailed summary of this OTA is described in Table 5.2.

5.4.3 Clocked Comparator

A wide swing clocked comparator (shown in Figure 5.12), which uses long-length MOSFETs, was used to get a better immunity to kick-back noise (Baker, 2008). The

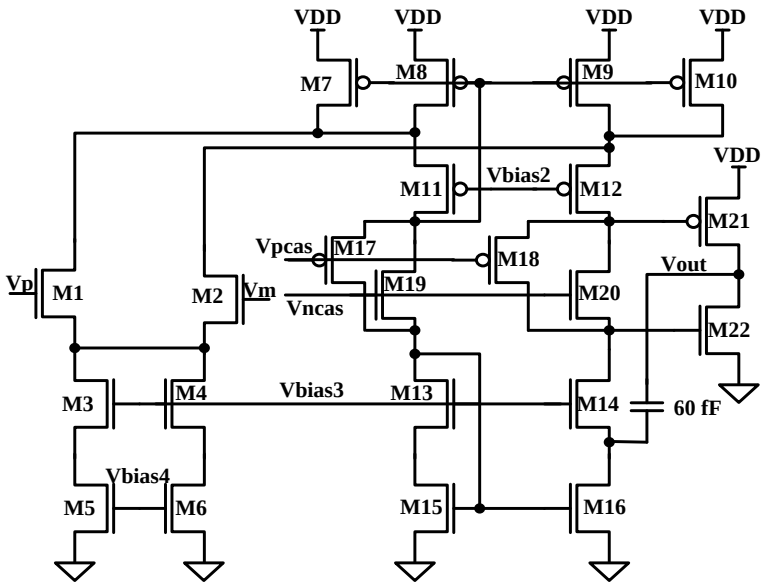


Figure 5.9: The folded cascode Operational Transconductance Amplifier (OTA) of high output resistance

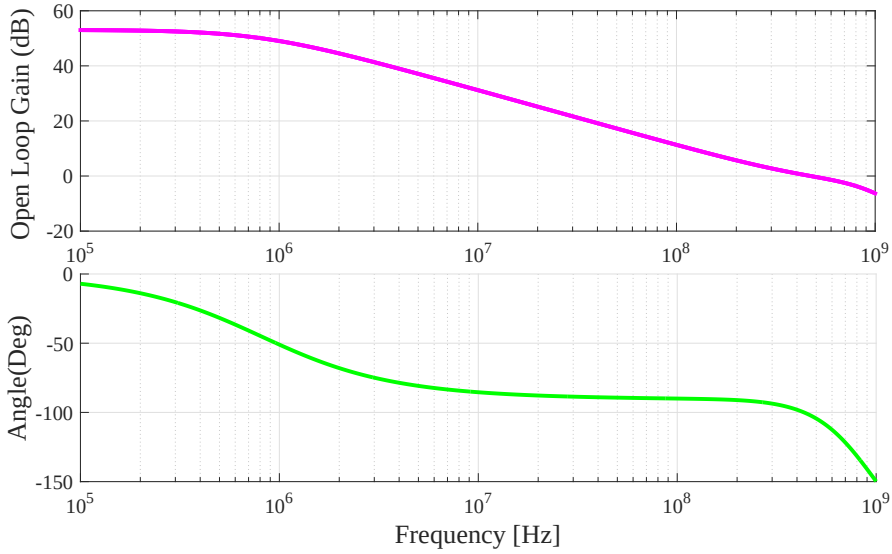


Figure 5.10: The open loop gain and phase response of the folded cascode OTA of Figure 5.9

SR latch is used to make the output of the comparator change on the rising edge of the clock signal. The waveforms demonstrating the operation of the clocked comparator, for a given test input is shown in Figure 5.13. This 1-bit clocked comparator is used

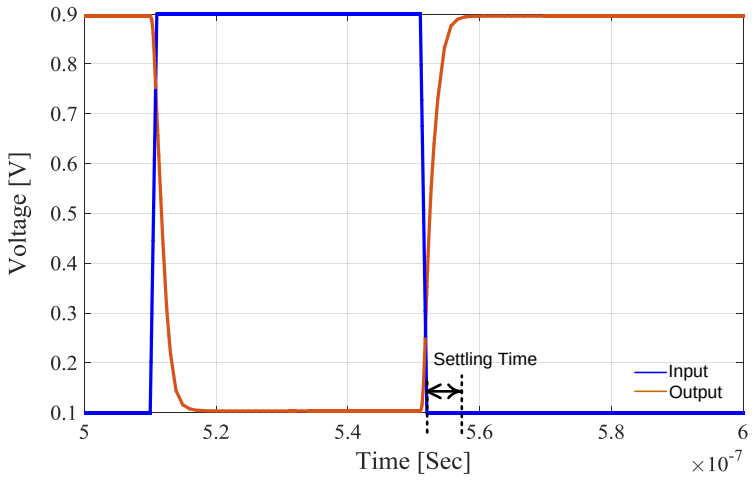


Figure 5.11: Step response of the OTA driving a 1pF load capacitance

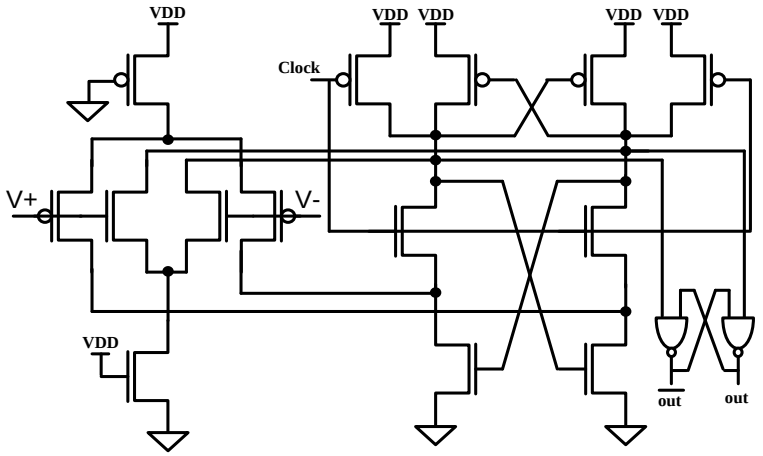


Figure 5.12: 1-bit clocked comparator

for making a 3-bit flash ADC and its output response is shown in Figure 5.14.

The output of the proposed MASH DQEFM obtained through circuit level simulation using HSPICE were evaluated through a 8192 point FFT to get the PSD. Figure 5.15(a) and Figure 5.15(b) shows the simulated output spectrum of the proposed architecture when simulated using HSPICE with 45 nm technology for 10 MHz and 20 MHz bandwidths respectively. The circuit level simulation of the MASH DQEFM using 45nm CMOS process for a bandwidth of 10 MHz yields an SNDR of 63.7 dB

Table 5.2: Performance Summary of Folded-Cascode OTA with Output Buffer

OTA Parameters	**Values**
DC Gain	53 dB
GBW (CL=1pF)	470 MHz
SR (CL=1pF)	245 V/µs
Phase Margin	77°
Settling Time (CL=1pF)	5 ns
Output Swing	1 V
Maximum Current	245.12 µA
Power Dissipation	248.99 µW
Technology	45 nm

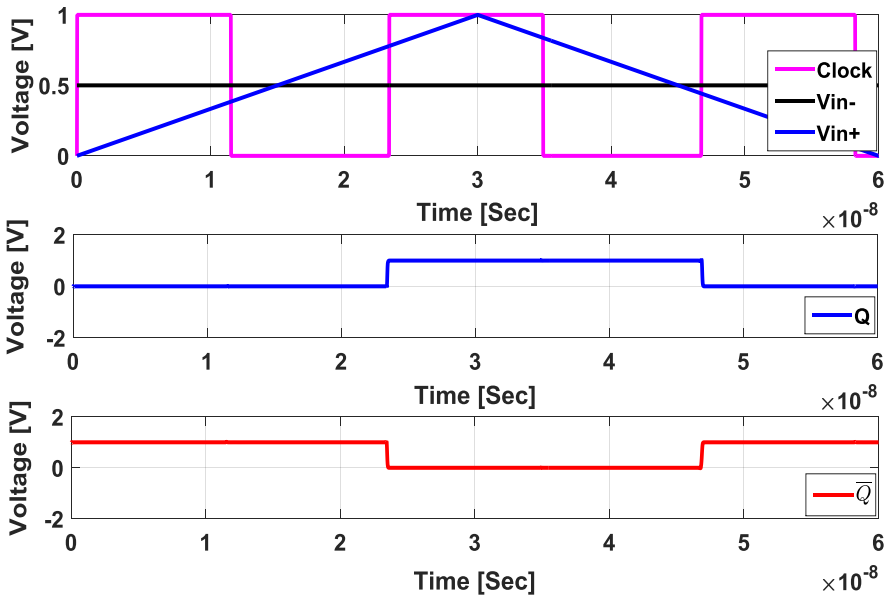


Figure 5.13: 1-bit Comparator waveforms for a given test input

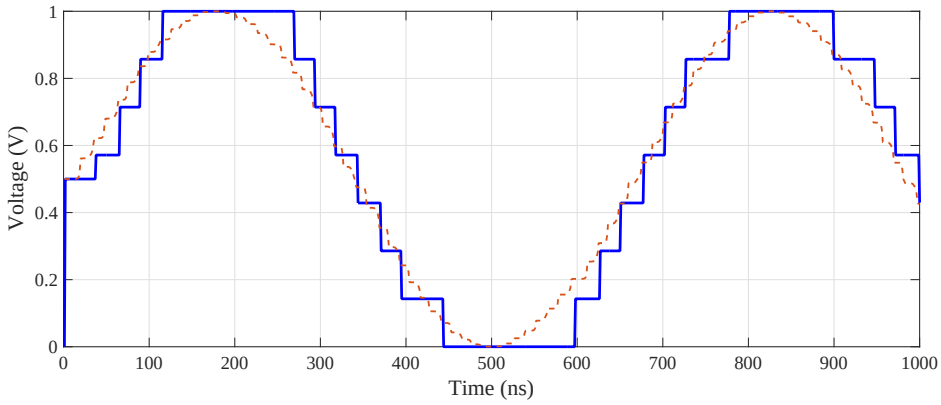


Figure 5.14: Output of a 3-bit flash ADC

(ENOB-10.29 bits). The circuit level simulation of the MASH DQEFM using 45nm CMOS process for a bandwidth of 20 MHz yields an SNDR of 58 dB (ENOB-9.34 bits) while dissipating 5.9 mW of power with 1V supply. A FoM of 0.23 pJ/conv-step is attained for the proposed LP MASH DQEFM structure when simulated for a bandwidth of 20 MHz.

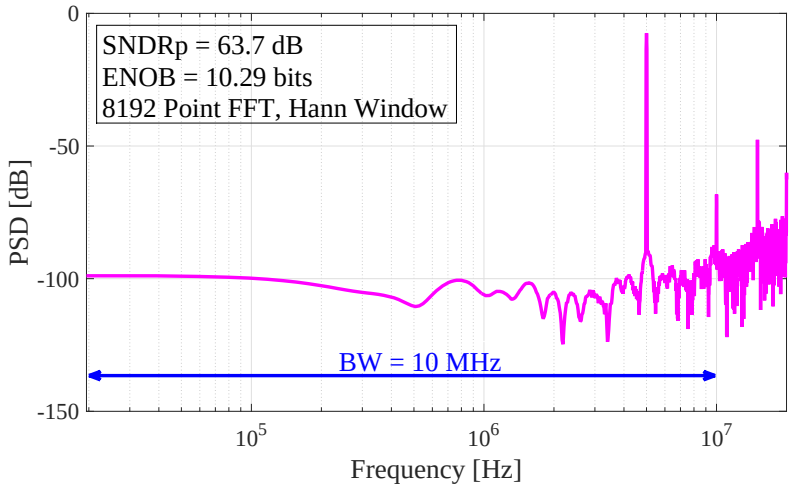
Figure of merit (FoM) is a useful tool which shows the conversion efficiency of A/D converters. FoM quantifies the trade-off between ADC speed, resolution and power dissipation. It is a parameter used to combine several performance metrics to get one single number. It is given by

$$FoM = \frac{Power}{2^{ENOB} * 2BW} \tag{5.8}$$

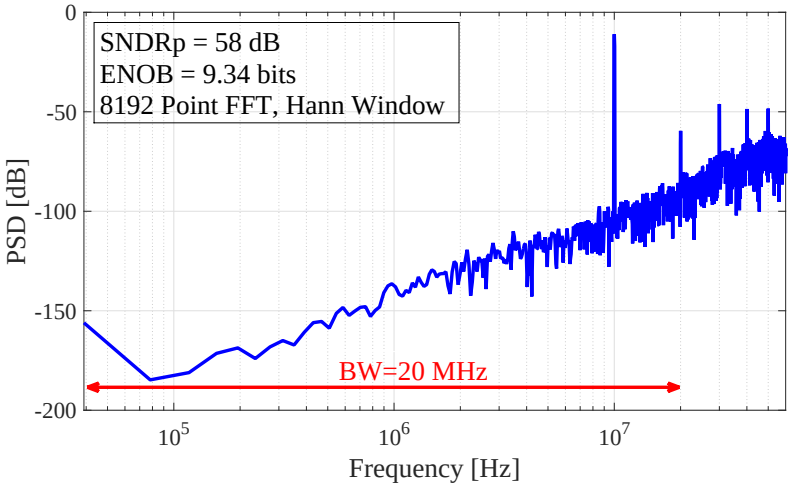
where BW denotes the signal bandwidth and the effective number of bits (ENOB) is obtained by

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{5.9}$$

Since the FoM is expressed in pJ/conversion-step, the architecture with least value of FoM shows the better performance. The LP MASH DQEFM attains a low FoM value when compared with other state-of-the-art $\Sigma\Delta$ architectures as shown in Table 5.3.



(a)



(b)

Figure 5.15: Output Spectrum of the LP MASH DQEFM simulated for 4G bandwidths obtained through Circuit Implementation using HSPICE (a) 10 MHz BW (b) 20 MHz BW

5.5 Chapter Summary

This chapter presents the design and simulation of a lowpass MASH DQEFM architecture that is intended for data conversion operation in 4G radios. The use of DQEFM structure for relaxed op-amp requirements, reduced sensitivity to mismatch effects, cascaded structure for better stability and lower operating frequency makes

Table 5.3: Comparison of the LP MASH DQEFM architecture with other state-of-the-art $\Sigma\Delta$ architectures

	(Ke *et al.*, 2010)	(Christen and Huang, 2010)	(Li *et al.*, 2013)	(Bettini *et al.*, 2015)	This work
Sampling Frequency[MHz]	640	400	640	400	320
Bandwidth [MHz]	20	20	20	20	20
Architecture	CT	DT	CT	DT	LP DQEFM
Order of Modulator	4	3	3	3	4
Quantizer bits	2	3.5	5	3.5	3
SNRp [dB]	-	66.9	59	65.3	66.3
SNDRp [dB]	56	64.4	58.4	62.1	58
ENOB	9	10.4	9.4	10.02	9.34
Power[mW]	8.5	34.7	21	35.7	5.9
Supply Voltage [V]	1	1.2	1.2	1.2	1
Technology [nm]	90	130	130	130	45
FoM [pJ/conv]	0.41	0.6	0.77	0.85	0.23

this superior among other architectures. The simulations were performed for a bandwidth of 10 MHz and 20 MHz. The circuit level simulations performed using HSPICE with 45nm CMOS process indicate that the proposed modulator attains a peak SNDR of 58dB over a bandwidth of 20 MHz while dissipating 5.9 mW of power. The lower value of FoM shows that performance of the proposed MASH DQEFM structure is much better compared to other state-of-the-art $\Sigma\Delta$ modulators

CHAPTER 6

A RE-CONFIGURABLE MASH BANDPASS DQEFM FOR GSM/WCDMA STANDARDS

A novel bandpass DQEFM (BP DQEFM) architecture and its cascaded implementation are presented in this chapter. The mathematical analysis and simulation results indicate the resemblance of the proposed BP DQEFM with the conventional $\Sigma\Delta$M. The circuit level simulations of the second order BP DQEFM for a digital radio application indicate the better performance of the proposed BP DQEFM in terms of hardware complexity and power. A re-configurable cascaded BP DQEFM architecture has been designed for data conversion operation in Global System for Mobile communications (GSM)/Wideband Code Division Multiple Access (WCDMA) standards. The circuit level simulations of the MASH BP DQEFM has been performed for a bandwidth of 200 kHz for GSM and bandwidth of 5 MHz for WCDMA. The re-configurability, reduction of power hungry active blocks and reduced sensitivity to circuit non-idealities makes this proposed MASH BP DQEFM a suitable candidate for a digital intermediate frequency (IF) receiver system.

The organization of the chapter is as follows. The basic operation of a bandpass $\Sigma\Delta$M and traditional second order BP $\Sigma\Delta$M architecture with feedback and feedforward topologies are described in Section 6.1. The working of newly introduced BP DQEFM architecture along with its mathematical analysis for the first and second order DQEFM and simulation results are also presented. The behavioural and circuit level simulation results for the bandpass DQEFM structure are discussed in Section 6.2. Section 6.3 reviews the conventional cascaded bandpass $\Sigma\Delta$M employing the feedforward topology and the MASH bandpass DQEFM architecture. The re-configurability of MASH BP DQEFM, mathematical analysis and behavioural

simulations are presented. Section 6.4 gives an insight into the performance of the proposed modulator in the presence of non-idealities. The circuit level simulation of the proposed modulator is described in Section 6.5. Finally, the summary of the chapter is provided in Section 6.6.

6.1 Bandpass Sigma Delta Modulator

The $\Sigma\Delta$ modulation technique initially used for low frequency signals has also been extended to perform digitization of relatively narrowband signals and the first bandpass (BP) version of $\Sigma\Delta$ modulation was proposed by Schreier and Snelgrove (Schreier and Snelgrove, 1989). The bandpass $\Sigma\Delta$M (BP $\Sigma\Delta$M) is capable to provide high resolution at higher frequencies for a bandlimited input, and finds application mainly in digital radio receivers (Keady and Lyden, 1998). The noise shaped out-of-band signals in BP $\Sigma\Delta$M can effectively be attenuated by a post digital BP filter. Thus BP $\Sigma\Delta$ ADCs offer high resolution conversion of a narrow frequency band and strong rejection of out-of-band signals (Keady and Lyden, 1995).

The architectural advances and scaling of semiconductor technologies makes the ADC operation moves closer to the antenna side, so many analog functions exist in a conventional superheterodyne receiver system can be processed at the digital domain. Such ADCs, operating at radio frequency (RF) or intermediate frequency (IF), require very stringent performance specifications. The BP $\Sigma\Delta$M utilizes the signal processing techniques such as oversampling and quantization noise shaping to achieve higher resolution in narrow band IF signals (Norsworthy *et al.*, 1997). The ability to lower the noise floor at RF or IF makes this modulator widely useful in wireless communication receiver systems. This noise shaping property at higher frequency bands without affecting the band of interest helps to digitize the signal directly without the down-conversion process (Galton, 2002). This property makes BP $\Sigma\Delta$ ADCs well suited for use in front end of radio receivers (Jantzi *et al.*, 1991).

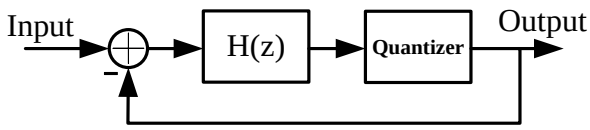


Figure 6.1: Block Diagram of a First order $\Sigma\Delta$ Modulator:
Lowpass if $H(z)$=$z^{-1}/(1-z^{-1})$; Bandpass if $H(z)$=$-z^{-2}/(1+z^{-2})$

The block diagram of a first order $\Sigma\Delta$M is shown in Figure 6.1. The loop filter $H(z)$ determines whether the modulator functions as lowpass or bandpass. LP $\Sigma\Delta$M can be transformed to a BP $\Sigma\Delta$M by applying a mapping $z^{-1} \Rightarrow -z^{-2}$ (Norsworthy *et al.*, 1997). The resonator forms the basic building block of traditional BP-$\Sigma\Delta$M and a typical BP resonator with double delay from input to output can be expressed as $-z^{-2}/(1+z^{-2})$. The integrators in the LP-$\Sigma\Delta$Ms are replaced by resonators and the zeros of the NTF change from DC ($z=1$) to a quarter of the sampling frequency, i.e $f_s/4$ ($z=i$) as a result of this transformation (Momeni *et al.*, 2008).

6.1.1 Traditional Second Order Feedback BP $\Sigma\Delta$M

The conventional second order feedback BP $\Sigma\Delta$M (BP FB $\Sigma\Delta$M) (Longo and Horng, 1993) is shown in Figure 6.2. The STF, NTF and the overall output of the second order BP FB $\Sigma\Delta$M, with a_1 = 0.5, a_2 = 2 and a_3 = 1, are given in equations (6.1) and (6.2).

$$STF_{BPFB\Sigma\Delta 2} = z^{-4}, \quad NTF_{BPFB\Sigma\Delta 2} = (1+z^{-2})^2 \tag{6.1}$$

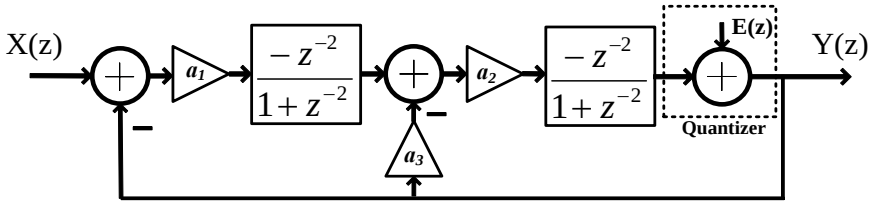


Figure 6.2: Conventional Second Order Feedback BP $\Sigma\Delta$M

$$Y(z)_{BPFB\Sigma\Delta 2} = z^{-4}X(z)_{BPFB\Sigma\Delta 2} + (1+z^{-2})^2 E(z)_{BPFB\Sigma\Delta 2} \tag{6.2}$$

Here $STF_{BPFB\Sigma\Delta i}$, $NTF_{BPFB\Sigma\Delta i}$, $X(z)_{BPFB\Sigma\Delta i}$, $E(z)_{BPFB\Sigma\Delta i}$ and $Y(z)_{BPFB\Sigma\Delta i}$ represents STF, NTF, input signal, quantization error and the overall output of the i^{th} order BPFB-$\Sigma\Delta$M, respectively.

6.1.2 Traditional Second Order Feedforward BP $\Sigma\Delta$M using Two-delay-loop Resonator

There are many different architectural approaches to implement the resonator function in BP $\Sigma\Delta$M. The relaxed settling time requirement of two-delay-loop (TDL) resonator makes it a suitable choice among many techniques to implement the resonator function (Keskin *et al.*, 2003), (Momeni *et al.*, 2008). The TDL structure shown in Figure 6.3 is utilized in making a second order feedforward BP $\Sigma\Delta$M (BP FF $\Sigma\Delta$M) depicted in Figure 6.4. The STF, NTF and the output of the BP FF $\Sigma\Delta$M, with a_1=-1, a_2=1 and a_3 =1 are given in equations (6.3) and (6.4).

$$STF_{BPFF\Sigma\Delta 2} = 1, \quad NTF_{BPFF\Sigma\Delta 2} = (1+z^{-2})^2 \tag{6.3}$$

$$Y(z)_{BPFF\Sigma\Delta 2} = X(z)_{BPFF\Sigma\Delta 2} + (1+z^{-2})^2 E(z)_{BPFF\Sigma\Delta 2} \tag{6.4}$$

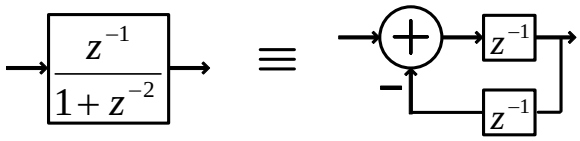


Figure 6.3: Two-delay loop (TDL) Resonator Structure

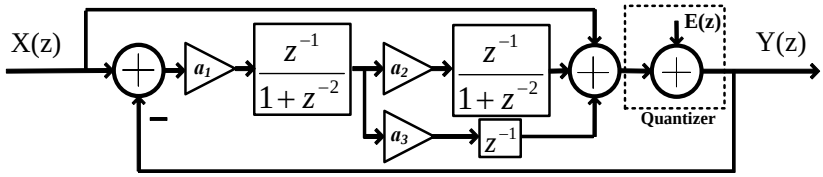
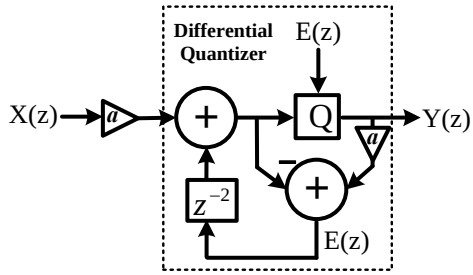


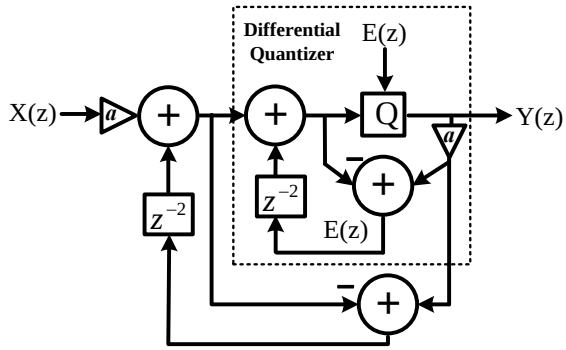
Figure 6.4: Conventional Second Order BP FF ΣΔM using TDL resonator

6.1.3 Differentially Quantized Bandpass Error Feedback Modulator Architecture

The first and second order bandpass DQEFM architectures are shown in Figure 6.5(a) and Figure 6.5(b) respectively. The error associated with the quantization process, i.e. quantization error is obtained by performing analog subtraction between the input and the output of the quantizer. In the case of BP DQEFM, the quantization error is



(a)



(b)

Figure 6.5: Block diagram of the BP DQEFM (a) First Order BP DQEFM Architecture, (b) Second Order BP DQEFM Architecture

delayed by two clock cycles before being fed back to the input of the modulator. The conventional $\Sigma\Delta$ architecture utilizes integrator/resonator functions in the loop filter implementation, where as DQEFMs use differential quantizer in order to generate the noise shaping transfer function (Prakash *et al.*, 2018).

The STF and NTF obtained for the first and second order BP DQEFM architecture are shown in equations (6.6) and (6.8) respectively. The value chosen for the scaling coefficient '*a*'is unity, for deriving these equations. The STF is unity for both first and second order BP DQEFM.

$$Y(z)_{BPDQM1} = X(z)_{BPDQM1} + (1 + z^{-2})E(z)_{BPDQM1} \tag{6.5}$$

$$STF_{BPDQM1} = 1, \quad NTF_{BPDQM1} = 1 + z^{-2} \tag{6.6}$$

$$Y(z)_{BPDQM2} = X(z)_{BPDQM2} + (1 + z^{-2})^2 E(z)_{BPDQM2} \tag{6.7}$$

$$STF_{BPDQM2} = 1, \quad NTF_{BPDQM2} = (1 + z^{-2})^2 \tag{6.8}$$

Here STF_{BPDQMi}, NTF_{BPDQMi}, $E(z)_{BPDQMi}$, $X(z)_{BPDQMi}$, and $Y(z)_{BPDQMi}$ denotes the STF, NTF, quantization error, input signal and the output of the i^{th} order BP DQEFM architecture respectively.

6.2 Simulation Results

6.2.1 Behavioural Simulation of the BP DQEFM

The second order BP DQEFM, shown in Figure 6.5b, has been simulated and compared with the conventional FF second order BP $\Sigma\Delta$ counterparts of Figure 6.4

using MATLAB/SIMULINK. The combined impact of all the non-idealities on the SNR performance is obtained by simulating DQEFM with clock jitter ($\Delta\tau$ = 20 ns), switches kT/C noise (C_s = 0.5 pF), input referred op-amp noise (V_n = 73 μVrms) and an op-amp of finite gain-bandwidth (GBW = 220 MHz), slew-rate (SR = 200 V/μs) and op-amp dc gain (A_{dB} = 20 dB), and resulting output spectra is compared with the second order BP FF ΣΔM, as shown in Figure 6.6. An OSR of 107, scaling coefficient a = 0.25, a 1-bit quantizer, and 65536 samples were used for simulating a 200kHz BW modulator. The op-amp gain requirements for the BP DQEFM is

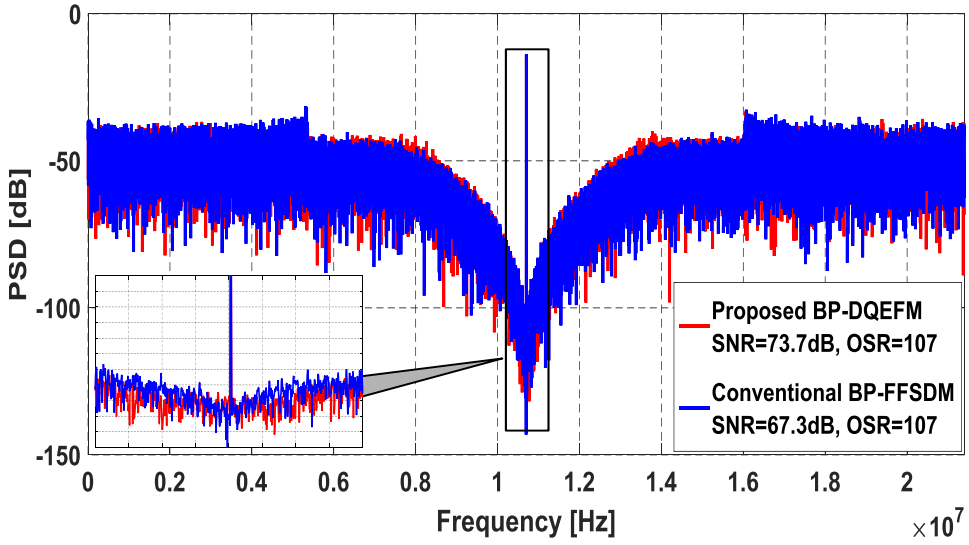


Figure 6.6: Comparison of output spectra considering all the non-idealities

relaxed when compared with the conventional BP FF ΣΔM as indicated by Figure 6.7. A gain of 20 dB is sufficient for DQEFM operation, where as conventional BP FF ΣΔM demands a minimum gain of 40 dB. This is because the op-amp serves as a simple Switched Capacitor (SC) S/H or as a unity gain buffer in DQEFM architecture in contrast to the integrator/resonator function in conventional ΣΔMs. The conventional ΣΔ architecture utilizes integrator/resonator functions in the loop filter implementation, where as DQEFMs use differential quantizer in order to generate the noise shaping transfer function (Prakash *et al.*, 2018). The effect of resonator associated non-idealities are less in BP DQEFM architecture. Likewise, 3D plots are also

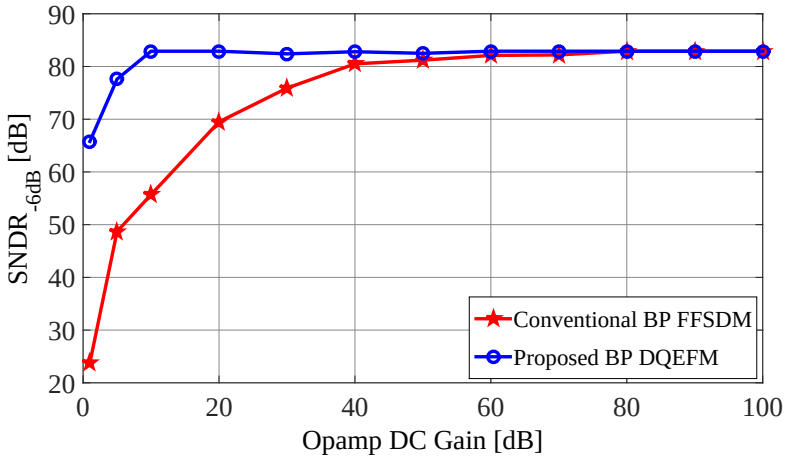
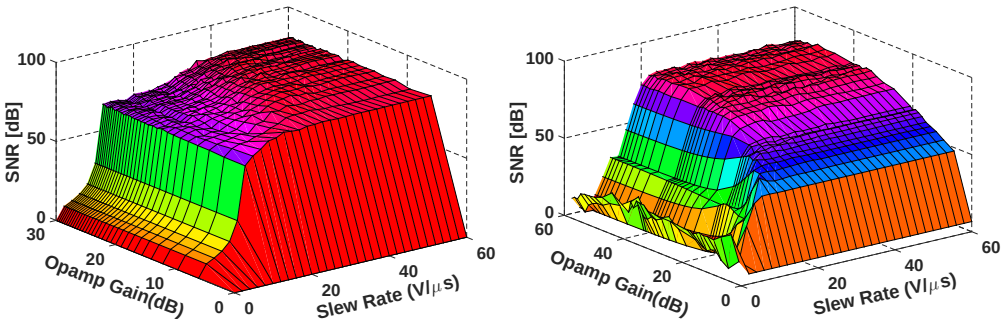


Figure 6.7: SNDR performance variation with op-amp finite DC gain for the second order conventional BP FF ΣΔM and proposed BP DQEFM architectures

obtained to understand the variation in SNR as a function of op-amp gain and slew rate for the proposed and conventional architectures as shown in Figure 6.8. Figure 6.9 denotes the variation in SNR against different values of OSR ranging from 16 to 128. The superior performance of the proposed BP-DQEFM for different values of OSR is easily understood from Figure 6.9



(a) BP- DQEFM architecture

(b) Conventional BP-FFΣΔM architecture

Figure 6.8: Variation in SNDR as a function of Op-amp Gain and Slew rate

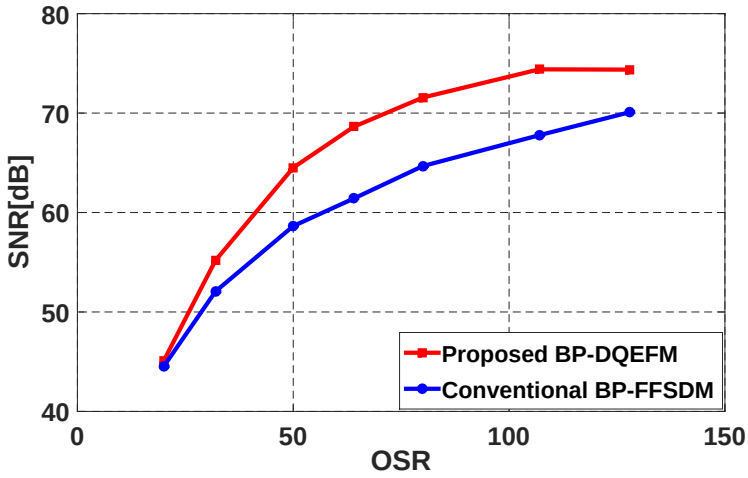


Figure 6.9: Variations in SNR with different OSR

6.2.2 Circuit Level Simulations for the BP DQEFM

Switched capacitor (SC) circuit level implementation of second order BP DQEFM using SC S/H circuit is depicted in Figure 6.10. The BP DQEFM implementation incorporates both delayed and delay-free S/H circuits. The sample and hold operation occurs in the same clock phase for delay-free S/H circuit, where as sample and hold operation happen in two different non-overlapping clock phases in the case of delayed S/H circuit and produces a half clock delay. The delayed and delay-free S/H circuit is utilized in the subtraction operation to get the quantization error. This proposed architecture doesn't require any active adder and saves one power hungry OTA in each stage. The OTAs in proposed architecture functions as an element of S/H circuits, but in conventional feedforward bandpass architecture they are acting as a part of resonator. So the effect of resonator associated non-idealities are less in BP DQEFM architecture.

A folded-cascode OTA with class AB output buffer (Baker, 2008) shown in Figure 5.9 was used for the active component needed in the switched capacitor sample and hold (S/H) circuits. The aspect ratios (W/L) of the MOSFETs used to build the OTA were modified to attain a gain of 75 dB, unity gain-bandwidth of 144 MHz and a

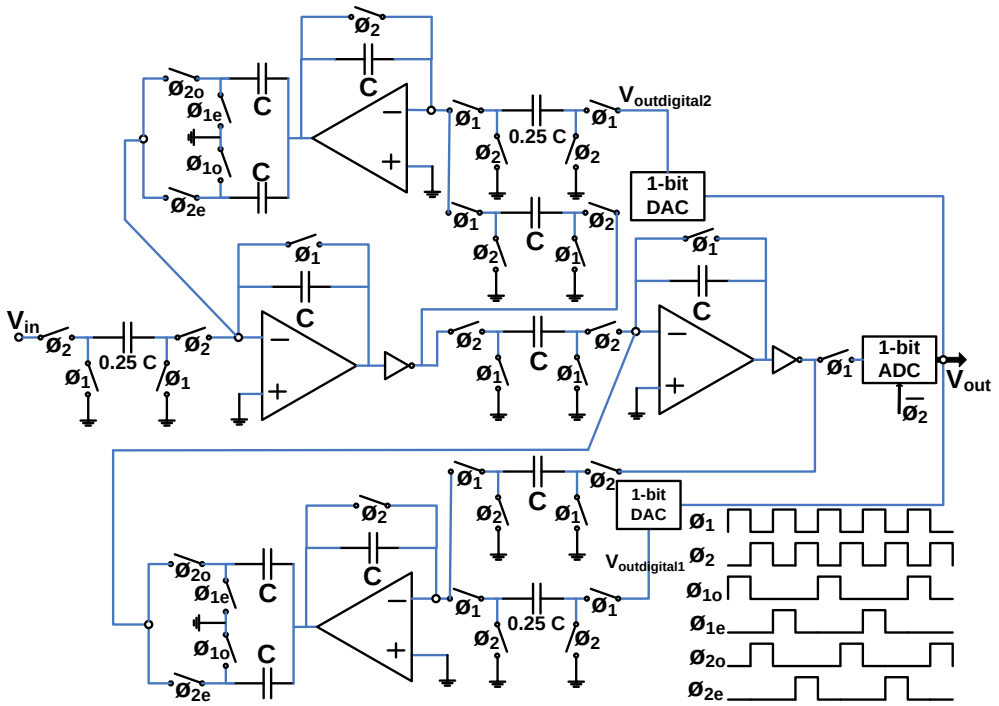


Figure 6.10: Single ended switched capacitor (SC) circuit implementation of second order BP-DQEFM using SC S/H circuit

phase margin of 50 degree. A wide swing clocked comparator (Baker, 2008) shown in Figure 5.12, which uses long-length MOSFETs, was used for 1-bit ADC operation. It consists of a preamplifier and a latch section. The output of the comparator changes during the rising edge of the clock. The circuit level simulation of the BP DQEFM was performed using HSPICE with 45 nm CMOS process and a supply voltage of 1V.

An OSR of 107 with a clock frequency of 42.8 MHz for a bandwidth of 200 kHz were used for the simulation of a 10.7 MHz digital radio IF signal input signal. The two non-overlapping clock phases, Φ_1 and Φ_2, were used to operate the complete switched capacitor model and the output spectra obtained is depicted in Figure 6.11. BP DQEFM follows a better noise shaping in the band of interest when compared with the conventional FF BP $\Sigma\Delta$M as indicated by the Figure 6.11. The circuit level

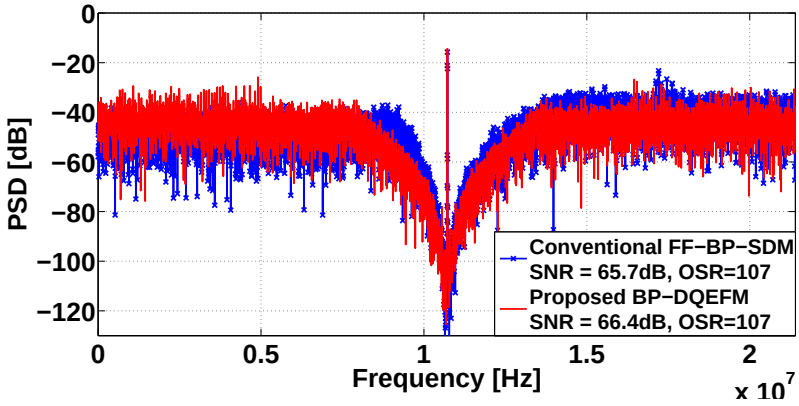


Figure 6.11: Output spectra of the switched capacitor (SC) circuit implementation of the conventional second order BP-FF-$\Sigma\Delta$M and proposed second order BP-DQEFM architectures from Hspice

simulations performed using HSPICE with 45 nm CMOS process shows a power consumption of 0.62 mW and 0.95 mW for the proposed and the conventional modulators respectively.

6.3 MASH Bandpass $\Sigma\Delta$M

The cascading of bandpass $\Sigma\Delta$ modulators provides a stable higher order BP modulator as well as higher dynamic range (DR).

6.3.1 Feedforward MASH Bandpass $\Sigma\Delta$M

The basic block diagram of a conventional feedforward MASH 2-2 bandpass $\Sigma\Delta$M (FF MASH 2-2 BP $\Sigma\Delta$M) made using TDL resonator structure is shown in Figure 6.12. The STF, NTF and the overall output of the MASH 2-2 BP $\Sigma\Delta$M, with a_{11},a_{21} =1, a_{12},a_{22} =1 and a_{13},a_{23} =1, are given in equations (6.9) and (6.10) respectively. The quantization error is extracted and multiplied by a gain, known as inter-stage gain, denoted by 'g'.

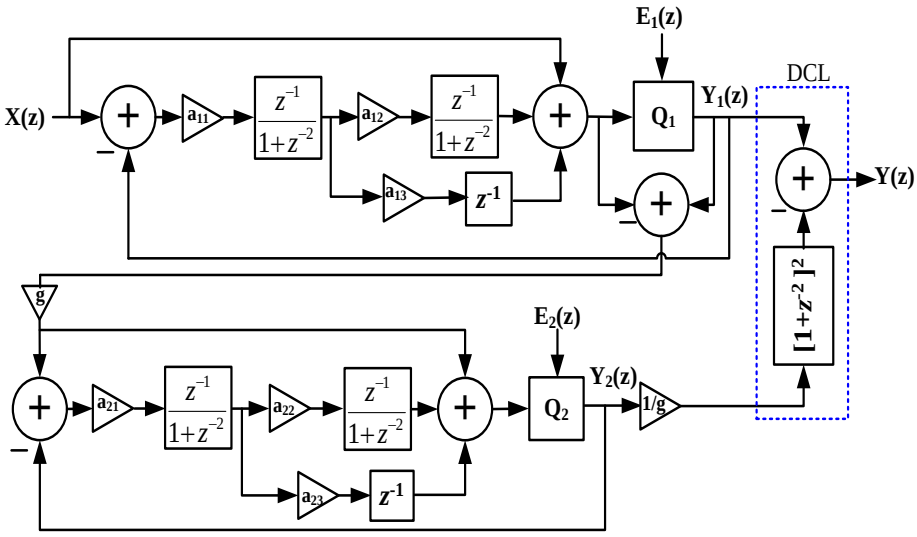


Figure 6.12: Conventional FF MASH 2-2 BP ΣΔM Architecture using TDL Resonator

$$Y(z)_{BP\Sigma\Delta M_{TDL}} = X(z)_{BP\Sigma\Delta M_{TDL}} - \frac{1}{g}(1+z^{-2})^4 E_2(z)_{BP\Sigma\Delta M_{TDL}} \tag{6.9}$$

where

$$STF_{BP\Sigma\Delta M_{TDL}} = 1, \quad NTF_{BP\Sigma\Delta M_{TDL}} = (1+z^{-2})^4 \tag{6.10}$$

6.3.2 MASH BP DQEFM Architecture

The second order BP DQEFM structure has been utilized in making a fourth order BP DQEFM architecture by cascading two second order modulators as depicted in Figure 6.13. The detailed architecture of the proposed re-configurable MASH 2-2 BP DQEFM is illustrated in Figure 6.14. This re-configurable modulator is able to perform data conversion in GSM and WCDMA standards. The switch '*S*' indicated in Figure 6.14 is utilized for selecting the mode of operation. The mathematical

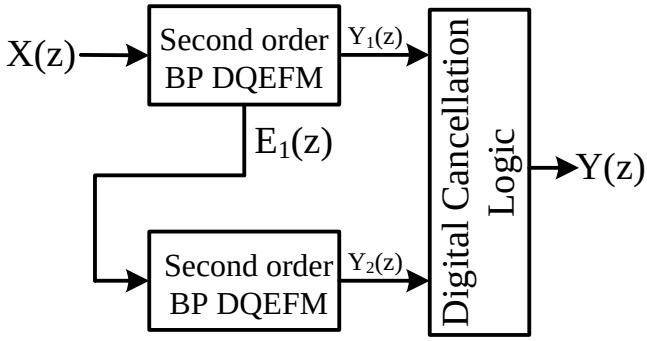


Figure 6.13: Block diagram of the proposed MASH 2-2 BP DQEFM Architecture

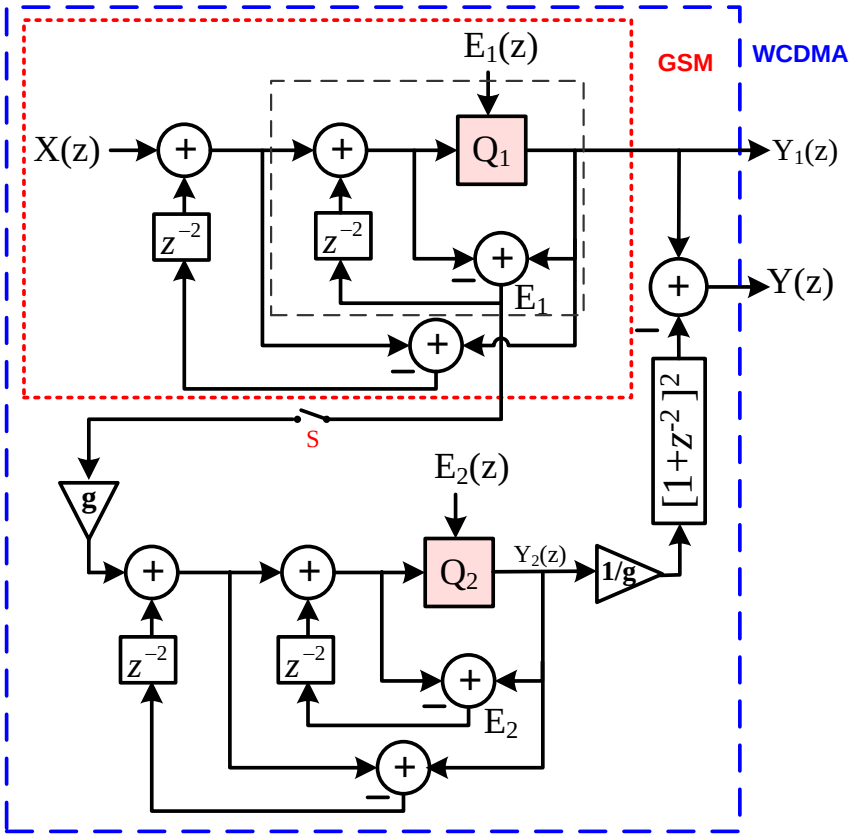


Figure 6.14: Proposed re-configurable MASH 2-2 BP DQEFM Architecture for GSM/ WCDMA standards

analysis of the proposed MASH 2-2 BP DQEFM architecture is given by

$$Y_1(z)_{BPDQM2} = X(z)_{BPDQM2} + (1+z^{-2})^2 E_1(z)_{BPDQM2} \tag{6.11}$$

$$Y_2(z)_{BPDQM2} = gE_1(z)_{BPDQM2} + (1+z^{-2})^2 E_2(z)_{BPDQM2} \tag{6.12}$$

where $X(z)_{BPDQM2}$, $Y_1(z)_{BPDQM2}$, and $E_1(z)_{BPDQM2}$ denotes the input signal, output of the first stage and quantization noise of the first stage respectively. The output of the second stage and quantization error associated with second stage quantizer are denoted by $Y_2(z)_{BPDQM2}$ and $E_2(z)_{BPDQM2}$ respectively. The gain between the stages is denoted by 'g' and the overall output of the proposed modulator is given by

$$Y(z)_{BPDQ22} = Y_1(z)_{BPDQM2} - \frac{1}{g}(1+z^{-2})^2 Y_2(z)_{BPDQM2} \tag{6.13}$$

$$Y(z)_{BPDQ22} = X(z)_{BPDQ22} - \frac{1}{g}(1+z^{-2})^4 E_2(z)_{BPDQ22} \tag{6.14}$$

where

$$STF_{BPDQ22} = 1, \quad NTF_{BPDQ22} = (1+z^{-2})^4 \tag{6.15}$$

Here STF_{BPDQ22}, NTF_{BPDQ22}, $X(z)_{BPDQ22}$, $E_2(z)_{BPDQ22}$ and $Y(z)_{BPDQ22}$ represents STF, NTF, input signal, quantization error of the second stage and the overall output of the MASH BP DQEFM respectively. The quantization error associated with the first stage, i.e. $E_1(z)$ is completely cancelled by selecting an appropriate digital cancellation logic and the second stage quantization noise is shaped by an NTF of order equal to four. The mathematical equivalence of the conventional FF MASH 2-2 BP $\Sigma\Delta$M can be examined by comparing equation (6.5) with (6.14).

The performance of the proposed MASH 2-2 BP DQEFM is compared against the conventional FF MASH BP $\Sigma\Delta M$, and the power spectral density (PSD) plots ob-

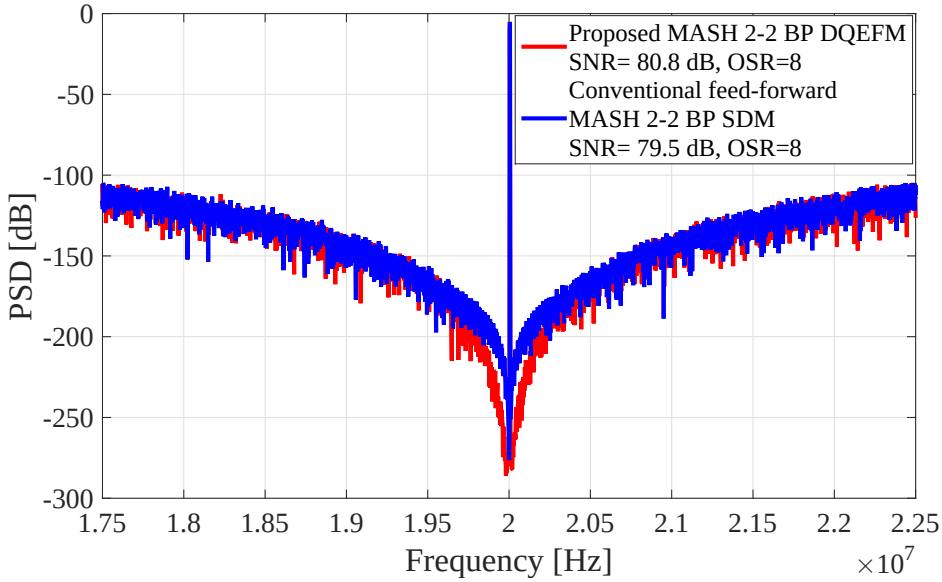


Figure 6.15: PSD plot of both Architectures

tained are shown in Figure 6.15. Both the architectures achieves an identical performance when behavioral model simulations were performed. The system level simulations were conducted using MATLAB/SIMULINK with an oversampling ratio (OSR) of 8, inter-stage gain g = 4, 3-bit quantizers in both stages and 65536 samples were used for all the simulations. The signal to noise ratio (SNR) is plotted against different values of input level amplitude shown in Figure 6.16. The peak SNR (SNRp) and overload level(OL) obtained for multiple values of OSR ranging from 8 to 64 is provided in Table 6.1. The proposed MASH DQEFM shows an improvement in dynamic range as well as a peak SNR value than conventional MASH structure.

6.4 Non-Ideality Analysis of the MASH BP DQEFM

The non-ideal effects associated with op-amp such as finite op-amp dc gain, finite gain bandwidth (GBW), finite slew rate and saturation voltages will contribute to the performance degradation occuring in analog circuit implementation of the modulator. The non-ideality analysis were conducted for the proposed and conventional modu-

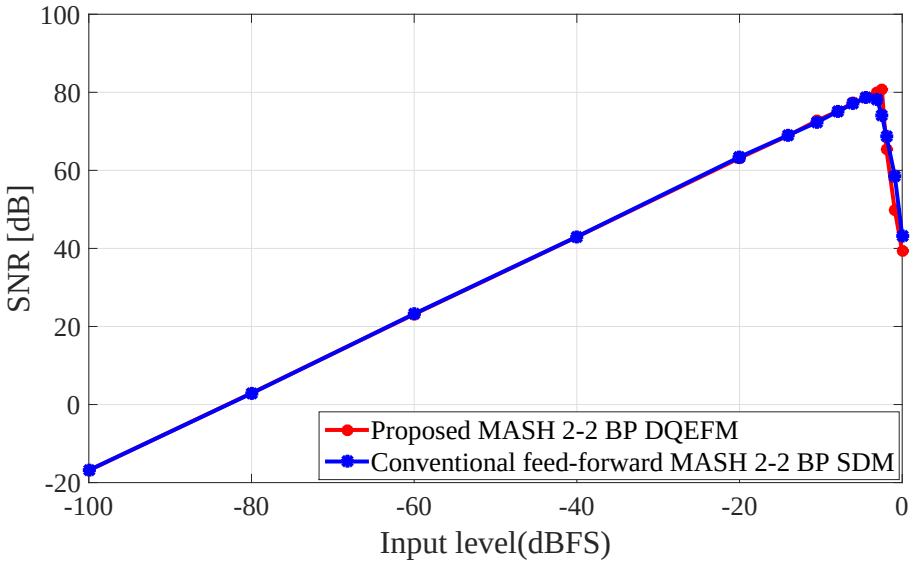


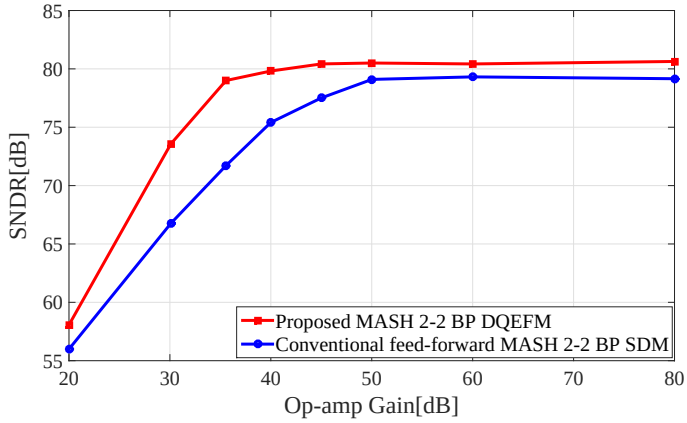
Figure 6.16: SNR vs Input Signal Amplitude

Table 6.1: SNRp and OL for the Conventional FF MASH 2-2 BP ΣΔM and the proposed MASH 2-2 BP DQEFM

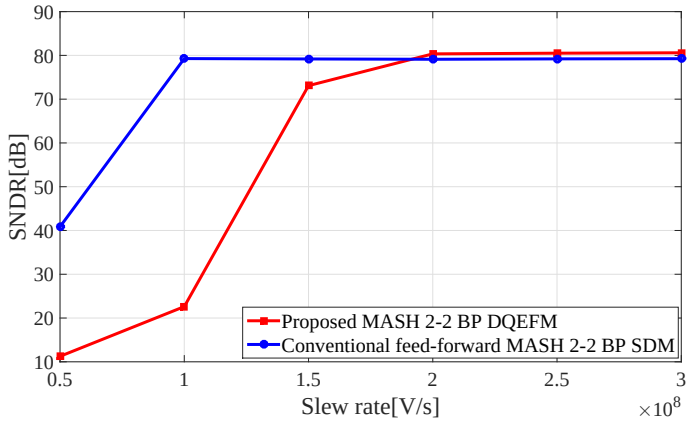
	Proposed MASH 2-2 BP DQEFM		Conventional FF MASH 2-2 BP ΣΔM	
OSR	SNRp (dB)	OL (Volts)	SNRp (dB)	OL (Volts)
8	80.8	0.75	79.5	0.65
16	108.1	0.74	106.6	0.63
32	134.4	0.75	133.0	0.64
64	161.8	0.75	160.6	0.63

lators for a bandwidth of 5 MHz. The variation in Signal to Noise plus Distortion Ratio (SNDR) against these non-idealities is found by considering the effect of each non-ideality at a time and the resulting plots are obtained for each non-ideality. The op-amp dc gain requirements are comparatively relaxed in the case of proposed modulator as indicated in Figure 6.17(a). An op-amp with 40 dB gain is sufficient to attain SNDR value of 80 dB for the proposed modulator. The slew rate and GBW requirements for the proposed modulator are around 200 V/μs and 150 MHz as illustrated in Figure 6.17(b) and Figure 6.17(c) respectively . The 3D plot shown in Figure 6.18

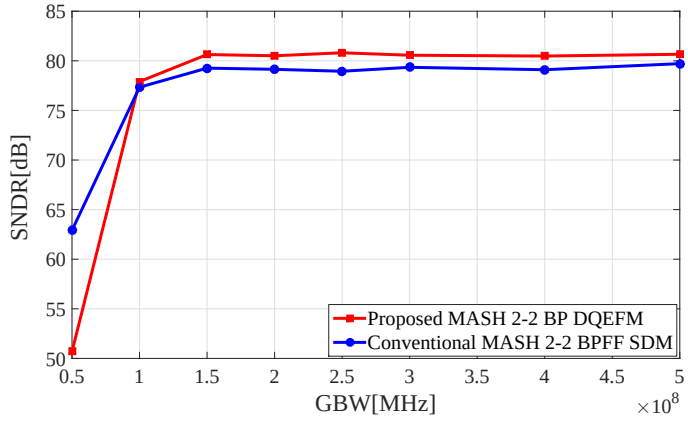
illustrates the variation of SNDR as a function of op-amp gain and GBW.



(a) SNDR vs Op-amp gain

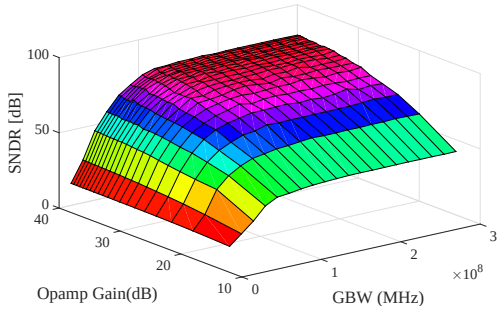


(b) SNDR vs Slew rate

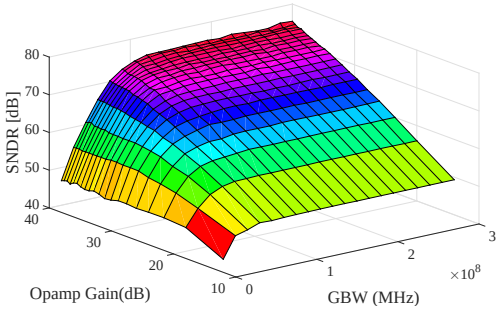


(c) SNDR vs GBW

Figure 6.17: Variation of SNDR against different op-amp non-idealities



(a) Proposed MASH 2-2 BP DQEFM architecture



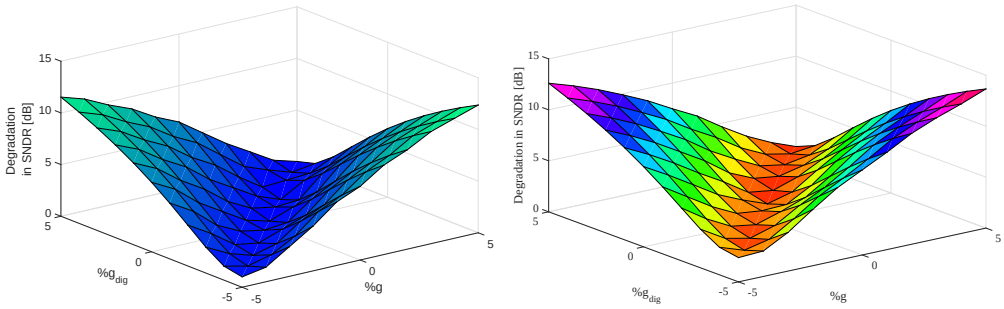
(b) Conventional FF MASH 2-2 BP$\Sigma\Delta$ architecture

Figure 6.18: Variation in SNDR as a function of op-amp gain and GBW

The other non-idealities that affect the performance of the modulator are the clock jitter, switch thermal noise and the op-amp noise. The behavioral level noise models of (Malcovati *et al.*, 2003) were used for simulating these non-idealities and the effect of each non-ideality is considered individually as well as their combined effect is simulated by considering all the non-ideal effects. The SNDRp values obtained for different non-idealities corresponds to the maximum amplitude of input signal in each modulator architecture. The obtained SNDR values shown in Table 6.2 denotes the superior performance of the proposed modulator over the conventional one in the presence of non-ideal effects. The performance of the MASH topology is also limited by the mismatch between the analog and digital coefficients. The decline in SNDR due to this mismatch effects are shown in Figure 6.19. A reduction of 12dB in SNDR is noted when the analog inter-stage gain (g) and its corresponding digital estimate (g_{dig}) are varied $\pm 5\%$ for the proposed MASH BP modulator.

6.5 Circuit Level Simulation

The switched capacitor (SC) implementation of conventional and proposed architectures were simulated in the circuit level using HSPICE. The operational transconductance amplifier (OTA) used for the switched capacitor circuit implementation of the



(a) Proposed MASH 2-2 BP DQEFM architecture (b) Conventional FF MASH 2-2 BP$\Sigma\Delta$ architecture

Figure 6.19: Degradation in SNDR versus mismatch between analog inter-stage gain 'g' and its digital estimate 'g_{dig}'

Table 6.2: Non-ideality analysis of the Proposed MASH 2-2 BP DQEFM and Conventional FF MASH 2-2 BP $\Sigma\Delta$M

Modulator Parameter	Parameter value	Proposed MASH 2-2 BP DQEFM SNDRp dB	Conventional FF MASH 2-2 BP $\Sigma\Delta$M SNDRp dB
Ideal modulator	-	80.8 dB	79.6 dB
Sampling Jitter	$\Delta\tau$ = 250 ps	79.7 dB	79.1 dB
Sampling capacitance	C_s = 10 pF	79.7 dB	78.8 dB
Input referred op-amp Noise	V_n = 0.5 mVrms	69.3 dB	67.8 dB
Op-amp Finite Bandwidth	GBW =300 MHz	80.5 dB	79.0 dB
Op-amp Finite Slewrate	SR = 250 V/μs	80.7 dB	79.2 dB
Saturation Voltage	Vmax = $\pm$1 V	80.8 dB	79.6 dB
Op-amp Finite Gain	A_{dB} = 40 dB	80.0 dB	75.4 dB
Modulator simulated including all non-idealities		68.8 dB	67.3 dB

modulator is a folded-cascode OTA with a class AB output buffer as shown in Figure 5.9 (Baker, 2008). It attains a gain of 53 dB, GBW of 470 MHz, phase margin of 77 degree, slew rate of 245 V/μs and has a settling time of 5 ns. It dissipates 248.99 μW power when implemented using 45 nm CMOS technology with 1V power sup-

ply. The use of multi-bit quantizers enhances the resolution and also provides better stability.

The proposed modulator employs a 3-bit quantizer in both stages. Each clocked comparator comprises of a pre-amplifier and an SR latch as shown in Figure 5.12 (Baker, 2008). A 3-bit flash ADC was made up of seven such clocked comparators . The pre-amplifier between the input and the comparator increases the sensitivity and the use of long-length MOSFETs provides protection from kickback noise. A change in the output of the comparator occurs during the positive edge of the clock.

The SC implementation of the conventional FF MASH 2-2 BP $\Sigma\Delta$M, using double delay resonator is depicted in Figure 6.20. The double-delay topology is widely adopted in implementing resonator function for bandpass modulators because the notch depth in a center frequency is not affected by a capacitor mismatch effects (Jeong *et al.*, 2008). The forward path in a TDL resonator provides a clock delay (z^{-1}) using two half-delayed ($z^{-1/2}$) sample and hold circuits(S/H) and the feedback path provides another clock cycle delay. The feedback path delay of one clock cycle is obtained through a parallel SC circuit consisting of switches and capacitors. A pair of TDL resonators, a 3-bit quantizer and an analog feedforward adder is necessary in each stage. Each TDL resonator is implemented with two OTAs and another OTA is required for active addition, especially when multi-bit quantizers are present in the loop. The output voltage swing of this adder can limit the input to the succeeding multi-bit quantizer. The output of the second resonator contains only the quantization noise due to the low-distortion topology, so this can be utilized as an input to the next stage. The output of both stages is applied to a digital cancellation logic to cancell the effect of first stage quantization noise.

The proposed BP DQEFM, which uses a double-delay based implementation is compared with the conventional FF BP $\Sigma\Delta M$ architecture. The proposed MASH 2-2 BP DQEFM implementation incorporates both delayed and delay-free S/H circuits as depicted in Figure 6.21. All the analog circuit elements like OTA, switches, capacitors

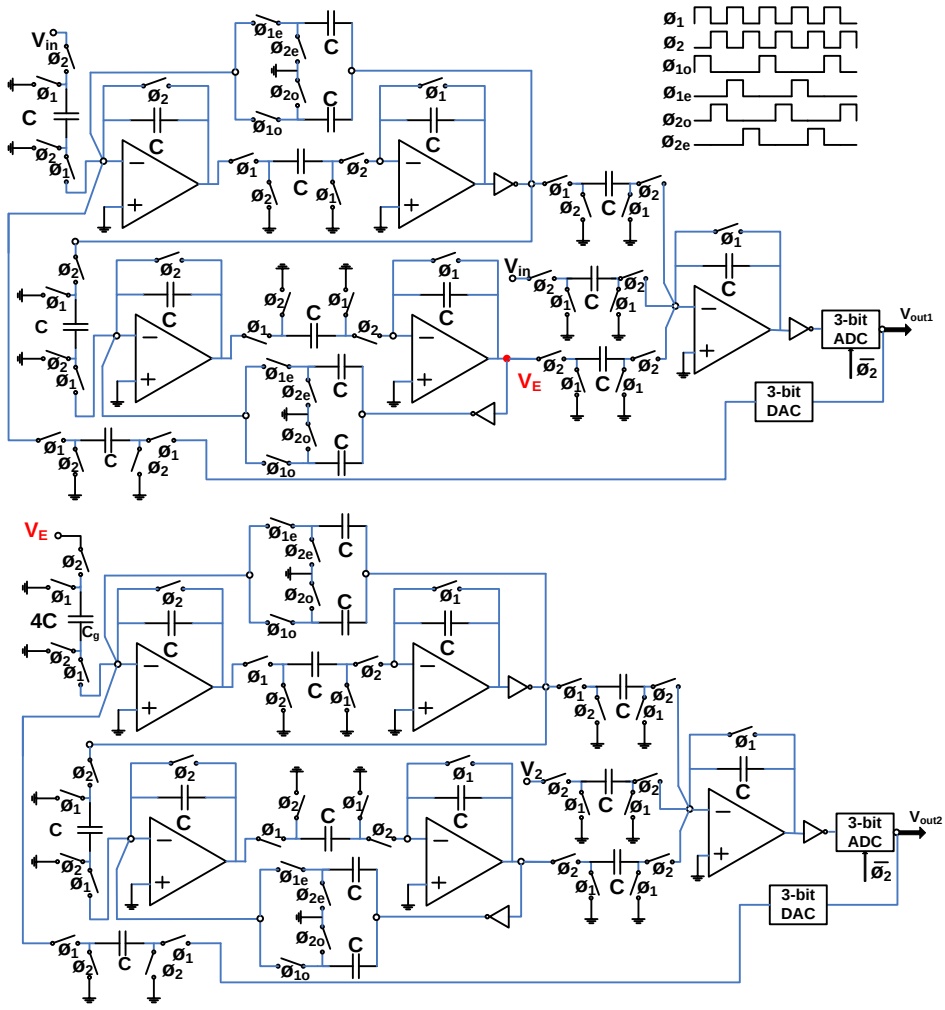


Figure 6.20: Single ended SC Circuit Implementation of Conventional FF MASH 2-2 BPΣΔM using TDL Resonator

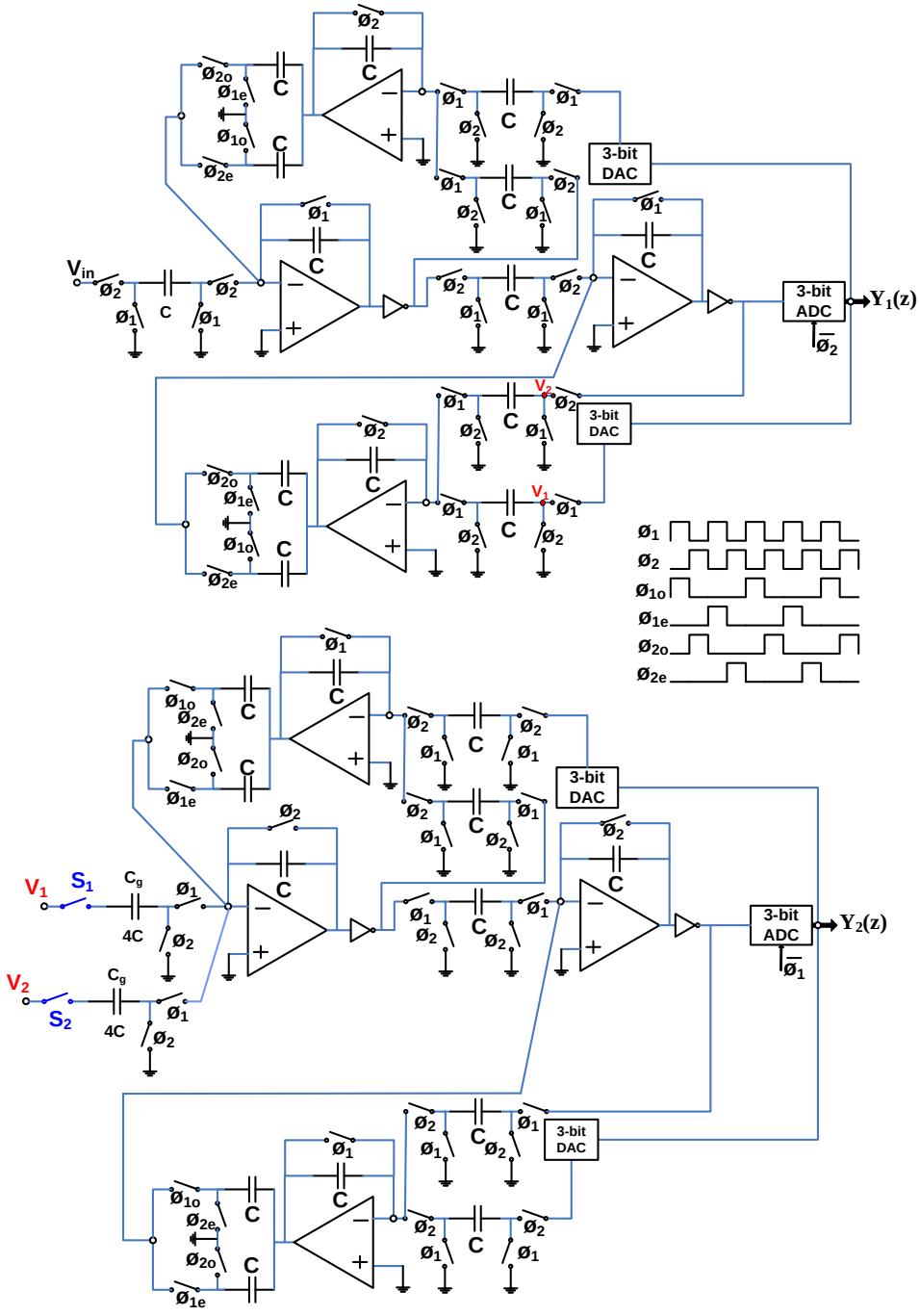
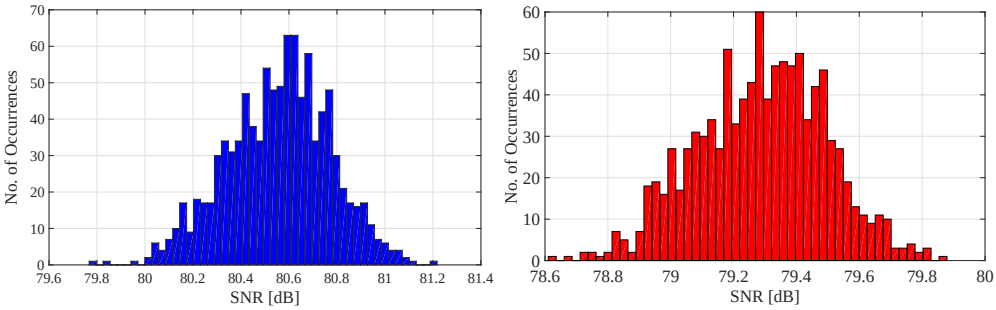


Figure 6.21: Single ended SC circuit implementation of MASH 2-2 BP DQEFM using S/H circuit

and comparators were implemented at the transistor level using 45nm CMOS technology. The circuit was operated with two non-overlapping clocks $\phi 1$ and $\phi 2$. Monte carlo simulation with 1000 iterations were conducted for the sampling capacitor (C_g) by assuming a mismatch of $\pm 1\%$ in the capacitor value. The histogram output based on Monte Carlo simulation for the conventional and proposed architecture are shown in Figure 6.22.

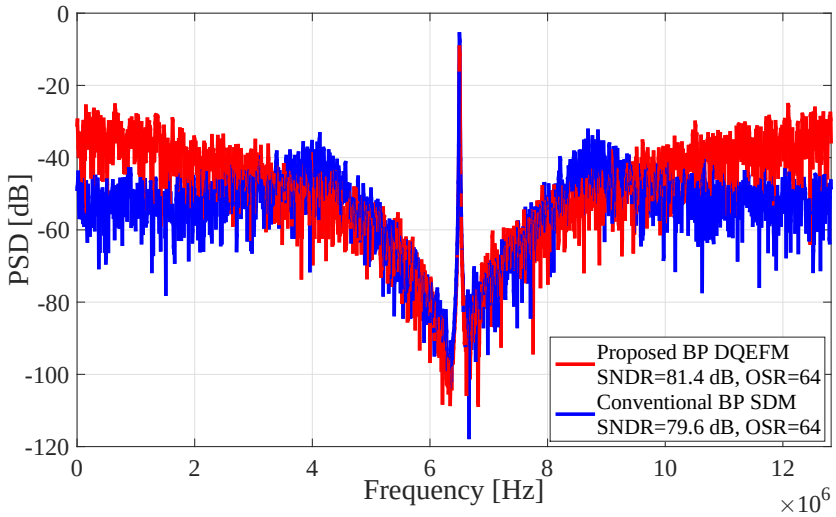


(a) Proposed MASH 2-2 BP DQEFM architecture (b) Conventional FF MASH 2-2 BP architecture

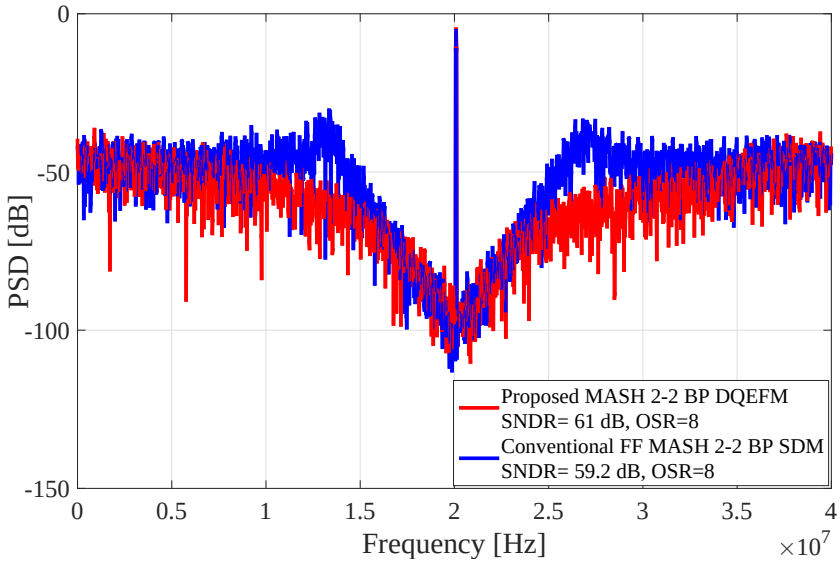
Figure 6.22: Histogram showing the Monte Carlo Simulation Results for the Capacitor Mismatch

The MASH BP DQEFM is made re-configurable to perform data conversion in GSM/ WCDMA standards. The GSM/WCDMA standards of operation can be selected by a simple mechanism, consisting of a pair of switches namely S_1 and S_2 as shown in Figure 6.21. When both switches are in the open state, the first stage become isolated from the second stage and a second order modulator comes into operation for the GSM mode. When both switches are closed, the complete 2-2 MASH structure operates in WCDMA mode. The second order modulator in the first stage of proposed MASH structure attains the necessary SNDR requirements for GSM standard and the complete 2-2 MASH circuit accomplishes the SNDR demanded in WCDMA operation. The output of the conventional and proposed modulators from HSPICE were evaluated through a 4096 point FFT to get the power spectral density (PSD). Figure 6.23 shows the simulated output spectrum of the conventional and proposed architectures implemented in HSPICE using 45 nm technology for GSM and WCDMA

standards.



(a) GSM



(b) WCDMA

Figure 6.23: Output Spectrum of the Conventional and the Proposed Architecture used in Multi-standard Applications obtained through Circuit Implementation using HSPICE

The circuit level simulation of the second order first stage of modulator using 45nm CMOS process for a band width of 200 kHz yields an SNDR of 81.4 dB (ENOB-13.22 bits) while dissipating 3.7 mW of power with 1V supply in the GSM mode. A

Table 6.3: Performance summary of the different BP modulators for GSM/WCDMA standards

	Conventional FF MASH 2-2 BP ΣΔM	(Salo *et al.*, 2003)	(Ho *et al.*, 2011)	(Huang and Wang, 2011)	(Jeong *et al.*, 2008)	(Esfahani *et al.*, 2003)	This work
Sampling Frequency[MHz]	25.6/80	80	51.2/120	80	26	13	25.6/80
Bandwidth [MHz]	0.2/5	0.27/3.84	0.27/5	5	5	0.27	0.2/5
Architecture	DT BP	DT BP	QBP CT	DT BP	DT BP	CT BP	DT BP
Order of Modulator	2/4	4/4	2/2	6	4	4	2/ 4
No. of quantizer bits	3/3	1/4	4/4	3	1	1	3/3
SNR [dB]	95/79.5	80/48	-	-	26	-	95/ 80.8
SNDRp [dB]	79.6/59.2	78/48	81/61.2	48.6	24	78.4	81.4/61
ENOB	12.93/9.54	12.66/7.68	13.16/9.87	7.78	3.69	12.73	13.22/9.84
Power[mW]	4.4/7.5	24/38	4.9/8.9	44	2.34	4.6	3.7/6.9
Supply Voltage [V]	1	3	1.8	1.5	1.8	2	1
Technology [nm]	45	350	180	180	180	250	45
FoM [pJ/conv]*	1.40/1.01	6.86/24.1	0.99/0.95	20	14	1.25	0.96/0.75

* Figure of Merit (FoM)= $\frac{Power}{2^{\frac{SNDR-1.76}{6.02}} \times 2BW}$

Figure of Merit (FoM) of 0.96 pJ/conv-step is attained in the GSM mode. The circuit level simulation of the complete MASH 2-2 BP DQEFM structure in the WCDMA mode using 45 nm technology attains an SNDR of 61 dB (ENOB-9.84 bits) for a bandwidth of 5 MHz, while dissipating 6.9 mW of power with 1V supply. A FoM of 0.75 pJ/conv-step is obtained while working in the WCDMA mode. The performance summary of the proposed MASH 2-2 BP DQEFM in comparison with other state-of-the-art modulators is provided in Table 6.3. The lower value of FoM shows that performance of our proposed modulator is much better compared to other state-of-the-art bandpass modulators.

6.6 Chapter Summary

The chapter presented a novel BP DQEFM structure and its mathematical equivalence to conventional BP $\Sigma\Delta$M have been validated through mathematical analysis and simulations. The cascaded BP DQEFM is able to accomplish data conversion in GSM and WCDMA standards. The DQEFM architecture is selected for the MASH topology because of its reduced sensitivity to circuit non-idealities and less hardware requirements. The second order BP modulator utilized in the first stage of MASH structure comes into operation while working in GSM mode, isolating the second stage inorder to reduce the power consumption. The complete fourth order MASH BP modulator is selected for operation in WCDMA mode. The circuit level simulation of the proposed MASH 2-2 BP DQEFM achieves an SNDR of 81.4 dB/61 dB, with a power consumption of 3.7 mW/6.9 mW from a 1V supply for GSM and WCDMA modes respectively. The FoM achieved for the proposed modulator shows that it is a good candidate for data conversion of narrow band IF signals in superheterodyne receivers.

CHAPTER 7

CONCLUSION

This chapter summarizes the major objectives, methodologies, research findings and finally a few perspectives for future work.

7.1 Summary of the Thesis

The thesis sheds light on advanced and more sophisticated $\Sigma\Delta$ modulator architectures for future wideband applications. The challenges in designing a wideband ADC are analyzed and addressed by suitable low power and hardware efficient cascaded $\Sigma\Delta$ architecture with resolution enhancement techniques. A significant contribution of this thesis is the architectural-level exploration of efficient cascaded discrete time $\Sigma\Delta$ architectures for data conversion in next generation low power and wide bandwidth wireless communication systems. The details of the major contributions made in this research work are as follows:

- The thesis commences with the basic concepts of $\Sigma\Delta$ modulation, and discusses about how this modulator achieves high resolution through oversampling and noise shaping techniques. The development phases of $\Sigma\Delta$ architectures, various architectural improvements occurred during the preceding decades and main classification of $\Sigma\Delta$ architectures are also discussed.

- An effective method to enhance the resolution of cascaded $\Sigma\Delta$ modulators through analog feedback paths between the cascaded stages is presented. This technique is adopted for a MASH/SMASH 2-1 $\Sigma\Delta$ structure for achieving

fourth and fifth order noise shaping, without affecting the digital cancellation logic. The higher order noise shaping attainment is at the expense of extra delay blocks and without any increase in the number of active blocks. The use of of low-distortion topology, selection of low operating frequency, higher order noise shaping with reduced number of active components are the main features of this architecture. Mathematical analysis and behavioral simulation results obtained for both MASH and SMASH architectures prove the fitness of this architecture. The comparison with the other state-of-the-art $\Sigma\Delta$ architectures indicates that the proposed architecture is a right candidate for low power wideband applications.

- The thesis proposes another improved low-distortion cascaded $\Sigma\Delta$ architecture for analog to digital conversion in higher bandwidths. This architecture is capable of attaining an enhancement in the resolution through techniques like resonation and NTF zero optimization. The shifted loop delay techniques introduced in the cascaded structure solves the timing issues in the critical path of the modulator. The low-distortion architecture, reduction in active components and elimination of a power hungry adder helps this modulator to be used in low power applications. The behavioral simulations, mathematical analysis and an SNDR and dynamic range of value above 90 dB prove the effectiveness and feasibility of this modulator.

- The thesis also presents the design and simulation of a lowpass MASH DQEFM architecture. The DQEFM structure has been chosen for obtaining benefits like relaxed op-amp requirements and reduced sensitivity to mismatch effects. The lower operating frequency and better performance of the proposed modulator in terms of hardware complexity and power makes it suitable for data conversion in 4G wireless radios. The sensitivity of the proposed modulator to

finite op-amp DC gain, bandwidth, slew rate, and mismatch effects have been analyzed. The circuit level simulations performed using HSPICE with 45nm CMOS process indicate that the proposed modulator attains a peak SNDR of 58dB over a bandwidth of 20 MHz while dissipating 5.9 mW of power.

- The thesis finally presents a novel BP DQEFM architecture and its cascaded implementation. The mathematical analysis and simulation results indicate the resemblance of the proposed BP DQEFM with the conventional BP $\Sigma\Delta$M. The circuit level simulations of the second order BP DQEFM for a digital radio application indicate the better performance of the proposed BP DQEFM in terms of hardware complexity and power. A re-configurable cascaded BP DQEFM architecture has been designed for data conversion operation in GSM/WCDMA standards. The circuit level simulation of the proposed MASH 2-2 BP DQEFM achieves an SNDR of 81.4 dB/61 dB, with a power consumption of 3.7 mW/6.9 mW from a 1V supply for GSM and WCDMA modes respectively. The FoM achieved for the proposed modulator shows that it is a good candidate for data conversion of narrow band IF signals in superheterodyne receivers.

7.2 Future Work

This section briefly describes some interesting research topics, which are worth investigating further to improve and extend the work presented in the thesis.

- The $\Sigma\Delta$ ADC consists of $\Sigma\Delta$ modulator part and a digital decimation filter. This thesis explores various cascaded $\Sigma\Delta$ modulator architectures. The complete converter operation requires the decimation filter part. It will be an interesting research topic to design and implement a low power hardware efficient

digital decimation filter (Cao *et al.*, 2013) part following the analog modulator section.

- The high-speed clock requirements of the ΣΔM in wideband applications can be alleviated by parallel processing techniques. However, this requires complex circuitry and more resources are needed in the implementation of ΣΔMs. The time-interleaving (TI) technique and many interconnected parallel modulators that are working concurrently can be utilized for getting higher sampling rate. By using this technique, the required resolution can be acquired without increasing the order of the modulator or the number of bits of the quantizer and also without utilizing a state of the art technology (Talebzadeh and Kale, 2018). TI and N-path operation of DQEFM architecture is another research area to be explored.

- Another prominent area for future research is the hybrid ΣΔM (Kulchycki *et al.*, 2008; Garca-Snchez and Sandoval-Ibarra, 2017). It combines the benefits of discrete time and continuous time ΣΔ modulators. The hybrid ΣΔM benefits the accurate loop filter characteristic of a DT ΣΔM and the inherent anti-aliasing of a CT ΣΔM. The initial stages of ΣΔM are implemented with CT integrators and the subsequent integrators in the loop filter are implemented in discrete time (Kwan *et al.*, 2008). The architectures proposed in this thesis can be implemented using a combination of discrete time and continuous time circuits to avail the benefits of hybrid ΣΔM.

- The architectures proposed in this thesis can be optimized for maximum performance at the system level and circuit level so that they can be used for the implementation of high speed, low power ADCs required for internet of things (IoT) applications. The sharing of op-amps (Q *et al.*, 2017) is an attractive design technique to attain a low power ΣΔM. The low power operation de-

manded by the portable devices can be satisfied by designing $\Sigma\Delta$M with passive switched capacitor integrators and passive adders in order to achieve power efficiency (Sadollahi and Temes, 2017; Li *et al.*, 2018).

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LIST OF PAPERS BASED ON THESIS

I. Refereed Journals

1. **Rijo Sebastian**, Jos Prakash, Babita Roslind Jose, Shahana T.K, "Multi-Stage Noise Shaping $\Sigma\Delta$ Modulator with Enhanced Noise Shaping for Low Power Wideband Applications", *Journal of Low Power Electronics*, vol. 13, no. 4, pp. 661-668, December 2017. (Scopus indexed, Impact Factor: 0.84) doi.org/10.1166/jolpe.2017.1511.

2. **Rijo Sebastian**, Babita Roslind Jose, Shahana T.K, Jimson Mathew, "A Low-distortion Hardware Efficient MASH Sigma Delta Modulator with Enhanced Noise Shaping", *Smart Science* - Taylor & Francis, vol. 6, no. 2, pp. 158-172, December 2017. (Scopus indexed) https://doi.org/10.1080/23080477.2017.1417962.

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4. **Rijo Sebastian**, Jos Prakash, Babita Roslind Jose, Shahana T.K., Jimson Mathew, "A Re-configurable MASH 2-2 bandpass DQEFM for Multi-standard Applications", *International Journal of Electronics- Taylor & Francis*, vol. 106, issue.10, pp. 1498- 1513, April 2019. (SCI indexed, Impact Factor: 0.939) https://doi.org/10.1080/00207217.2019.1600737

II. Presentations in Conferences

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4. **Rijo Sebastian**, Jos Prakash, Babita Roslind Jose, Shahana T.K, Jimson Mathew, "A lowpass MASH DQEFM for 4G wireless receivers", *7th International Conference on Smart Computing and Communications (ICSCC 2019)*, Curtin University, Malaysia, 28-30 June 2019.

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