Fabrication of thin film transistors and development of complementary metal oxide semiconductor inverters

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Fabrication of thin film transistors and development of complementary metal oxide semiconductor inverters

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Certificate

Certified that the work presented in this thesis entitled ***"Fabrication of thin film transistors and development of complementary metal oxide semiconductor inverters"*** is based on the authentic record of research carried out by Shijeesh M. R. under my guidance in the Department of Physics, Cochin University of Science and Technology, Cochin-682 022 and has not been included in any other thesis submitted for the award of any degree. All the relevant corrections and modifications suggested by the audience during the pre-synopsis seminar and recommendations by the doctoral committee of the candidate have been incorporated in the thesis.

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Declaration

I hereby declare that the work presented in this thesis entitled ***"Fabrication of thin film transistors and development of complementary metal oxide semiconductor inverters"*** is based on the original research work carried out by me under the supervision and guidance of Dr. M. K. Jayaraj, Professor, Department of Physics, Cochin University of Science and Technology, Cochin-682 022 and has not been included in any other thesis submitted previously for the award of any degree.

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Dedicated to my friends and family

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CONTENTS

Preface

Transparent electronics is developing as one of the most hopeful technologies for future electronic products; as it delivers an innovative advancement in the light weight, transparent and flexible electronic devices. The next generation electronics will be based on these transparent materials as they meet the demands and requirements of the present day technology. The transparent electronics attracted more attention after the revolutionized invention of transparent-conducting materials such as ITO, SnO_2 and ZnO. These transparent conducting oxides (TCOs) are commonly used in the transparent window electrodes and circuit interconnections of modern electronic devices. The invention of p-type $CuAlO_2$ by Kawazoe *et. al.* made a breakthrough in the field of transparent electronics because it opened a window for the development of new p-type materials. Also, the material engineering idea of TCO gave a proper understanding of the conduction mechanism of such materials and also helped to tune the electrical conductivity of TCO. The tuning of conductivity enables development of novel TCOs as active material in the field effect devices such as thin film transistors (TFTs). Semiconductors that can be used as an active material having both transparency and controlled electrical conductivity is called transparent semiconductor oxides (TSOs). The collective use of TCO and TSO enables the development of fully transparent thin film transistors (TTFTs). The present work focuses on the fabrication of organic and

inorganic semiconductor TFTs for the development of complementary metal oxide semiconductor inverters.

Chapter 1 gives an introduction to transparent electronics and their applications in future electronic products. A brief literature review of different semiconductor materials studied under the present work and their properties are also discussed. A detailed description of the working principles of TFT and applications are included in this chapter.

Chapter 2 describes the working principles of thin film transistors and extraction of various performance parameters of TFTs. The basic device physics for the calculation of DOS inside the channel layer from the temperature dependent transfer characteristics are discussed in detail. Also the design and working of CMOS inverter is described in brief and method of finding the device parameters from the characteristics are discussed.

Chapter 3 describes the fabrication and electrical characterization of pentacene (p-type) and PTCDI-C8 (n-type) organic thin film transistors. The thermally activated channel conductance was examined and the density of localised states in the gap of both pentacene and PTCDI-C8 was calculated. In order to compare the stability and degradation of pentacene and PTCDI-C8 OTFTs, the devices were exposed to air for 2 h before performing electrical measurements in air. The DOS measurements revealed that a level with defect density of 10^{20} cm^{-3} was formed in PTCDI-C8 layer when exposed to air. The oxygen adsorption into the PTCDI-C8 active layer was attributed to this level and it is located at around 0.15 eV below the LUMO level. The electrical charge transport strongly affected by the oxygen traps and hence p-type organic materials are more stable than n-type organic materials.

Chapter 4 describes the fabrication of amorphous zinc tin oxide thin film transistors (a-ZTO TFTs) by RF magnetron sputtering. In the present study, the device stability with respect to ambient parameters was well studied by analyzing the variation of DOS in the active ZTO channel layer by MTR model. The comparison of transfer characteristics of as prepared and 20 days air exposed ZTO TFT indicated that the performance of TFTs are highly deteriorated by ambient conditions. The deposition of passivation layer on top of the device reduced the aging effect and subsequently the stability of device under ambient condition was improved. Also, we investigated the stability of a-ZTO TFTs under negative gate bias illumination stress (NBIS) at various post-annealing temperatures. A clear dependence of stability of the TFTs on annealing temperature was seen in the NBIS study of ZTO TFTs. The oxygen vacancies present in the channel region created defect states and caused instability under NBIS. The temperature dependent transfer characteristics were measured to investigate oxygen vacancy generated trap states variations. The present study conclude that stability of the devices can be improved by depositing a passivation layer over the channel layer while the post-annealing reduce oxygen vacancies and instabilities under NBIS.

Chapter 5 deals with the deposition of transparent p-type semiconducting Cu_2O and CuO thin films using RF sputtering for the fabrication of thin film transistors. The phase purity of Cu_2O and CuO films were confirmed using XRD, Raman and XPS data. The optical absorption studies revealed the existence of large number of subgap states inside CuO films than Cu_2O films. Cu_2O and CuO thin film transistors were fabricated in an inverted staggered structure by using post-annealed

channel layer. The mobility values of bottom gate structured Cu_2O and CuO TFTs were 5.20×10^{-4} $cm^2V^{-1}s^{-1}$ and 2.33×10^{-4} $cm^2V^{-1}s^{-1}$, respectively. The poor values of sub-threshold swing, threshold voltage and field effect mobility of the TFTs were due to the charge trap density at copper oxide/dielectric interface as well as defect induced trap states originated from the oxygen vacancies inside the bulk copper oxide. The defect induced subgap DOS in fabricated copper oxide TFTs were investigated using temperature dependence of the drain currents. The high-density hole trap states in the CuO channel was figured to be the possible reason for the lower mobility in CuO TFT than Cu_2O TFT.

Chapter 6 describes the fabrication of copper oxide and zinc tin oxide complementary inverters where both the p-type and n-type channels are deposited by RF magnetron sputtering. We have designed comparatively low voltage and high gain complementary inverters by combining a set of p-type copper oxide and n-type zinc tin oxide thin film transistors with different aspect ratios. The voltage gain was found to increase with aspect ratio and a maximum value of 4.2 was reached for an aspect ratio of 2.

Chapter 7 summarizes the main results in the thesis and recommends the scope for future studies.

List of Abbreviations

AFM	Atomic force microscope
AOS	Amorphous oxide semiconductor
CB	Conduction band
CBM	Conduction band minimum
CMOS	Complementary metal oxide semiconductor
DOS	Density of states
E_A	Activation energy
GIXRD	Grazing incidence X-ray diffraction
HOMO	Highest occupied molecular orbital
I_D	Drain current
LED	Light emitting diode
LTPS	Low temperature poly-silicon
LUMO	Lowest unoccupied molecular orbital
MOSFET	Metal oxide semiconductor field effect transistor
NBIS	Negative gate-bias illumination stress
NM	Noise margin
OLED	Organic light emitting diode
PLD	Pulsed laser deposition
PVD	Physical vapour deposition
RF	Radio frequency
TCO	Transparent conducting oxide
TFT	Thin film Transistor
TSO	Transparent semiconducting oxide
VB	Valence band
VBM	Valence band maximum
V_{DS}	Drain-source voltage
V_{GS}	Gate-source voltage
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction

Publications related to the work presented in the thesis

Journal publications

1. *Investigations on the reasons for degradation of zinc tin oxide thin film transistor on exposure to air,* **M. R. Shijeesh**, AC Saritha, MK Jayaraj, ***Materials Science in Semiconductor Processing*** 74, 116-121 (2018)

2. *Low temperature fabrication of Cu_xO thin-film transistors and investigation on the origin of low field effect mobility*, **M. R. Shijeesh**, MK Jayaraj, ***Journal of Applied Physics*** 123 (16), 161538 (2018)

3. *Zinc tin oxide thin film transistor: Effect on channel isolation and channel width*, **M. R. Shijeesh**, MK Jayaraj, ***Invertis Journal of Science & Technology*** 10 (3), 155-160 (2017)
4. *Degradation study and calculation of density-of-states in PTCDI-C8 channel layer from the electrical characteristics of thin-film transistors* **M. R. Shijeesh,** L. S. Vikas, M. K. Jayaraj, and J. Puigdollers, ***Journal of Applied Physics*** 116, 024507 (2014)

5. *Effects of post-annealing on negative bias illumination stress-induced instability of zinc tin oxide thin-film transistor* ***M*****. R. Shijeesh** and M. K. Jayaraj (communicated)

6. *Complementary inverter circuits based on p-Cu_2O and n-ZTO thin film transistors* **M. R. Shijeesh** and M. K. Jayaraj (communicated)

Other publications to which the author has contributed

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2. *Growth and characterization of p-ZnO:Cu thin film and its homojunction application* A C Saritha,**M. R. Shijeesh**,L S Vikas, Rajeev R Prabhu and M K Jayaraj, ***Journal of Physics D: Applied Physics*** 49, 295105 (2016)

3. *Exceptionally crystalline and conducting acid doped polyaniline films by level surface assisted solution casting approach* Anand B. Puthirath, **M. R. Shijeesh** Sreekanth J. Varma, and Jayalekshmi, ***Applied Physics Letters*** 108, 161901 (2016)

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5. *Solution processable PEDOT: PSS/Multiwalled Carbon Nanotube composite films for flexible electrode applications,* M. Jasna, **M. R. Shijeesh**, S. Jayalekshmi, R. Reshmi and M. K. Jayaraj (under review)

Conference presentations

1. Amorphous oxide thin film transistors for the application of transparent flexible electronics, M K Jayaraj and **M R Shijeesh**, ICEAME 2017, Kanjirappally, Kerala.

2. Fabrication and characterization of zinc tin oxide n-channel thin film transistors**, M R Shijeesh**, A C Saritha, and M K Jayaraj, IWPSD- 2017, Kolkata

3. Fabrication of novel organic and inorganic thin film transistors and exploration of subgap density of states, **M R Shijeesh** and MK Jayaraj, ASCII-2017, CUSAT, Kochi, India.

4. Fabrication and characterization of pentacene based transparent flexible thin film transistors, **M R Shijeesh**, Kurias K Markose, and M K Jayaraj, CEMAT-2016, IISC, Bangalore.

5. ZTO Thin Film preparation for TFT application, **M R Shijeesh**, A C Saritha, and M K Jayaraj, IWPSD-2015, IISC, Bangalore.

6. Comparative study on degradation and trap density-of-states of p-type and n-type organic semiconductors, **M. R. Shijeesh**, L. S. Vikas, M. K. Jayaraj, and J. Puigdollers,SPIE Proc9185, 918519 (2014)

7. Nonlinear properties of IGZO thin films prepared by RF magnetron sputtering, KC Sanal, K Vishnu, **MR Shijeesh**, MK Jayaraj, SPIE Proc91611B-91611B-8 (2014)

Chapter 1

Transparent electronic materials

1.1 Introduction

Transparent electronics is developing as one of the most hopeful technologies for future electronic products; as it delivers an innovative advancement in lightweight, transparent and flexible electronic devices. The next generation electronics will be based on transparent materials because it fulfills the requirements and one of the most viable technology for the consumer electronics. A combination of optical transparency and electrical conductivity is not common in materials. Transparent electronics accomplished more attention after the revolutionized invention of transparent-conducting materials such as indium tin oxide (ITO), SnO_2 and ZnO. They are known as transparent conducting oxides (TCOs) and are commonly used in the transparent electrodes and circuit interconnections of modern electronic devices [1,2]. From the initial developmental period, most of the known TCOs are n-type materials and the absence of p-type TCOs are the main hindrance to the development of the active transparent devices such as diodes and LEDs. The invention of p-type TCO, $CuAlO_2$ by Kawazoe *et al.* [3] marked the breakthrough in the field of transparent electronics because it gave an open window for the development of new p-

type materials. Also, the material engineering idea of TCO gave the proper understanding of conduction mechanism of such materials which in turn helped in tuning the electrical conductivity of TCOs. The tuning of conductivity enabled the recent development of TCOs as an active material in the field effect devices such as thin film transistors (TFTs). The semiconductors that can be used as an active material having both oxide transparency and controlled electrical conductivity are called transparent semiconductor oxides (TSOs). The collective use of TCO and TSO enables the development of fully transparent thin film transistors (TTFTs).

Most of the n-type TFTs are made of amorphous silicon and polycrystalline silicon. They are mainly used in the liquid crystal display (LCD) technology and the display manufacturers are focusing on the development of high-performance large area display units. TFTs are also used in digital X-ray imagers, radio-frequency identification (RFID) tags, sensing devices, several medical applications, and low-cost disposable electronics [4–6]. Modern technologies are now focused on devices having lower power utilization and lower manufacturing cost [7]. To meet the future requirements for novel electronic applications, they are in search of better materials for TFT fabrication. The motivation behind the search for novel materials is to meet certain requisites such as low manufacturing cost, flexible electronics, development of organic light emitting diodes (OLED) displays and new functionality for the wide electronic applications [8,9].

The cost issue is not only related to the sophisticated equipment used for the fabrication but also the cost of materials used in the device fabrication. To reduce the overall cost of fabrication, it is essential to discover alternate novel inexpensive and abundant materials for device fabrication. For example, in the case of metal oxide semiconductor based

TFTs, indium-based compounds are the most established active materials for the TFT fabrication, which certainly needs cheap and efficient alternatives [10].

Flexible electronics is an emerging field of the modern electronic industry because it delivers future needs of a lightweight, foldable and rollable electronic devices such as smartphones, laptops and smart watches etc. Today's electronic products mainly fabricated on easily breakable glass substrates cannot be considered suitable for the above mentioned flexible electronic applications. The scope and hope for an immense success of flexible electronics shortly lead to the intensive search for novel materials. Organic semiconductors and metal oxide semiconductors are the prominent class of materials that seem to be promising for these applications since organic TFT (OTFT) and metal oxide semiconductor TFT can be fabricated on flexible plastic substrates [11].

In an LCD unit, the backplanes consist of a-Si or low-temperature poly-silicon (LTPS) TFTs for driving each pixel, and this technology has been in place over the last few decades. For the emerging OLED display, neither of these TFTs are suitable enough for driving the pixels. The mobility of a-Si TFTs are comparatively low because of the inherent properties of that materials and it needs five times higher for OLED applications. Though the mobility of LTPS is large enough for TFT application, the non-uniformity restrict the use of LTPS TFTs in the OLED display. So to replace the LCD with OLED display, the manufacturers are in a serious search of novel materials. For the past ten years, many research groups were working on finding potential candidates for the development of TFTs having high mobility. Metal oxide semiconductors and organic semiconductors are the possible alternatives of a-Si and LTPS TFTs

because they have high mobility, low processing temperature, low manufacturing cost and large area uniformity which are the essentials for all the future electronic applications.

1.2 Metal oxide semiconductors

In recent years, metal oxide semiconductors have turned out to be a strong candidate for the development of future electronic devices. They possess high carrier mobility and transparency which are highly recommendable for modern electronic devices and applications. Many research groups and industrialists all over the world are showing extreme interest in this material class and some electronic products based on these novel efficient metal oxide semiconductors have already entered the market. Since the first report on the development of high mobility amorphous oxide semiconductor InGaZnO (IGZO) TFT in 2004, extensive research has been initiated on these materials for the development of large area high definition flat panel display [4]. Many flat panel display (FDP) manufacturers such as Samsung, LG and Sharp have already developed large area active matrix OLED display based on IGZO [12–14].

Oxide TFTs have now been fabricated with oxides of various metals such as In, Ga, Zn, and Sn and also with their alloy compounds. At present, indium gallium zinc oxide (InGaZnO), zinc indium oxide (ZnInO), zinc tin oxide (ZnSnO), zinc indium tin oxide (ZnInSnO) etc. are the most used n-type channel materials for the fabrication of amorphous oxide semiconductor based TFTs [15–18]. Indium-free systems are highly preferred for their cost-effectiveness. Hence, among the above-mentioned materials, zinc tin oxide (ZTO) is more favorable and economical for fabricating high-performance TFT. A field effect mobility as high as 50

$cm^2V^{-1}s^{-1}$ and $I_{on/off}$ ratio 10^7 has been reported for ZTO TFT [19]. All the above-mentioned TFTs are based on n-type oxide materials and there is a difficulty in realizing p-type TFTs with comparable performance as that of n-type TFTs.

1.2.1 N-type oxide semiconductors

Metal oxide semiconductors for TFT applications are classified mainly into two categories: 1) Binary oxides and 2) multi-component oxides. These wide bandgap materials have good transparency in the visible region which allows the fabrication of transparent TFT, the key component in the idea of invisible electronics.

The first TFT was reported in 1964 fabricated by evaporating SnO_2 as the channel layer on a glass substrate having bottom gate configuration [20]. The first TFT had poor performance with no saturation and with high off current. Even though the device could not turn off, it was a milestone to the invention of modern TFT. After that, TFT based on ZnO as channel material was developed in 1968 [21]. The first ZnO TFT also suffered from lack of saturation and good TFT parameters. Since then, historical developments have occurred in the field of metal oxide TFTs. Now, metal oxide semiconductors are being used in novel display units proving themselves as potential candidates for the development of future transparent flexible electronics.

i. Binary oxide semiconductors for TFT application

The most studied binary oxide semiconductors for TFT applications are ZnO, SnO_2 and In_2O_3 [22]. In earlier days, these transparent conducting oxides were much explored because of their inherent high conducting nature (10^{-2} Scm^{-1} to 10^3 Scm^{-1}) due to the existence of shallow defects

inside the materials and high transparency owing to wide bandgap. The heavy post-transition metal cations in these materials have the electronic configuration of $(n-1)d^{10}ns^0$ $(n\geq4)$. The spherical symmetry of s orbitals leads to the overlapping of neighboring s orbitals even if there is structural randomness. This enables the electron conduction even in the amorphous states of metal oxide semiconductors. For these reasons, the above three materials are still considered as the base materials for amorphous oxide semiconductors. The present research and development in oxide materials as TFT channel layers focus on controlling the electrical conductivity of these oxides by fine-tuning the deposition conditions. Table 1.1 shows the summary of the performance of TFTs fabricated using n-type binary oxide channel layers.

The transparent TFT has grown through continuous development in material and process technology since the first fabrication of fully transparent ZnO TFT by Hoffman *et al.* in 2003 [6]. They fabricated the TFT by ion beam sputtering and got saturation mobility of 2.5 $cm^2V^{-1}s^{-1}$, high $I_{on/off}$ ratio of 10^7 and an optical transmission of 75%. The annealing temperature was 800 °C in oxygen ambiance and the better performance was due to the improvement in crystallinity of ZnO channel layer. In the same year, Masuda *et al.* reported ZnO TFT on a silicon dioxide substrate by pulsed laser deposition technique and the obtained field effect mobility was 1 $cm^2V^{-1}s^{-1}$ [23]. In this work, a processing temperature of 450 °C was followed to reduce the carrier concentration. The high-temperature processing of ZnO was the main hindrance for the development of flexible electronics and intense research work was devoted to minimizing the processing temperature.

Table 1.1. Summary of the performance of thin-film transistors (TFTs) fabricated using n-type binary oxide channel layers.

Binary oxide materials	Technique	Mobility ($cm^2V^{-1}s^{-1}$)	$I_{on/off}$	year	Ref
ZnO	Sputtering	>2	10^6	2003	[24]
ZnO	PLD	1	10^5	2003	[23]
ZnO	Ion beam sputtering	2.5	10^7	2003	[6]
ZnO	Sputtering	27	3×10^5	2004	[25]
ZnO	ALD	21.3	10^7	2014	[26]
ZnO	PEALD	12	3.4×10^9	2018	[27]
InO_x	RF-PERTE	0.02	10^4	2006	[28]
In_2O_3	Ion-assisted deposition	120	10^5	2006	[29]
In_2O_3	Thermal Evaporation	34	10^4	2008	[30]
SnO_2	Sputtering	2	10^5	2004	[31]
TiO_2	PLD	0.08	10^4	2006	[32]
TiO_2	PEALD	1.64	10^5	2009	[33]
TiO_2	Sputtering	0.69	10^7	2011	[34]

ALD = Atomic layer deposition, PEALD = Plasma enhanced atomic layer deposition, PLD = Pulsed laser deposition, RF-PERTE = radio frequency plasma enhanced reactive thermal evaporation

ZnO TFT was fabricated at room temperature for the first time in 2003 by Carcia *et al.* [24]. They obtained better performance in TFT with a field effect mobility >2 $cm^2V^{-1}s^{-1}$ and $I_{on/off}$ ratio 10^6. Later, successful

demonstration of transparent ZnO TFT using radio frequency (RF) magnetron sputtering technique was reported at lower processing temperature. A high-performance ZnO TFT with high mobility at room temperature was fabricated by Fortunato *et al.* in 2004 [25]. In 2014, Geng *et al.* successfully fabricated ZnO TFT with field effect mobility of 21.3 $cm^2V^{-1}s^{-1}$ and an $I_{on/off}$ ratio of 10^7 using atomic layer deposition (ALD) process [26]. In 2017, Li *et al.* reported ZnO TFT by depositing dual layer ZnO channel with the mobility of 12 $cm^2V^{-1}s^{-1}$ and $I_{on/off}$ ratio of 3.4×10^9 [27]. Active research in the ZnO TFT fabrication at room temperature is still going on to improve the properties for application in transparent flexible electronics.

Another important binary oxide candidate indium oxide (In_2O_3) entered into the field of TFT after three years following the development of the first ZnO TFT. Normally, In_2O_3 is used as transparent conducting oxide due to its high carrier concentrations ($>10^{19}$ cm^{-3}) and it was a very difficult task to control the electron concentration favoring transistor application. The report by Lavareda *et al.* in 2006 investigated the optimization of carrier concentration by controlling the RF power and oxygen content during the radio-frequency plasma enhanced reactive thermal evaporation of In_2O_3 [28]. They observed a reasonable performance of TFT having a field effect mobility of 0.02 $cm^2V^{-1}s^{-1}$ and an $I_{on/off}$ ratio of 10^4. Vygranenko *et al.* in 2006 fabricated completely transparent In_2O_3 TFTs at room temperature exhibiting excellent performance by using ion-assisted deposition [29]. The transparent TFTs were found to exhibit large field effect mobility of 120 $cm^2V^{-1}s^{-1}$ and an $I_{on/off}$ ratio of 10^5 with an ultrathin high-capacitance/low-leakage organic gate dielectric. Bottom gate - top contact TFT have been fabricated with

various channel layer thickness ranging from 5-20 nm in 2008 [30]. It was found that the grain boundary effect was reduced with increasing thickness and enhances the TFT performances.

The first enhancement mode SnO_2 TFT was fabricated by Presley *et al.* in 2004 by RF magnetron sputtering followed by rapid thermal annealing in O_2 at 600 °C [31]. The devices were highly transparent with channel layer thickness ranging from 10-20 nm and showed a good performance with field effect mobility of 2 $cm^2V^{-1}s^{-1}$. Another aspiring metal oxide candidate, TiO_2 based TFT was reported on 2006 by Katayama *et al.* [32] that exhibited a field effect mobility of 0.08 $cm^2V^{-1}s^{-1}$ and $I_{on/off}$ ratio of 10^4. This report was the realization of TiO_2 TFT by atomic scale surface control for the application of electronic and magnetic devices. In 2009, Park *et al.* reported improved TiO_x active-channel TFTs grown by low-temperature plasma enhanced atomic layer deposition (PEALD) which showed the field effect mobility of 1.64 $cm^2V^{-1}s^{-1}$ [33]. Choi *et al.* in 2011 reported amorphous TiO_2 TFT by direct-current magnetron sputtering using an oxygen-deficient TiO_2 target. The device had high $I_{on/off}$ ratio of 10^7 and mobility of 0.69 $cm^2V^{-1}s^{-1}$ [34].

ii. Multicomponent oxide semiconductors for TFT application

The inherent electronic configuration of transparent conducting oxides makes such materials suitable for application in the field of transparent electronics. They have high conductivity even in the amorphous phase due to the spherical symmetry of vacant s orbitals. The electronic conduction occurs due to the overlap of s orbitals of the neighboring cations even if the materials have disordered state in the amorphous phase. For the application of semiconductor thin films as TFT channel layer, their

amorphous nature is preferred over crystalline films; since the former one can get easily deposited at lower temperatures with high uniformity. The non-uniformity and high processing temperature are the main disadvantages of crystalline materials for the fabrication of transparent flexible TFTs.

Table 1.2. Summary of performance of thin-film transistors (TFTs) fabricated using n-type multicomponent oxide channel layers.

Multi-component oxide materials	Technique	Mobility ($cm^2V^{-1}s^{-1}$)	$I_{on/off}$	year	Ref
InZnO	Sputtering	20	10^8	2006	[35]
InGaZnO	PLD	9	10^3	2004	[4]
InGaZnO	Sputtering	12	10^8	2006	[36]
InGaZnO	Sputtering	35.9	4.9×10^6	2007	[37]
HfInZnO	Sputtering	10	10^8	2009	[38]
ZrInZnO	Sputtering	3.9	10^7	2009	[39]
AlSnInZnO	Sputtering	31.4	2×10^9	2010	[40]
SiInZnO	Sputtering	21.6	10^7	2010	[41]
SnInZnO	Sputtering	24.6	10^9	2009	[42]
SnInZnO	Sputtering	12.4	10^8	2008	[43]
ZnON	ALD	6.7	9.4×10^7	2007	[44]
ZnSnO	Sputtering	14	10^6	2005	[10]
ZnSnO	Sputtering	50	10^7	2005	[19]
GaZnSnO	Sputtering	24.6	10^6	2005	[10]
ZrZnSnO	Sputtering	8.9	7.5×10^8	2011	[45]

The easiest way of creating amorphous state in semiconductors is mixing of individual semiconductors with different crystal structures. The mixing of ZnO, SnO_2 and In_2O_3 have been widely carried out for the preparation of amorphous oxide semiconductors because of their unique electronic configurations. Table 1.2 shows the summary of the performance of TFTs fabricated using multicomponent amorphous materials channel layers. The most common and established multicomponent amorphous materials are indium zinc oxide (IZO) and zinc tin oxide (ZTO) [19,46,47].

Indium zinc oxide is prepared by mixing ZnO and In_2O_3 having wurtzite and bixbyite structures, respectively. This compound has become one of the most important materials for application as transparent electrodes for manufacturing flat panel displays. The high mobility (>20 $cm^2V^{-1}s^{-1}$) and uniformity of IZO films make it superior to other indium-based amorphous semiconductors. Though IZO showed excellent properties, the researchers were searching for other materials for the replacement of expensive indium in IZO TFTs as channel layer. Normally, IZO thin films have high electron concentration (>10^{17}) and the reduction of the concentration by varying the deposition conditions is trickier. It is very important to maintain a minimum off current for the TFT, and for this, the channel layer must have moderate carrier concentration approximately between 10^{13} and $10^{17}/cm^{-3}$ [48].

In 2004, Nomura *et al.* succeeded in reducing the carrier concentration by excellent doping mechanism at normal temperatures [4]. They doped Ga into the IZO (IGZO) host matrix and reduced the carrier concentration (<10^{17}) of IZO thin films having high mobility of 10 $cm^2 V^{-1}s^{-1}$. The high ionic potentials of Ga^{3+} facilitates the decrease of carrier concentration through the suppression of oxygen vacancies by tightly

binding oxygen ions. IGZO is the most explored amorphous oxide semiconductor for TFT applications and it has been used recently in the display units of smartphones. After observing the intriguing performance of IGZO, persistent efforts were made to explore more and more multi-component amorphous oxide semiconductors by doping different metals (Hf, Zr, Mg, La, Sc, and Si) into the IZO host matrix [4,38,49–51]. All these materials showed better performance as TFTs and they are widely used in the electronic components.

Among these TFTs AlSnInZnO showed better performance and seems to be a suitable candidate for the application of future electronics [40]. But all the above multi-component amorphous oxide semiconductors had the most expensive and scarce material as an inevitable ingredient i.e. Indium. So the research community eventually looked for another class of suitable material which is more economic. They mixed ZnO and SnO_2 to form inexpensive stable amorphous zinc tin oxide (a-ZTO), for the fabrication of TFT. ZnO and SnO_2 have different crystal structures, wurtzite and rutile, respectively. Hence, mixing of the two easily gives rise to amorphous phase of ZTO. The ZTO is cheaper than IGZO because of the absence of expensive Ga and In metals. As in the case of IZO, researchers are trying to dope different metals into the ZTO host matrix and hopefully they are getting good results.

1.2.2 P-type oxide semiconductors

The development of transparent p-type oxide semiconductors will enable many of the potential transparent electronic applications. The applications which require only unipolar n-type semiconductors are currently well established and they are available in the market. The n-type

TSOs have high performance by its good electron mobility and the devices based on such n-type semiconductors are used in electronic circuits. The p-type counterpart of such n-type oxide semiconductors is very difficult to develop because of the inherent electronic structure of p-type oxide semiconductors. The development of high-performance p-type TSOs will be a great thrust into the future electronic revolution in the field of metal oxide semiconductors. Transparent complementary metal oxide semiconductor (CMOS) devices can be realized through the development of p and n-type TFTs and the CMOS circuits have a very significant role in modern electronic circuits when considering its advantages over silicon technology such as low power dissipation, low process complexity and high noise margin [52]. So the search for high-performance p-type TSOs is still a sought-after topic among the modern research community.

In n-type oxide semiconductors oxygen vacancies produce electrons in the conduction band and the better transport mechanism comes by its electronic configuration. The s orbitals are responsible for the electron transport in the conduction band minimum (CBM) of n-type TSO and so it facilitates smooth conduction of electrons in the material. The spatially spread s orbitals enable adequate hybridization with neighboring s orbitals and forms well delocalized CBM. The highly dispersed CBM causes low electron effective mass and hence high electron mobility. But in the case of p-type TSOs, the valence band maximum (VBM) is composed of highly localized oxygen 2p orbitals which cause large hole effective mass and low hole mobility [53]. The creation of holes in the p-type materials is hindered by the high formation energy of native acceptors and the low formation energy of native donors which annihilates holes. This lack of creation and inefficient transport of holes in p-type material

are the main problems hindering the realization of high-performance p-type TSOs.

To develop high-performance p-type TSOs, novel materials with dispersed VBM have to be designed for attaining large hybridization between orbitals of metal cations and oxygen anions. The first such chemical design was put forwarded and realized by Kawazoe *et al.* in 1997 which was realized by the delafossite structure [3]. They proposed that p-type oxides must have cations with closed shell configurations with energy levels close to oxygen 2p levels. Following this idea, a series of p-type materials having delafossite structure were revealed with a generic formula $CuMO_2$ (M=Al, Ga and In) [54–56]. However, due to the lack of hole mobility of such materials for application in transparent electronics researchers moved towards new materials such as ternary Cu-bearing oxides, spinel-type oxides, PbO, Bi_2O_3, SnO, Cu_2O, CuO and NiO etc.

i. Ternary Cu-bearing oxides

The general chemical formula for the ternary Cu- bearing oxides are $CuMO_2$ (M=Al, Ga, In, Sr, Y, Sc and Cr) and they are commonly deposited by PLD, RF/DC sputtering, CVD, thermal evaporation and hydrothermal methods. The $CuAlO_2$ was first proposed by Kawazoe *et al.* and the cations have closed shell electronic configuration ($d^{10}s^0$) which can easily overlap with O2p orbitals [3]. Even though it was first proposed in 1997, active devices such as TFT based on $CuAlO_2$ were not realized until 2012. The first TFT was fabricated by Yao *et al.* in 2012 and this was the first application level demonstration of p-type $CuAlO_2$ delafossite TSO [57]. The active layer was deposited by radio frequency magnetron sputtering at a substrate temperature of 940 °C and the film had Hall

mobility of 8.4 cm^2V^{-1} s^{-1}. The TFT exhibited a good field effect mobility of 0.97 $cm^2V^{-1}s^{-1}$ which was attributed to the sufficient hybridization of orbitals at the VBM. It also showed good performance with an I_{on}/I_{off} of $8x10^2$ and V_{on} of 5 V.

ii. Binary copper oxides

Copper oxides have two well-known forms, they are cuprous oxide (Cu_2O) and cupric oxide (CuO) and both oxides are reported as outstanding p-type materials [58]. Cu_2O holds excellent hole mobility (exceeding 100 $cm^2V^{-1}s^{-1}$) compared to CuO due to the Cu_2O band structure near the top of the valence band. Oxygen vacancies are responsible for the p-type nature of Cu_2O.The valence band of metal oxides are composed of the localized and anisotropic O2p orbitals and leads to low hole mobilities. But in the case of Cu_2O, the valence band is formed by the hybridization of Cu3d and O2p orbitals and creates fully occupied levels in the VB [59,60]. The smooth hole transport through the VBM is achieved because of the delocalization in the VBM by the dominance of Cu d states.

Though the research on copper oxide has a long history, the fabrication of copper oxide TFT became successful very recently. Matsuzaki *et al.* in 2008 realized first Cu_2O TFT with moderate performance and it was a breakthrough for the research in transparent electronics [61]. The active layer in the Cu_2O TFT was fabricated by PLD method and a stable state of Cu_2O was deposited by varying the oxygen partial pressure and substrate temperature during deposition. The TFT exhibited a field effect mobility of 0.26 $cm^2V^{-1}s^{-1}$ and an $I_{on/off}$ ratio of 6. They reported that the low field-effect mobility and hence the overall poor performance was due to the subgap sates formed by the defect states in the Cu_2O thin films. These subgap states existed even in the films which were

grown under the optimum conditions of 0.65 Pa oxygen pressure and 700 °C substrate temperature.

Polycrystalline Cu_2O nanowire FET was fabricated by Liao *et al.* in 2009 by an Ar/H_2 atmosphere reduction from CuO nanowires [62]. The annealing was performed at a temperature of 400 °C for 24 h and the nanowires were transferred to Si/SiO_2 substrate for the fabrication of Cu_2O nanowire FET. A high-performance FET with field effect mobility of 95 $cm^2V^{-1}s^{-1}$ and large $I_{on/off}$ ratio of 10^6 was obtained.

The above attempts of TFT fabrication involve high-temperature processing which is not favorable for novel flexible electronic applications. In 2010, Fortunato *et al.* fabricated Cu_2O TFT at room temperature for the first time by using RF magnetron sputtering method [63]. Though the post-annealing process involved a temperature of 200 °C, the study gained much importance in the industrial application aspect. The TFT was having a field effect mobility of 1.2×10^{-3} $cm^2V^{-1}s^{-1}$ and $I_{on/off}$ ratio of 2×10^2, which was a breakthrough in the Cu_2O TFT fabrication. Following this room temperature fabrication, many research groups such as Jeong *et al.* [64], Matsuzaki *et al.* [65] and Figueiredo *et al.* [66] tried to fabricate Cu_2O TFT at low processing temperatures. The performance was rather poor for all the fabricated TFTs and the efforts to increase the performance continued.

In 2010, Sung *et al.* successfully fabricated CuO TFT by oxidizing the Cu_2O thin films which were deposited by RF magnetron sputtering [67]. Cu_2O target was used for the deposition of Cu_2O thin films and the as-deposited films were annealed at 300 °C in air to convert Cu_2O to CuO via oxidation process. The TFT showed better performance with field effect mobility 0.4 $cm^2V^{-1}s^{-1}$ and $I_{on/off}$ ratio 10^4.

Another high-performance Cu_2O TFT was reported by Zou *et al*. by PLD method in 2010 [68]. The films were deposited at various substrate temperatures ranging from 400 °C to 700 °C and an optimized condition for the single phase polycrystalline Cu_2O was attained at a temperature of 500 °C. The suppression of scattering of charge carriers from the impurities and grain boundaries in the films were reduced by annealing processes, and the film showed better Hall mobility of 107 $cm^2V^{-1}s^{-1}$. Cu_2O TFT was fabricated using HfON as gate insulator and the interface quality between Cu_2O channel layer and HfON was very good. So the TFT showed better performance with saturation mobility of 4.3 $cm^2V^{-1}s^{-1}$, $I_{on/off}$ ratio of 3×10^6 and an excellent sub-threshold swing of 0.18 V/dec. This high Hall mobility and the better performance of TFT was a promising result in the field of p-type semiconductor research and the scientific community gave more attention to Cu_2O channel layers.

Cu_2O TFT with bilayer structure of SiO_2 and HfO_2 as gate insulator was fabricated by the same group in 2011 at a substrate temperature of 500 °C by PLD method [69]. This bilayer gate structured TFT showed better performance compared to SiO_2 single-layer structured TFT and the improved performance was due to the better interface quality of Cu_2O channel layer with bilayer structure. They observed saturation mobility of 2.7 cm^2V^{-1} s^{-1}, $I_{on/off}$ ratio 1.5×10^6 and a subthreshold swing of 0.137 V/dec.

Researchers were looking for novel approaches and methods to fabricate TFTs and they succeeded in using nanowires for fabricating TFT. In 2011, Han and Meyyappan fabricated Cu_2O TFT using the Cu/Cu_2O core-shell structure formed by thermal oxidation in which core and shell were used as the gate and channel, respectively [70]. The observed mobility

was 26.3 $cm^2V^{-1}s^{-1}$ and $I_{on/off}$ ratio was 10^4 in which the mobility was low when compared to the expected value due to the presence of metallic Cu in the oxide channel layer. This TFT was found to respond very efficiently to humidity and it has potential applications in the modern lightweight humidity sensors.

The active layer thickness dependence on the performance of Cu_2O TFT was well studied by Nam *et al.* in 2012 [71]. Using RF magnetron sputtering they deposited Cu_2O channel layers of thickness varying from 15 nm to 155 nm. The films were annealed at 500 °C for 7 min and the film with 45 nm thickness showed better optical and electrical properties. The fabricated TFT showed a positive shift in turn-on voltages and several humps in the transfer curves. This behavior was noticed in TFTs with thicker channels and it may be due to the formation of multiple channels in the conductive surfaces. Such behavior was less in TFT having 45 nm thickness and it showed field effect mobility of 0.06 $cm^2V^{-1}s^{-1}$ and $I_{on/off}$ ratio of 1.8×10^4.

The potential application of Cu_2O TFT in the low cost, flexible and large area electronic applications was realized by Yao *et al.* in 2012 by fabricating the device on a flexible substrate at room temperature [72]. The Cu_2O thin film was deposited by magnetron sputtering on a flexible polyethylene terephthalate (PET) substrate and the film showed nanocrystalline structure. The Cu_2O TFT exhibited a field effect mobility of 2.4 $cm^2V^{-1}s^{-1}$ and $I_{on/off}$ ratio of 3.96×10^4. The room temperature fabrication of p-type TFT on a flexible substrate with an enhanced performance attracted much attention.

Even though many research groups were working on the fabrication of Cu_2O TFT following different novel methods, any detailed study on the

fundamental transport mechanism of Cu_2O TFT has not been reported hitherto. Jeong *et al.* in 2013 reported a study of the charge transport mechanism in Cu_2O TFT from the temperature dependent transfer characteristics [73]. TFT characteristics were measured at various temperatures ranging from 25 °C to 75 °C and it was concluded that the transport mechanism in the Cu_2O TFT was according to the multiple trapping and release model. The TFT exhibited field effect mobility of 0.06 $cm^2V^{-1}s^{-1}$ and $I_{on/off}$ ratio of 10^4. This poor performance was due to the presence of defect-induced trap states in the channel layer as well as in the channel/insulator interface.

Transparent CuO TFT with aluminium–titanium oxide (ATO) as gate insulator was fabricated by Sanal *et al*. in 2014 at room temperature by RF magnetron sputtering [74]. The TFT exhibited field effect mobility of 0.01 $cm^2V^{-1}s^{-1}$ and $I_{on/off}$ ratio of 10^4.

Solution process fabrication methods are nowadays attaining much importance in transparent flexible electronics due to their low-cost aspect. The solution-processed Cu_2O TFT was fabricated by Kim *et al.* in 2013 by spin coating method [75]. The spin-coated films had to undergo a two-step annealing process at 400 °C in the N_2 atmosphere and at 700 °C annealing in the O_2 atmosphere. Two-step annealing process helps to form a uniform and continuous films of Cu_2O which confirms high-quality semiconductor/insulator interface. The Cu_2O films had a good Hall mobility of 18.9 $cm^2V^{-1}s^{-1}$ and a carrier concentration of $10^{15}cm^{-3}$. The fabricated Cu_2O TFT had field effect mobility of 0.16 $cm^2V^{-1}s^{-1}$ and $I_{on/off}$ ratio of 10^2. The achievement in solution process fabrication of Cu_2O TFT was noteworthy in the field of low-cost p-type TFT assembly.

Several solutions processed Cu_2O TFTs were reported after that with enough potential to achieve high performance. But all the solution processed Cu_2O TFTs were suffering from low field-effect mobility and people are still working hardly on improving the mobility. Pattanasattayavong *et al.* reported Cu_2O TFT fabricated by solution-based spray pyrolysis method in 2013 and the TFT showed low field effect mobility of 3×10^{-4} $cm^2V^{-1}s^{-1}$ and an $I_{on/off}$ ratio of 4×10^3 [76]. Inkjet printing technique is also identified as a good method for the fabrication of solution based TFTs while concerning the low cost of device processing. High-performance CuO TFT was fabricated by Vaseem *et al.* in 2013 by inkjet printing [77]. They achieved a field effect mobility of 31.3 $cm^2V^{-1}s^{-1}$ and an $I_{on/off}$ ratio of 7×10^3.

iii. Tin monoxide

Two stoichiometric forms of tin oxides have been identified until now, namely tin monoxide (SnO) and tin dioxide (SnO_2). SnO_2 is a well-known n-type semiconductor and it had been widely used as gas sensing active material. But SnO was only used as anode material for lithium batteries and as catalyst in organic synthesis. The potential of SnO as a p-type material was first theoretically predicted by Watson and co-workers [78] and Togo *et al.* [53] in 2001. According to them the low formation energy of V_{sn} imparts SnO its p-type conduction nature. Also the VBM in SnO is composed of hybridized Sn5s and O2p orbitals. The presence of highly dispersed VBM due to the contribution from 5s orbitals is coined on the reason for higher hole mobility. After this prediction, researchers started to develop p-type SnO thin films and in 2008 Ogo *et al.* successfully fabricated thin films having high Hall mobility of 2.4 $cm^2V^{-1}s^{-1}$ [79]. They

deposited epitaxial SnO thin films on yttria-stabilized zirconia (YSZ) substrate for the first time.

In 2011 Fortunato and co-workers made a breakthrough by depositing SnO thin films at room temperature via radio frequency magnetron sputtering [80]. The as-deposited films were subjected to post-annealing in air at 200 °C and they observed Hall mobility of 4.8 $cm^2V^{-1}s^{-1}$. The ambipolar nature of SnO thin films was also reported and this is because of the unique electronic structure of SnO [53,81]. The contribution of Sn 5s orbitals to VBM and Sn 5p orbitals to CBM makes SnO both p and n-type semiconductor simultaneously without any doping mechanism. Several groups have fabricated SnO thin films by different physical vapor deposition methods such as sputtering, pulsed laser deposition and electron beam evaporation etc. Atomic layer deposition of SnO and chemical vapor deposition were also reported [79,82].

The first TFT using SnO as channel layer was fabricated by Ogo *et al*. in 2008 by PLD using yttria-stabilized zirconia (YSZ) as substrate [79]. The substrate temperature for the deposition of SnO thin films was 575 °C and PLD deposited Al_2O_3 dielectric films were used as the gate insulator. The TFT had a field effect mobility of 1.3 $cm^2V^{-1}s^{-1}$ and $I_{on/off}$ ratio of 10^2. The low $I_{on/off}$ ratio was due to the large off current present in the device because of the large density of holes around 2.5×10^{17} in the SnO active channel layer. Fortunato *et al.* successfully fabricated SnO TFT at room temperature (RT) by comparatively simpler method of sputtering deposition [80]. The TFT possessed field effect mobility of 4.6 $cm^2V^{-1}s^{-1}$ and $I_{on/off}$ ratio of 7×10^4. This noticeable result was a milestone for the

research in p-type SnO TFT because the existing commercial TFT technology is equipped with magnetron sputtering.

All the reports on SnO TFTs show a large sub-threshold swing (SS) and this detrimental behavior is due to the presence of large defect induced trap states in the active SnO channel layer. The high value of SS limits the successful application of SnO TFTs in electronic circuits such as CMOS inverter. Many research groups are reporting SnO TFTs by using novel methods and deposition conditions.

Several research groups have reported SnO TFTs with various PVD methods [83–86]. In 2012, Okamura *et al.* fabricated first solution processed p-type SnO channel layer for TFT [87]. This promising method encouraged researchers to fabricate SnO TFT with low-cost solution methods like spin coating. The stability study of TFT is very important when concerned with the practical application of SnO TFT on displays. Chiu *et. al.*[88], U *et al.* [89] and Han *et al.* [90], etc. have studied in detail about the stability and durability of SnO TFT under various stress conditions.

iv. Nickel oxide

Nickel oxide (NiO) is a well-known p-type semiconductor with a large work function of 5.4 eV and high bandgap ranging from 3.6 to 4 eV. NiO has a cubic structure and the p-type conduction is attributed to the Ni vacancies. From the band models, NiO is expected to have a metallic character since the VB in NiO is formed by the hybridization of O_{2p} and partially filled metal d orbitals. The p-type conductivity of NiO was explained by different models such as Mott-Hubbard insulator model [91]. The acceptor level created by the Ni vacancies in NiO is situated not very

close to the VBM and the appropriate doping of impurities such as Li can be used to increase the hole conductivity.

The high Hall mobility was reported for NiO films grown by sputtering (Hall mobility - 28.56 cm^2V^{-1} s^{-1}) and spray pyrolysis (Hall mobility - 11.96 cm^2V^{-1} s^{-1}) [92]. Usually NiO thin films are prepared by PVD technique such as sputtering, PLD, electron beam evaporation and chemical methods such as spray pyrolysis, ALD and sol-gel methods.

The first NiO TFT was fabricated by Shimotami *et al.* in 2008 by electric double layer gating technique [93]. They deposited NiO single crystal as channel layer and the TFT showed poor performance with field effect mobility of 1.6×10^{-4} $cm^2V^{-1}s^{-1}$ and $I_{on/off}$ ratio of 10. Jiang *et al.* in 2013 reported NiO TFT with better performance where the channel layer were grown by thermal oxidation of processes [94]. The Ni films were evaporated by e-beam evaporation and the films were thermally oxidized to form p-type NiO thin films by controlling the annealing time. They exhibited field effect mobility of 5.2 $cm^2V^{-1}s^{-1}$ and $I_{on/off}$ ratio of 2.2×10^3. The NiO TFT was fabricated through chemical routes by Takami *et. al.* [95], Liu *et. al.* [96] and Matsubara *et. al.* [97].

1.3 Organic semiconductors

Over the last two decades, significant advance has been achieved in making electronic components for flexible electronic applications. The modern technology needs high performance organic semiconductors for realizing the commercial applications. The novel organic TFTs are the main focus for the development of high performance modern electronic devices such as OLED displays. The cost effectiveness, low processing temperature, high mobility and potential applications in flexible devices

makes organic semiconductors most promising materials for the future electronics.

Organic semiconductors are classified into two categories: conducting polymers and small molecules. The higher molecular weight of polymers makes it suitable for low mobility semiconductors and the mobility depends on the grain size of semiconductors. The device shows better performance when the active channel layer is fabricated by ordered thin films of polymers. The maximum mobility obtained by a polymer TFT was 0.9 $cm^2V^{-1}s^{-1}$ and it was a rather poor mobility as considered for the practical applications of TFT in flexible and rollable displays [98].

Another efficient and acceptable candidate for the organic TFT are the small molecules. Several small molecules were studied for the fabrication of active devices and better performance as compared to amorphous silicon TFT was obtained. Both n-type and p-type small molecules were investigated and the p-type semiconductor was more stable than n-type small molecules. For example, a high mobility of 3.2 $cm^2V^{-1}s^{-1}$ was reported in the case of pentacene which is a p-type organic small molecule [99]. Majority of the organic semiconductors which showed excellent performance, were chemically stable and were found to have p-type conductivity.

1.3.1 P-type organic semiconductors

The materials based on hole transport have been extensively studied for the fabrication of active devices especially on the flexible substrates because of their better mobility. Polymers and π-conjugated oligomers are the most studied p-type organic materials. Poly (3-hexylthiophene) (P3HT) [100], Poly (3-octhlthiophene) (P3OT) , poly 3, 3”-dialkylquarterthiophene

(PQT-12) [101], Poly-9,9'dioctyl-fluorene-co-bithiophene (F8T2) [101] and Poly (2-methoxy-5-(2'-ethyl-hexyloxy)-1,4-phenylene vinylene) (MEH-PPV) [102] are the most common and well-studied p-type organic semiconductor polymers. Even though P3HT exhibits lower mobility, the outstanding solubility of this semiconductor in a wide range of organic solvents makes it an excellent candidate for the solution processed TFT fabrication. Bao *et. al.* [103] first demonstrated P3HT TFT in 1996 after the initial synthesis of P3HT by Mc-Cullough *et. al.* in 1993 [104].

In the case of p-type small molecules, the best reported material is pentacene with a good mobility, better chemical stability, high orderly formation of thin films and good interface properties with source and drain electrodes in TFTs. Even though, pentacene shows better performance than other small molecules, the inability to dissolve in organic solvents limits the fabrication by solution process. All the reported pentacene TFTs were fabricated by thermal evaporation methods. In order to fabricate solution process based pentacene TFT, researchers tried with various precursors using spin coating technique. Herwig *et. al.* [105] in 1999 successfully synthesized a soluble pentacene precursor and started low cost TFT fabrication. Further, Afzali *et. al.* [106] and Anthony *et. al.* [107] successfully fabricated pentacene thin film by low cost deposition methods. The pentacene precursors such as 6,13-bis-triisopropyl-silylethynyl (TIPS) pentacene, tetracene and difluro-trietetracenethylsilylethynyl anthradithiophene (diF-TESADT) are commonly used for TFT fabrication [107–109].

1.3.2 N-type organic semiconductors

The development of n-type organic semiconductor will also enable several applications in the future electronic industry. The majority of the reported works on the organic semiconductors are high performance p-type materials and their n-type counterparts with same performance have not been reported so far. Little efforts have been carried out to synthesize novel n-type organic semiconductors because of two main reasons that limits the processes. First one is that n-type organic semiconductors are very unstable in the ambient conditions. They easily react with atmospheric oxygen/water and the mobility of the material rapidly decreases [110]. The degradation of such n-type semiconductors is the most common problem and this behavior limits the extensive research in the case of n-type materials. Secondly, in order to develop an n-type semiconductor based organic TFT, it has to use metal contacts with suitable work function in which the electrons must be injected into the LUMO level ($E < 2.5$ eV) of organic semiconductor. But the most common metals have a work function suitable for injecting holes into the HOMO levels ($E > 4.5$ eV). So the development of n-type organic semiconductors is a difficult task and the researchers are intensively working on the designing of novel n-type materials.

The easiest way to synthesize n-type organic semiconductor is adding Cl or F into the outer most orbitals of certain organic molecules which can in turn withdraw electrons for conduction. The n-type semiconductor was designed from this idea was Bao *et. al.* [111], by adding F into the copper hexadecafluorophthalocyanine ($F_{16}CuPc$). The OTFT had poor performance having a field effect mobility of 0.03 $cm^2V^{-1}s^{-1}$ and $I_{on/off}$ ratio of 28. Several research groups reported n-type OTFT with moderate performance and still efforts are being made to improve the performance.

Other promising stable n-type materials are N,N'-dioctyl-3,4,9,10-perylene tetracarboxylic diimide (PTCDI-C8) [112], fullerene and soluble fullerene derivatives such as 6, 6-phenyl C61 butyric acid methyl ester (PCBM) [113], perfluoropentacene ($C_{22}F_{14}$) and perfluoro-p-sexiphenyl ($C_{36}F_{26}$) [114].

1.4 Conclusions

Transparent electronics is developing as one of the most hopeful technologies for future electronic products; as it delivers an innovative advancement in the light weight, transparent and flexible electronic devices. This chapter briefly explained an introduction to transparent electronics and their applications in future electronic products. A brief literature review of different semiconductor materials studied under the present work and their properties are also discussed.

Chapter 2

Thin film transistor and CMOS inverter

2.1 Thin film transistors

Thin film transistors are three terminal field effect devices similar to metal oxide semiconductor field effect transistor (MOSFET) and they are widely used in the display industry because of its simple structure. The pixels in flat panel displays such as liquid crystal display (LCD) and modern active matrix organic light emitting diode (AMOLED) disaplys each pixel is controlled by the TFTs which are the main components of these circuits. The development of HD modern display and quality of these displays depends on the performance of TFTs used in the display circuits. The n-type oxide and p-type organic TFTs have already been used in the display industry they showed better performance than p-type oxide and n-type organic TFTs [12,14]. The development of high-performance p-type oxide and n-type organic TFTs are necessary for the implementation of the complementary metal oxide semiconductor (CMOS) device which is working under low power compatibility for the future electronic applications.

Thin film transistors are composed of three components namely, semiconductor channel layer, insulating dielectric layer and three

electrodes. The electrodes are source, drain and gate in which the voltage applied to the gate electrode controls the source-drain current through the semiconductor channel layer. The gate electrode is separated from the source-drain electrode by the dielectric layer and the structure behaves like a capacitor in the metal oxide semiconductor (MOS) structure. Depending on the position of the three electrodes, the TFTs can be classified into two, namely, coplanar (C) and staggered (S) types (figure 2.1). The source and drain electrodes and gate insulator are on the same side of the channel in coplanar configuration. In a staggered configuration, the source and drain electrodes and the insulator are on the opposite side of the channel. The TFTs can be further divided into two depending on the positions of the gate electrode i.e. the TFTs with electrode on the top or bottom of the stack is named as top gate and bottom gate TFTs, respectively.

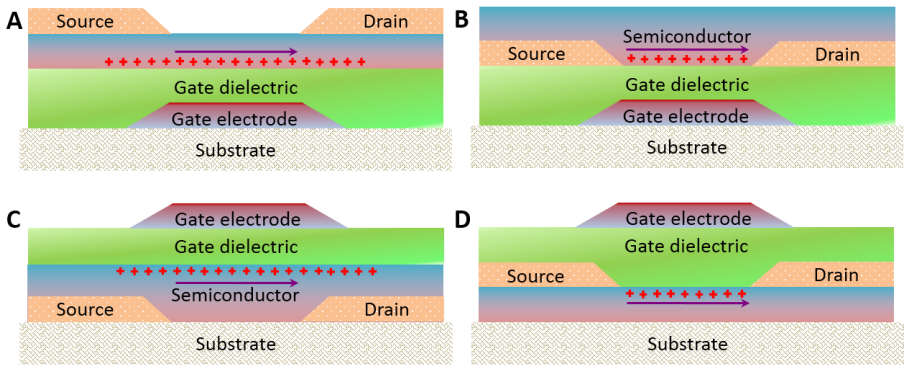

Figure 2.1. Schematic cross-sections of the four principle TFT structures. (A) Bottom gate staggered TFT. (B) Bottom-gate coplanar TFT (C) Top-gate staggered TFT (D) Top-gate coplanar TFT.

Among the above device structures, the selection of suitable TFT structure can be made based on the fabrication processes, materials used and the working conditions of the TFTs [5]. Top-gate (TG) structure can

be used in the case wherein the channel layer needs to be deposited with the high-quality crystal structure. The highly oriented pre-deposited substrates such as Si allows the fabrication of highly oriented channel layer. The TG structure is also preferred when the semiconductor channel layer needs high-temperature annealing processes, as this process may damage other layers in bottom-gate (BG) structure.

The most commonly used TFT structure is BG structure because of the easiness of the fabrication processes. The gate electrode and the insulator were prepared initially before depositing active semiconductor channel layer on top of it. Most of the researchers used commercially available substrates having gate/insulator structure, for example, ITO/ATO and Si/SiO_2 substrates. The advantages of this BG structure is that the researchers can easily optimize the channel properties by depositing channel layer on top of well-defined gate/insulator substrate at various deposition conditions rather than changing the device structure.

Another advantage of this structure is that in some cases the channel layer needs to be annealed at a specific temperature in specific atmospheric gas such as N_2 or air. This structure allows to perform this easily because the channel layer exposed to the atmosphere. Also, by considering display application of TFT the BG structure has a benefit since the bottom gate electrode blocks the backlight. The instability caused by the illumination of TFTs by backlight can be reduced and the performance of display can be improved.

2.1.1 Basic device operations

The basic principle of TFT is similar to a field effect device in which the applied gate voltage modulates the flow of carriers through the

semiconductor. The conduction between the source and drain electrodes on a semiconductor channel layer is controlled by the gate voltage applied to the gate electrode. The parallel plate capacitor structure formed by the metal, semiconductor and oxide dielectric (MOS structure) allows easy control of the flow of electrons (holes) through the channel layer. The modulation of channel conductance is achieved by the accumulation of charge carriers near the semiconductor/insulator interface through the applied gate voltage. The accumulation of electrons or holes will occur depending on whether the channel layer is n-type or p-type [115].

There always existed an ambiguity regarding the difference between MOSFET and TFT, since these two devices have similar characteristics and operations. The important differences between MOSFET and TFT are in the deposition of channel layer and the formation of conducting channel layers. In MOSFET, the semiconductor channel layer is formed on a single crystalline silicon substrate whereas in TFT it is deposited on rigid glass/plastic substrate. The thin films of channel layer in TFTs are realized by various deposition methods even at room temperature. In MOSFET, the semiconductor channel layer formation requires high-temperature processes. In the case of conducting channel layer formation, inversion layer of charges is formed for MOSFET and accumulation layer of charges is formed for TFT by applying suitable gate voltages.

2.1.2 Thin film transistor characterization

The static characteristics of TFT are similar to that of MOSFET which includes the output and transfer characteristics. All the TFT parameters can be evaluated from these measurements. Typically, the transfer characteristics give an overall performance of TFT (figure 2.2).

The output characteristics are obtained by measuring the drain current (I_D) flowing between the drain and source through the channel layer by varying the drain-source voltage (V_{DS}) for fixed gate-source voltage (V_{GS}). There are two regions of operations in the output characteristics namely linear region and saturation region of operation. In linear region of operation, the TFT behaves similarly to a resistor in which the current flowing through the conductive channel is linearly dependent on the V_{DS}. A conductive channel is formed in the semiconductor by the application of V_{GS} and the accumulated charges are uniformly distributed in the channel region. A small current between the source and drain electrode is linearly increased with increasing V_{DS}. This region of operation occurs when $V_{DS} \leq V_{GS} - V_T$, where V_T is called the threshold voltage and current follows the relation as,

$$I_D = \mu_{lin} C_i \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right], \quad \text{for } V_{DS} \leq V_{GS} - V_T \quad (2.1)$$

Where μ_{lin} is the linear field effect mobility, C_i is the capaciatance per unit area of the gate dielectric, and W and L are the width and length of the channel layer.

The second region of operation of TFT is saturation region and occurs when the drain voltage is higher than the gate voltage, ie $V_{DS} \geq V_{GS} - V_T$. When we increase the V_{DS} into a higher value, the voltage drop across the gate dilectric near the drain electrode increases and it effectively reduces the field across the dielectric. So the thickness of accumulation layer near the drain electrode becomes narrow and a small conductive path exists near this elecrtode. So the current flowing through the channel region between drain and source electrode is reduced and the current flow becomes independent of V_{GS} voltages. The depletion of charge carriers near

the drain electrode is termed as the pinch off condition and after this pinch off, a constant current flows through the channel layer [116]. This mode of operation of TFT is modeled using the following relation (2.2),

$$I_D = \frac{1}{2}\mu_{sat} C_i \frac{W}{L}(V_{GS} - V_T)^2 , \quad \text{for } V_{DS} \geq V_{GS} - V_T \qquad (2.2)$$

where μ_{sat} is the saturation mobility.

There are two possible modes of operations in TFTs, depletion mode and enhancement mode of operations. In depletion mode of operations, a small drain current flows through the channel layer even at zero V_{GS} voltage. i.e., in depletion mode TFT, the channel layer has a higher carrier concentration and hence there exists a conductive path even in V_{GS}=0 V. This mode of operation is used in the sensor applications of TFTs. But in the case of enhancement mode TFT, negligible drain current flows at V_{GS}=0 V and this TFT is termed as normally-off device. The channel layer with lower carrier concentration helps in realizing these possibilities of TFTs and such TFTs are widely used in the normal display units and circuits.

The transfer characteristics measured in linear and saturation region depending upon the V_{DS} voltage will give the respective values of the parameters of the TFT. The most common parameters to gauge the performance of a TFT are threshold voltage (V_T), on-off ratio ($I_{on/off}$), mobility (μ) and sub-threshold swing (SS).

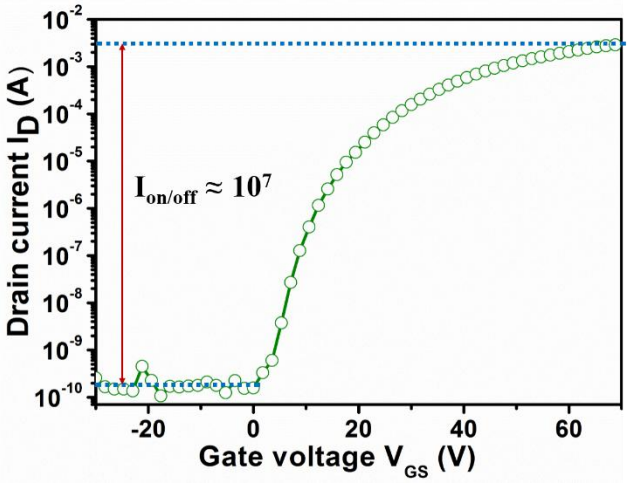

Figure 2.2. Typical transfer characteristics of an n-channel TFT.

Threshold Voltage: The threshold voltage is defined as the minimum gate voltage required to accumulate charge carriers in the channel layer between the source-drain electrodes. Depending on the threshold voltage values, it can be distinguished whether the TFT follows enhancement mode or depletion mode [117]. More clearly, for the n-type channel layer, the enhancement mode TFT has positive V_T whereas depletion mode TFT has negative V_T. The value of V_T can be extracted from the $I_D^{1/2}$ vs V_{GS} characteristics by extrapolating the linear region of operation and V_T can be measured from the x-intercept as shown in figure 2.3.

On-off ratio: $I_{on/off}$ is defined as the ratio of the maximum drain current to the minimum drain current and this value can be found from the transfer characteristics plotted in logarithmic scale (Figure 2.2). The minimum current or off current depends on the noise level of measuring instruments and leakage current through the dielectric of TFT. The off current should be minimized to get a low power dissipation during the practical

applications of TFT in circuits [118]. Actually, the ideality of the switching characteristics of TFT is represented by the $I_{on/off}$ ratio value.

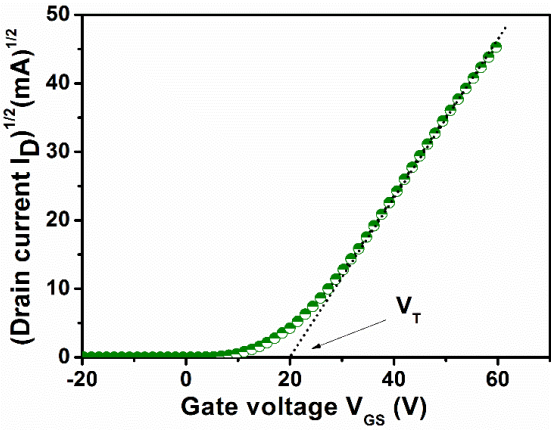

Figure 2.3. Determination of threshold voltage and saturation mobility from the saturation region of device operation.

Mobility: The mobility is an important parameter of TFT and it reflects the efficiency of charge transport in semiconductor channel layer. The value of mobility must be higher for the practical application of TFT and it depends on the various properties and scattering mechanism present in the channel layer due to impurity, surface roughness and other defects inside the channel layers. Two kinds of mobility values can be extracted from the transfer characteristics depending on the V_{DS} values, linear field effect mobility (μ_{lin}: for small V_{DS}) and saturation field effect mobility (μ_{sat}: for higher V_{DS}). The value of μ_{lin} can be extracted from the slope calculated in the linear region of V_{DS}-I_D curve by following the equation (2.3),

$$\mu_{lin} = \frac{slope}{C_i(W/L)V_{DS}} \tag{2.3}$$

The value of μ_{sat} can be extracted from the slope calculated in the linear region of V_{DS}-$I_D^{1/2}$ curve by following equation (2.4),

$$\mu_{sat} = \frac{slope^2}{1/2C_i(W/L)} \quad (2.4)$$

Sub-threshold swing: The SS value can be measured from the inverse of the maximum slope in the sub-threshold region of the transfer characteristics (Figure 2.4) and it is given by,

$$SS = \left(\frac{dlog(I_D)}{dV_{GS}}\right)^{-1} \quad (2.5)$$

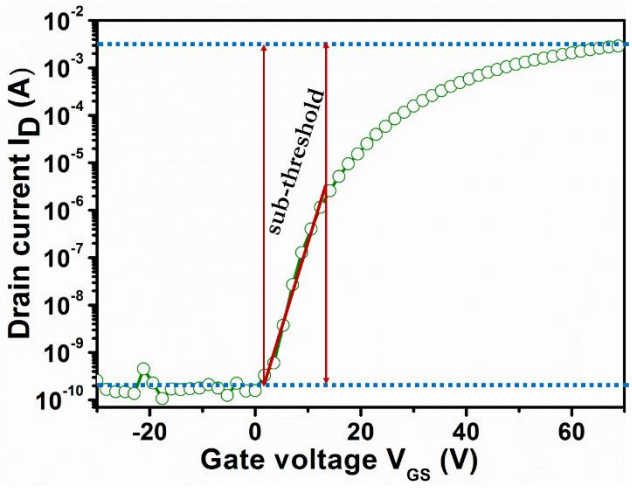

Figure 2.4. $\log(I_D) - V_{GS}$ characteristics for sub-threshold slope analysis.

SS value represents the effectiveness of gate voltage to increase the drain current by one decade. Small value of SS (generally 0.1 to 0.5 V/decade) is desirable and it represents a very sharp transition from off to on state. This SS value highly depends on the tail states present in the bandgap of the semiconductor channel layer [119]. In the present work, electrical characterizations of the TFTs were performed using Keithley 4200 semiconductor characterization system.

2.2 Calculation of the trap density of states in the band gap of semiconductors

2.2.1 Crystalline nature of solids

In a crystal all the atoms are arranged in a pattern that repeats periodically in three dimensions to an infinite extent. The periodic nature of crystalline solids leads to perfect electronic structure of the material. The density of electronic states takes the form of alternating energy region called bands separated by bandgap. The band represents the large densities of electronic states and no such states are allowed in the bandgap. The well-defined structures in the valence and conduction bands are the main features of the crystalline semiconductors. The energy distributions of the density of electronic states have the sudden ends at the valence band maximum and the conduction band minimum.

Both long range and short range order empowers the perfect band structure of the crystalline solids. Even though crystalline solids are characterized by long range periodic order they contain defects such as vacancies, interstitials and dislocations.

2.2.2 Amorphous nature of solids

The structure of amorphous semiconductors is defined by three principle features - the short range order, the long range disorder and the coordination defects. Amorphous and crystalline phases of the same material have comparable band gaps because of the similarity of the covalent bonds in crystalline and amorphous solids. The overall electronic structure of amorphous material compared to equivalent crystal arises from

the preservation of the short range order. Although amorphous solids have short range order, a long range structural disorder is predominant in these materials [120].

The deviation from the perfect structure of bands in amorphous solid arises from the change in the bond length and bond angles of solid. Such disorder causes electron and hole localization and scattering of carriers. The abrupt band edges of crystal are observed to transform as broadened tail states and extend to forbidden bandgap which arises from the long range structural disorder. The broadened band tail states have significant effect on the electronic transport because electronic transport takes place in the band edge [121].

Electronic states called deep states which lie in the bandgap arises from the defects in the solids called coordination defects. Deep states are the consequence of broken bonds in the amorphous solid which play a significant role in tuning or modifying many properties of an amorphous solid by trapping and recombination. The densities of these localized tail and deep states in amorphous solids have profound effect on the electronic transport mechanism [122].

Charge transport in amorphous silicon transistors has been studied from the temperature dependent transistor characteristics. In amorphous semiconductors, localized states induced by defects or impurities are distributed in the band gap. Study of those distributions of localized states in the band gap leads to exploration of charge transport mechanism in the semiconductor. Considering that the subgap DOS strongly affects the electrical properties in the thin film transistors with disordered materials, the knowledge about the charge transport mechanism and subgap DOS is essential not only for the fundamental understanding of the device

operation but also for improving the device performances. Many reports suggesting different analytical methods to estimate the distribution of the trap density of states are prevalent, hence we have adopted one such method to establish the exponential distribution of density of states observed in the thin film transistors developed in the present work.

The localized states in amorphous materials, for example amorphous silicon that limits electronic transport can be divided into two types, tail states and deep states as shown in figure 2.5. The tail states exist just below the band edges and they are formed by the broadening of bands of amorphous silicon [123].

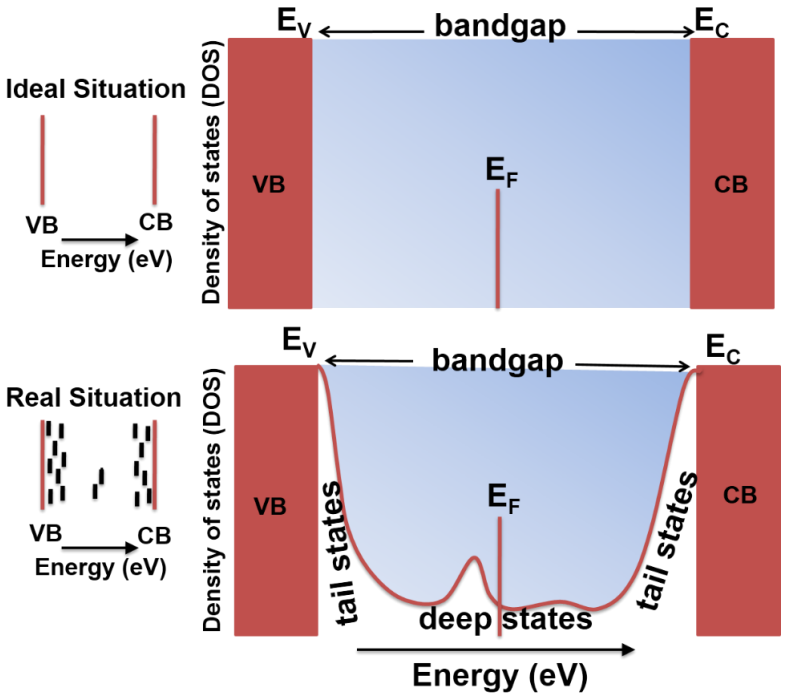

Figure 2.5. The band structure of crystalline and amorphous semiconductors.

The Fermi level can be easily shifted through the exponential distribution of the localized states by applying gate voltage so that thin film transistors can serve as useful tools for the study of DOS. These tail states determine the conduction above threshold voltage and hence the field-effect mobility. The deep states actually arise from the defect in amorphous silicon and which decide the threshold voltage of TFT [124]. Density and nature of those localized states determine the transition from below to above threshold conduction and rate of transition can be associated to the activation energy. In short, by applying the gate voltage, the Fermi level in the accumulation region moves from the deep to tail states in the energy bandgap. The movement of Fermi level, and hence the rate of change of activation energy, with gate voltage provides a clear idea about the localized trap density in the bandgap of semiconductor [125].

2.2.3 Analytical description of an ideal field effect transistor

The density of localized states in the band gap of amorphous solid was determined from the measurements of the temperature and gate-voltage dependence on the field-effect conductivity of the thin film transistor. The fundamental principles of device physics can be used for the easy determination of subgap DOS [123].

As an initial step towards the DOS estimation, electrical characterization of TFT such as output characteristics and transfer characteristics are measured by varying the temperature. Different parameters such as threshold voltage, field effect mobility, saturation mobility and sub-threshold voltage swing are then derived from these characteristics.

The following figure 2.6 illustrates the basic operation of the TFT by plotting density of states of the electronic sates. The amount of band bending and the occupancy of electronic states can be controlled by varying the applied gate voltage.

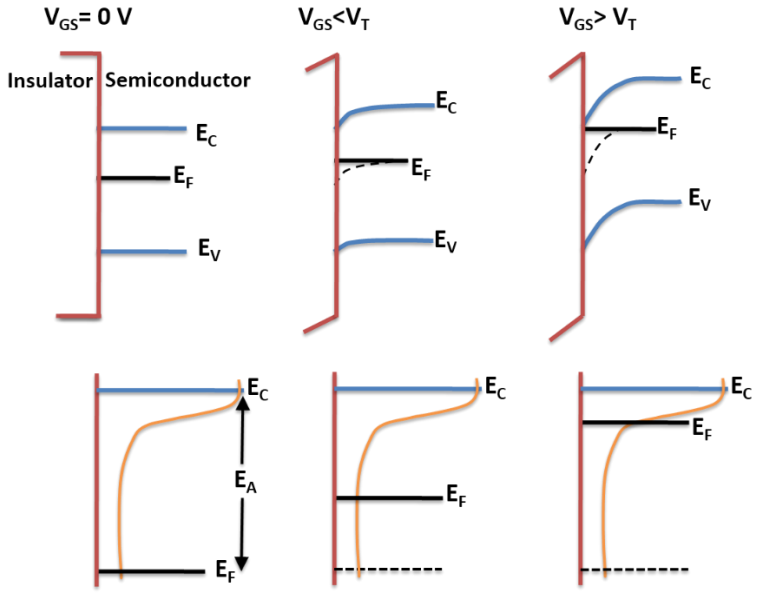

Figure 2.6. Schematic representation of operation of TFT showing energy band bending (top) and the distribution of localized states.

At zero gate voltage, the bands have no bending i.e., in flat band condition. When a non-zero gate voltage, less than the threshold voltage is applied, downward band bending occurs. Small gate voltage enables Fermi level movement through the deep states and the occupancy of deep states. On increasing the voltage, the band bending increases slightly and the space charge in the deep states increases which results in exponential current increase in the pre-threshold region. Further increasing the gate voltage,

above threshold voltage, the space charge in the tail states increases linearly with the gate voltage and the device exhibit well defined thermally activated field effect mobility [126].

2.2.4 Calculation of density of states

The equations which represents the drain current in linear and saturation region of TFTs are valid for devices with a low trap density and insignificant contact resistances. The trapping and releasing times of carries in traps are expected to be much shorter than the time needed to measure a transistor characteristic [127]. But in reality, the high density of traps has made deviations in the characteristics and in order to use the basic equations following assumptions are made [128].

1) The semiconductor is homogenous perpendicular to the insulator-semiconductor interface and hence the charge density is homogenous along the transistor channel
2) Insulator surface states only contribute to a non-zero flat band voltage
3) The Fermi function for the trapped carriers is approximated by a step function

The calculated trap DOS from the measured data can have a significant effect on the assumptions. The incorrect simplification may lead to ambiguous output and which results in underestimation of density of trap states.

The drain current in the linear regime may be written as

$$I_D = \frac{W}{L}\sigma V_{DS} \tag{2.6}$$

and the field-effect conductivity is

$$\sigma = \mu C_i (V_{GS} - V_{FB}) \tag{2.7}$$

V_{FB} is the flatband voltage and μ is the gate-voltage dependent field-effect mobility. The field-effect conductivity can be calculated from:

$$\sigma(V_{GS}) = \frac{L}{W}\frac{I_D}{V_{DS}} \quad (2.8)$$

In order to study the distribution of the trap states, we have examined the temperature dependent transfer characteristics of transistors in the temperature range between 300 K and 360 K (Figure 2.7). Similar works reported on amorphous oxide materials have the temperatures within this range [129]. The range of temperature, 310 K to 360 K, for evaluating the activation energy is reasonable because the observed activation energy value lies around 0.4 eV. A thermally activated Arrhenius like behavior was observed where the drain currents increased with increase in temperature. The current follows the relation,

$$\sigma(V_{GS}) = A\ exp\left(-\frac{E_A}{kT}\right) \quad (2.9)$$

where, σ is the conductivity of the channel, E_A is the activation energy, k is the Boltzmann constant and A *is* a constant.

The observed positive shift of transfer characteristics with increasing temperature was due to the releasing of trapped carriers from the defect induced traps. The value of E_A, which is the energy difference between the Fermi level and the transport band edge, can be found for each gate voltage. Arrhenius plot for each gate voltage drawn between ln(I_D) and 1000/T enables the determination of activation energy. The equation connecting E_A and I_D is,

$$\ln I_D = \ln A - E_A/kT \quad (2.10)$$

The slope of Arrhenius plot gives the value of E_A for each gate voltage and it can be plotted as a function of gate voltage as shown in figure 2.8. In multiple trapping and thermal release model (MTR), E_A is defined

as the energy required to release a trapped carrier from the trap inside the semiconductor to the conduction band. By this model the density of defect induced traps can be found from the derivative of the activation energy with respect to gate voltage. A slow variation of E_A with gate voltage indicates a large value of DOS whereas a fast change indicates a low value of DOS in the bandgap region of the channel material of the TFT [125].

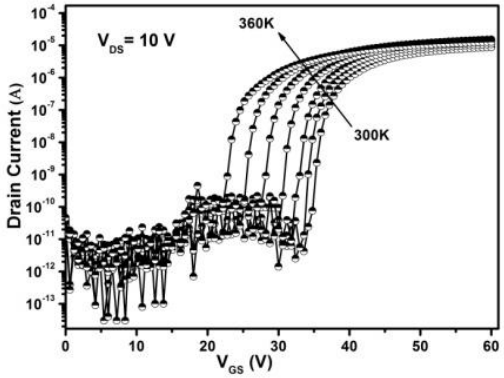

Figure 2.7. Transfer characteristics of organic PTCDI-C8 n-type TFTs measured at different temperatures.

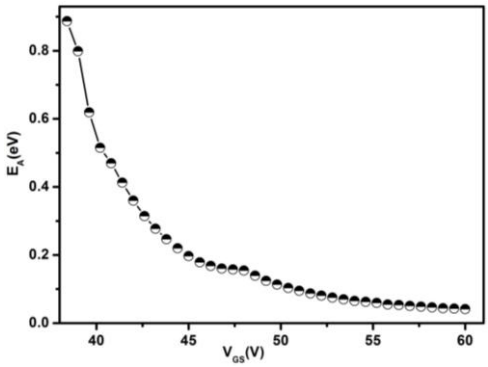

Figure 2.8. Dependence of E_A with gate voltage of organic PTCDI-C8 n-type TFTs.

An exponential decay of E_A with gate voltage was observed which indicates a low value of DOS. The DOS inside the bandgap of active layer can be written as [122],

$$N(E) = \frac{C_i}{q} \frac{1}{t\frac{dE_A}{dV_{GS}}} \quad (2.11)$$

Where E is the energy measured from the band edge, C_i the insulator per unit area, q the elementary charge and t is the channel thickness. This method has been extensively used in the case of amorphous silicon thin film transistors for the evaluation of DOS. This approach is also expected to be applicable in the case of TFTs with novel amorphous, polycrystalline and organic semiconductors having large number of trap states. In figure 2.9, it can be shown that the density of states in the bandgap of channel layer calculated from the derivative of the activation energy varied exponentially.

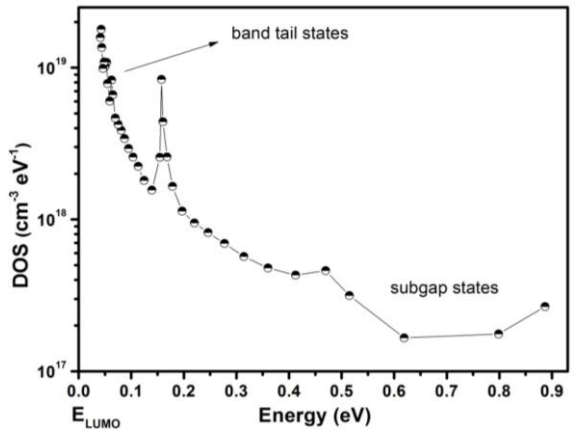

Figure 2.9. Density of states in the bandgap of organic PTCDI-C8 channel layer calculated from the derivative of the activation energy.

The estimation of subgap DOS is very important and essential since they strongly affect the electrical properties of TFTs. A thorough knowledge about the origin and density of these subgap levels is therefore imperative in order to put into action the preventative measures both during fabrication and operation of the device, to achieve an improved performance.

2.3 CMOS Inverter

Complementary metal oxide semiconductor (CMOS) architecture is the most elementary building block in many integrated circuits. The CMOS device is designed by using high performance n and p-type channel thin film transistors. The CMOS technology is very important because it delivers circuits with more complex functionality for emerging transparent flexible electronics. The low power consumption, low waste heat generation and efficient noise control of CMOS devices are the advantages over the existing technology and the development of high performance CMOS devices will bring a new technological revolution in the future electronic applications [130,131].

Inverter is the nucleus of the digital design and the inverter is used to reverse the input signal, ie, a low voltage in the input becomes a high voltage in the output and vice versa. In digital electronics, low voltage is termed as binary 0 and high voltage as binary 1. The CMOS inverter is actually a NOT gate and it consists of a n and p-type TFT and the drains of TFTs are connected in series with common gate electrode. Although the NOT gate function can be achieved by using NMOS (n-type metal oxide semiconductor) devices, CMOS inverter devices are superior to NMOS

because of the lower power dissipation and higher logic switching performance.

The lack of high performance p-type oxide TFT as compared to n-type TFT has hampered the fabrication of oxide based CMOS inverter. The research community has attained tremendous achievements to give a breakthrough in the development of novel oxide CMOS inverter (Table 2.1). They have constantly tried to improve the performance of CMOS inverter by choosing different novel p and n-type TFTs and geometries. SnO and Cu_xO are the most studied p-type materials and many n-type materials such as IGZO, ZnO and SnO_2 are tried for the fabrication of oxide based CMOS inverters.

Table 2.1. Summary of oxide based CMOS inverters fabricated using different p and n-type oxide materials

Channel		**Mobility (cm^2 /Vs)**		**Gain**	**Substrate**	**Method**	**Year**	**Ref**
n	p	n	p					
GIZO	Cu_2O	1.58	2.2×10^{-3}	120	PES	RFMS	2011	[132]
SnO_x	SnO_x	-	0.011	2.8	Si/SiO_2	TE	2008	[133]
In_2O_3	SnO_x	0.054	0.0047	11	Si/SiO_2	TE	2008	[134]
SnO	SnO	0.0011	0.78	2.4	Si/SiO_2	PLD	2011	[135]
GIZO	SnO	23	1.3	4.5	Paper/paper	RFMS	2011	[136]
SnO_2	SnO	0.52	0.42	3	Si/Al_2O_3	DCMS	2014	[137]
SnO_2	SnO	0.23	2.39	4	Glass/ATO	DCMS	2015	[138]
ZnO	SnO	1.6	0.06	12	ITO/HfO_2	RFMS	2016	[139]
GIZO	SnO	11.9	0.59	24	Si/SiO_2	RFMS	2017	[140]
GIZO	SnO	10.05	1.19	112	Si/SiO_2	RFMS	2018	[141]
ZTO	Cu_2O	6.4×10^{-1}	1.3×10^{-4}	4.2	Si/SiO_2	RFMS	2018	*

RFMS = radio frequency magnetron sputtering, TE= thermal evaporation, PLD = Pulsed laser deposition, DCMS = direct current magnetron sputtering, * = present work by author.

The structure and schematic circuit diagram of CMOS inverter having p-type Cu_2O TFT and n-type ZTO TFT are shown in figure 2.10. The input voltage is given through the common gate electrode (V_{IN}) and the inverted output of the device can be taken from the common drain electrode (V_{OUT}).

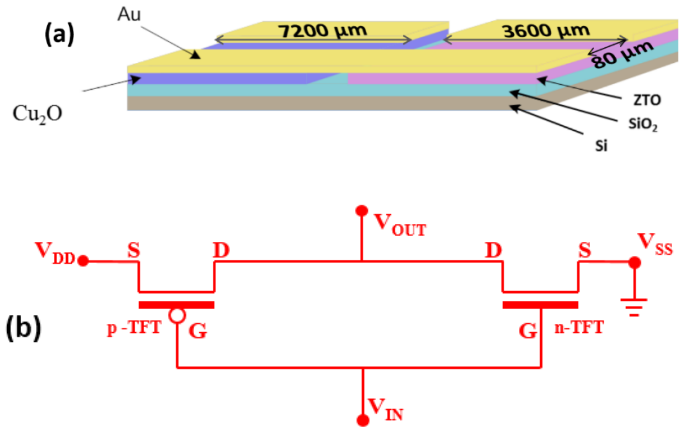

Figure 2.10. Typical structure (a) and schematic circuit diagram (b) of a complementary metal-oxide semiconductor (CMOS) inverter.

The voltage transfer characteristics (VTC) is the plot of the voltage measured at output electrode (V_{OUT}) and the applied voltage given to the input electrode (V_{IN}). From VTC (figure 2.1), the inverter parameters such as gain and noise margins can be measured [142].

Gain: The gain represents the quality of CMOS inverter and it can be measured from the negative slope of the VTC curve.

$$Gain = \frac{d\,V_{OUT}}{dV_{IN}} \tag{2.12}$$

Noise margin (NM): This important parameter determines the allowable noise voltage on the input side so that the output voltage will not be affected. The NM represents amount of noise value that can be tolerated by a digital circuit and it is an optimum value for a digital circuit to differentiate the appropriate signal from 0 or 1. The NM value of CMOS inverter can be found from the unit gain positions of VTC curve. In figure 2.11 the voltages V_{OH}, V_{OL}, V_{IH} and V_{IL} represent the corresponding coordinates of the unit gain positions in the VTC curve.

Two NM can be defined, high NM (N_{MH}) and low NM (N_{ML}). The N_{MH} is defined as the difference in magnitude between the minimum HIGH output voltage and the minimum input HIGH voltage.

$$N_{MH} = V_{OH}-V_{IH} \tag{2.13}$$

Where V_{OH} = minimum HIGH output voltage and V_{IH} = minimum HIGH input voltage.

The low NM can be defined as the difference in magnitude between the maximum LOW input voltage and the maximum output LOW voltage.

$$N_{ML}= V_{IL}-V_{OL} \tag{2.14}$$

Where V_{IL}= maximum LOW input voltage and V_{OL}= maximum LOW output voltage.

Generally, for high gain CMOS inverter it should have V_{IH} =V_{IL} so that the inverter can be switched abruptly in the transition region.

The basic operations of CMOS inverter can be divided into five regimes (a to e as shown in Figure 2.11) in the VTC curve which outlines

the various regions of operations for n and p transistors. Let V_{TN} and V_{TP} are the threshold voltages of n and p-type TFTs, respectively.

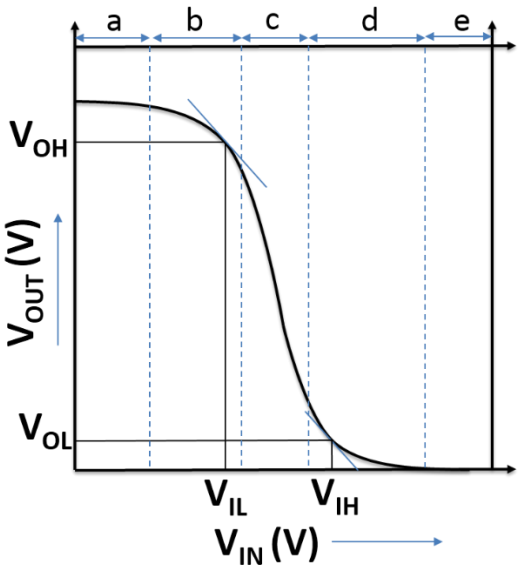

Figure 2.11. Typical VTC curve of a CMOS inverter during operation and noise margins extraction and different operation regimes of CMOS inverter.

In **region a** ($0 \leq V_{IN} \leq V_{TN}$), the n-TFT is in cut off region and the p-TFT is in linear region so that the output voltage is equal to the supply voltage $V_{OUT} = V_{DD}$. The positive increase of V_{IN} would forward the operation into the **region b** ($V_{TN} \leq V_{IN} \leq V_{DD/2}$) in which the n-TFT is in saturation and p-TFT is still in linear region of operation. The current, I_{DD}, through both TFTs have the same value; therefore, turning on the n-TFT causes a drop in the output voltage. The following relation can represent the output voltage:

$$V_{OUT} = (V_{IN} - V_{TP}) + \left[(V_{IN} - V_{DD} - V_{TP})^2 - \frac{g_{mn}}{g_{mp}}(V_{IN} - V_{TN})^2\right]^{1/2} \quad (2.15)$$

Where, g_{mn} and g_{mp} are the transconductance of the n and p-TFTs.

In this regime, the current starts to flow through the n channel TFTs and it flows from V_{DD} to V_{SS} through both TFTs. Further increase of V_{IN} will tend to operate p-TFT into saturation region so that a maximum current will flow through both the TFTs. i.e., the **region c** is characterized by the saturation operations of both n and p-TFTs and it happens near a voltage $V_{IN}= V_{DD}/2$. In this region, I_{DD} and hence the inverter gain has a maximum value.

Eventually, when the V_{IN} value increases beyond this $V_{DD}/2$ value leads n-TFT enters into the linear region. The working of the inverter in the **region d** ($V_{DD}/2 < V_{IN} \leq V_{DD} - V_{TP}$) is similar as region b with the operation region of both TFTs being reversed. i.e in this region of operation, the n-TFT is in linear region and p-TFT is in saturation mode of operations. Further increase of V_{IN} ($V_{IN} \geq V_{DD}-V_{TP}$) beyond threshold voltage value V_{TP} the inverter works in the **region e**, ie, the p-TFT enters into the cut off region but n-TFT remains still in the linear region. The ideal output of inverter in this region is zero.

The region c is very important because the sharp steep of this region defines the gain of the inverter. The transition from the zero and one and vice versa is characterized by this region and this transition has to be very fast. Actually, a large current flows through the inverter during this region of operation only. The power dissipation during other regions of operations is very small because negligible current flows through the TFTs. The CMOS inverter dissipates power only during the switching period so that

the overall heat dissipation and power loss is very minimum as compared to other switching circuits based on NMOS [143].

2.4 Conclusions

The working principles of thin film transistors and extraction of various performance parameters of TFTs are briefly explained in this chapter. The basic device physics for the calculation of DOS inside the channel layer from the temperature dependent transfer characteristics are discussed in detail. Also the design and working of CMOS inverter is described in brief and method of finding the device parameters from the characteristics are discussed.

Chapter 3

Fabrication of organic thin film transistors and investigation of density of states in the bandgap of active layer

3.1. Introduction

Over the past two decades, impressive improvements have been made in organic thin film transistor (OTFT) [144–146] by synthesizing new high-performance organic semiconductors and optimizing the device fabrication conditions [147,148]. The electrical performance of best OTFT fabricated by vacuum evaporation of small molecules is comparable with those of amorphous silicon thin film transistors and as a result there is a greater industrial interest in using OTFTs [149]. The organic semiconductors are one of the active research areas because of their possible applications in low-cost, large area, and flexible devices [52,150,151]. At present, p-type organic semiconductors, such as

pentacene and oligothiophenes derivatives, are the most popular materials used in organic electronics [152].

The n-type organic semiconductors show poor performance on considering the charge carrier mobility [153–155]. The fabrication of high performance novel n-type materials can lead to new era in organic electronics because it enables the realization of complementary logic circuits, p-n junctions, and solar cells [149]. Many n-channel organic semiconductor materials have been synthesized, including metal-phthalocyanine [155] C60 [156,157], oligothiophene [158,159], naphthalene [160,161] and perylene [162,163]. Small-molecule perylene diimides are most promising n-type organic semiconductors for making OTFTs because their electrical properties can be modified by attaching different functional groups [164]. The n-channel device instability and degradation in air are the main problem of n-type OTFTs. The multiple and thermal release model (MTR) refer to the charge transport mechanism in small molecules and it describes the generation of charge carriers from the localised states created by traps. Hence, the electrical performance and nature of degradation of OTFTs have mainly related to the density of localized states (DOS).

In this chapter, the electrical characteristics and degradation study of n-type OTFTs using N, N'-Dioctyl-3,4,9,10-perylenedicarboximide (PTCDI-C8) as channel layer is described in part I. The high degree of molecular packing in the PTCDI-C8 thin films leads to high performance organic semiconductor devices [165]. In part II, fabrication and characterization of p-type pentacene OTFTs are described along with the investigation of DOS of channel layer.

3.2. Part I: Degradation study and calculation of density of states in n-type PTCDI-C8 TFT channel layer

3.2.1. Experimental details

The n-type OTFT for the present study was fabricated in the inverted-staggered (top contact) structure. A heavily doped n-Si (100) wafer was used as the gate electrode and thermally grown silicon dioxide (SiO_2) having thickness of 108 nm served as gate dielectric. The PTCDI-C8 layer was deposited using vacuum thermal evaporation system maintained at a base pressure of 10^{-6} mbar and having a substrate temperature of 120 $^{\circ}$C. The active layer thickness of 50 nm at a deposition rate of 0.3 Å /s was measured using a quartz crystal oscillator thickness monitor. PTCDI-C8 was evaporated through the metallic shadow mask in order to get isolated devices. The gold drain and source contacts were deposited by thermal evaporation through shadow masks that define a channel length (L) and width (W) as 80 µm and 2000 µm, respectively. The electrical measurements were carried out using Agilent 4156 C semiconductor parameter analyzer under vacuum (10^{-1} mbar) in the absence of light, immediately after the fabrication of the devices. The degradation of the devices on exposure to air was investigated by characterizing the devices after exposure to air for 2 h. During the electrical characterization, the device temperature was varied from 300 K to 360 K in steps of 10 K by means of an MMR Technologies controller (model K-20). The electrical measurements of the OTFTs were performed after stabilizing the temperature at each set value.

3.2.2. Results and discussion

Figure 3.1(a) shows the output characteristics of the fabricated PTCDI-C8 OTFTs, which exhibit expected electrical characteristics of n-channel field effect transistors. The V_{DS} is varied from 0 to 60 V and the I_D is measured for different gate voltages varied from 0 to 32 V. Figure 3.1(b) shows I_D on log scale versus V_{GS} and $I_D^{1/2}$ versus V_{GS} plot at fixed V_{DS} = 10 V (transfer characteristics). The fabricated device exhibited good n-type characteristics. Using Equations. (2.1) and (2.3), the device parameters of the PTCDI-C8 TFT have been extracted, resulting in a saturation field effect mobility of 0.02 $cm^2V^{-1}s^{-1}$, threshold voltage of 25.3 V, sub-threshold swing of 0.73 V/dec, and an on/off ratio of 6.5×10^5.

Considering that the sub gap states in the active layer strongly affects the electrical properties of the OTFTs, the knowledge about sub gap states is essential for improving device performances [125]. In order to get more information about the electronic properties of the PTCDI-C8 active layer, the transfer characteristics of the OTFT were measured over the temperature range 300 K– 360 K (figure 3.2).

The increase in measured drain currents with temperatures shows a thermally activated Arrhenius like behaviour. At constant V_{DS}, the drain current and the conductivity of the accumulation channel are related by the following equation [166].

$$I_D = V_{DS} t \frac{W}{L} \sigma \qquad (3.1)$$

where t is the thickness of the accumulation channel.

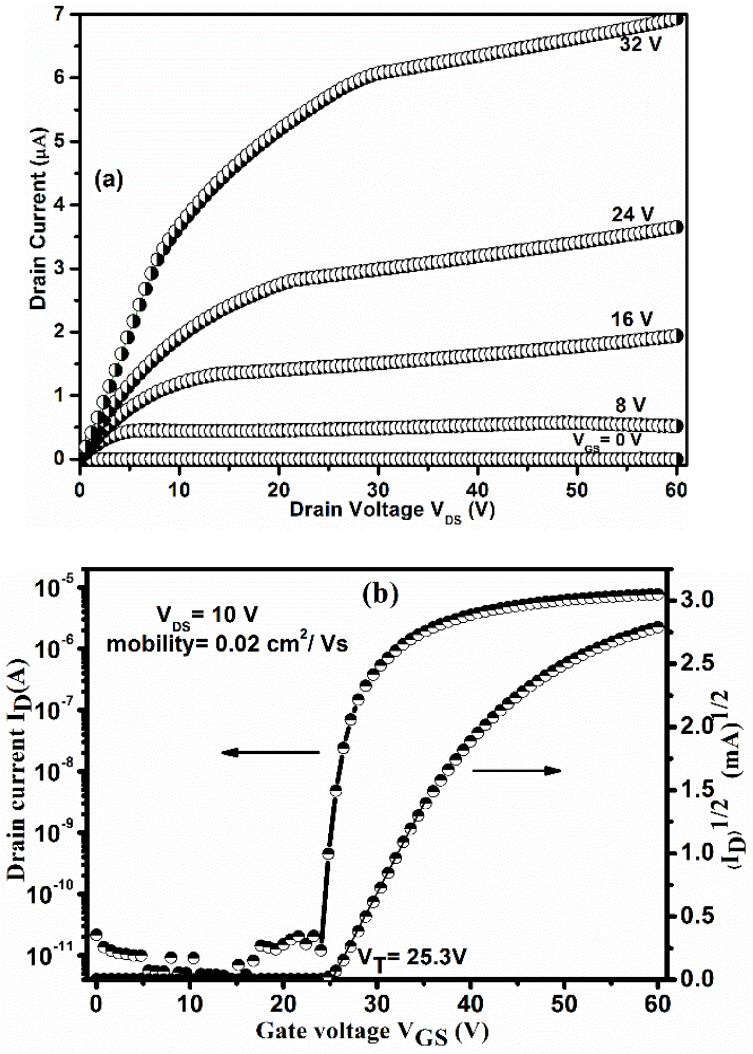

Figure. 3.1. (a) The output characteristics of PTCDI-C8 TFT and (b) the transfer curve of PTCDI-C8 TFT.

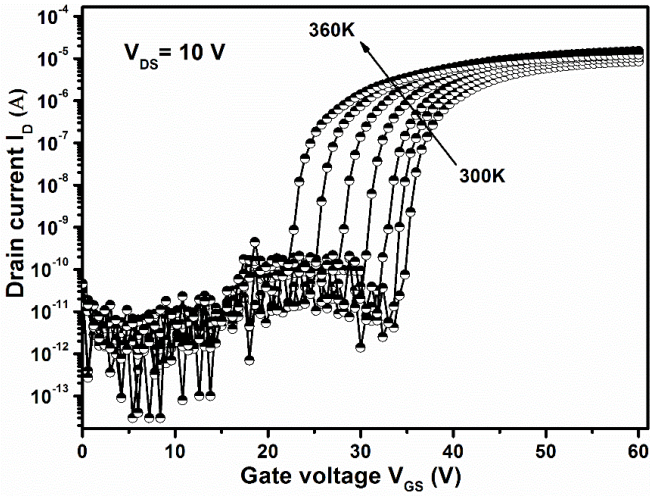

Figure. 3.2. The transfer characteristics of OTFTs measured at different temperatures.

The plot of drain current as a function of the reciprocal temperature (Arrhenius plot) for different gate voltages is shown in figure 3.3 (a). The current follows the relation

$$\sigma = \sigma_0 \exp(-E_A/kT) \qquad (3.2)$$

Where k is the Boltzmann constant. The slope of the Arrhenius plot gives the activation energy (E_A) for different gate voltage V_{GS}.

The Fermi level position in the channel material can be described by the activation energy. In the semiconductor theory, E_A indicates the energy difference between Fermi level position and the transport band edge (here, Lowest Unoccupied Molecular Orbital/LUMO level). Figure 3.3 (b) shows the variation of E_A with gate bias voltage.

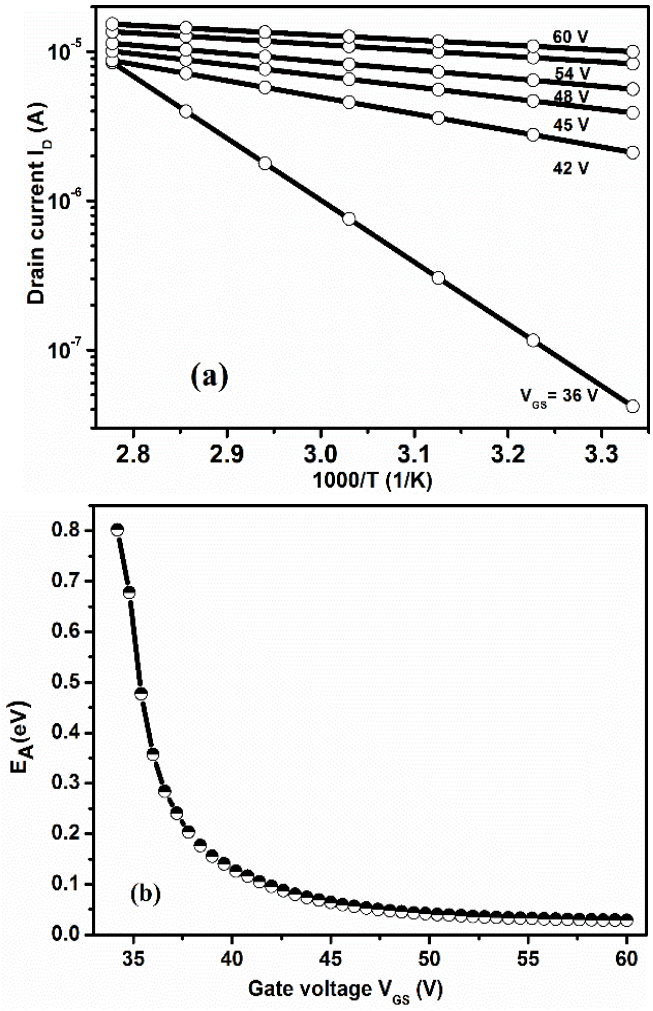

Figure. 3.3. (a) The Arrhenius plot of the drain current for different gate voltages and (b) the variation of E_A with the gate voltage.

The exponential decrease in the activation energy with gate voltage indicated that Fermi level moved toward the band edge very quickly. In the multiple and thermal release model (MTR), the energy required for thermal

release of trapped carriers is interpreted as the activation energy [167]. It means that the low density of localised states that have to be filled by the trapped carriers leads to the fast variation of E_A with gate voltage. At low V_{GS}, the activation energy has relatively very high value (0.8 eV) which indicates that the Fermi level was situated far from the LUMO level and it enters in deeper states. As the V_{GS} increases, Fermi level moves toward the LUMO level, hence the E_A value (57 meV) decreases very drastically. Also, the slow variation of E_A for higher gate voltages revealed that the Fermi level position was not changed smoothly. It means that the density of localized states near the LUMO level (band edge) was higher. So the DOS could be connected to the derivative of the activation energy with respect to gate bias [125,168].

$$N(E) = \frac{C_i}{q} \frac{1}{t\frac{dE_A}{dV_G}} \tag{3.3}$$

where E is the energy measured from the LUMO level, C_i the capacitance of the insulator per unit area, and q the elementary charge.

In order to calculate the DOS, equation (3.3) has been applied to the data shown in figure 3(b). The DOS exponentially increases up to 10^{21} cm^{-3} close to the LUMO level (figure 3.4) and decreases to 10^{18} cm^{-3} in the midgap. Puigdollers et al [169] also reported similar DOS measurements of PTCDI- $C_{13}H_{27}$ active layers and the value was around 10^{18} cm^{-3}. However, there is no report on DOS of PTCDI-C8. The large amount of subgap DOS related to the relatively small field effect mobility extracted in fabricated OTFTs. The exponential region of the DOS can be assumed as band tail of localised states induced by structural disorder [170]. The

deep/subgap states far from the band edge also contribute for the DOS distribution of the semiconductor material.

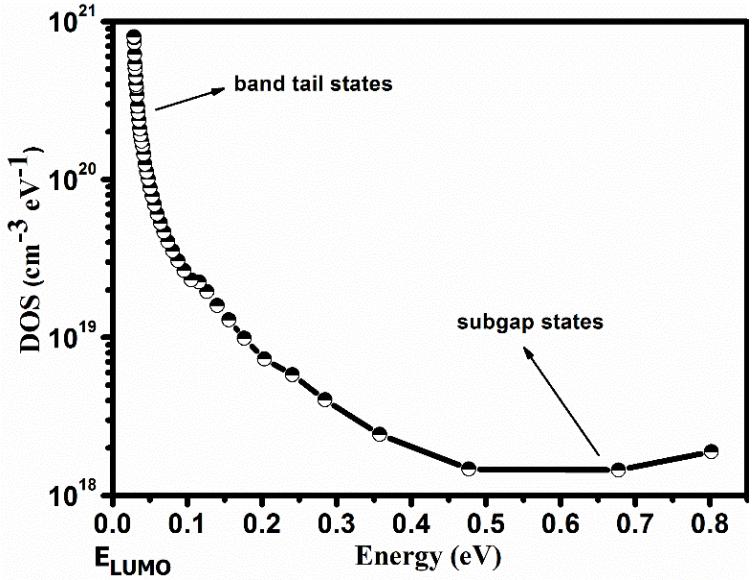

Figure. 3.4. Density of states in the band gap of PTCDI-C8 calculated from the derivative of the activation energy.

The fabricated OTFTs were exposed to air for 2 h in order to study the stability and degradation of the devices on exposure to ambient conditions. After 2 hour, the transfer characteristics (figure 3.5(a)) of the degraded devices measured in air show a reduction in the on current compared with freshly prepared devices (non-degraded devices).

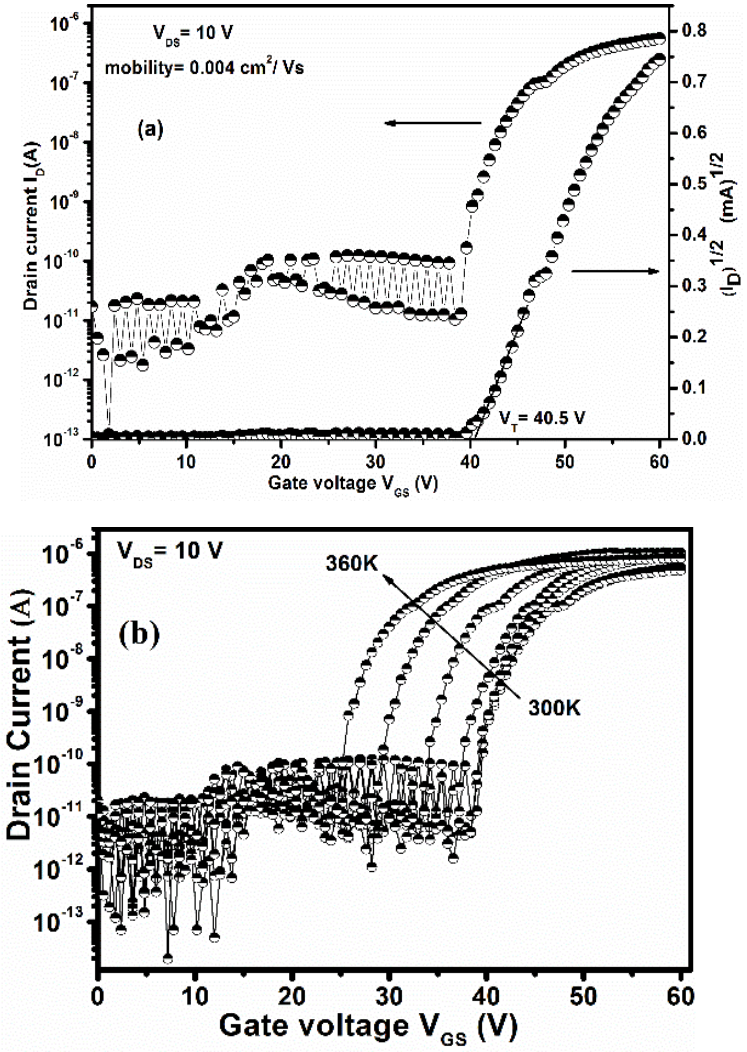

Figure. 3.5. (a) The transfer curve of PTCDI-C8 TFT after exposure in air for 2 h and (b) the transfer characteristics were measured at different temperatures during heating after the air exposure.

The extracted field effect mobility decreases from 0.02 to 0.004 cm^2 $V^{-1}s^{-1}$ and threshold voltage increases from 25.3 V to 40.5 V. The change

in the value of these parameters was due to the trapping of majority charge carriers (i.e., electrons) by adsorbed oxygen in the PTCDI-C8 layer. Upon exposure to air, the oxygen can be easily adsorbed in the organic semiconductor active layer which leads to the degradation of OTFTs. The electrical charge transport is strongly affected by the oxygen traps because they act as localised states in the semiconductor material [171]. The transfer characteristics in the same temperature range (300 K– 360 K) were measured to study the nature of localised states created by the oxygen (figure 3.5(b)). The drain current was decreased by one order of magnitude (10^{-5} A -10^{-6} A) because of degradation of OTFTs when exposed to air.

The activation energy (E_A) was calculated for various gate bias (figure 3.6(a)). Then the DOS was estimated from the derivative of the activation energy with respect to gate voltages (figure 3.6(b)). The inset graph of figure 3.6(b) shows the Arrhenius plot (I_D vs 1000/T) for different gate voltages for degraded device. The overall values of E_A increased when compared with non-degraded device. It could also be seen that the DOS at 0.05 eV, the values of both degraded and non-degraded devices are quite similar, is 10^{20} cm^{-3} (figure 3.6(b)). However, since the threshold voltage has increased for the degraded device as a result of trapping of electrons by adsorbed oxygen in the PTCDI-C8 layer, higher V_{GS} voltage is needed to shift the Fermi level close to the LUMO level [125]. For this reason, the values of E_A are higher in the case of degraded device (figure 3.6(a)) and the Fermi level located close to the LUMO level for the non-degraded device.

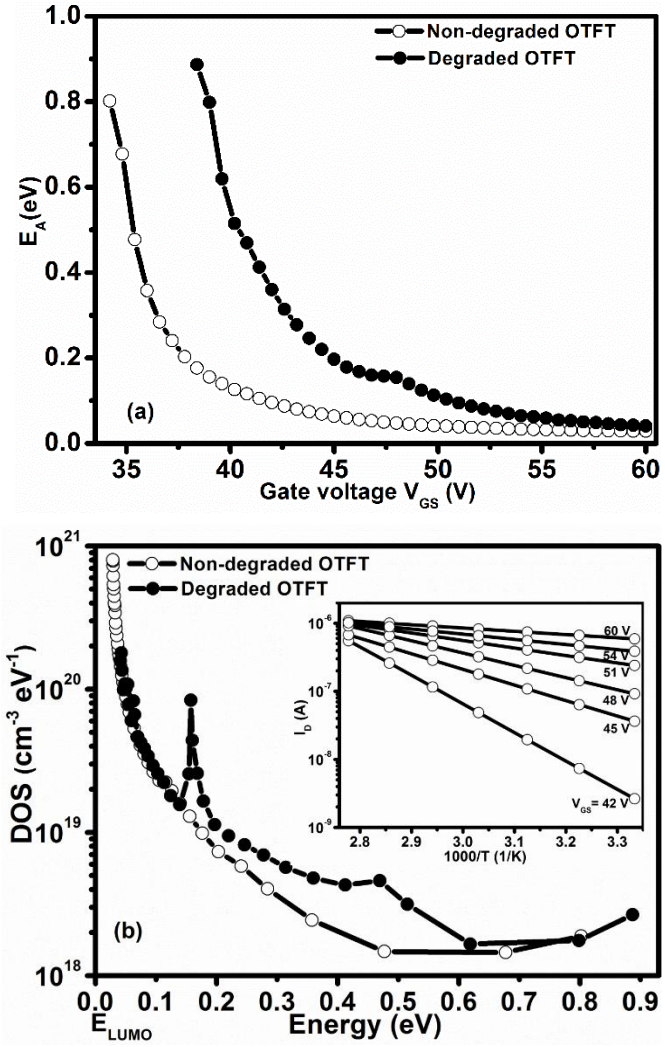

Figure. 3.6. (a) The dependence of E_A with the gate voltage and (b) density of states in the gap of PTCDI-C8 calculated from the derivative of the activation energy. The inset graph of (b) shows the Arrhenius plot for different gate voltages for degraded OTFT.

A new level with defect density of 10^{20} cm^{-3} was formed and it was located around $|E_{LUMO} + 0.15|$ eV. They behaved as traps for charge carriers and that may be attributed to the oxygen adsorption in the PTCDI-C8 layer [171]. The high electronegativity of oxygen causes attraction of electrons from the organic molecules and acted as traps for electrons [32]. Another defect level at $|E_{LUMO} + 0.49|$ eV was observed which may be related to water molecules adsorbed to the SiO_2 dielectric. Goldmann et al. [172] have analysed the defects created due to the adsorption of water molecules to the dielectric of pentacene single crystal field effect transistors. The polar nature of water molecules enables interactions with electrons on exposure to ambient air [173]. The reduction in drain current and mobility value was due to the localised trap states. Generally, the density of localised states in the organic semiconductor layer determines the performance of OTFTs.

3.2.3. Conclusions

PTCDI-C8 organic thin film transistors were successfully fabricated and were electrically characterized. The thermally activated channel conductance was examined and the density of localized states in the gap of PTCDI-C8 was calculated. In order to study the stability and degradation of OTFTs, the devices were exposed to air for 2 h before performing electrical measurements in air. The DOS measurements revealed that a new level with defect density of 10^{20} cm^{-3} was formed. The oxygen adsorption into the PTCDI-C8 active layer creates this level and it is located at around 0.15 eV below the LUMO level. Also, found a defect level at $|E_{LUMO} + 0.49|$ eV and they related to water molecules adsorbed to the SiO_2 dielectric.

3.3. Part II: Density of states in p-type pentacene TFT channel layer

3.3.1. Experimental section

The p-type OTFT for the present study was fabricated in the inverted-staggered (top contact) structure. A heavily doped n-Si (100) wafer was used as the gate electrode and thermally grown silicon dioxide (SiO_2) having thickness of 108 nm served as gate dielectric. The pentacene layer was deposited using vacuum thermal evaporation system maintained at a base pressure of 2.6×10^{-6} mbar and at a substrate temperature of 160 $^{\circ}$C. The active layer thickness of 50 nm deposited at a rate of 0.3 Å/s was measured using a quartz crystal oscillator thickness monitor. Pentacene was evaporated through the metallic shadow mask in order to get isolated devices. The gold drain and source contacts were deposited by thermal evaporation through shadow masks that define a channel length (L) and width (W) of 80 µm and 2000 µm, respectively. The electrical measurements were carried out using Agilent 4156 C semiconductor parameter analyzer under vacuum (10^{-1} mbar) in the absence of light and after 2 hour air exposure of TFT. During the electrical characterization under, the device temperature was varied from 300 K to 360 K by means of an MMR Technologies controller (model K-20). The devices were electrically characterized between 300 K and 360 K for each 10 K steps. The electrical measurements of the OTFTs were performed after keeping 5 minutes at set temperatures for stabilizing the temperature at each set value.

3.3.2. Results and discussion

Figure 3.7(a) shows the output characteristics of the fabricated pentacene OTFTs measured in vacuum, which exhibit expected electrical characteristics of p-channel field effect transistors. Figure 3.7(b) shows the

transfer characteristics in which I_D on log scale versus V_{GS} and $I_D^{1/2}$ versus V_{GS} plot at fixed V_{DS} = -10 V.

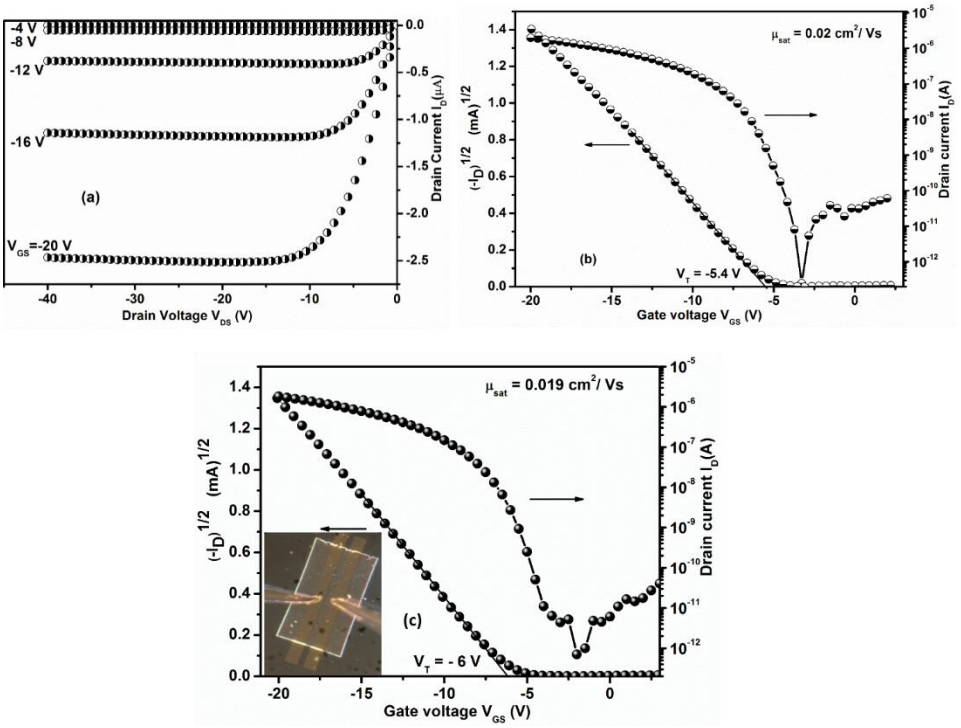

Figure 3.7. (a) The output and (b) transfer characteristics of pentacene TFT measured in vacuum. (c) The transfer characteristics of 2 h air exposed pentacene TFT. Inset of 3.7. (c) shows the optical image of pentacene TFT.

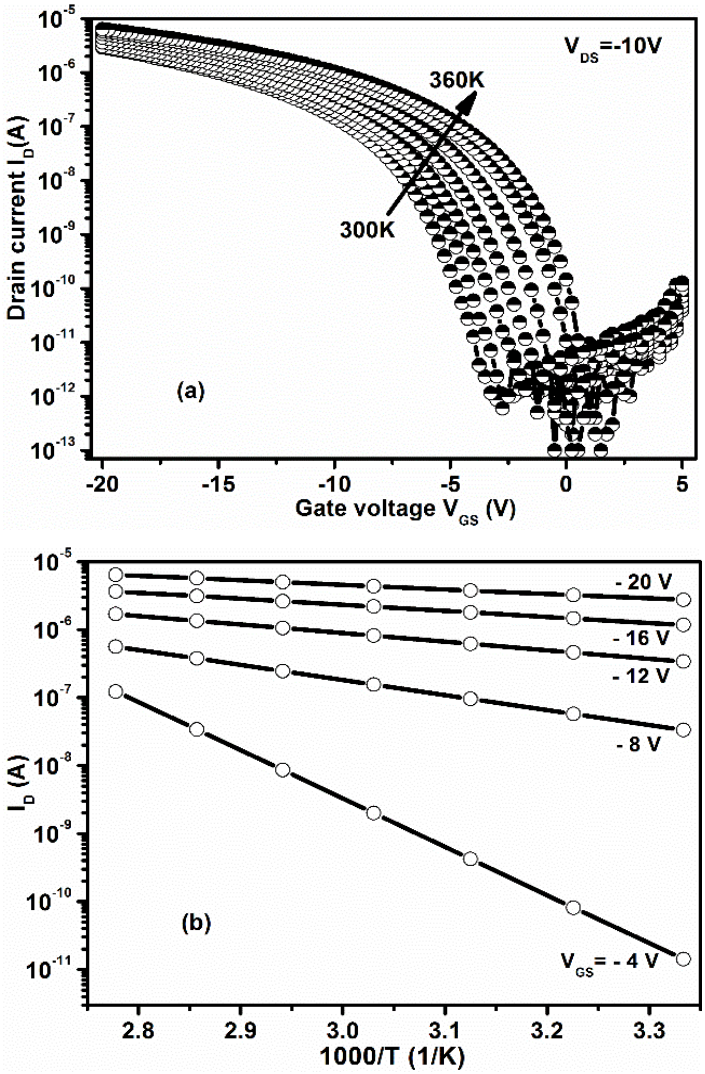

Figure 3.8. (a) The transfer characteristics were measured at different temperatures during heating (b) The Arrhenius plot of the drain current for different gate voltages.

The field-effect mobility was calculated at room temperature from a linear fit to the saturation characteristic obtaining a relatively high value of 0.02 $cm^2V^{-1}s^{-1}$, on-off ratio of 10^5 and the threshold voltage was -5.4 V. The output and transfer characteristics were measured in both vacuum and in ambient conditions (after 2 h air exposure) but there was no observable change in the OTFT parameters (figure 3.7 (c)).

The DOS measurements of OTFTs were carried out in ambient conditions after 2 h air exposure by measuring transfer characteristics at different temperatures ranging from 300 K to 360 K (figure 3.8 (a)). The data obtained from this characteristics were used for the calculation of E_A from the Arrhenius plot. The Arrhenius plot of the drain current for different gate voltages shown in figure 3.8 (b). The E_A values for different V_{GS} can be obtained by measuring the slopes curves (figure 3.9 (a)). The E_A value is relatively high (0.76 eV) for low gate voltages (just above threshold), but it steadily decreases with V_{GS} until it saturates in a value below 57 meV (strong accumulation).

The density of states in the bandgap of pentacene was calculated from the derivative of the activation energy (figure 3.9 (b)) [166]. The DOS exponentially increases up to 10^{19} cm^{-3} close to the valence band edge.

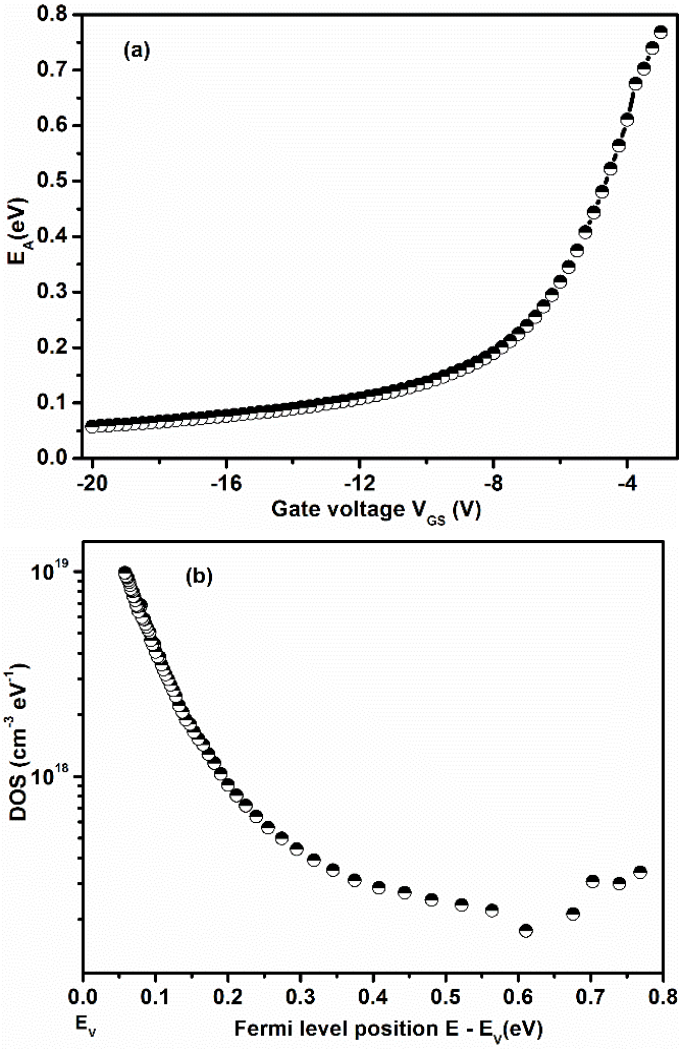

Figure 3.9. (a) The dependence of E_A with the gate voltage (b) density of states in the bandgap of pentacene calculated from the derivative of the activation energy.

3.3.3. Comparative study on degradation and trap density of states of n-type PTCDI-C8 and p-type pentacene OTFTs

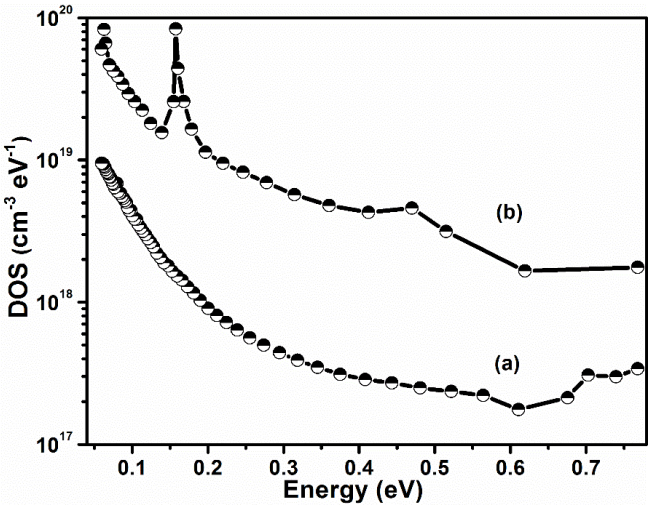

Figure 3.10. Density of states in the bandgap of pentacene (curve a) and PTCDI-C8 (curve b) calculated from the derivative of the activation energy.

Figure 3.10 shows the comparison of DOS in the bandgap of 2 h air exposed pentacene and PTCDI-C8 OTFTs. The exponential region of the DOS can be assumed as a band tail of localised states induced by structural disorder. The amount of those localised states was one order higher in the case of PTCDI-C8 when compared with pentacene. So the overall current value and the field effect mobility of pentacene OTFT was one order higher than PTCDI-C8 OTFT. The oxygen could be easily adsorbed in the n-type organic semiconductor active layer which leads to the degradation of PTCDI-C8 OTFTs [173]. Figure 3.10 (curve b) shows a peak at 0.15 eV indicate the formation of level with defect density of $10^{20}cm^{-3}$ in case of

PTCDI-C8 OTFT. They behaved as traps for charge carriers and that may be attributed to the oxygen adsorption in the PTCDI-C8 layer, whereas no such peak was present in the pentacene. The degradation of PTCDI-C8 OTFT was the reason for higher value of threshold voltage (40.5 V) than pentacene OTFT (-5.4 V). The electrical charge transport strongly affected by the oxygen traps because they act as localized states in the organic semiconductor material and hence p-type organic materials are more stable than n-type organic materials.

3.4. Conclusions

Pentacene (p-type) and PTCDI-C8 (n-type) organic thin film transistors were successfully fabricated and were electrically characterised. The thermally activated channel conductance was examined and the density of localised states in the gap of both pentacene and PTCDI-C8 was calculated. In order to compare the stability and degradation of pentacene and PTCDI-C8 OTFTs, the devices were exposed to air for 2 h before performing electrical measurements in air. The DOS measurements revealed that a level with defect density of 10^{20} cm^{-3} was formed in PTCDI C8 layer when exposed to air. The oxygen adsorption into the PTCDI-C8 active layer was attributed to this level and it is located at around 0.15 eV below the LUMO level. The electrical charge transport strongly affected by the oxygen traps and hence p-type organic materials are more stable than n-type organic materials.

Chapter 4

Fabrication of amorphous zinc tin oxide thin film transistors and the investigation on the reasons for instabilities

4.1 Introduction

Amorphous oxide transparent semiconductors (AOS) are quite attractive materials for the reason that they require a low processing temperature and can be grown on flexible plastic substrates [4]. The display industry is mainly based on thin film transistors (TFTs) made of the conventional materials like amorphous hydrogenated silicon and polycrystalline silicon. In the near future they will be replaced by the high potential AOS-based thin film transistors (TFT) [174]. At present indium gallium zinc oxide, zinc tin oxide, zinc indium oxide, zinc indium tin oxide etc are the most used channel materials for the fabrication of AOS-based TFTs [5,175–178]. Indium free systems are highly preferred for their cost effectiveness. Hence among the above mentioned materials zinc tin oxide

(ZTO) is more favourable and economical for fabricating high performance TFT. Field effect mobility as high as 50 $cm^2V^{-1}s^{-1}$ and on-off ratio10^7 has been reported for ZTO TFT [19].

Though the mobility of amorphous TFT is superior to amorphous silicon, the environmental conditions detrimentally affect ZTO device parameters. While considering the commercialization of AOS TFTs, the reliability and stability of such devices are the important factors. In recent years major studies have been focused on the stability of AOS TFTs under various aging parameters and stress conditions [179,180]. It is reported that the adsorbed oxygen captures electrons from the conduction band of the channel layer and creates a depletion region in the back of the channel which in turn increases the threshold voltage of TFTs [181]. The deviation of device performance with respect to different ambient conditions arises due to the creation of localised defects in the active channel layer. For instance, in the ambient condition the water vapor adsorption creates large number of deep acceptor like trap levels in the bandgap region of ZTO channel layer and consequently deteriorates the sub-threshold swing [182]. One of the most effective ways to reduce the instability of TFTs is to apply a passivation layer onto the device [183].

The correlation between the stability and density of states (DOS) is an important aspect regarding the reliability of AOS material based devices because it contains large number of localized defect states in the bandgap. The stability studies have more significance in the field of modern transparent electronics since stability under bias and illumination are the main concerns of modern displays [184–186]. Stability of TFT under various ambient conditions mainly depends on the quality of the channel layer which can be improved by choosing different thermal treatments

during or after deposition of the channel layer. The shifting of threshold voltage and sub-threshold swing are the major stability issues in the ZTO TFT.

In this chapter, part I describes the exploration of DOS inside the channel layer with and without passivation layer of TFTs under aging conditions. The distribution of those defect states can be examined from the temperature dependent transfer characteristics of TFTs under different aging conditions. Generally, modified variable range hopping (VRH) and multiple trapping and thermal release (MTR) models were used for the calculation of DOS in the bandgap of AOS channel layers [126,187]. In the present study, the device stability with respect to ambient parameters is well studied by analyzing the variation of DOS in the active ZTO channel layer by MTR model.

In part II, we have investigated the stability of amorphous Zn-Sn-O thin film transistors under negative gate-bias illumination stress after the post-annealing at various temperatures. The instability of ZTO TFT under negative gate-bias illumination stress (NBIS) is arising from the defects due to the oxygen vacancies as well as defects from the channel-insulator interface. On increasing the annealing temperature, the observed reduction in shift of the threshold voltage can also attributed to the reduction in the defect induced trap density inside the channel material.

4.2 Part I: Investigations on the reasons for degradation of zinc tin oxide thin film transistor on exposure to air

4.2.1 Device fabrication

Zinc tin oxide (Zn_2SnO_4) thin films were deposited via RF magnetron sputtering using ZTO powder target. Generally ZnO-SnO_2

system has two stable phases: Zn_2SnO_4 and $ZnSnO_3$. For the preparation of phase pure ZTO powder, ZnO and SnO_2 powders were mixed in 2:1 ratio and calcined at 1100 °C for 1 h. All other ZnO:SnO_2 mixture ratio and calcination temperatures resulted in the formation of either $ZnSnO_3$ phase or a mixture of Zn_2SnO_4, SnO_2 and ZnO phases. The Zn_2SnO_4 has a spinel structure and is chemically and thermally highly stable. Figure 4.1 shows the XRD spectra of ZnO, SnO_2 and ZTO powders. The observed XRD data of ZTO powder exactly matches with the JCPDS data (JCPDS No. 24-1470) of cubic spinel phase and no peaks corresponding to any secondary phases were detected.

During sputtering the base pressure and working pressure were 7×10^{-6} and 5×10^{-3} mbar respectively. Figure 4.1(b) shows the XRD spectra of as deposited and post-annealed ZTO thin films. All the films were amorphous in nature even after post-annealing at 300 °C. The optical and electrical properties of the ZTO thin films were studied before TFT fabrication. The films were highly transparent, with an average transmittance of 85% in the visible region (figure 4.1(c)). From the Tauc plot shown in the inset of figure 4.1(c) the bandgap of the film was calculated as 3.5 eV. The carrier concentration and mobility of the as-deposited films were 10^{14} cm^{-3} and 1 cm^2 $V^{-1}s^{-1}$ respectively. On post-deposition annealing at 300 °C for 1 h under ambient conditions, the carrier concentration and mobility values increased to 10^{16} cm^{-3} and 5 $cm^2V^{-1}s^{-1}$ respectively. The observed optical and electrical parameters of the ZTO thin films were comparable to those of ZTO thin films prepared by PLD and sputtering [15,188].

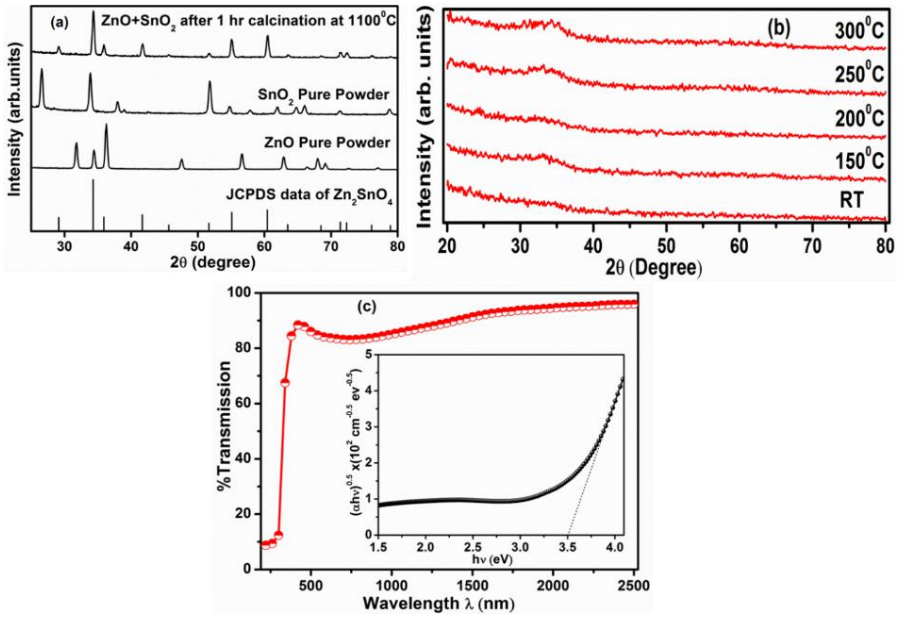

Figure 4.1. (a) XRD spectra of ZnO, SnO_2 and ZTO powders (b) XRD of ZTO thin films annealed at different temperatures (c) Transmission spectrum of ZTO thin films annealed at 300 °C. Inset shows the Tauc plot.

The n-type amorphous ZTO TFTs with and without passivation layer were fabricated in the inverted-staggered (top contact) structure as shown in figure 4.2. Heavily doped n-type silicon wafer was used as the gate electrode, with 100 nm of thermally grown silicon dioxide serving as the gate dielectric. By making use of a shadow mask, patterned ZTO channel layer was deposited on silicon dioxide layer. After deposition, the channel layer was annealed at 300 °C for 1 h under ambient conditions. Shadow mask was used to deposit Ti (10 nm)/Au (100 nm) source-drain contacts thereby defining the channel length and width as 65 and 1000 μm respectively. In this type of unpassivated TFT, the back of the channel is

exposed to the environment, which will adversely affect the performance and long term stability of the device. To overcome these concerns titanium oxide (TiO_2) passivation layer of 100 nm thickness was deposited by RF sputtering on the top of the device. The passivated and unpasssivated devices were exposed to air for 20 days and the transfer characteristics were measured to study the aging effect.

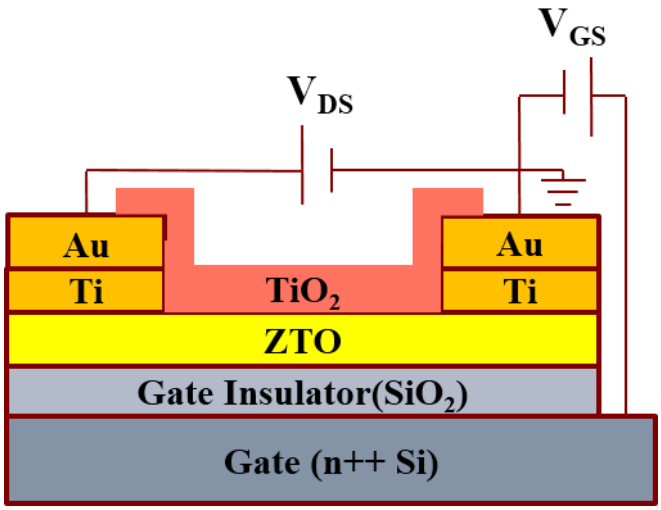

Figure 4.2. Schematic cross-section of passivated ZTO thin film transistor.

4.2.2. Experimental results

Figure 4.3(a) shows the transfer characteristics of as prepared unpassivated ZTO TFT having isolated channel layer as shown in the inset of figure 4.3(b). Compared to the non-isolated channel layer TFT the number of defects in the gate dielectric which take part in the conduction mechanism is found to be reduced in the isolated channel layer TFT. This is evident from the low leakage current and high on-off ratio observed for the isolated device.

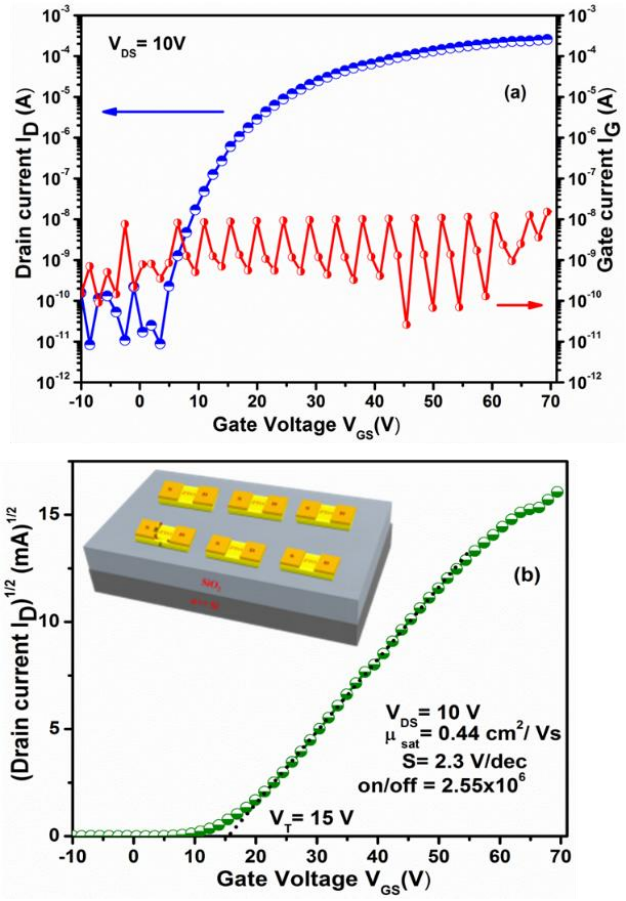

Figure 4.3. (a) Transfer characteristics (I_D-V_{GS} and I_G-V_{GS}) of unpassivated ZTO TFT at fixed V_{DS}=10 V (b) Plot of square root of I_D versus V_{GS} to find TFT parameters. Inset shows the schematic structure of isolated unpassivated ZTO TFT.

All the above measurements were done immediately after the device fabrication. The devices were then exposed to air for 20 days and the transfer characteristics were measured again to study the aging effect (figure 4.4). From the measurements it is observed that the saturation

mobility (μ_{sat}) and on-off ratio of the device doesn't change much but the threshold voltage (V_T) and sub-threshold swing (SS) change considerably on air exposure. The values of μ_{sat}, V_T and SS of the device changed from 0.44 cm^2 /Vs, 15 V and 2.3 V/dec to 0.49 cm^2 /Vs, 18.5 V and 9 V/dec respectively. These effects are a result of oxygen and water adsorption and subsequent trap level formation in the channel layer of the TFT [119,181,189]. The positive shift of threshold voltage was due to the oxygen adsorption. Oxygen can absorb electrons from the conduction band of ZTO and cause depletion of electrons. The reduction in the electron concentration in the channel region leads to positive shift of threshold voltage [190]. But the deterioration in the SS value doesn't depend on the oxygen adsorption but depends on the water adsorption [191].

Depending on the film thickness two mechanisms were proposed to explain the influence of adsorbed water on the behavior of oxide channel layers [191]. Firstly a large negative shift of threshold voltage happens due to the 'donor effect' in which the water molecules donate electrons to the channel material [192]. Such large number of electron contribution occurs by water adsorption only in the thicker channels (t >100 nm). When the channel thickness is <100 nm the mechanism which dominates is the water induced creation of acceptor like trap states in the channel region [191]. In this work the channel thickness was 50 nm and there observed no negative shift of threshold voltage. Moreover the large deterioration in the SS value also is a clear indication of creation of acceptor like trap levels in the channel layer by the adsorbed water molecules. Hence it can be concluded that in this particular work the adsorbed water molecules are acting as acceptor like traps rather than donor like traps.

The trap levels, especially the deep-levels present in the bandgap of channel layer greatly affects the sub-threshold swing (SS) value of a TFT [13]. In general, SS value is an indicator of the total trap densities and it shows how easily a transistor can be switched from off-state to on-state [193]. The trap densities mainly constitute two types, tail states and deep states. The increase in tail states will decrease the field effect mobility and increase in deep states will cause the deterioration of SS value [191]. On air exposure of ZTO TFT only the SS value changed and the field effect mobility remained almost unchanged. So it confirms the creation of deep level acceptor like traps in the bandgap of channel layer by water adsorption. It is already reported that the amount of acceptor like trap created by water adsorption depends on the amount of water content in the atmosphere [182]. The deteriorated SS value due to water adsorption can be recovered by thermal annealing at or above 100 °C. Park et al. have already studied the water desorption effect on SS value and the recovery time was found to be very high [191].

The SS value can be defined as,

$$SS = \frac{dV_G}{d(\log I_d)} \tag{4.1}$$

Comparing the transfer characteristics of as prepared and air exposed TFTs shown in figure 4.4 the slope of the curve is found to decrease on aging with resultant high SS value. Generally transistors with active materials like amorphous silicon, amorphous oxides and organic semiconductors are observed to show such behavior [123,128,194,195].

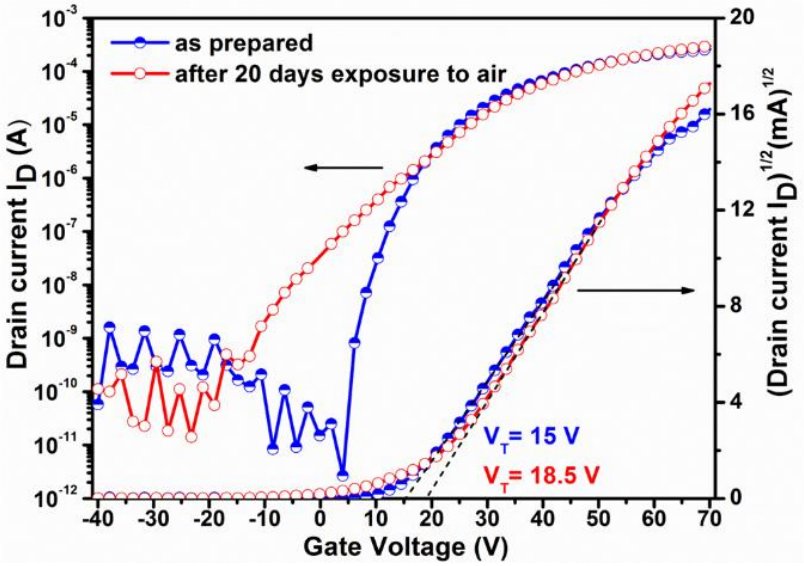

Figure 4.4. Transfer characteristics of unpassivated ZTO TFT before and after aging.

To acquire a thorough understanding of the changes in the behavior of TFT on aging, variation of density of states (DOS) on aging was studied [194]. In order to calculate the DOS in the band gap of ZTO thin film the temperature dependent transfer characteristics were measured at different temperatures varying from 310 K to 360 K for both as prepared and 20 days air exposed TFT (figure (4.5a) and (4.5b)).

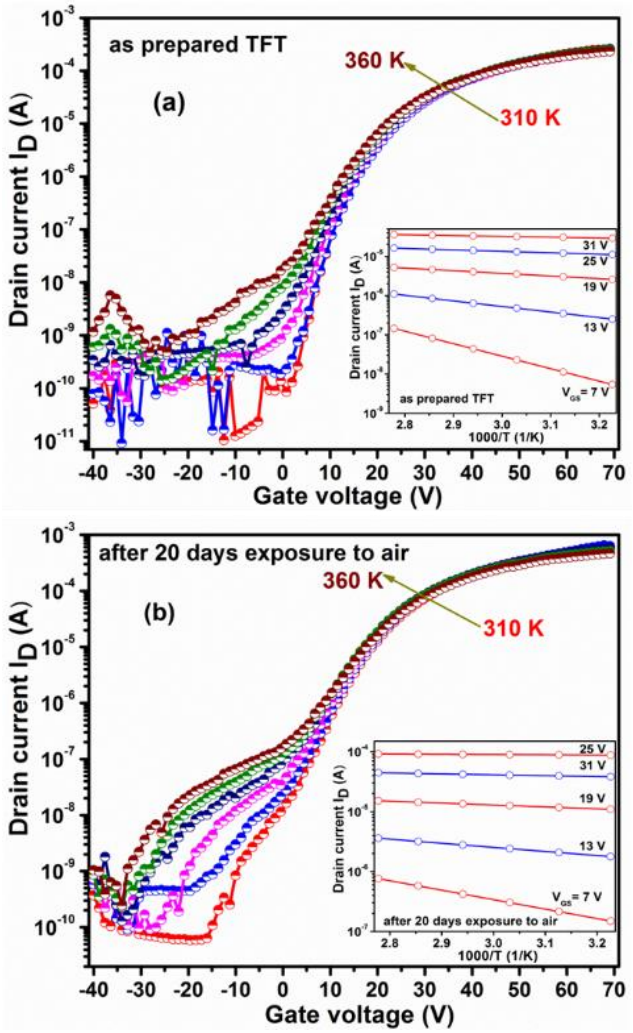

Figure 4.5. The transfer characteristics of (a) as prepared and (b) 20 days air exposed unpassivated ZTO TFT measured at different temperatures. Insets show the Arrhenius plots for different gate voltages.

A thermally activated Arrhenius like behaviour was noticed and it was in good agreement with the multiple trapping and thermal release model (MTR) [127]. The model is based on the variation of activation energy (E_A) with respect to the gate voltage. It is well studied in the case of highly disordered and localised trap assisted semiconductors such as amorphous silicon and organic TFTs [124,170,196] It has been proposed that the rate of change of E_A with respect to gate voltage can be related to the density of states in the semiconductor [126].

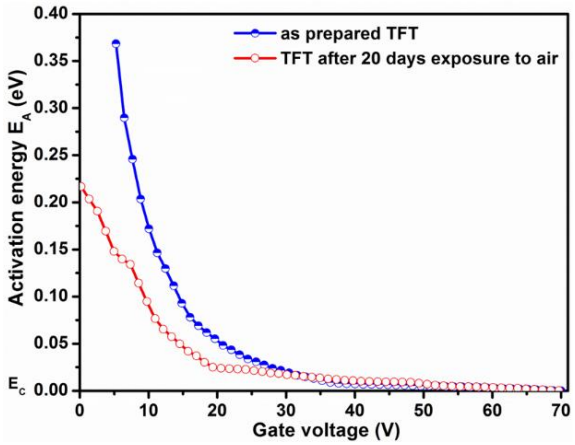

Figure 4.6. Dependence of E_A with gate voltage for as prepared and 20 days air exposed unpassivated TFTs.

Arrhenius plot for different gate voltages, i.e. the plot of measured drain current as a function of the reciprocal of temperature, gives a clear idea about the activation energy (Insets of figure 4.5(a) and figure 4.5(b)). Figure 4.6 shows the variation of activation energy with gate voltage for the as prepared and 20 days air exposed TFTs. It is clearly seen that the rate of change of activation energy is faster in the case of as prepared TFT than

that in the case of air exposed TFT. The rate of change of E_A gives a clear idea about the DOS inside the channel material. The fast variation of activation energy indicates the fast variation of Fermi level inside the bandgap. This evidently demonstrates the existence of fewer number of trap states in the bandgap of as prepared TFT.

The expression for calculating DOS is [125]:

$$N(E) = \frac{C_i}{q} \frac{1}{t\frac{dE_A}{dV_G}} \tag{4.2}$$

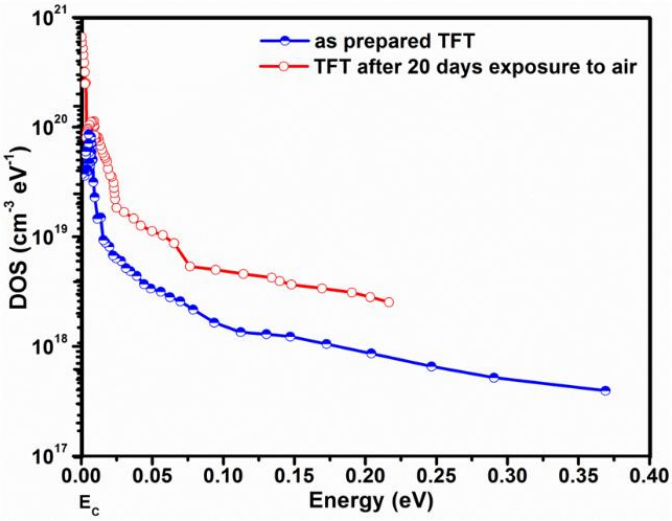

Figure 4.7. Density of states in the bandgap of ZTO channel calculated from the derivative of the activation energy for as prepared and 20 days air exposed unpassivated TFTs.

Figure 4.7 shows the variation of DOS of localized trap levels in the band gap of ZTO channel layer. The overall value of DOS of air exposed TFT is high when compared to that of as prepared TFT. The

adsorption of water molecules results in the formation of additional trap states and thereby increases the DOS. The values of defect density at the band edge (energy = E_c) of air exposed and as prepared devices were 10^{21} and 10^{20} cm^{-3} eV^{-1} respectively. Considering the tail states (say at energy = 0.005 eV) of the devices with and without air exposure, it can be seen that the change in DOS were much smaller on comparing with the change in the deep states (say at energy = 0.2 eV). From figure 4.7, it can be seen that the DOS at energy of E = 0.005 eV of air exposed and as prepared devices were 1.1×10^{20} and 9×10^{19} cm^{-3} eV^{-1}, respectively. Deeper inside the bandgap, the exposed TFT exhibits a significant increase in the localised states as compared to the as prepared TFT i.e. DOS at energy of 0.2 eV of air exposed and as prepared devices were 3×10^{18} and 8×10^{17} cm^{-3} eV^{-1}, respectively. We already indicated that the SS and mobility values may change with change in deep and tail states, respectively. Here, the tail states of as prepared and air exposed devices were similar and hence the mobility did not change much. Nevertheless, the SS value changed from 2.3 V/dec to 9 V/dec and it was in accordance with the significant change in deep states inside the bandgap of ZTO channel layer.

The detrimental effect of air exposure on TFT parameters can be avoided by passivating the back side of the channel of TFTs. The passivations of AOS TFTs are commonly carried out by several materials including SiO_2, Al_2O_3 and SiN etc. Recently, a comprehensive study by Jie Wu *et.al.* [183] on different passivation layers for the IGZO TFTs showed TiO_2 is good for passivation. Also, the superior optical absorption rate of TiO_2 among other passivation layers is highly favorable for the steady working of TFTs even under white light illumination. In the present study, TiO_2 thin film having thickness of 100 nm was deposited on top of ZTO

TFT as passivation layer. After that, the transfer characteristics of as deposited and 20 days air exposed passivated ZTO TFTs were measured. Figure 4.8 shows transfer characteristics of the as deposited ZTO TFTs (I- unpassivated and III- passivated) and after 20 days exposure to air (II- unpassivated and IV- passivated). From figure 4.8, the curves of as-deposited TFTs (I and III) shows that the process of deposition of the TiO2 passivation layer over the channel of TFT does not affect the transport properties of ZTO thin films. Further, it can be seen that the passivated TFTs are stable even after 20 days air exposure when compared to unpassivated TFTs. In the case of passivated TFTs there observed no remarkable change in the values of V_T and SS indicating the considerable reduction in oxygen and water adsorption in the channel of TFT.

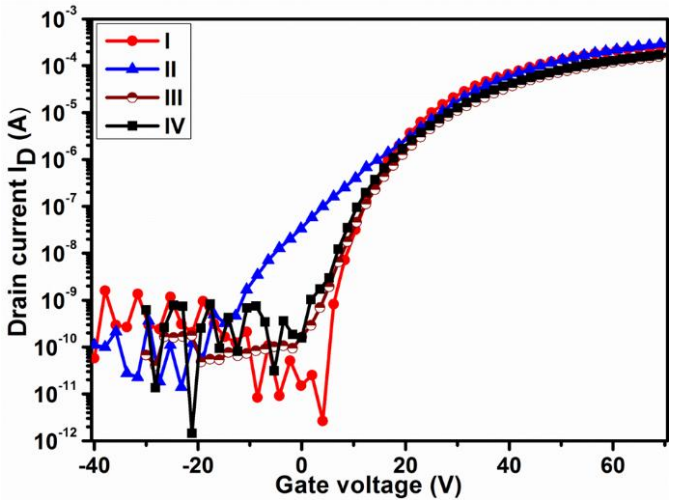

Figure 4.8. Transfer characteristics of the as-deposited ZTO TFTs (I- unpassivated and III- passivated) and after 20 days exposure to air (II- unpassivated and IV- passivated).

The positive effect of passivation on TFT performance was further confirmed by DOS analysis. Figure 4.9 shows the DOS in the channel layer of as deposited ZTO TFTs (I), unpassivated (II) and passivated (III) ZTO TFTs after 20 days exposure to air. The overall value of localized DOS in the band gap of ZTO channel layer of unpassivated TFT was higher than that of passivated TFT. Hence passivation of channel layer was proved to be an effective way to block oxygen and water entering into the channel of the TFT thereby increasing the device stability.

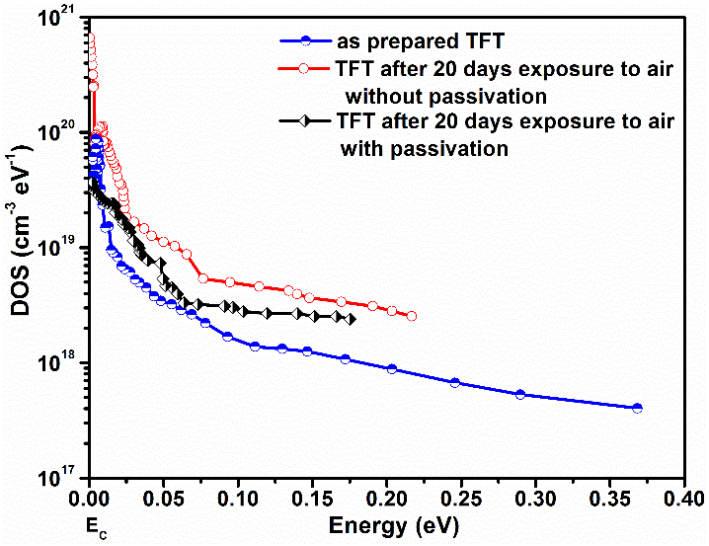

Figure 4.9. Density of states in the bandgap of ZTO channel for as-prepared and 20 days air exposed passivated and unpassivated TFTs.

4.2.3. Conclusions

In conclusion, we fabricated amorphous ZTO TFT on Si/SiO_2 substrate and investigated the aging effect on TFT performance. The

positive shift in threshold voltage and increase in sub-threshold swing after air exposure suggests trap level creation in the channel layer. The DOS variation for the 20 days air exposed TFT in comparison with the as-prepared TFT indicated the formation of large number of trap levels in the channel layer due to water adsorption. Passivation of channel of TFT using TiO_2 layer significantly reduced oxygen and water adsorption and an effective way of improving the stability of the devices.

4.3. Part II: Effects of post-annealing on negative bias illumination stress-induced instability of zinc tin oxide thin film transistor

4.3.1. Experimental details

Figure 4.10 shows a schematic structure of inverted-staggered ZTO TFTs with SiO_2 gate insulator on the highly-doped n-type Si substrate. A 50 nm ZTO film was deposited by RF magnetron sputtering at room temperature with a 2 inch diameter powder target of ZTO (SnO_2: ZnO = 2:1). Sputtering was carried out at a pressure of 5×10^{-3} mbar with Ar as sputtering gas. By making use of a shadow mask, patterned ZTO channel layer was deposited on silicon dioxide layer at an RF power of 25 W. The films were then subjected to post-annealing in air for 1 h. Annealing was carried out at temperatures ranging from 200 °C to 400 °C in steps of 50 °C. Later, Ti (10 nm)/Au (100 nm) source-drain contacts were deposited thorough a shadow mask onto the channel layer defining its length and width as 65 and 1000 µm respectively. A passivation layer of TiO_2 having a thickness of 100 nm was deposited by RF sputtering on each device to isolate it from the ambient atmosphere.

The electrical parameters of the TFT were evaluated using Keithley SCS 4200 semiconductor parameter analyzer at room temperature under dark condition. Structural and compositional analyses were performed using a gracing incidence X-ray diffractometer (GIXRD) and X-ray photoelectron spectroscopy (XPS), respectively.

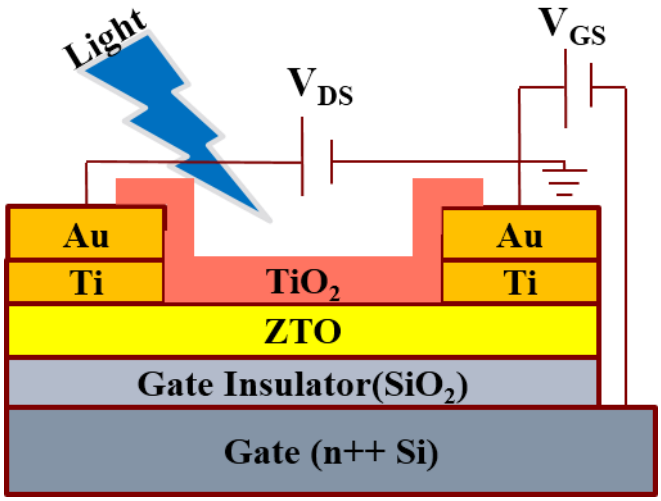

Figure 4.10 Schematic structure of inverted-staggered (top contact) ZTO TFT.

4.3.2. Results and discussion

The ZTO thin films were post-annealed in air for 1 h at different temperatures ranging from 200 °C to 400 °C in steps of 50 °C. Figure 4.11 shows the XRD patterns of the 100 nm as-deposited and post-annealed ZTO films deposited on glass substrate. As shown in the figure, all the films are in amorphous state and the structural characteristics of the films are not changed by post-annealing. No sharp peaks corresponding to any of the

crystalline phases such as SnO_2 or ZnO were observed which agree with other reports [197].

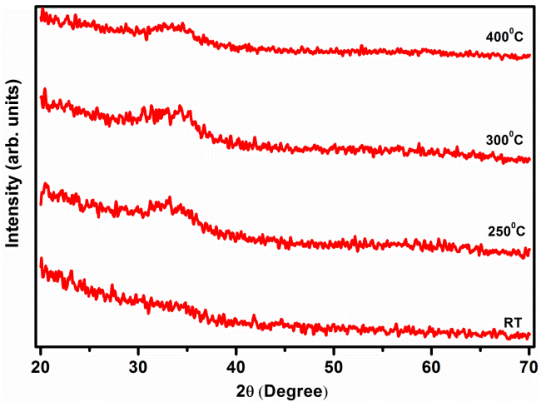

Figure 4.11. XRD patterns of the 100 nm as-deposited and post-annealed (250 °C, 300 °C and 400 °C) ZTO films deposited on glass substrate.

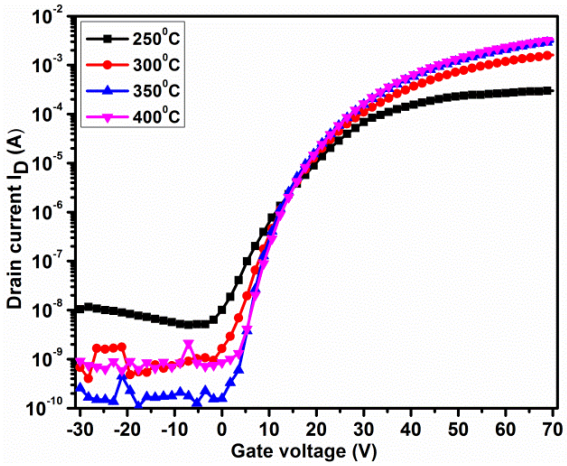

Figure 4.12. Transfer characteristics of the ZTO TFTs with channel layer annealed at various temperatures for 1 h.

Figure 4.12 shows the transfer characteristics of the ZTO TFTs where the channel layer was subjected to annealing at various temperatures for 1 h. Electrical parameters of the devices are listed in table 4.1.

From the measurements, it was seen that the saturation mobility (μ_{sat}), on-off ratio ($I_{on/off}$) and threshold voltage (V_T) of the devices increased with increasing annealing temperature. It was observed that the values of μ_{sat}, $I_{on/off}$ and V_T increases from 1.15 cm^2/Vs, 5.4×10^4 and 14.6 V to 6.23 cm^2/Vs, 5.8×10^6 and 19.5 V, respectively upon increasing the post annealing temperature from 250 °C to 400 °C. In the case of an amorphous ZTO thin film, thermal energy is necessary to rearrange the atoms on the local sites. During the annealing process atomic rearrangement improves, leading to higher mobility value and on-off ratio [15,198]. The increase in the threshold voltage with increasing post annealing temperature may be related to the decrease in the conductivity of the ZTO channel material. Oxygen vacancies are responsible for the conduction in amorphous oxide materials such as ZTO and the concentration of these vacancies tend to decrease with increasing post-annealing temperature [199]. Further, the TFTs with ZTO channel layer annealed at higher temperatures indicated the best sub-threshold swing (SS) values compared with other samples annealed at lower temperatures. It was observed that the SS value of ZTO TFTs initially decreased from 6.2 V/dec to 2.4 V/dec and then increasesd to 3.3 V/dec as the post-annealing temperature increased from 250 °C to 400 °C. TFT annealed at 350 °C shows better SS and on-off ratio of 2.4 V/dec and 2.4×10^7, respectively. The extracted value of interface traps (N_{SS}) between the channel/insulator layers of TFT fabricated with post annealed channel at 350 °C was 0.85×10^{13} $cm^{-2}eV^{-1}$ and it was the lowest value observed among all the

annealing temperatures. The better values of SS, N_{SS} and on-off ratio for TFTs with 350 °C post-annealing were related to the reduction in the channel/insulator interface traps. The reduction in SS and on-off ratio observed in the case of 400 °C annealing may be due to the creation of interface traps on annealing in this temperature range. The extracted N_{SS} value for 400 °C post annealed TFT was 1.17×10^{13} $cm^{-2}eV^{-1}$. The internal stress in the ZTO films and gate dielectric may be disturbed and causes the increased value of N_{SS}. Even though, the SS and on-off ratio deteriorated on 400 °C post annealing the defects associated with oxygen vacancies are reduced and it was confirmed by XPS measurements. Moreover, the improvements in saturation mobility, on-off ratio and sub-threshold swing with increasing post-annealing temperature is obviously associated with reduction in defect induced trap density originated from the oxygen vacancy [200].

Table 4.1. Electrical parameters of the ZTO TFTs annealed at various annealing temperatures for 1 h.

Device annealing Temp (^{0}C)	**μ (cm^2/Vs)**	**V_T (V)**	**SS (V/dec)**	**$I_{on/off}$**	**ΔV_T Under NBIS (V)**	**N_{SS} ($cm^{-2}eV^{-1}$) $\times10^{13}$**
250	1.15	14.6	6.2	5.4×10^4	5.8	2.22
300	2.74	17.5	4.1	2.6×10^6	5.5	1.46
350	5.50	19.1	2.4	2.4×10^7	3.9	0.85
400	6.23	19.5	3.3	5.8×10^6	1.1	1.17

The stability under negative bias illumination stress (NBIS) is a serious issue for the practical application of metal oxide TFTs in which it causes severe threshold voltage shift (ΔV_T) in the negative direction [201].

It has been reported that the ΔV_T under NBIS originates from charge trapping mechanism through bulk traps in channel layer and interface traps between the gate insulator and channel layers. Generally, the oxygen vacancies present in the channel region creates defect states and causes instability under NBIS [202].

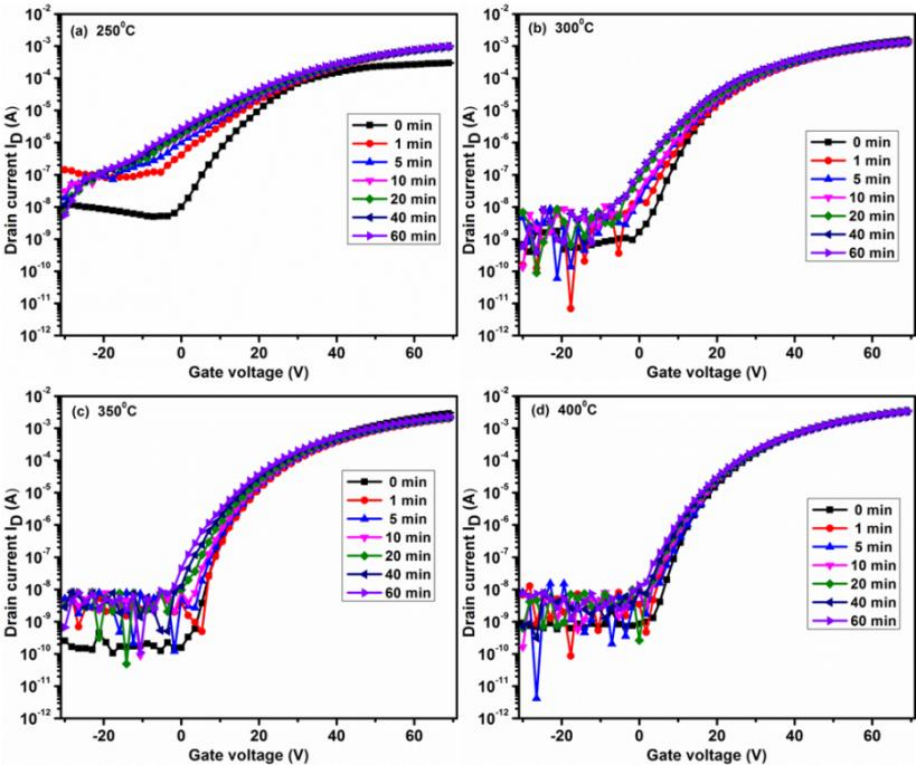

Figure 4.13. Transfer characteristics of ZTO TFTs with channel layer post- annealed at different temperatures (a) 250 °C (b) 300 °C (c) 350 °C and (d) 400 °C under different NBIS time.

To study the effect of NBIS on TFTs fabricated after post-annealing the channel layer at different temperatures, the transfer characteristics of TFTs were measured as a function of NBIS time. A white light illumination with an irradiance of 350 W/m^2 was used for the NBIS study in which TFTs were negatively gate biased under identical -10 V stress and 0 V drain-bias stress.

A clear dependence of stability of the TFTs on annealing temperature can be seen in the NBIS study of ZTO TFTs, as shown in figure 4.13. The TFT annealed at 250 °C shows a large ΔV_T which indicates that there exists large number of trap states in the interface as well as in the ZTO bulk material. As the post-annealing temperature increases up to 400 °C, the change in threshold voltages decreases due to the decrease in the trap states. On annealing, the oxygen vacancies decrease in number thereby decreasing the traps inside the channel layer which in turn increases the channel resistivity. The mechanism behind the NBIS is reported earlier; according to which the combination of visible light and negative gate bias creates ionized oxygen vacancies (V_O^{2+}) from neutral oxygen vacancies (V_O). Furthermore, this process induces electron hole pair formation and delivering additional electrons into conduction band of the channel material [17,203].

XPS measurements were performed (figure 4.14) to analyze the oxygen composition in as-deposited and post-annealed ZTO thin films at different temperatures (250 °C, 300 °C and 400 °C). The XPS spectrum of as prepared ZTO thin films shows a broad peak of O1s which is then de-convoluted to identify the different types of oxygen species. We observed three peaks corresponding to different chemical bonding states of oxygen, centered at 529.9 eV (O1), 531.6 eV (O2) and 532.3 eV (O3), respectively.

The lower binding energy peak (O1) is associated to the oxygen present in the lattice whereas peak O2 is related to the oxygen vacancies existing in the ZTO thin films. The presence of surface adsorbed oxygen content in the film is indicated by the high binding energy peak at 532.3 eV (O3) [199].

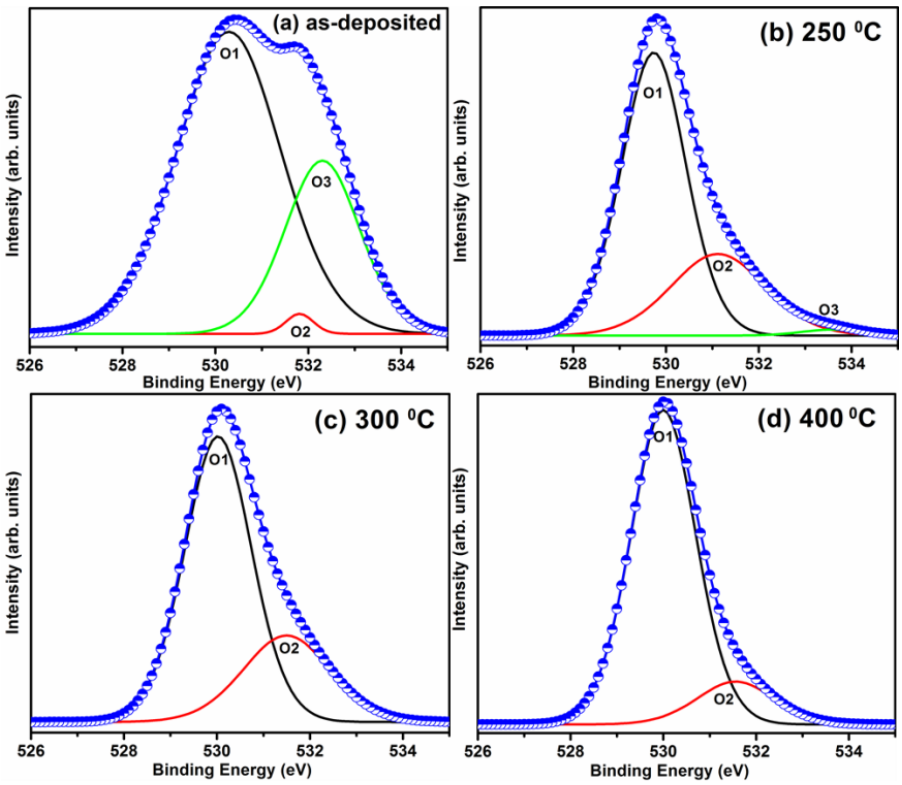

Figure 4.14. XPS O 1s spectra for the (a) as-deposited and post-annealed ZTO thin films at (b) 250 °C, (c) 300 °C and (d) 400 °C.

Table 4.2. Variation of different types of oxygen content in ZTO films post annealed at different temperatures.

Annealing Temp (°C)	**O1 (%)**	**O2 (%)**	**O3 (%)**
As prepared	70	1	29
250	69	29	2
300	72	28	-
400	86	14	-

Table 4.2 shows the variation of different types of oxygen content in as-deposited and post-annealed ZTO films. On increasing the annealing temperature from 250 °C to 400 °C, the percentage of O1 was increased from 69% to 86% and the O2 percentage was decreased from 29% to 14%. It was a clear indication of reduction of oxygen vacancies in the ZTO thin film during the post-annealing in air. Also, intensity of the highest binding energy peak (O3) decreased considerably on annealing and it completely vanishes upon high temperature annealing. The adsorbed oxygen species can be easily desorbed from the surfaces of ZTO thin films using the thermal energy [204]. The annealing temperature results in the internal rearrangements in the ZTO films which enhances the TFT performances. The rearrangements in the oxygen vacancies have a considerable role in improving the properties of thin films i.e. by reducing the oxygen vacancies via post-annealing at high temperatures can reduce the traps states in the channel layer [198]. Here, the ZTO film annealed at 400 °C shows minimum percent of oxygen vacancies and hence the TFT annealed at that particular temperature shows minimum ΔV_T and maximum mobility value.

The origin of NBIS was due to the existence of oxygen vacancy related trap density inside the ZTO channel layer and from the XPS study it was confirmed that oxygen vacancies strongly depend on post-annealing temperature. Hence, a quantitative assessment of the trap density inside the ZTO channel layer is highly desirable. The temperature dependent transfer characteristics were studied to investigate the trap density variation at different post-annealing temperatures of ZTO channel layer.

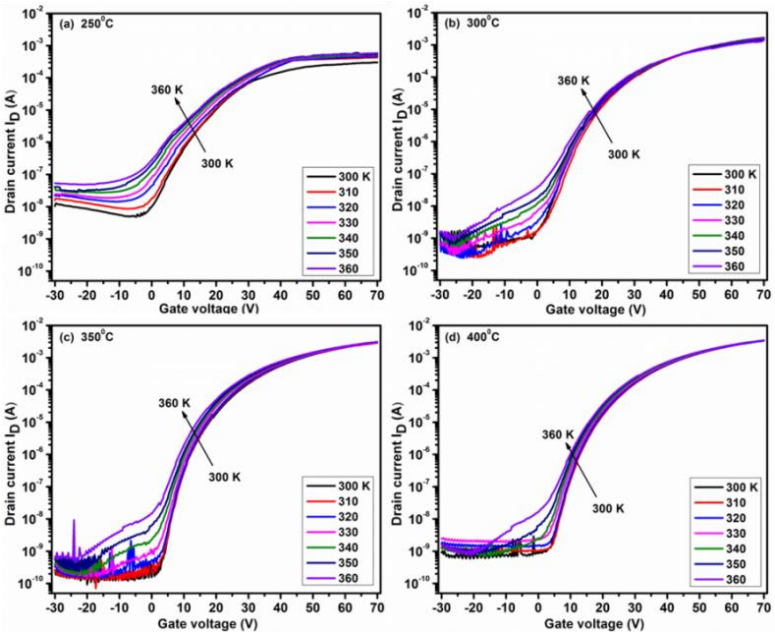

Figure 4.15. Transfer characteristics of ZTO TFTs channel post-annealed at different temperatures (a) 250 °C (b) 300 °C (c) 350 °C and (d) 400 °C measured in a temperature regime 300 K to 360 K.

In order to explore the distribution of the trap states in the ZTO channel layer, the temperature dependent transfer characteristics of transistors in the temperature range between 300 K and 360 K was measured [123,205]. The measurements were done on TFTs whose channel layer were post-annealed at different temperatures 250 °C, 300 °C, 350 °C and 400 °C. To attain a detailed understanding of the modifications in the behavior of TFT on post annealing, a thorough study on variation of oxygen vacancy generated trap states (DOS) inside the bandgap of ZTO channel layer were carried out.

From figure 4.15, a thermally activated Arrhenius like behaviour was observed for all TFTs. The measured drain current increases with increasing temperature which is in good agreement with the multiple trapping and thermal release model (MTR) [127]. The increase in current was observed due to the releasing of carriers from the trap states in the bandgap of ZTO channel layer.

The activation energy is easily calculated from the measured data by plotting logarithm of I_D versus 1/kT for each gate voltage (Arrhenius plot). The plot of activation energy variation with gate voltage of different post annealed TFTs are shown in figure 4.16. In MTR model, the activation energy is taken as the energy barrier for thermal release of trapped carriers and the variation of E_A with gate voltage permits the identification of trap states in the channel layer. The slow variation of E_A with gate voltage represents the large density of trap states and vice versa. The falling rate of E_A/dV_{GS} can be easily connected to the density of trap states in the band gap of channel layer [169,196].

Figure 4.16 (a) shows that the E_A variation with gate voltage was different for each TFT and it confirms that post-annealing temperatures

have significant effect on the defect states in the channel layer. The Fermi level movement inside the ZTO channel layer was influenced by the post-annealing temperature as a consequence of different defect densities.

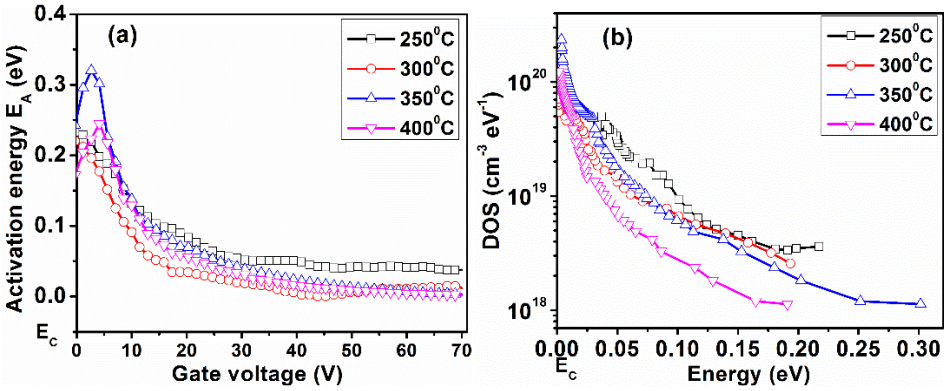

Figure 4.16 (a). Activation energy (E_A) as a function of gate voltage and (b) DOS of the ZTO TFTs at different post-annealing temperatures.

From figure 4.16(b), the DOS distribution was found to strongly depend on the post-annealing temperature. The DOS values at an energy of 0.1 eV below the conduction band edge are decreased from 9.68×10^{18} cm^{-3} eV^{-1} to 2.84×10^{18} cm^{-3} eV^{-1} with increase in post annealing temperatures from 250 °C to 400 °C, respectively. The defect states inside the bandgap of ZTO are mainly due to the oxygen vacancies present in the material. The post-annealing of ZTO channel layer in air enables the suppression of the oxygen vacancies and accordingly the oxygen vacancy related trap densities inside the ZTO channel layer decreased with increase in the post-annealing temperature. Therefore, post-annealed TFT at 400 °C displays only a slight shift of V_T than TFTs annealed at other temperatures which

ensures that the improved stability under a negative gate bias can be attributed to the least oxygen vacancy trap densities.

4.3.3. Conclusions

The effect of post-annealing treatment on negative bias illumination stability in Zn-Sn-O (ZTO) thin film transistors (TFTs) fabricated by RF sputtering was investigated. A clear dependence of stability of the TFTs on annealing temperature was seen in the NBIS study of ZTO TFTs. The oxygen vacancies present in the channel region created defect states and mainly caused instability under NBIS. The temperature dependent transfer characteristics were measured to investigate oxygen vacancy generated trap states (DOS) variations. The DOS values were decreased with increase in post-annealing temperatures from 250 °C to 400 °C. The improvement in saturation mobility, on-off ratio, sub-threshold swing and stability under NBIS with increasing post-annealing temperature was obviously associated with reduction in defect induced trap density originated from the oxygen vacancy. Post-annealing of channel layer improve the performance and stability of the ZTO TFTs.

Chapter 5

Low temperature fabrication of Cu_xO thin film transistors and investigation on the origin of low field effect mobility

5.1 Introduction

Recently oxide semiconductor thin film transistors (TFTs) gained considerable interest due to their excellent electrical performance, environmental stability and high optical transparency in the visible range [4]. High performance p-type oxide TFTs along with n-type TFTs have the potential to realize low power-consumption electronic circuits such as complementary circuits [206,207]. Nevertheless, only a few studies have reported on good performance p-type oxide TFTs compared to high performance n-type TFTs [208]. The most promising candidates to work as channel materials for p-type oxide TFTs are Cu_2O, CuO, and SnO [209]. Among them Cu_2O and CuO are well known p-type semiconductors and

they have direct bandgaps in the range of 2.1 eV–2.6 eV and 1.3 eV–2.1 eV, respectively [74]. The Hall mobilities of all reported copper oxide films were found to be higher than that of field effect mobility derived from the TFT measurements. Defects and impurities present in copper oxide channel layers create large number of hole traps and consequently the field effect mobility decreases [73]. In this work, we have investigated the origin of the low field effect mobility by estimating the defect induced subgap density of states (DOS) in fabricated copper oxide TFTs based on the optical absorption studies and temperature dependence of the drain currents. Electronic trap states in copper oxide semiconductors rigorously affect the performance of such devices; therefore, the understanding of such defect states is important to enhance the device parameters. For instance, in TFT the key device parameters such as field effect mobility, threshold voltage, sub-threshold swing as well as electrical and environmental stability are significantly affected by trap states inside the semiconductor. Analyzing the nature of the trap states inside novel materials can help in the better and accurate prediction of their optical and electrical properties.

5.2 Experimental section

Copper oxide thin films having 200 nm thicknesses were deposited via radio frequency (RF) magnetron sputtering using metal copper target. Thicknesses of the films were controlled by adjusting the deposition time. Depending on the oxygen partial pressure during deposition in the chamber Cu_2O and CuO thin films could be obtained. Electrical and optical properties of copper oxide thin films were found to strongly affected by even the slight variations in deposition conditions and hence post-annealing was observed to be very important for optimizing the film properties [210].

All the as-deposited copper oxide films were subjected to post-annealing at 300 °C for 30 minutes to improve the microstructural, optical and electrical parameters. After optimization of the growth conditions of Cu_2O and CuO thin films, TFTs were fabricated in an inverted staggered structure, where a heavily doped n-type silicon wafer was used as the substrate and the gate electrode. A 100 nm thermally grown silicon dioxide layer served as the gate insulator. Active layers of Cu_2O and CuO thin films having thickness of 15 nm were deposited over the gate insulator. A base pressure of 7×10^{-6} mbar and a working pressure of 5×10^{-3} mbar were maintained for all the depositions. RF power applied to metallic copper target of 2 inch diameter (99.99% pure) was 50 W and the substrate was kept at room temperature during deposition. Controlled atmosphere of oxygen and argon in the deposition chamber favoured the formation of Cu_2O and CuO phases. A gas ($Ar+O_2$) mixing ratio of $Ar/O_2 = 20/1.3$ (sccm/sccm) and $Ar/O_2 = 20/3$ (sccm/sccm) were used for preparing Cu_2O and CuO thin films, respectively. Using shadow mask, Au (100 nm) source-drain contacts were deposited on channel layer which defined the channel length and width as 65 and 1000 μm, respectively.

5.3 Results and discussion

5.3.1 Characterization of copper oxide thin films

Figure 5.1 (a) shows the X-ray diffraction patterns of as-deposited Cu_2O and CuO thin films (RT Cu_2O and RT CuO). Thin films deposited at $O_2 = 1.3$ sccm and $O_2 = 3$ sccm showed XRD peaks corresponding to Cu_2O with orientation along (111), (200)) and CuO with orientation along (002) planes respectively. It indicates that at lower oxygen partial pressure copper

was at Cu^{1+} oxidation state (Cu_2O) and on increasing the oxygen partial pressure, Cu^{1+} was oxidised to Cu^{2+} (CuO).

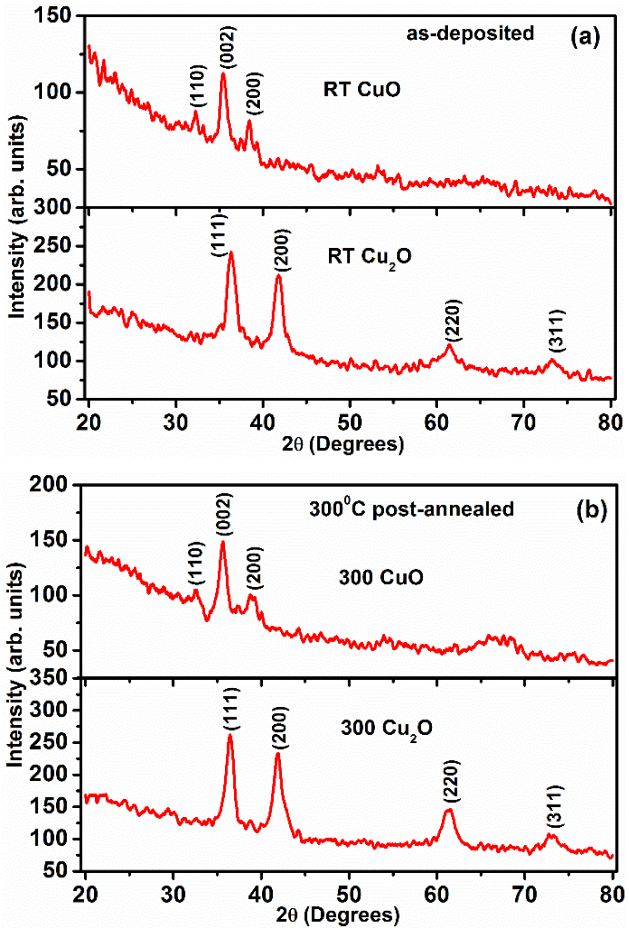

Figure 5.1. X-ray diffraction patterns of Cu_2O and CuO thin films (a) as-deposited (b) post-annealed at 300 °C for 30 minutes.

Further, as-deposited copper oxide films were post-annealed at 300 °C in air for 30 minutes, to improve the crystallinity. Figure 5.1 (b) shows

the X-ray diffraction patterns of 300 °C annealed Cu_2O and CuO thin films (300 Cu_2O and 300 CuO). The average crystallite size of the films was calculated using the Scherrer equation. The average crystallite size of RT CuO, RT Cu_2O, 300 CuO and 300 Cu_2O films was found to be 8, 9, 10 and 11 nm, respectively. The observed XRD peak intensities are moderately higher than that of as-deposited films which confirms the improvement in crystallinity due to post-annealing. Even though the crystal quality of the copper oxide films was improved, crystal phase was not affected by the post-annealing. Apart from the improvement in the crystallinity, mobility and transparency of the copper oxide films, which are crucial parameters for TFT performance were also increased on post-annealing treatment. The fabrication processes of thin film transistors are nowadays focused on low temperature annealing because of the recent developments in flexible electronics. So we limit the annealing temperature to comparatively low processing temperature.

The phase purity of Cu_2O and CuO films were confirmed using Raman spectroscopy and X-ray photoelectron spectroscopy (XPS). Raman spectroscopy is a sensitive probe for the identification of different oxides by utilizing the local atomic arrangement and their vibrations in oxide materials. The room temperature Raman scattering measurements on copper oxide thin films also provides the information about the presence of even lower content of undesired phases in the samples [211]. Raman spectra of as-deposited and 300 °C post-annealed films deposited at O_2 = 1.3 sccm and O_2 = 3 sccm (figure 5.2) shows the presence of prominent Raman peaks of Cu_2O and CuO films, respectively. In case of Cu_2O films, the strongest peak at 219 cm^{-1} was attributed to the second order overtones $2\Gamma_{12}$. The other two weaker peaks at 150 cm^{-1} and 628 cm^{-1} correspond to

Γ_{15} oxygen vacancies (LO) and the red-allowed mode $\Gamma_{15}^{(2)}$ (TO) corresponds to the phonon vibrations of Cu_2O [212], respectively. The Raman spectrum of CuO thin films also shows the characteristics peaks of CuO. Raman peak around 292 cm^{-1} (A_g mode) was found which is consistent with an earlier report on Raman spectra of CuO [213]. A broad peak observed in CuO samples around the 590 cm^{-1} can be attributed to the convolution of B_{2g} peak of CuO (631 cm^{-1}) with an undesired phase of $Cu(OH)_2$ [214].

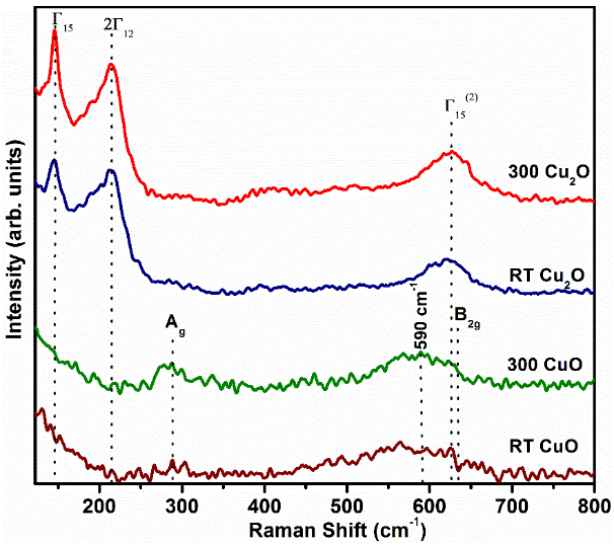

Figure 5.2. Raman spectra of as-deposited and 300 °C post-annealed Cu_2O and CuO thin films.

In order to further investigate the presence of any undesired phases, XPS study was conducted for post-annealed samples. The XPS core level spectra of 300 °C post-annealed copper oxide thin films grown at two different oxygen pressures (Ar/O_2 = 20/1.3 (sccm/sccm) and Ar/O_2 = 20/3 (sccm/sccm)) are shown in figure 5.3. It can be seen that at lower oxygen

partial pressure copper was at Cu^{1+} oxidation state (Cu_2O) having 932.92 eV as binding energy of Cu $2p_{3/2}$. Upon increasing the oxygen partial pressure, the binding energy of Cu $2p_{3/2}$ in the films increased from 932.92 to 933.05 eV due to the oxidation of Cu^{1+} to Cu^{2+} (figure 5.3 (a)). The binding energies of O1s were observed to be 530.92 eV for the Cu_2O films and 529.34 eV for CuO films (figure 5.3 (c)).

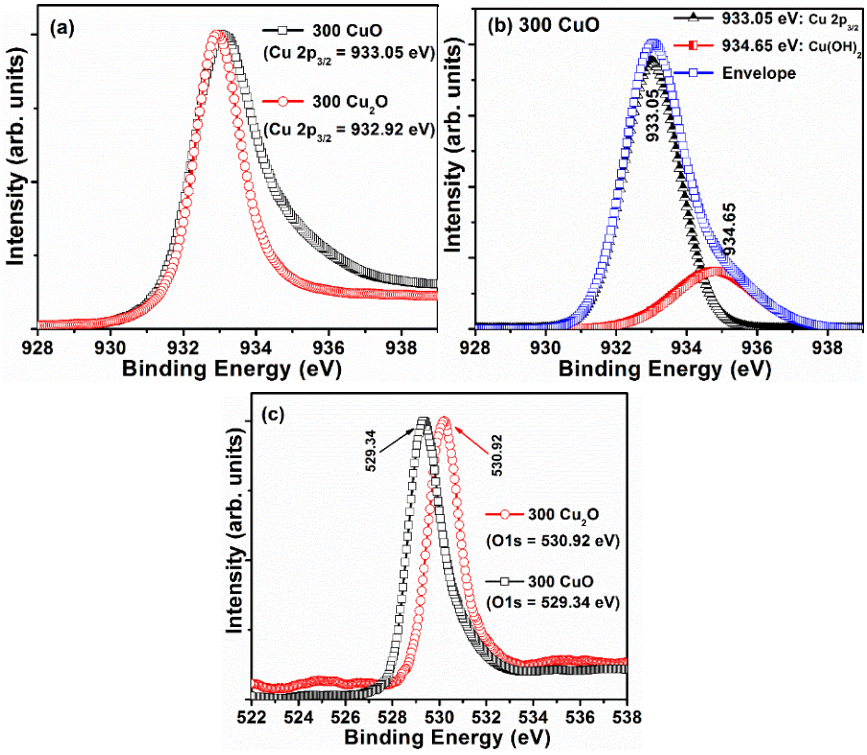

Figure 5.3. XPS spectra of 300 °C post-annealed Cu_2O and CuO thin films. (a) Cu $2p_{3/2}$ core levels (b) de-convolution of Cu $2p_{3/2}$ core level of CuO (c) O1s core levels.

On de-convolution, an additional peak at 934.65 eV was observed in the XPS spectra of the post-annealed CuO thin films, due to the presence of the copper hydroxide ($Cu(OH)_2$) phases on the surface of thin films (figure 5.3 (b)). These results indicated that, in the post-annealed Cu_2O films only one main peak of Cu^{1+} is present but in CuO films both Cu^{2+} and copper hydroxide ($Cu(OH)_2$) phases are observed. The adsorbed hydroxide phase present in CuO film is a surface species and it will affect the surface properties of the annealed sample.

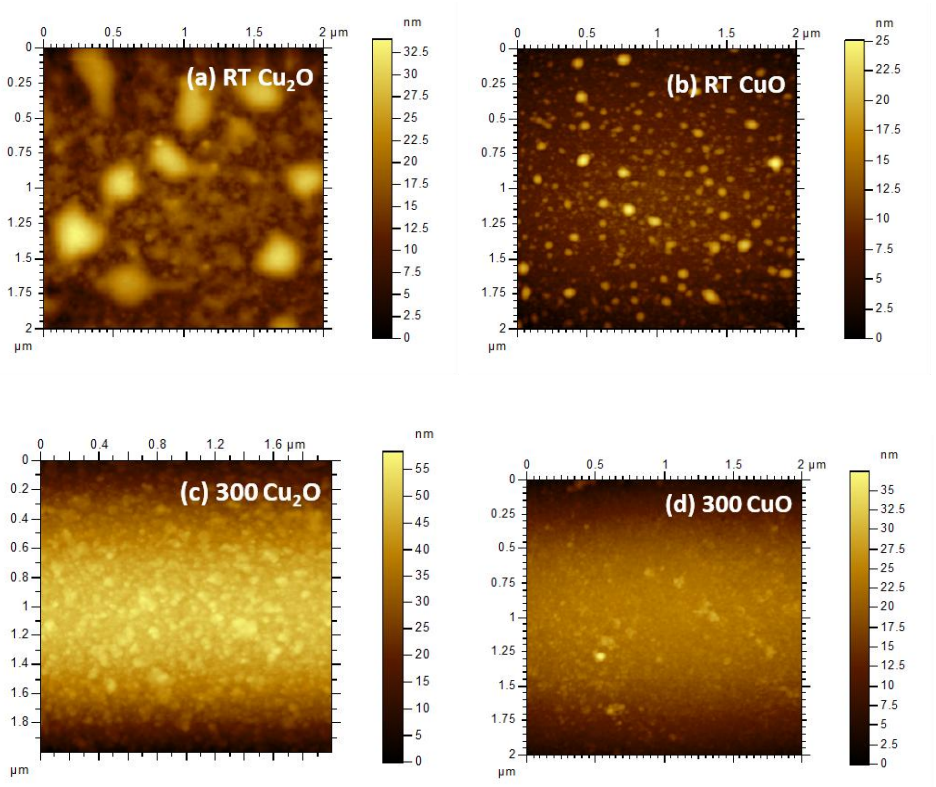

Figure 5.4. AFM images of Cu_2O and CuO thin films: as-deposited (a and b) and post-annealed (c and d).

The surface morphology and roughness of the thin films were examined by atomic force microscopy (AFM). Figure 5.4 illustrates two dimensional AFM images for the as-deposited and 300 °C annealed copper oxide thin films. The as-deposited thin films were composed of very fine grains and showed a very smooth surface with root mean square (RMS) roughness of 5.17 nm and 3.07 nm for Cu_2O and CuO thin films respectively. The average grain size and roughness were found to increase on post-deposition annealing. The post-annealed thin films showed an increased RMS roughness of 13.4 nm and 6.09 nm for Cu_2O and CuO thin films respectively. This indicates an improvement in the crystallinity of the films and a significant increase in the roughness suggests a decrease in the surface smoothness [215,216].

From figure 5.5 (a) it can be seen that the average transmittance of all the as-deposited films are >50 % and on post-annealing the value increased due to the improvement in crystallinity of thin films. The bandgap value of as-deposited Cu_2O and CuO thin films were 2.36 eV and 1.55 eV, respectively. After post-annealing of Cu_2O and CuO thin films, the bandgap values were increased to 2.43 eV and 1.74 eV, respectively (figure 5.5 (b)). To have a deeper insight into the subgap states near the band edge, we followed the Urbach's rule wherein the optical absorption edge exhibits an exponential behavior such as, $\propto (h\nu) = \propto_0 exp[(h\nu - E_0)/E_u]$, especially for semiconducting and alkali halides. Where E_u is called as Urbach energy and $\propto_0$ and E_0 are material parameters. Generally, the subgap absorption can be estimated using optical absorption techniques with higher resolution such as photothermal deflection spectroscopy (PDS) or constant photocurrent method (CPM) [217]. The spectra of subgap absorption are mainly divided into two, band

to tail and band to deep defect states. The later one can be estimated only using a higher resolution technique such as PDS because the photon energy involved and the absorption coefficient values are very small. But we have focused on the former one, the band-tail structure, which involves higher value of absorption coefficient and its dependence on deviation from the ideal crystal stoichiometry can be estimated using simple absorption/transmission spectroscopy. The plot of log α vs hν (figure 5.5 (c)), reveals the existence of sub band absorption below the band edge (tail states absorption) in the copper oxide thin films [65]. The tail states extending in the band gap is termed as the Urbach tail and the energy associated with the tail is called the Urbach energy. The smaller slope of Urbach tail is a measure of the large amount of localized trap states available in the optical bandgap. The slopes obtained for the CuO films are smaller than that of Cu_2O films and it confirms higher number of localized trap states existing in the CuO films than Cu_2O films. The tail states act as trap states for the charge carriers in thin films obstructing the charge transport in thin films. The considerable absorptions in the subgap region of Cu_2O (i.e., $E_g < 2.43$ eV) and CuO (i.e., $E_g < 1.74$ eV) thin films confirms the presence of high-density subgap defect states. The subgap defect absorption is reduced on post-annealing for both Cu_2O and CuO films. Moreover, the overall tail states absorption of Cu_2O films are lesser than that of CuO films which suggests the higher value of mobility in the case of Cu_2O thin films.

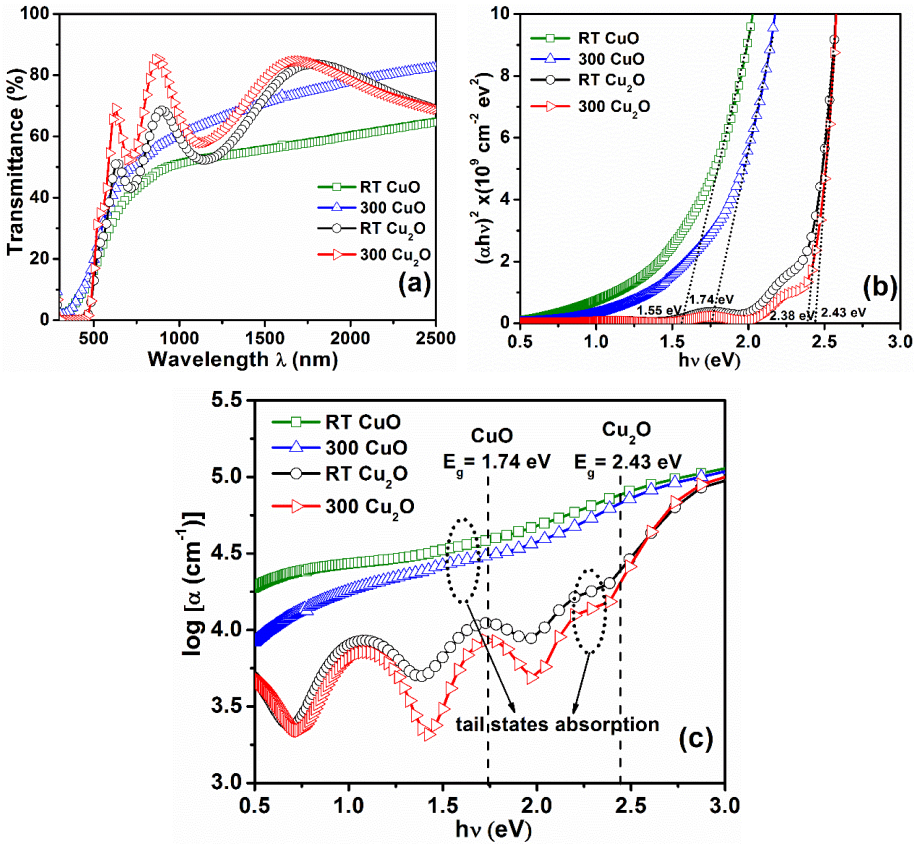

Figure 5.5 (a) Transmittance spectra of as-deposited and post-annealed copper oxide thin films. (b) Relationship of hυ vs $(\alpha h\upsilon)^2$ for the copper oxide thin films and (c) log α vs hυ plot for copper oxide thin films.

The Hall effect measurements at room temperature shows that all the copper oxide thin films are p-type and the hall mobility of copper oxide films was increased on post-annealing. The electrical parameters of as-deposited and post-annealed copper oxide films are listed in table 5.1. The lower values of Hall mobility, observed in the present study, can be

attributed to the large amount of subgap states present in the films as seen in the absorption spectra. The mobility values of the thin films were increased slightly after post-deposition annealing and it was a direct evidence for the reduction in the subgap states [218].

Table 5.1. Electrical parameters of as-deposited and post-annealed copper oxide films.

	Mobility (cm^2/Vs)	Hole concentration (cm^{-3})
Cu_2O RT	1.17	1.36×10^{17}
Cu_2O 300	2.03	1.07×10^{17}
CuO RT	0.22	3.30×10^{17}
CuO 300	1.20	6.03×10^{17}

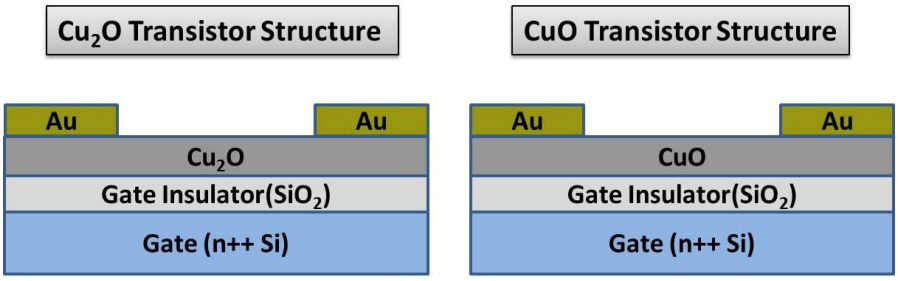

Figure 5.6. Schematic structure of Cu_2O and CuO TFTs.

5.3.2 Fabrication of copper oxide thin film transistor

The p-type Cu_2O and CuO TFTs were fabricated in the inverted staggered (top contact) structure (figure 5.6). Heavily doped n-type silicon wafer was used as the gate electrode, with 100 nm thick thermally grown silicon dioxide serving as the gate dielectric. By using a shadow mask,

patterned channel layer having thickness of 15 nm was deposited on silicon dioxide layer. After deposition, the channel layer was annealed at 300 °C for 30 minutes under ambient conditions. Shadow mask was used to deposit Au (100 nm) source-drain contacts thereby defining the channel length and width as 65 and 1000 µm, respectively.

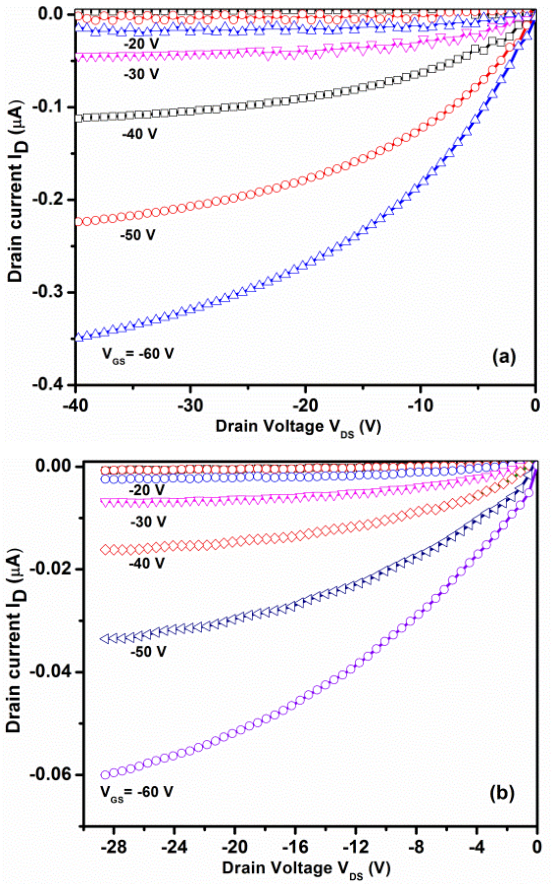

Figure 5.7. Output characteristics of (a) Cu_2O and (b) CuO TFTs (V_{GS} = 0 to -60 V in steps of 10 V).

Figure 5.7 shows the output characteristics of the fabricated Cu_2O and CuO TFTs, which display predictable electrical characteristics of p-hannel thin film transistors. The hole mobilities of p-type semiconductors are generally low when compared to the electron mobilities in n-type semiconductors [210]. Because of the large number of trap states present in the channel and interface regions, the reports on high performance copper oxide TFTs are only few [209]. The mobility values of Cu_2O and CuO TFTs in the present work are 5.20×10^{-4} $cm^2V^{-1}s^{-1}$ and 2.33×10^{-4} $cm^2V^{-1}s^{-1}$, respectively. The maximum value of drain current of Cu_2O TFT is one order higher than that of CuO TFT at fixed gate-source and drain-source voltages. This observation in current values is in agreement with the higher mobility value of Cu_2O TFT than that of CuO TFT. This is due to the higher crystalline nature of Cu_2O films than CuO films. Also, it is evident from the AFM images that post-annealing substantially increases the roughness value of the film. The Cu_2O samples have higher roughness value indicating improved crystallinity of Cu_2O films than CuO films. The threshold voltages for both TFTs are around 26 V and the high value of threshold voltage suggests larger number of trap states in the channel layer [124]. The sub-threshold swing of Cu_2O and CuO TFTs are 4.2 and 8 V/dec, respectively. When comparing with Cu_2O thin films there exists large number of subgap states in the CuO thin films as observed in the absorption spectra (figure 5.5 (c)). It could be the reason for the poor performance of CuO TFT that leads to the large value of sub-threshold swing of CuO TFT. Also from the XPS spectra of CuO thin films presence of the surface states in the post-annealed samples is observed which can also affect the overall performance of CuO TFT.

The poor value of sub-threshold swing, threshold voltage and field effect mobility of the TFT measured can be attributed to the charge trap density at copper oxide/dielectric interface as well as traps inside the bulk copper oxide. The interfacial trap density at the semiconductor/dielectric interface N_{SS} can be calculated by the equation [219],

$$N_{SS} = \left[\frac{SS\ \log(e)}{kT/q} - 1\right].\ \frac{C_i}{q} \qquad (5.1)$$

where q is the electronic charge, SS is the sub-threshold swing, in V/dec, k is the Boltzmann's constant, and C_i is the capacitance/area of the gate dielectric.

Table 5.2. The parameters of Cu_2O and CuO thin film transistors.

TFT	V_T (V)	Mobility (cm^2/Vs)	SS (V/dec)	N_{SS} ($cm^{-2}eV^{-1}$)
Cu_2O 300	26	5.20×10^{-4}	4.2	1.50×10^{13}
CuO 300	26	2.33×10^{-4}	8.0	2.87×10^{13}

Table 5.2 shows the parameters of Cu_2O and CuO thin film transistors. The extracted N_{SS} values of Cu_2O and CuO are 1.50×10^{13} and 2.87×10^{13} cm^{-2} eV^{-1}, respectively and in effect they are much higher than that observed in amorphous silicon TFTs which is around 10^{12} cm^{-2} eV^{-1} [219].

5.3.3 Analysis of density of states

The estimation of subgap DOS is very important and essential since they strongly affect the electrical properties of thin film transistors (TFTs). A thorough knowledge about the origin and density of these

subgap levels is therefore imperative in order to put into action the preventative measures both during fabrication and operation of the device, to result in an improved performance. The fundamental principles of device physics can be used for the easy determination of subgap DOS [123,125].

The DOS in the band gap of Cu_2O and CuO channel layers was calculated by analyzing the temperature dependent transfer characteristics of TFTs (figure 5.8 (a) and (b)). The measurements were carried out in the temperature range between 300 K and 340 K. A thermally activated Arrhenius like behavior was observed where the drain currents increased with increase in temperature.

The observed positive shift of transfer characteristics with increasing temperature was due to the releasing of trapped carriers from the defect induced traps. The value of $E_{A,}$ which is the energy difference between the Fermi level and the transport band edge, can be found for each gate voltage. Arrhenius plot for each gate voltage drawn between ln I_D and 1000/*T* enables the determination of activation energy.

The slope of Arrhenius plot gives the value of E_A for each gate voltage and it can be plotted as a function of gate voltage (figure 5.9 (a)). In multiple trapping and thermal release model (MTR), E_A is defined as the energy required to release a trapped carrier from the trap inside the semiconductor to the conduction band [127]. By this model the density of defect induced traps can be found from the derivative of the activation energy with respect to gate voltage. A slow variation of E_A with gate voltage indicates a large value of DOS whereas a fast change indicates a low value of DOS in the bandgap region of the channel material of the TFT [170,196].

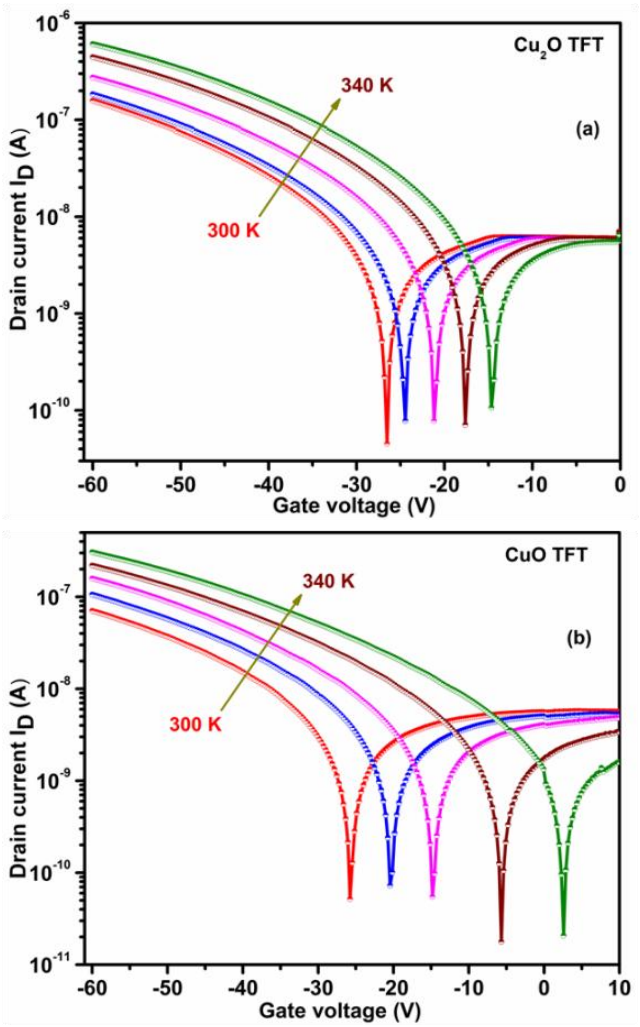

Figure 5.8. Transfer characteristics of (a) Cu_2O and (b) CuO TFTs measured at different temperatures.

For Cu_2O and CuO TFTs, an exponential decay of E_A with gate voltage was observed which indicates a low value of DOS. The DOS, [N(E)] inside the bandgap of active layer can be written as [125],

$$N(E) = \frac{C_i}{q} \frac{1}{t\frac{dE_A}{dV_{GS}}} \tag{5.2}$$

Where E is the energy measured from the valence band edge, C_i the capacity of the insulator per unit area and q the elementary charge. In this work, a channel thickness (t) of 15 nm has been considered for the calculation of DOS.

Figure 5.9 (a) shows the variation of E_A with gate bias voltages of Cu_2O and CuO TFTs. The exponential decrease in the activation energy with gate voltage was a clear indication of quick movement of Fermi level toward the band edge. From figure 5.9 (b), the exponential region of the DOS can be assumed as a band tail of localised states induced by oxygen vacancies in the materials. As shown in figure 5.9 (b), the DOS distributions of both Cu_2O and CuO have a value of 5×10^{19} $cm^{-3}eV^{-1}$ near the bandedge. It was observed that the subgap states are exponentially decreasing inside the bandgap and CuO TFT shows higher subgap states than Cu_2O TFT. The high-density hole trap states in the CuO channel is one of the plausible reasons for the lower mobility in CuO TFT than Cu_2O TFT. A possible origin of these subgap states is due to the impurities or oxygen vacancies present in the CuO channel layer.

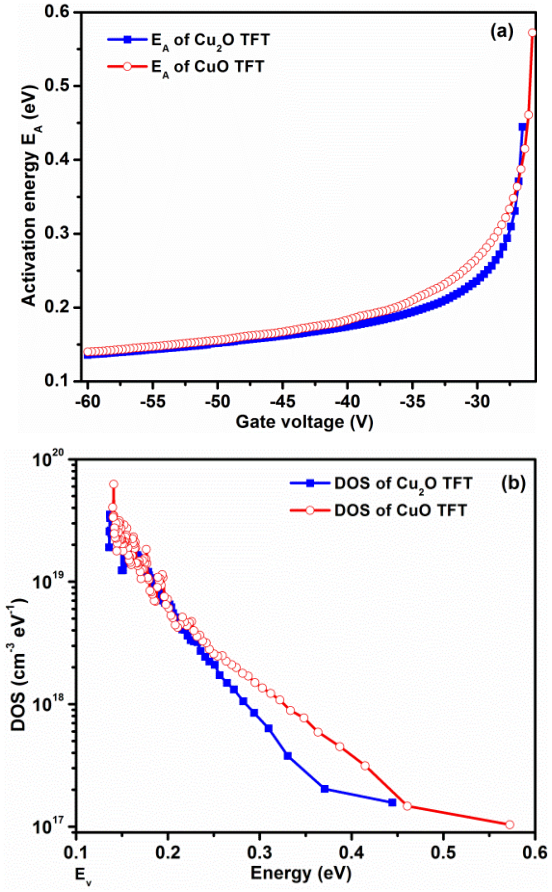

Figure 5.9. (a) Plot showing the dependence of E_A with gate voltage and (b) density of states in the gap of Cu_2O and CuO TFT calculated from the derivative of activation energy.

5.4 Conclusions

Transparent p-type semiconducting Cu_2O and CuO thin films were deposited using RF sputtering for the fabrication of thin film transistors. The phase purity of Cu_2O and CuO films were confirmed using XRD, Raman and XPS data. The optical absorption studies revealed the existence

of large number of subgap states inside CuO films than Cu_2O films. The post annealed films at 300 °C for 30 minutes showed better properties. Hence, these films were chosen for the fabrication of TFTs. The mobility values of bottom gate structured Cu_2O and CuO TFTs were 5.20×10^{-4} $cm^2V^{-1}s^{-1}$ and 2.33×10^{-4} $cm^2V^{-1}s^{-1}$, respectively. The poor values of sub-threshold swing, field effect mobility and large threshold voltage of the TFTs were due to the charge trap density at copper oxide/dielectric interface as well as defect induced trap states originated from the oxygen vacancies inside the bulk copper oxide. The extracted interfacial trap density values of Cu_2O and CuO are 1.50×10^{13} and 2.87×10^{13} cm^{-2} eV^{-1}, respectively and in effect they are much higher than that observed in amorphous silicon TFTs. The defect induced subgap DOS in fabricated copper oxide TFTs were investigated using temperature dependence of the drain currents. The high-density hole trap states in the CuO channel was figured to be the possible reason for the lower mobility in CuO TFT than Cu_2O TFT.

Chapter 6

Complementary inverter circuits based on p-Cu_2O and n-ZTO thin film transistors

6.1 Introduction

Oxide semiconductors are the most sought after materials due to their processing versatility and intriguing structural and electronic properties. Also, they are open to a wide area of applications demanding films on large area, low processing temperature, flexibility and especially low cost [130,131]. Thin film transistor based complementary metal oxide semiconductor (CMOS) inverter is the basic component in the modern logic circuits and it enables fabrication of circuits with large area, high integration density and low power consumption [143,220,221]. These new applications raise the need of combining both p and n-types of semiconductors in circuit designs, which is a major challenge. Many research groups have already demonstrated comparatively high performance inverters with different p and n-type semiconductors [85,222,223]. The performances of the inverters are rather poor because of

the poor performance of p-type TFTs. Zinc tin oxide (ZTO) is the most popular n-type oxide semiconductor not only for its good electrical performance in TFTs but also for its environmental stability [224,225]. Moreover, copper oxide is a promising p-type oxide semiconductor which exhibits good electrical characteristics but not at par with ZTO which is a consequence of its lower mobility and higher threshold voltage [208,226]. A simpler solution to circumvent the differences in the performance of n and p-TFTs is to reduce channel resistance, either with wider or with shorter TFT channels. Following this notation, we have combined inverters with different W/L ratios in order to minimize differences in mobility and threshold voltage between the two types of semiconductors, subsequently attaining some tunable electric characteristics for inverters such as gain and noise margins. The p-channel Cu_2O and n-channel ZTO TFTs having an inverted-staggered bottom-gate structure was fabricated with a common channel length of 80 µm and channel width ranging from 900 µm up to 9900 µm.

6.2 Experimental results

The n type a-ZTO and p-type Cu_2O TFTs were fabricated by radio frequency (RF) magnetron sputtering at room temperature with the bottom gate structure. The a-ZTO and Cu_2O channel layers were deposited on SiO_2 (100 nm)/n-type Si (heavily doped) substrate using ZTO (Zn:Sn ratio 2:1) and Cu metallic targets, respectively. The sputtering was carried out at a working pressure of 5×10^{-3} mbar and the constant pressure was achieved by controlled mixing of O_2 and Ar gases (for the deposition of ZTO and Cu_2O, the Ar to O_2 flow rate ratios were 20:0 and 20:1.3, respectively). Initially, a 50 nm thick layer of Cu_2O was deposited through a shadow mask

at a power of 50 W. Then, a 100 nm thick layer of ZTO was deposited at 50 W using another shadow mask. After deposition, the ZTO and Cu_2O films were post-annealed for 30 minutes at 300 °C. Finally, gold source and drain electrodes having a thickness of 100 nm were deposited through another shadow mask. The set of masks allowed for the fabrication of 4 different inverters on the same substrate, with a common channel length of 80 µm and channel width ranging from 900 µm up to 9900 µm. Since channel length was constant, the term aspect ratio denotes the ratio between p-type and n-type channel width (W_p/W_n). In the present work these aspect ratios were: 11, 2, 0.47 and 0.091 and a schematic representation of inverters are shown in figure 6.2. Electrical characterisations were carried out using Keithley SCS 4200 semiconductor parameter analyzer at room temperature under dark conditions.

The static transfer characteristics of Cu_2O and ZTO TFTs with different W/L ratios are shown in figure 6.1(a) and 6.1(b), respectively. The well-known relation connecting the saturation current and the mobility are as follows: $I_D = \frac{1}{2}\mu C_i \frac{W}{L}(V_{GS} - V_T)^2$ where µ is the average mobility of the carriers in the channel layer, C_i is the capacitance of the insulator per unit area, W is the channel width, L is the channel length, V_{GS} is the gate-source voltage, V_{DS} is the drain-source voltage and V_T is the threshold voltage [178]. The V_T is the gate voltage at which a conducting channel formed at the semiconductor/channel interface and a significant current starts to flow between the source and drain electrode. The charge carrier transport effectiveness of channel layer can be inferred from the mobility value and it depends on device configuration and the various scattering mechanisms due to defect states in the channel layer. Usually the plot of

$I_D^{1/2}$ versus V_{GS} was used to obtain the values of mobility and threshold voltages [208]. Table 6.1 shows the extracted parameters of Cu_2O and ZTO TFTs.

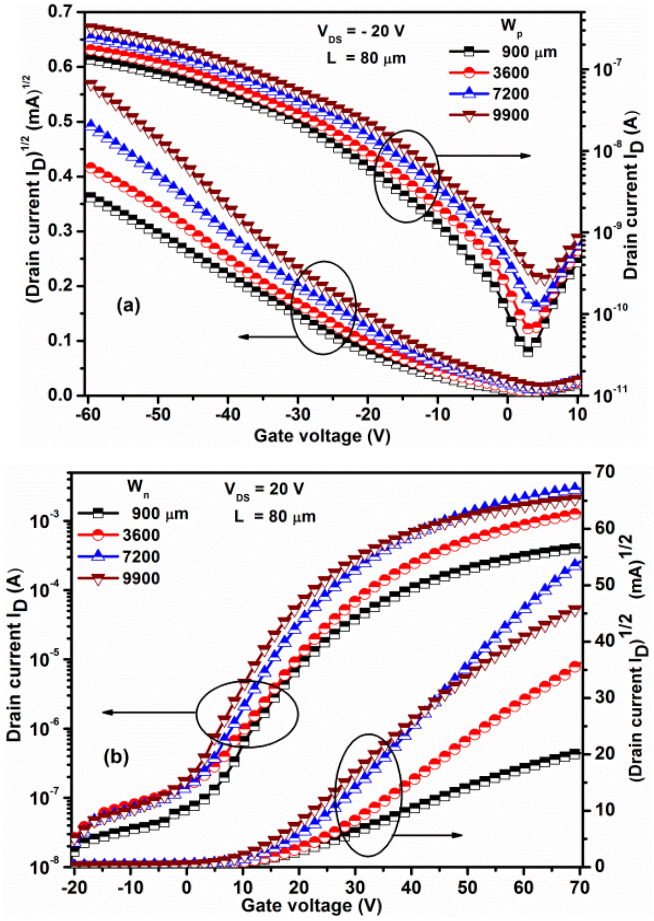

Figure 6.1. Transfer characteristics of the (a) Cu_2O and (b) ZTO TFTs having various channel width.

The large number of defect induced trap states in the Cu_2O channel layer particularly leads to lower field-effect mobility [73]. But, in the case

of ZTO TFT, the extracted mobility was three orders higher than the Cu_2O TFT. The n-type ZTO channel layer leads to high mobility than p-type Cu_2O mainly due to fewer number of defect induced trap states in the ZTO channel layer [73,203]. The switching performance of TFT was evaluated through the sub-threshold swing (SS) value, i.e., lower SS value indicates better performance and it was defined as the inverse of sub-threshold slope. The poor value of V_T and sub-threshold swing (SS) of Cu_2O TFT was due to the existence of significant trap states at the semiconductor/gate dielectric interface.

Table 6.1. Electrical parameters of the Cu_2O and ZTO TFTs having various channel width.

W (µm)	**Cu_2O mobility (cm^2/Vs)**	**V_T (V)**	**SS (V/dec)**	**ZTO mobility (cm^2/Vs)**	**V_T (V)**	**SS (V/dec)**
900	2.80×10^{-4}	-30	7.31	6.97×10^{-1}	14.35	9.43
3600	1.32×10^{-4}	-30	7.12	6.43×10^{-1}	18.3	7.50
7200	9.68×10^{-5}	-29.4	6.38	6.83×10^{-1}	16.5	7.17
9900	6.35×10^{-5}	-30	8.48	2.96×10^{-1}	11	6.72

The complementary inverters with four different geometric aspect ratios were fabricated using top-contact configuration, as shown in figure 6.2(a). The geometric aspect ratios are defined as the width-to-length ratio of p-TFT divided by the width-to-length ratio of n-TFT $[(W_p/L_p)/(W_n/L_n)]$. The channel length was fixed at 80 µm and channel widths were varied from 900, 3600, 7200 and 9900 µm for each inverter so that the calculated geometric aspect ratios were 11, 2, 0.47 and 0.091, respectively. The figure 6.2(b) and 6.2 (c) shows the schematic structure and equivalent circuit diagram of inverter having geometric aspect ratio of 2, respectively.

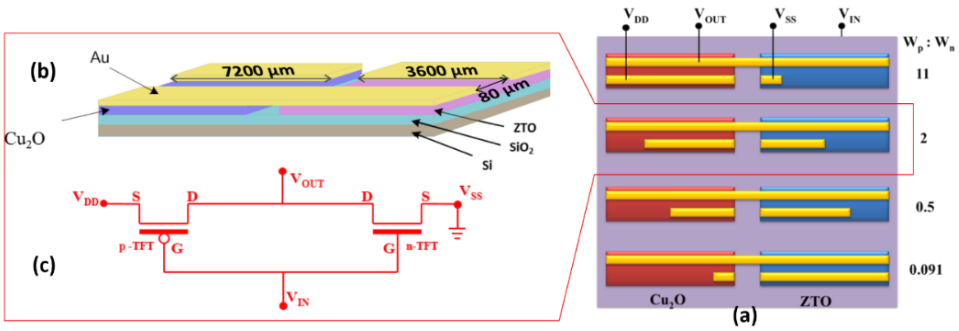

Figure 6.2. (a) Schematic of inverters with four different geometric aspect ratios, (b) the schematic structure and (c) equivalent circuit diagram of inverter having geometric aspect ratio of 2.

The basic functionality of an inverter is to generate an opposite logic level of its input V_{IN} at its output V_{OUT}. Figure 6.3(a) and (b) shows the plot of V_{OUT} as a function of V_{IN} (Voltage transfer characteristics- VTC) and plot of voltage gain (dV_{OUT}/dV_{IN}) of different inverters with different geometric aspect ratios operated at V_{DD} = 20 V respectively. The voltage gain increased with aspect ratio and reached a maximum value of 4.2 for an aspect ratio of 2 (W_p:W_n = 7200/3600). It was observed that the p-type TFT with W_p = 7200 had a lower SS value of 6.38 V/dec. It means that the voltage gain is dependent on the SS value of p-type TFTs [142]. Upon further increasing the aspect ratio to 11, the gain decreased to 3.04 because of the poor performance of the constituent p and n-type TFTs having width W_p= 9900 µm and W_n= 900 µm respectively. In those two TFTs, only fewer number of traps states exist in the channel layer/insulator interface and hence the observed SS values of those two TFTs are relatively lower when compared to other TFTs. The measured voltage gain value is comparatively small when compared with other reported Cu_2O-IGZO CMOS inverter because of poor SS value and on-off value of TFTs [206].

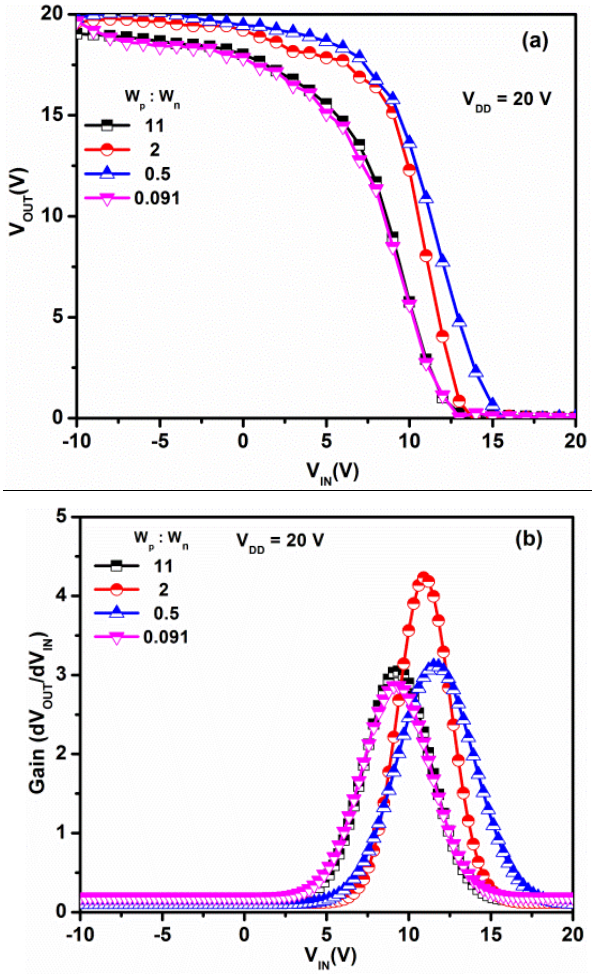

Figure 6.3 (a). The VTC and (b) gain (dV_{OUT}/dV_{IN}) of different inverters with different geometric aspect ratios operated at V_{DD}= 20 V.

The important parameters such as noise margin high (N_{MH} = V_{OH}-V_{IH}) and noise margin low (N_{ML} = V_{OL}-V_{IL}) can be calculated from the VTC curve and tabulated in the table 6.2. Here, the voltage V_{IH} and V_{IL} are the input voltages in the VTC curve in which the slope of VTC is equal to

-1. The voltages V_{OL} and V_{OH} are the output voltage corresponding to the V_{IH} and V_{IL}, respectively. From the table, it can be shown that inverter having a geometric aspect ratio of 2 gave better voltage gain and noise margin values. For a V_{DD} = 20 V, the N_{MH} and N_{ML} values are 7 V and 6.5 V respectively. Ideally the noise margin values should be $V_{DD}/2$. Moreover, those values of gain and noise margin can be further improved by changing W/L ratios and threshold voltages of individual TFTs [207].

Table 6.2 The switching parameters of different inverters with different geometric aspect ratios.

Wp:Wn	**Gain**	**NM_L (V)**	**NM_H (V)**
11	3.04	5	6
2	4.2	7	6.5
0.5	3.1	8	4.8
0.091	2.8	5	6.6

The inverter having the geometric aspect ratio of 2 was further characterized by changing the V_{DD} voltages. Figure 6.4 (a) shows the VTC curve of inverter by varying the V_{DD} voltages. From the figure 6.4 (b), it can be seen that the gain values are increased with increasing V_{DD} voltages. There was a small shift in the peak position corresponding to the maximum gain values with increasing V_{DD} voltages because of the occurrence of charge trapping in the channel/dielectric interface [224].

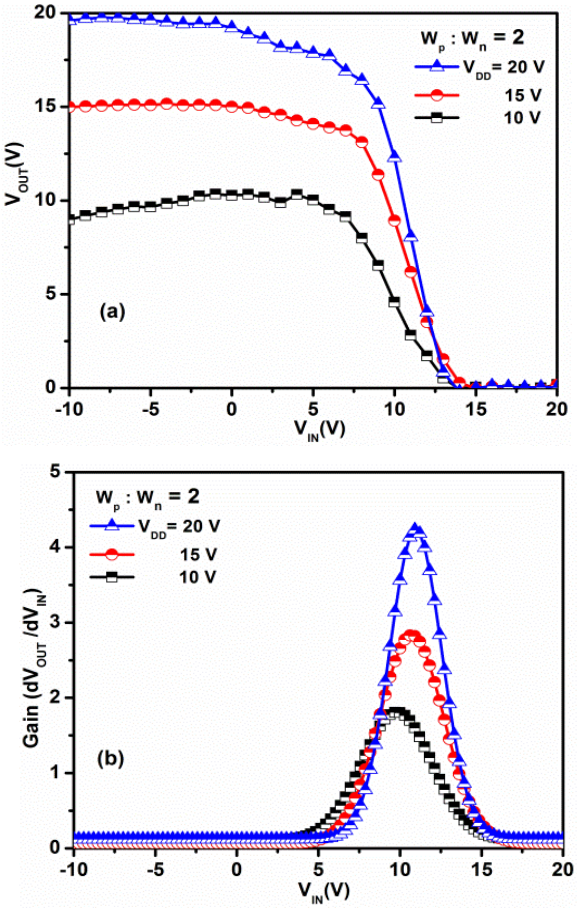

Figure 6.4. (a) The VTC and (b) gain (dV_{OUT}/dV_{IN}) of inverter having the geometric aspect ratio of 2 with different V_{DD} voltages.

6.3 Conclusions

In conclusion, we have fabricated the complementary metal oxide inverter with ZTO and Cu_2O TFTs as n and p-channel TFTs respectively. We have fabricated inverters with different geometric aspect ratios in order to minimize differences in mobility and threshold voltage between the two

types of TFTs, thus getting also some tunable electric characteristics for inverters such as gain and noise margins. The voltage gain increases with aspect ratio and reached a maximum value of 4.2 for an aspect ratio of 2. The inverter parameter can be further improved by changing W/L ratios and threshold voltages of individual TFTs.

Chapter 7

Summary and scope for further study

7.1 Summary of the present study

Transparent electronics is developing as one of the most hopeful technologies for future electronic products; as it delivers an innovative advancement in the light weight, transparent and flexible electronic devices. The next generation electronics will be based on these transparent materials as they meet the demands and requirements of the present day technology. The transparent electronics attracted more attention after the revolutionized invention of transparent-conducting materials such as ITO, SnO_2 and ZnO. These transparent conducting oxides (TCOs) are commonly used in the transparent window electrodes and circuit interconnections of modern electronic devices. The material engineering idea of TCO gave a proper understanding of the conduction mechanism of such materials and also helped to tune the electrical conductivity of TCO. The tuning of conductivity enables development of novel TCOs as active material in the field effect devices such as thin film transistors (TFT). Semiconductors that

can be used as an active material having both transparency and controlled electrical conductivity is called transparent semiconducting oxides (TSOs). The collective use of TCO and TSO enables the development of fully transparent thin film transistors (TTFTs).

The present work focused on the fabrication of organic and inorganic semiconductor TFTs for the development of complementary metal oxide semiconductor inverters. In active channel materials of TFTs, localized states induced by defects or impurities are distributed in the band gap. Therefore the detailed study of the distributions of localized states in the band gap leads to the exploration of charge transport mechanism in the semiconductor. Considering that the subgap density of states (DOS) strongly affects the electrical properties in the thin film transistors (TFTs) with disordered materials, the knowledge about the charge transport mechanism and DOS is essential not only for the fundamental understanding of the device operation but also for improving the device performances. The DOS was determined from the temperature dependent transfer characteristics of TFT following the Multiple Trapping and Releasing (MTR) model.

The organic thin film transistors (OTFTs) with both p-type and n-type channel layers were fabricated using the inverted staggered (top contact) structure by thermal vapor deposition on Si/SiO_2 substrate. Pentacene and N,N'-Dioctyl-3,4,9,10-perylenedicarboximide (PTCDI-C8) were used as channel layers for the fabrications of p-type and n-type OTFTs, respectively. A comparative study on the degradation and DOS of p-type and n-type organic semiconductors has also been carried out. The DOS measurements revealed that a level with defect density of 10^{20} cm^{-3} was formed only in PTCDI C8 layer on exposure to air. It was also inferred

that the electrical charge transport is strongly affected by the oxygen traps in the n-type organic materials and hence p-type organic materials are stable than n-type organic materials.

The bottom gate amorphous zinc tin oxide thin film transistors (a-ZTO TFTs) were fabricated by RF magnetron sputtering. The device stability with respect to ambient parameters was well studied by analyzing the variation of DOS in the active ZTO channel layer by MTR model. The deposition of passivation layer on top of the device reduced the aging effect and subsequently the stability of device under ambient condition was improved. Also, we investigated the stability of a-ZTO TFTs under negative gate bias illumination stress (NBIS) at various post-annealing temperatures. The oxygen vacancies present in the channel region created defect states and caused instability under NBIS. The study concluded that stability of the devices can be improved by depositing a passivation layer over the channel layer while the post annealing reduce oxygen vacancies and instabilities under NBIS.

The deposition of transparent p-type semiconducting Cu_2O and CuO thin films were carried out using RF sputtering and thin film transistors were fabricated in an inverted staggered structure by using post-annealed channel layer. The optical absorption studies revealed the existence of large number of subgap states inside CuO films than Cu_2O films. The mobility values of bottom gate structured Cu_2O and CuO TFTs were 5.20×10^{-4} $cm^2V^{-1}s^{-1}$ and 2.33×10^{-4} $cm^2V^{-1}s^{-1}$, respectively. The defect induced subgap DOS in fabricated copper oxide TFTs were investigated using temperature dependence of the drain currents. The high-density hole trap states in the CuO channel was figured to be the possible reason for the lower mobility in CuO TFT than Cu_2O TFT.

Copper oxide and zinc tin oxide complementary inverters were fabricated wherein both the p-type and n-type channels were deposited by RF magnetron sputtering. We have designed comparatively low voltage and high gain complementary inverters by combining a set of p-type copper oxide and n-type zinc tin oxide thin film transistors with different aspect ratios. The voltage gain was found to increase with aspect ratio and a maximum value of 4.2 was reached for an aspect ratio of 2.

7.2 Scope for the further study

In terms of future electronic applications there are several important issues that have to be addressed. In organic n-type TFT, the required mobility for the future flexible electronic applications have not been achieved till now. So the designing of new n-type organic TFTs with different channel materials and passivation layers are gaining intense research interest. The combination of both high performance p and n-type OTFT enables a breakthrough in the field of flexible electronics. In the case of inorganic TFTs, the operational stability of amorphous ZTO TFT under various environmental conditions has major concerns and overcoming these problems will help the widespread use of indium free ZTO TFT in future electronic industry. The instability of TFT arises from the trap states residing in the bandgap and fine tuning of the deposition conditions of ZTO channel layer can certainly improve device stability. The effect of passivation layer over the channel layer used for improving the device stability can also be a hot area of research, since a large number of possible insulator materials suitable as passivation layer needs to be explored in detail. The ZTO TFTs described here are fabricated at a post annealing temperature of 300 °C and when considering the flexible electronics, the

TFT has to be fabricated on a flexible plastic substrate at low temperature. So efforts towards developing low temperature fabrication technique has to be investigated.

The off current issue of p-type copper oxide TFT must be considered for the future studies because all the reported copper oxide TFTs are suffering from the large off current values. The copper oxide TFTs also show high sub-threshold swing values due to the existence of large number of traps inside the copper oxide channel layer. The deposition of defect free copper oxide thin films and fabrication of TFTs with lesser interfacial defect states between the insulator and channel layer will reduce the off current as well as sub-threshold swing. The relative low mobility of copper oxide TFT is a severe drawback and hence the CMOS design using copper oxide TFTs is very difficult. So improving the mobility has to be achieved by fundamental material engineering such as doping to get a proper orbital overlapping and band dispersion.

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