Microwave Plasma Assisted ALD Development for the Deposition of Gate Oxides & ALD of High-k Dielectrics

A thesis submitted to

Cochin University of Science and Technology

in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

by

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Cochin University of Science and Technology

November 2015

Microwave Plasma Assisted ALD Development for the Deposition of Gate Oxides & ALD of High-k Dielectrics

Ph.D. thesis in the field of Applied Physics

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Cover page illustration: Microwave plasma in homemade ALD system.

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Certificate

Certified that the thesis entitled ***" Microwave Plasma Assisted ALD Development for the Deposition of Gate Oxides & ALD of High-κ Dielectrics"*** submitted by ***Subin Thomas*** is an authentic record of research work carried out by him under my supervision at the ***Department of Instrumentation*** in partial fulfilment of the requirements for the award of degree of Doctor of Philosophy of ***Cochin University of Science and Technology*** and the work embodied in this thesis has not been included in any other thesis submitted for the award of any degree.

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This is to certify that the thesis entitled ***" Microwave Plasma Assisted ALD Development for the Deposition of Gate Oxides & ALD of High-κ Dielectrics"*** submitted by ***Subin Thomas*** has incorporated all the relevant corrections and modifications suggested by the audience during the pre-synopsis seminar and recommended by the Doctoral Committee.

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Declaration

I hereby declare that the work presented in the thesis entitled ***" Microwave Plasma Assisted ALD Development for the Deposition of Gate Oxides & ALD of High-κ Dielectrics"*** is based on the original work done by me under the guidance of ***Dr. K. Rajeev Kumar***, Associate Professor, ***Department of Instrumentation, Cochin University of Science and Technology***, Cochin- 682 022, India and has not been included in any other thesis submitted for the award of any degree.

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Preface

The semiconductor industry's urge towards faster, smaller and cheaper integrated circuits has lead the industry to smaller node devices. The integrated circuits that are now under volume production belong to 22 nm and 14 nm technology nodes. In 2007 the 45 nm technology came with the revolutionary high-κ/metal gate structure. 22 nm technology utilizes fully depleted tri-gate transistor structure. The 14 nm technology is a continuation of the 22 nm technology. Intel is using second generation tri-gate technology in 14 nm devices. After 14 nm, the semiconductor industry is expected to continue the scaling with 10 nm devices followed by 7 nm. Recently, IBM has announced successful production of 7 nm node test chips. This is the fashion how nanoelectronics industry is proceeding with its scaling trend.

For the present node of technologies selective deposition and selective removal of the materials are required. Atomic layer deposition and the atomic layer etching are the respective techniques used for selective deposition and selective removal. Atomic layer deposition still remains as a futuristic manufacturing approach that deposits materials and films in exact places. In addition to the nano/microelectronics industry, ALD is also widening its application areas and acceptance. The usage of ALD equipments in industry exhibits a diversification trend. With this trend, large area, batch processing, particle ALD and plasma enhanced like ALD equipments are becoming prominent in industrial applications. In this work, the development of an atomic layer deposition tool with microwave plasma capability is described, which is affordable even for lightly funded research labs.

The report starts with a brief introduction about the atomic layer deposition tool and its operational procedure. The importance of ALD in depositing high-κ dielectric thin films and the microelectronics scenario

with the role of high-κ materials is also briefed.

The design and fabrication of microwave plasma assisted atomic layer deposition system is explained in the second chapter. The components of the system and their functions are also mentioned. The system was optimized with deposition of Al_2O_3 thin films.

In the third chapter a detailed account of plasma assisted atomic layer deposition of Al_2O_3 thin films done at different substrate temperature, using two different ALD systems is presented. One is the home made ALD system and other one is a commercial ALD unit. The Al_2O_3 thin films were characterized as a gate dielectric candidate material. The physical properties were measured and analysed together with electrical ones. The electrical characterizations mainly include the oxide and interface charge studies.

Al_2O_3 thin films were prepared in the conventional thermal ALD mode also using the home made and commercial systems and a comparison of their properties is attempted. A detailed description of these studies is presented in chapter four.

Fifth chapter is about deposition and characterisation of $HfZrO_2$ thin films prepared with plasma assisted ALD. A trial was made to stabilise the tetragonal phase in $HfZrO_2$ thin films which helps to improve the dielectric constant. Further studies are required for establishing an optimized process. The work is summarised and a few notes on future possibilities are given in sixth chapter.

Acknowledgements

This thesis is a result of support and help from many people and most of them are beyond scientific aspects. First of all, I wish to thank my supervisor Dr. K. Rajeev Kumar for his numerous suggestions, great interest and his support through out my research period. His support during this period was never limited to our research assignments. I would also like to express my gratitude to Prof. M. K. Jayaraj for providing excellent resources of his lab at my disposal. I extend my thanks to Dr. Johney Issac, Prof. K. N. Madhusoodanan, Prof. Jacob Philip, and other faculty members of Department of Instrumentation. I am thankful to Prof. K. P. Vijayakumar for allowing me to avail the facilities of his lab.

This work would not have been complete without the support from Indian Nano electronics Users Programme & Center of Excellence in Nanoelectronics, IIT Bombay. I would like to mention specifically the support from Dr. Nageswari and Nayana Ramesh.

I want to thank a special person Savitha for her friendship and for careful reading of the entire manuscript to check for technical and grammatical correctness and for providing appropriate comments and corrections.

Many of our ideas regarding ALD system would not have realized without the insights and skills of A. V. Muraleedharan and Joshy V. G. and support from A. Kasmir and Shaji K. V. I am highly obliged to these people for their help.

I am also thankful to the technical and administrative staffs of our department Jose Jacob, Alekkutty P. M., Antony Ferdinand C. J., Maniram K. A., Mathew V. M., Prakash P., Rani, Fazil.P, Babu Varghese and all other staffs for their support as members of the Instrumentation department.

I am also very grateful to all my colleagues, especially, Soumya, Nisha R, Hasna, Abdul Rahman, Nissamudeen, Manjusha, Rakhi, Uma, Melby, Rahna, Lidia, Jayalakshmi and Nisha M. R for their friendship and for

many valuable suggestions.

Living at CUSAT was a real fun with a lot of friends. I like to mention a few names with thanks: Rajeshmon, Sasank kumar, Deepu, Shijeesh, Sajeesh, Priyesh, Nijo, Sanal, Arun, Vikas, Tharanath, Titu, Sreeroop, Aneesh, Sajan, Santhosh, Poornima, Rajesh C S, Vinod, Tina, Deepa, Rajesh Menon.

Financial support provided by the University Grants Commission through Maulana Azad National Fellowship is gratefully acknowledged.

Last but not least I would like to acknowledge my parents and siblings for loving support and patience during the research period. I can't replace my children's (Tom & Tessa) time that I have stolen for this thesis. The continuous support and encouragement from my wife Anu was the actual driving force which enabled me to complete this work. This work could not be completed without her support initially as a colleague and then as life partner.

By God's grace, let me thank all once again for their support to all my endeavours.

Contents

Abbreviations

AC	Alternating Current
ALD	Atomic Layer Deposition
ALE	Atomic Layer Epitaxy
ASTeX	Applied Science and Technoology Inc.
BE	Binding Energy
C-V	Capacitance Voltage
CAGR	Compound Annual Growth Rate
CET	Capacitance Equivalent Circuit
CMOS	Complementary Metal Oxide Semiconductor
CVD	Chemical Vapor Deposition
DC	Direct Current
DRAM	Dynamic Random Acess Memory
ECR	Electron Cyclotron Resonance
EOT	Equivalent Oxide Thickness
FESEM	Field Emission Scanning Electron Microscopy
FNS	First Negative System
FPS	First Positive System
G-V	Conductance Voltage
GPC	Growth Per Cycle
GXRD	Glancing Angle X-Ray Diffraction
HF	Hydrofluric Acid
IC	Integrated Circuit

IR	Infra Red
ITRS	International Technology Roadmap for Semiconductors
KE	Kinetic Energy
LPM	Liter Per Minute
MIM	Metal Insulator Metal
MIS	Metal Insulator Semiconductor
MOCVD	Metal Organic Chemical Vapor Deposition
MOS	Metal Oxide Semiconductor
MOScap	Metal Oxide Semiconductor capacitor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPALD	Microwave Plasma Assisted Atomic Layer Deposition
NIRIM	National Institute for research in Inorganic Materials
NMOS	N-type Metal Oxide Semiconductor
NTRS	National Technology Roadmap for Semiconductors
OES	Optical Emission Spectra
PALD	Plasma Assisted Atomic Layer Deposition
PBTI	Positive Bias Temperature Instability
PDA	Post Deposition Anneal
PVD	Physical Vapor Deposition
RCA	Radio Corporation of America
RF	Radio Frequency
RFALD	Radio Frequency Plasma Assisted Atomic Layer Deposition
RRAM	Resistive Random Acess Memory
SC1	Standard cleaning 1
SC2	Standard cleaning 2
SEM	Scanning Electron Microscopy
SPS	Second Positive System
TE	Transverse Electric
TMA	Trimethylaluminium
USSR	Union of Soviet Socialist Republics

UV	Ultra Violet
VUV	Vacuum Ultra Violet
XPS	X-ray Photoelectron Spectroscopy
XRD	X-Ray Diffraction
XRR	X-Ray Reflectivity

Chapter 1

ALD, high-k dielectrics and their role in microelectronic scaling

1.1 Introduction

Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) are the basic units of around 90% of the electronic devices that we are using today. Figure 1.1 shows the basic structure of a MOSFET, in which the Metal Oxide Semiconductor (MOS) part can be considered as the heart of the MOSFET. Metal Insulator Semiconductor (MIS) is the most correct terminology to represent this kind of devices. The conventionally used MOS terminology came from the silicon/silicon dioxide, semiconductor/insulator system which predominated for around five decades. This thesis deals with Atomic Layer Deposition (ALD) of oxide layers for MOSFET application and their characterizations. An atomic layer deposition system

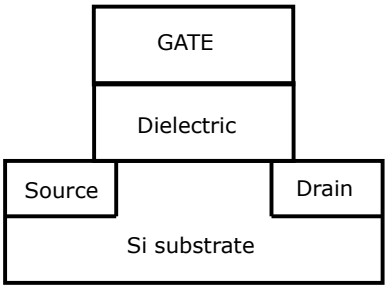

FIGURE 1.1: Schematic representation of a planar MOSFET

was developed for the deposition of oxide layers. Presently the major application area of ALD thin films is the semiconductor devices which are ever diminishing in their size. But its applications are never limited; it is still a fast developing method for thin film deposition.

1.2 Atomic layer deposition

Atomic layer deposition is a unique chemical process that yields ultra thin film coatings with exceptional conformality even on highly non-uniform and non-planar surfaces, often with subnanometer scale control of the coating thickness [1]. The history of ALD starts with independent works done by research group of Prof. Aleskovskii in USSR in 1960s and by Dr. Suntola and co workers in Finland in 1970s [2]. The most acknowledged history of ALD is the work done by Dr. Suntola's group and a patent based on their work in 1970s [3]. The involvement of complicated surface chemistry hindered the growth of ALD upto the early 1990s. In mid 1990s, the rapidly increased interest towards ALD was originated from the silicon based microelectronics [4]. Gradually ALD became a matured deposition technique and consequently several application areas were evolved. Now ALD can be used for developing complex shaped

nanostructures, surface modification of hybrid nanostructures with high aspect ratio [5] and in functionalizing nanomaterials [6]. High temperature lubricious oxide coating is an example of mechanical application of ALD [7]. In electronics, besides the CMOS, ALD is used in solar cell surface passivation, non-volatile memory devices and in energy storage [8, 9]. In essence, now ALD is the standard nanofilm deposition technique for various industries, including but not limited to electronics, optics, energy, chemical, mechanical and biological. Figure 1.2 shows the first commercial application that utilized ALD. It is the flight information board installed at Helsinki-Vantaa airport in 1983. The display board was manufactured by Lohja corp. ALD market is expected to grow at a CAGR (Compound Annual Growth Rate) of 36.10% from 2013 to 2018; for a comparison the expected CAGR for CVD is 11.43% and that for crystalline silicon solar cell market is 7.82% [10]. In semiconductor industry ALD market is going to overtake the broader equipment market. Figure 1.3 shows the spending by wafer fabs for equipments required for different nodes over the years and it is clear that the spending for smaller nodes becomes prominent in forthcoming years [11].

ALD can be considered as a cyclic repetition of self terminated gas-solid reactions implemented during the alternate pulsing of reactive precursors. This self terminative nature of the alternate chemical reactions plays a key role in imparting its peculiarities to ALD. The ALD of a binary material involves the following four steps:

(1) Self terminated reaction of the first gas phase precursor with the solid substrate.

(2) Purging out of the un-reacted precursor and reaction by-products either using an inert gas purge or by evacuation.

(3) A self terminated reaction of the second gas precursor over the presently saturated surface.

(4) Purge out of the reaction chamber.

FIGURE 1.2: The first commercial application utilizing ALD: The flight information display by Lohja Corp. Display Electronics Division installed at Helsinki-Vantaa airport in 1983. [12]

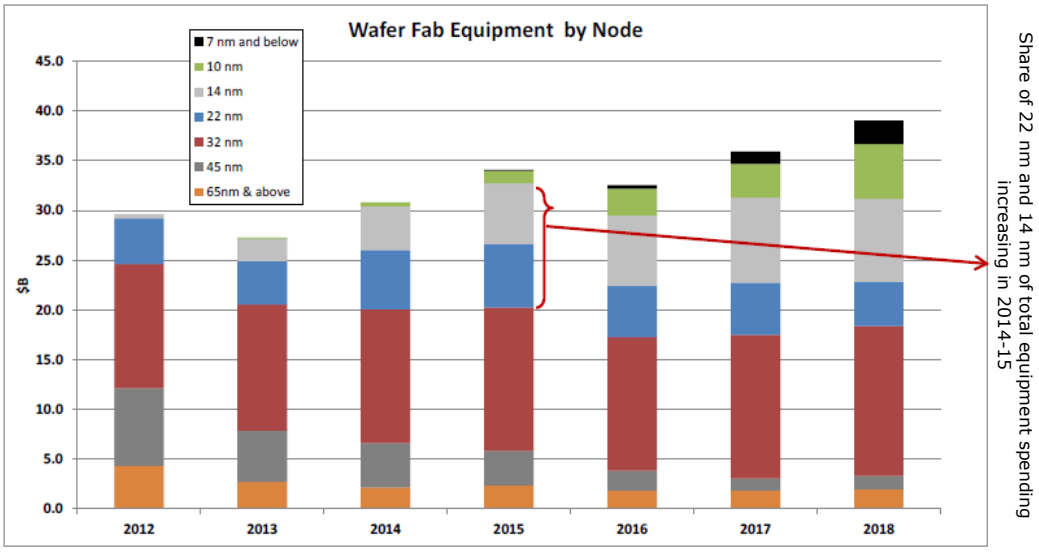

FIGURE 1.3: Spending by wafer fabs for equipments belongs to different nodes.

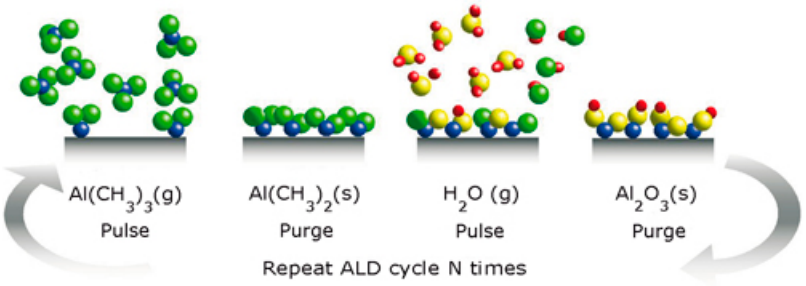

FIGURE 1.4: Schematic representation of different steps in ALD of Al_2O_3 using trimethylaluminum and water.

The different steps in a deposition cycle for ALD of Al_2O_3 using trimethylaluminum and water can be represented pictorially as shown in figure 1.4 [13]. During a precursor exposure step, the precursor molecules can either react or chemisorb on the substrate surface depending on the substrate and precursor chemistry. The extent of chemisorption or surface reaction would depend on the availability of surface states. The purging can expel the unwanted reaction possibilities. The amount of material deposited during each reaction cycle is known as Growth Per Cycle (GPC). In earlier days, the concept of ALD window was a common idea used to represent the surface saturating nature of ALD. The self limiting nature of ALD is usually attained by careful selection of the precursors and by control over the process temperature. The range of temperature for which the growth per cycle of the ALD process remains invariant with respect to temperature is known as the ALD window for that process. It is difficult to establish a clear ALD window for certain process like ternary ALD and processes involving organic/inorganic hybrid films and hence the representation is no far frequent. ALD can be considered as a modified version of Chemical Vapour Deposition (CVD). In CVD, gas phase reaction products are deposited on to a suitable substrate surface. Comparing to the CVD counterpart, the ALD processing window is often wide. Figure 1.5 shows the ALD window for a binary ALD process. If the temperature

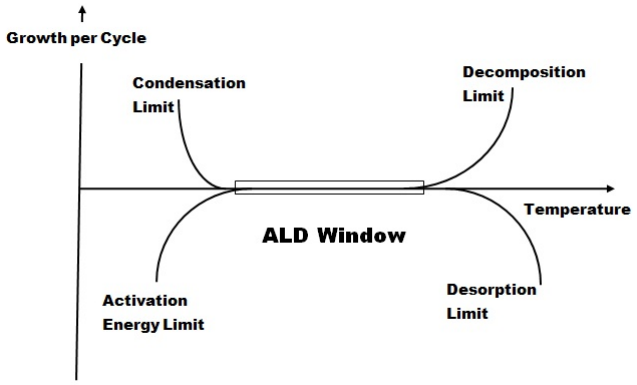

FIGURE 1.5: The concept of ALD window-The region independent of temperature.

is lower than the ALD window, then there is a chance of more than one monolayer deposition due to condensation of the precursors or there is a chance of forming un-saturated surface, because of insufficient precursor activation. At too high temperatures there are possibilities of precursor decomposition and desorption from the adsorbed ALD layer.

1.2.1 ALD precursors

Successful design of an ALD process will also depend on the selection of precursors. For each and every application level chemical selection, there should be some basic criteria like cost effectiveness, ease of production, eco-friendliness and non-toxicity. In addition to these basic requirements ALD precursors have some extra requirements as follows. An ALD precursor should be volatile and should have sufficient vapour pressure at a minimum temperature. A vapour pressure of atleast 0.1 Torr at the applicable maximum source temperature is preferred for research level systems [14]. Higher source temperature requirement will affect the cost effectiveness and a deficiency in vapour pressure will result in unsaturation. The precursor is expected to be aggressive in its reaction. Only an

aggressive reactant can complete the surface saturation in a short time. The precursor ligands should be small so that maximum surface states can participate in the reaction. The by products produced during the surface reactions should need to be un-reactive and should leave the deposition pristine.

1.2.2 ALD reactors

Initial ALD systems were CVD chambers with associated rapid switching valves. Due to large volume of CVD chambers this kind of ALD systems were highly inefficient as they cause large chemical loss and excess time. Together with the increasing application areas, the ALD technique has improved a lot and is now a matured process. Equipments and processes that operate in a near saturation mode by utilizing a little parasitic CVD are also available in the market now. This type of processes will provide better efficiency without compromising film quality [15]. The mere addition of rapid valves to a CVD process does not ensure an ALD process. The ALD process need to satisfy the stringent condition of surface saturated growth with a stabilized growth per cycle. A surface saturated growth still requires the control of substrate temperature and sufficient vapour pressure of the precursor in the chamber. The precursor chemistry also need to be good enough. Every ALD system should have (a) process and purge gas control unit, (b) deposition or reaction chamber and (c) exhaust unit. To get a uniform film thickness it is desirable to have a chamber design with uniform gas distribution throughout the deposition area. The precursor and purge gas control unit will handle the fast sequential pulsing of the precursors and carrier gas. Actual ALD reaction takes place on the substrate surface. The exhaust unit will manage the chamber pressure and gas flow control.

Several different classification schemes of atomic layer deposition systems

are mentioned in the literature. Based on purge out mechanism Reactors can be classified as evacuation type and flow type. Cross flow type and top injection type ALD systems differ in their gas feed direction to the ALD chamber. Based on the method of achieving saturation, ALD systems are classified as open, close, semi-open and semi-close.

1.2.3 Advantages and disadvantages

The possibilities opened up by ALD technology are unavoidable to any application area which requires some kind of thin films. Currently the major application areas for ALD are semiconductor industry, microelectronics, electroluminescent displays and magnetic recording heads. Still now, 40 years after the invention of ALD, the application areas are expanding further. Regardless of the industry or application, it seems that the same film properties that attracted industry and research over 40 years ago are still valid. The key features of ALD are so unique that it would be foolish for other industries not to look at ALD as a potential solution to existing problems or hurdles they face in the development of next generation devices [16].

As the growth per cycle is limited by the substrate surface, ALD film thickness depends only on the number of cycles. So the thickness control in ALD is simple and precise. Conformal is a major peculiarity of ALD and conformal coating is possible even in high aspect ratio structures. In Physical Vapor Deposition (PVD) methods conformality is restricted by line of sight deposition and in CVD an initial excess growth at the opening of a high aspect ratio structure can limit the further deposition to deep trenches. But ALD is a non line of sight method with self saturated deposition cycles.

Uniformity of the films is another direct consequence of self saturated

growth mechanism. A sufficient gas flow is the mandatory condition to get a uniform film. ALD is a deposition technique with large area and batch processing capability and excellent reproducibility.
In ALD the deposition of multilayer thin films is a straight forward process. Separate dosing of the precursors prevents gas phase reactions, which allows the use of highly reactive precursors and gives enough time for each reaction step to reach completion. This results in the deposition of pure films at relatively low temperatures. The ALD processing window is often wide, which makes the process insensitive to small changes in temperature and precursor flows and allows the processing of different materials to multilayer structures in a continuous process [17].

The major limitation of the ALD process is its slowness; only a fraction of a monolayer is deposited per cycle in many ALD processes. Typical reaction rates for lab reactors is usually <2 nm/minute [18]. Utilization of the large area and batch processing capabilities as well the thinness of the films required for many future applications together make the slowness insignificant. Another disadvantage of ALD is its stringent requirements on precursor chemistry, which is an active research area and the researchers have already developed precursors for most of the industrially relevant elements.

1.3 Prospects of plasma assisted ALD

Plasma assisted ALD (PALD) is an energy enhanced variant of conventional thermal ALD. In plasma assisted ALD, energetic species arising out of plasma is used as one of the precursor. Plasma can be considered as a collection of free charged particles moving randomly and the collection as a whole would be electrically neutral. Plasmas used in thin film

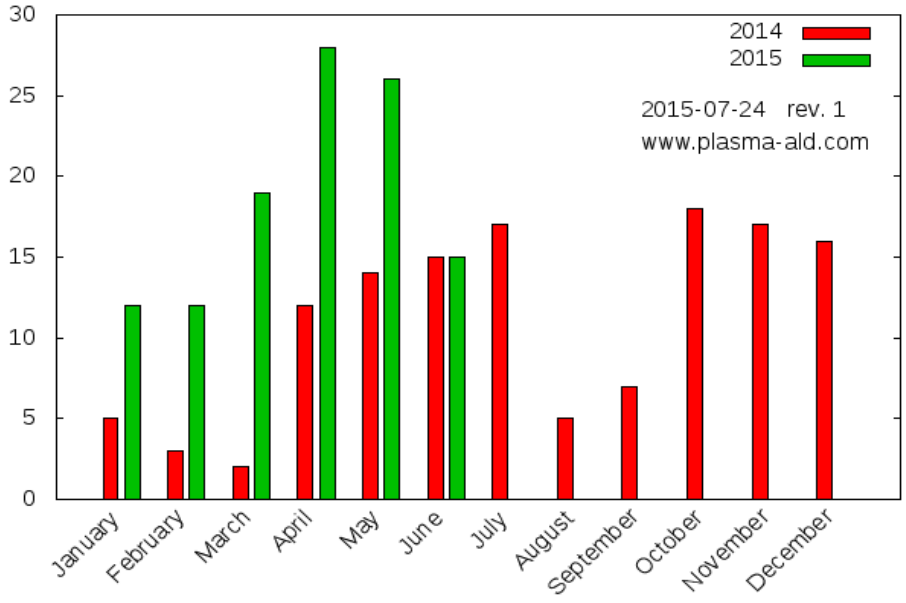

FIGURE 1.6: A histogram showing accepted plasma ALD publications in 2014 and first half of 2015 [20].

deposition and material processing are usually plasma discharges with a lower degree of ionization; weakly ionized plasma is a common term used to represent them. The plasma assisted ALD is also known as plasma enhanced ALD or radical enhanced ALD. Typical plasmas used during plasma assisted ALD are those generated by O_2, N_2 and H_2 reactant gases or combinations thereof. Such plasmas can replace ligand-exchange reactions typical of H_2O or NH_3 and they can be employed to deposit metal oxides, metal nitrides and metal films [19]. Figure 1.6 shows a histogram of plasma ALD publications accepted in 2014 and first half of 2015. In comparing with 2014 we can find a 120% growth for plasma ALD publications [20]. The commonly used plasmas in thin film and material processing are the Direct Coupled (DC) discharges, inductively coupled and capacitively coupled Radio Frequency (RF) plasma and Microwave

plasma with or without Electron Cyclotron Resonance (ECR). Figure 1.7 shows the energy and density of different kind of laboratory and space plasmas. The plasma assisted ALD have a number of advantages over the conventional ALD. (1) Plasma ALD films are found to exhibit improved properties for certain applications [21–28]. (2) The plasma species are highly reactive and hence the deposition is possible at relatively lower temperature [19, 29–31]. (3) A wide choice of substrates and precursors are possible with plasma assisted ALD [19, 32–34]. (4) Increased growth rate is possible with plasma assisted deposition [35–40]. (5) In plasma assisted ALD there are possibilities for more versatile processes. The plasma can be used for substrate treatments, treatments of film after deposition and for cleaning etc [19]. (6) Additional variables like plasma parameters are available for more control over the depositing film.

1.4 Microelectronic scaling

Soon after Bardeen, Brattain, and Shockley invented a solid-state device-Bipolar junction transistor- in 1947 to replace electron vacuum tubes, the microelectronics industry and a revolution started. Since its birth, the industry has experienced four decades of unprecedented explosive growth driven by two factors: Noyce and Kilby invented the planar integrated circuit and the advantageous characteristics that resulted from scaling (shrinking) solid-state devices [42]. The scaling of microelectronic devices has followed a trend predicted by Gordon E. Moore, the co-founder of Intel. The down scaling will integrate more functionality to a device and hence the cost per function and power consumption will reduce and performance will increase. So the industry with latest technology will get better market share. The brilliant prediction made by Gordon E. Moore

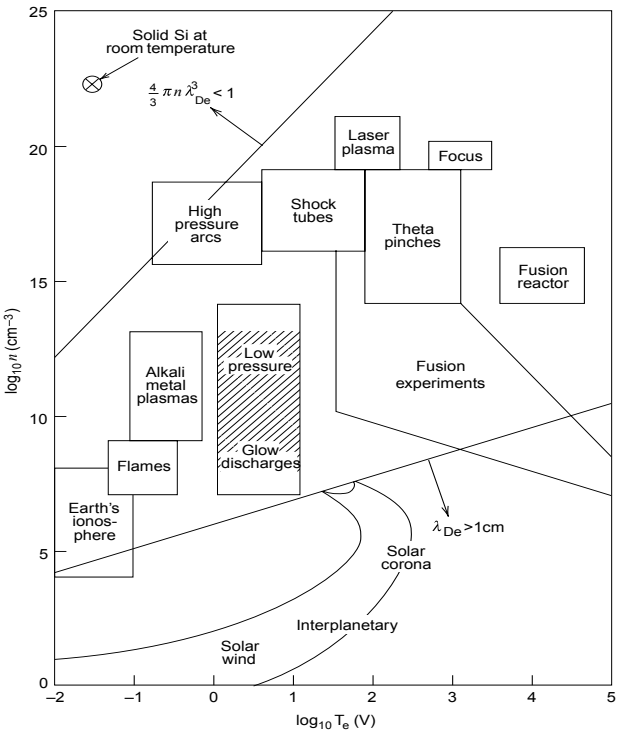

FIGURE 1.7: Space and laboratory plasmas on a density (n) vs electron temperature (T_e) diagram [41].

in 1965 (six years after the first commercial transistor) has now been termed as Moore′s law. According to Moore, the number of components in an integrated circuit will undergo an exponential increase so that it will be doubled every year [43]. A decade after the initial prediction, in 1975 he revisited the prediction and changed the trend from doubling every year to doubling every two years [44]. The industry followed the new Moore′s Law trend throughout the 1980s and early 1990s [45]. National Technology Raodmap for Semiconductors (NTRS) was formulated in 1994 by semiconductor association to make industry standard roadmap for the future semiconductor scaling and related trends. In 1999, NTRS became International Technology Roadmap for Semiconductors (ITRS) and is now setting the roadmap and renewing it periodically.

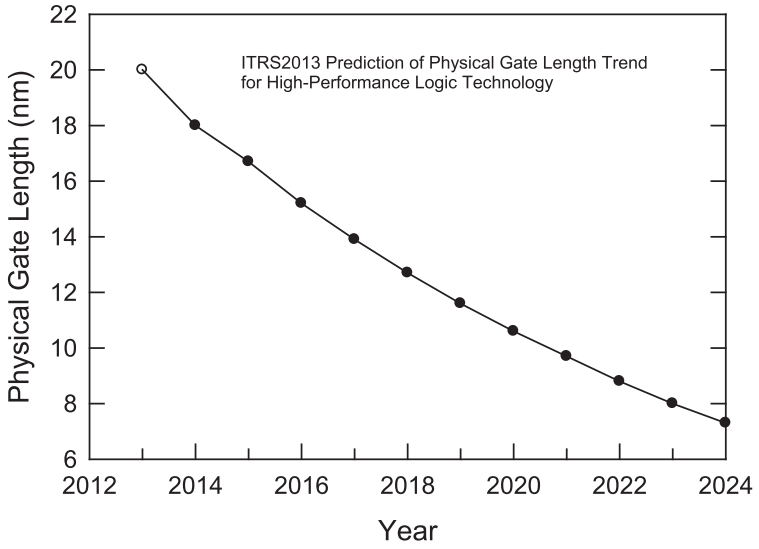

FIGURE 1.8: Trend of downsizing of MOS devices as predicted by SIA in ITRS 2013. [47]

The transistor scaling period can be broadly divided into two regimes: the classical scaling era or Dennard era and the modern era. In Dennard era the scaling was according to Dennard's classical paper [46], in which he and co-authors presented the scaling relationships which show how a MOSFET can be reduced in size. If we reduce all the dimensions of a MOSFET by a scaling factor we will get a power reduction as square of the scale factor. According to them the performance improvement can be represented by,

$$I_d = \frac{W}{L}\mu C_{ox}(V_g - V_t)^2 \tag{1.1}$$

where I_d is the drain current, W and L are the channel width and length, μ is the mobility, C_{ox} is the gate oxide capacitance and V_g and V_t are the gate and gate threshold voltages.

The Dennard era was upto the initial few years of 2000, after that the channel scaling was limited by the lithographic limitations. It is required

to have a higher doping density in the channel with reduced channel length. This will result in increased ionized impurity scattering and hence mobility became less. By this time, the gate oxide had also reached its scaling limit as it became few atomic layer thick in the 130 nm and 90 nm technologies. i.e, All the basic aspects of the Dennard scaling became under threat in a period between 2000 to 2005. The industry was able to manage the situation and started the modern era of scaling using some non-conventional techniques. The scaling was continued as per Moore. The atomic layer deposition and the high-κ dielectrics are the two major tools which enable the modern era scaling.

In 2007, Intel Corporation brought a revolutionary change by introducing High-k/metal gate devices (45 nm) instead of the conventional SiO_2/poly Silicon devices. This enabled the industry to remain at the planar MOS technology upto 32 nm feature size devices. At 22 nm device technology (2011), 3D transistors were introduced again by the Intel, based on an original idea from Thoshiba Corporation. These 3D devices together with the high-k and metal gate are expected to stand for ten more years. It was expected that the 2D scaling will reach the fundamental limit towards the end of 2013 ITRS period. Figure 1.8 shows the gate length downsizing trend of MOS devices as predicted by the 2013 ITRS. Figure 1.9 shows a calculated scaling trend for equivalent oxide thickness (EOT), a term used to represent the gate oxide thickness reduction, supply voltage (V_{DD}) and oxide electric field. The 2013 ITRS had suggested extending the functionality of the CMOS platform via heterogenious integration of new technologies and devices supporting new information processing paradigms as future technologies [48]. Shortly, in CMOS scaling and in "more than Moore" devices ALD technique and high-κ dielectrics will play a crucial role atleast for the next decade.

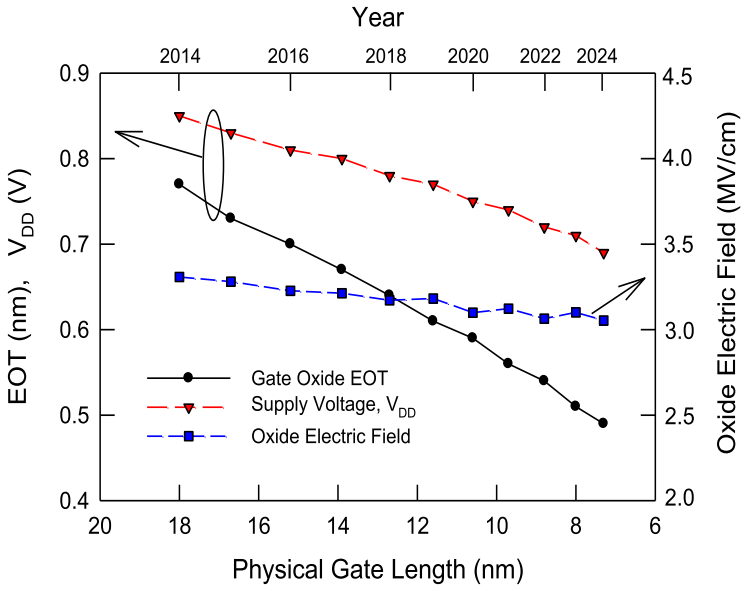

FIGURE 1.9: Predicted trends of gate oxide EOT and supply voltage, V_{DD}, scaling for the technology node in the coming decade. Oxide electric fields are calculated based on the physical thickness of gate oxide and VDD as predicted by ITRS 2013. [47]

1.5 High-k dielectrics

A fundamental aspect of silicon technology is the fortuitous nature of silicon as a material, which can be reacted with oxygen or nitrogen in a controlled manner to form superb insulators with excellent mechanical, electrical and dielectric properties [49]. As stated in the very beginning of this thesis MOS capacitor (MOScap) is the heart of MOSFET. MOSFET's are the basic building blocks of Integrated Circuits (IC) and most of the electronic devices. MOSFET is a lateral device, so it provides a large room for dimensional scaling. It was foreseen that with continuous scaling of the semiconductor electronics, around mid 2000, the silicon based insulator could reach a scaling limit. As the silicon based dielectric

reached a few atom thick and leakage current due to tunneling through the material touched unacceptable levels, the industry was confronted with a huge technical problem. The replacement of the silicon based dielectric with a material having higher dielectric constant has emerged as a potential solution. Gradually the terminology 'high-κ' became accepted in the semiconductor community to represent dielectric materials with dielectric constant greater than that of SiO_2. The dielectric constant for SiO_2 is 3.9. In the year 2007 Intel commercialized Integrated Circuits (IC) made of high-κ materials.

The high-κ materials can provide a higher physical thickness and an electrical thickness similar to SiO_2. So the higher physical thickness of high-κ material will reduce the tunneling and reliability issues. At the same time it will give electrical performance similar to scaled SiO_2. The excess scaling possible by use of high-κ material is usually represented by Equivalent Oxide Thickness (EOT) or by Capacitance Equivalent Thickness (CET). The CET can be calculated as follows

$$CET = \frac{\kappa \varepsilon_0}{C_{acc}} \tag{1.2}$$

where C_{acc} is the accumilation capacitance per uni area, κ is the dielectric constant of SiO_2 and ε_0 is the vacuum permittivity. The term EOT represents the reduced theoretical thickness of SiO_2 that is required to achieve the same capacitance density provided by the high-k dielectric. EOT can be calculated as follows

$$EOT = \frac{\kappa_{SiO_2}}{\kappa_{high-k}} \times t_{high-k} \tag{1.3}$$

where $t_{high-\kappa}$ and $\kappa_{high-\kappa}$ are the thickness and dielectric constant of the high-κ material respectively. κ_{SiO_2} is the dielectric constant of SiO_2. From CET, we can reach EOT by applying a quantum mechanical correction

(QM_{corr}),

$$EOT = CET - QM_{corr}. \tag{1.4}$$

Usually the quantum mechanical correction is approximately 0.3 - 0.4 nm [50]. The silicon based dielectric in a MOSFET had a huge list of advantages both in properties and in process compatibility. So a replacing material need to satisfy a number requirements those were initially believed as hard-to-attain [51]. The dielectric constant of the material should be high enough to get sufficient capacitance density. The hike in the dielectric constant should not be by sacrificing the band offset requirements of the material with silicon and the electrode. A band offset less than 1.5 eV with silicon will lead to unacceptable leakage currents. A material that react with silicon at semiconductor processing temperatures can not be accepted as the gate dielectric; so thermodynamic stability with silicon should be maintained. However the quality of interface between any dielectric and silicon will never be upto Si/SiO_2 interface. An interface state density of 10^{12} cm^{-2} or less is required. At a first sight itself, it was clear that polycrystalline and crystalline material will add some leakage current but amorphous materials should be fine for the purpose. Also the fabrication process should match the existing fab facilities so that they can be adopted in a cost effective manner. The reliability of the material as such and in the structure should be acceptable [52].

Atomic layer deposition rendered the semiconductor industry to attain the high-k requirements. High dielectric constant insulators were the first semiconductor related application for ALD. The success of the process for such a critical layer has established ALD as a manufacturing worthy process. It has opened interest in the use of ALD for several other applications in semiconductor manufacturing where thickness, conformality, and/or interface control are key criteria [53].

1.6 Objectives of the thesis

Atomic layer deposition is identified as the method of deposition of high-k dielectric layers for MOSFETs and has a number of other important applications in nano scale device fabrication. Even the research level atomic layer deposition systems by any industry with basic features will cost at least rupees one crore. That means atomic layer deposition is a tool affordable only by highly funded labs. Our primary aim is to make a low cost atomic layer deposition system and its process optimization. The present work tries to explore microwave plasma assisted ALD as a low thermal budget alternative to conventional ALD. The microwave plasma can give a reasonably good density of plasma species. The ALD process is optimized for High-κ dielectric thin films for research level applications, especially Al_2O_3 films deposited via plasma assisted mode of ALD and conventional thermal mode ALD. The MOS structure fabrication and characterization will enable to optimize the deposited films. Attempt is made to study the system feasibility by comparing the quality of the deposited films with depositions done in well established industry made ALD system. The deposition of higher-κ $HfZrO_2$ dielectric material and their characterization is an another objective of this thesis.

Chapter 2

Microwave plasma assisted ALD: System and process development

In contrast to conventional thermal ALD, at least one of the precursor is a chemically active plasma in plasma assisted ALD. In general the plasma should be a weakly ionized one, having the following features: (1) they are driven electrically, (2) charged particle collisions with neutral gas molecules are important, (3) there are boundaries at which surface losses are important, (4) ionization of neutrals sustains the plasma in the steady state and (5) the electrons are not in thermal equilibrium with the ions [41]. The ionized nature of plasma can create a reactive atmosphere even at low temperatures. The inclusion of plasma to any ALD process will add functional diversity to the process. Plasma assisted ALD usually has a higher growth per cycle especially at low temperatures.

2.1 ALD System: Varients and classifications

Atomic layer deposition is a true nanotechnology allowing ultra-thin films of a few nanometres to be deposited in a precisely controlled way. There are two defining characteristics for atomic layer deposition: Self-limiting atomic layer-by-layer growth and higher conformality of the coating [54]. The concept of ALD has widened to new and improved formats and one of the common variant of atomic layer deposition is the energy enhanced ALD. The most common form of energy enhanced ALD is the plasma assisted ALD. The plasma enhanced ALD can be classified further as direct plasma ALD (using either DC plasma or capacitively coupled RF plasma) and remote plasma ALD or radical enhanced ALD (usually inductively coupled RF plasma or Microwave plasma). Another emerging variant of ALD is the spatial ALD [55] instead of the usual temporal ALD. The conventional method of ALD is to pulse the precursors alternatively at different times. In spatial ALD, the precursors are separated in space rather than in time. The different precursors are supplied continuously separated by inert gas flow regions and the substrate is used to move between the different flow regions. The spatial ALD can generally provide higher growth rates in comparison with other forms of ALD. The major difficulties with spatial ALD are the requirement of high vapour pressure precursors and the deposition of good quality films in a vacuum less environment [56]. The ALD particle reactor is another variant of atomic layer deposition which allows extreme conformal ALD deposition even on nano powders.

Atomic layer deposition systems can be classified based on the working pressure of the ALD system as atmospheric pressure ALD, low pressure ALD and ALD working with moderate vacuum. Since vacuum pumps are not required, atmospheric pressure ALD systems have an advantage

of low initial and working cost. The high and moderate vacuum ALD usually provide better quality thin films in comparison with atmospheric pressure ALD process.

Another common classification of ALD system is based on the gas flow to achieve the saturation. It can be open, close, semi-open or semi-close. In an open system each reactant molecule hits the substrate surface only once. So the beam of reactant pulse should be sufficient for saturation of the whole surface. In a closed system each reactant molecule either makes a permanent bond with a surface or continues to hit the surface until a permanent bond is formed [57]. Usually closed systems will be of hot wall type.

Evacuation type and flow type ALD reactors are available in the market. The radical enhanced type reactors are usually evacuation type and most of thermal reactors are flow type [58]. In an evacuation type reactor, the purge out is done by simple evacuation. The major drawback of evacuation type ALD is the longer purge time. The requirement of better pumping system and large pressure variations during precursor pulsing are other retreats. In contrast, flow type ALD using some purge gas is usually operated at medium vacuum and the precursors are pulsed using a carrier gas. Based on the gas feed direction, ALD reactors can be classified as cross flow type and top injection type [59]. In a cross flow reactor the chamber will be like a flow channel with a little bit excess width and height than the substrate. The gas entering through one side of this channel will pass over the wafer at a high velocity. The majority of the gas reaching at the trailing edge of the substrate will be reacted gas. So there is a chance for insufficient precursor dosage at the trailing edge. In top injection reactors, there is a possibility of turbulent gas flow in the system. This will affect the efficiency of the reaction.

2.2 ALD industry

There are several industrial firms engaged in the production of ALD tools, which include both established and developing ones. According to the website of ASM International NV, a key supplier of industrial ALD, ASM International's net sales increased 22% driven by their ALD and PALD products, substantially outperforming the wafer fab equipment market, which declined 5 to 10% year-over-year up to 2013. This is due to the fact that, virtually all of the leading players in the logic, foundry and memory sectors have now adopted PALD in high volume manufacturing. Picosun is another major ALD system supplier which was started by the co-workers of Suntola, the inventor of ALD. Beneq is the present name of Lohja Corporation, who produced the first commercial ALD application, photograph of which is included in the first chapter. Lohja Corporation, changed its name to Planar International and now it is Beneq. Camridge NanoTech was a firm which mainly focussed on research level ALD systems. Now it is adopted by Ultratech. Sentech, Oxford Instruments, Kurt J Lesker, Nanomaster and Aixtron are well developed industries which focus on ALD equipments for research based applications. Now the industries offer a list diverse and application specific ALD tools.

2.3 Early stage development of plasma assisted ALD

The use of plasma for film deposition has begun with the invention of sputtering by Grove in 1852 [60]. Work on plasma ALD, also called plasma-enhanced ALD or plasma-assisted ALD (PALD), started in 1991 when De Keijser and Van Opdorp at Philips Research Laboratories reported the use of plasma during atomic layer epitaxy (ALE) to generate atomic

hydrogen for GaAs ALE [61, 62]. In this work atomic hydrogen was generated using microwave source of 2.45 GHz with 200 W power. The plasma was ON continuously throughout the process but the hydrogen supply to the reaction chamber was alternative. Instead of hydrogen, helium was used as the plasma gas for rest of the cycle. The substrate temperature was also independent of the plasma. Anyhow, it took a long period to develop PALD after this first work and the field got wide acceptance from the year 2000 onwards, mainly because of the works done by Rossnagel et al. at IBM [62, 63]. They prepared tantalum and titanium metal layers using PALD at a nominal temperature of 250-400^{0}C, compared to the deposition temperature of its CVD counterpart (800^{0}C). The plasma source was inductively coupled RF plasma at 13.56 MHz frequency with 300 to 1200 W power. Kim and Rossnagel have conducted a detailed study of reaction mechanism of plasma assisted titanium growth by ALD using quartz crystal micro-balance [64]. Soon after the works of Rossnagel, S-M Kang et. al. came with a solid proof for the usefulness of PALD; they prepared TaN films with lower resistivity (400 $\mu\Omega$cm) and higher density in comparison with the thermal ALD TaN (resistivity >20k $\mu\Omega$cm) [24, 25]. Plamsa ALD was reviewed at the early stage of its development by Kim, as part of his ALD review in 2003 [65] and pointed out its benefits and shortcomings. The initial developments in PALD were reduction based metalization processes. PALD of metal oxides and metal nitrides soon gained attention and the ALD community modified the existing ALD processes to PALD. A complete revision of PALD is vast and beyond the scope of this thesis.

2.4 Design and fabrication of microwave plasma assisted ALD

Two classification schemes are possible for PALD reactors; first according to method of plasma production and the second based on the position of plasma and substrate. Inductively coupled radio frequency plasma is the most common plasma used in PALD systems [63, 66]. Direct coupled discharges, normal [58] and ECR microwave plasma and capacitively coupled radio frequency plasma [35, 67, 68] are the other major plasma sources. A plasma source in PALD can be used either in direct mode or in remote plasma mode. In direct plasma configuration the plasma and the substrate surface arein a direct contact. The major advantage of remote plasma ALD over the direct mode is the limited number of ions reaching the substrate surface. A higher number of ions can introduce large defects in the film. The best suited plasma configurations for remote plasma ALD are the inductively coupled RF and microwave based plasma. The DC and capacitively coupled RF are mainly used for direct plasma configurations.

The most studied and common plasma configuration in plasma assisted ALD is the inductively coupled RF plasma. Microwave plasma has the advantage of higher plasma density in comparison with the RF plasma. Generally the microwave plasma is less uniform and it is difficult to sustain the microwave plasma during alternate precursor pulsing. There is no industrial ALD system which utilizes the microwave plasma for ALD operation, but there are few literature reports on research level microwave plasma assisted ALD systems. In 2005, the group lead by M. Leskela and M. Rittala of Helsinki University reported metallic copper deposition using a surface wave microwave plasma assisted atomic layer deposition system [58]. They utilized the downstream of plasma for making the deposition remote. In 2007, the same ALD system was used for Tantalum

oxide deposition in remote plasma configuration [69]. In 2008, Jae-Gun Park et al. used electron cyclotron resonance (ECR) type microwave plasma for plasma ALD-Al_2O_3 on organic substrates [70]. They did the deposition at room temperature and obtained a growth rate of 2.2 A^0 per cycle. Deposition of Al_2O_3 thin films by microwave plasma assisted ALD was done by the group from Tokyo University of Science in 2010 [71] with a wave guide cavity plasma source. In 2013, Tokyo University of Science group reported the simultaneous formation of aluminum germanate while deposition of microwave plasma assisted ALD of Al_2O_3 on germanium substrate [72].

Every ALD system should have (a) precursor and purge gas control unit, (b) deposition or reaction chamber and (c) exhaust unit. Following section contains a detailed discussion of each of these unit in our microwave plasma assisted ALD system.

2.4.1 Precursor and purge gas control system

For successful operation of an ALD process, controlled sequential delivery of precursors and purge gas is necessary. The gas feed/control system consists of gas cylinders, precursor sources, mass flow controllers, needle valves and solenoid valves. Figure 2.1(b) shows the schematic of the gas feed system used in our ALD. The inert gas line contains a needle valve (NV1), a mass flow controller (MFC2) and a normally open solenoid valve (SV3) to control the gas flow. The inert gas line is connected to one side of the precursor bubbler just after the solenoid valves (SV1 & SV2). In usual process the inert gas (nitrogen) flow is 100 sccm. There are several different possible ways to pulse the precursors: (a) In the case of high vapour pressure precursor, we can use a simple pulsing method. In this method a valve connected between the precursor and chamber opens during precursor exposure sequence and delivers the precursor in to the chamber. The

major draw back of this method is the chance of residual precursors on the precursor supply lines. Another drawback is the necessity of high vapour pressure for the precursor. (b) In the second method, a carrier gas is used for the precursor transportation. Solenoid valves for admitting carrier gas to precursor bubbler and the precursor delivery valve (valve on chamber side of the bubbler) are operated simultaneously. This method can also be used for low vapour pressure precursors. The second method is more complicated than the first one and still there is a chance of precursor residue. (c) As an extension of the second method, the precursor can be pressurized using short carrier pulse before opening precursor outlet valve. This will enable the use of precursors with very low vapour pressure. (d) Third method uses one inert gas valve between the precursor delivery valve and the reactor. The flow of inert gas will be zero during precursor pulse and then the inert gas valve opens and helps the complete purging of the lines.

In our system, inert gas line is connected to the precursor lines just after the precursor pulsing solenoid valves for effective complete purging out of the precursor gases in a simple manner (Figure 2.1(b)). The inert gas flow is maintained continuously and it acts as both carrier and purge gas. We utilized two different arrangements for the thermal and plasma ALD process. During plasma ALD the gas line configuration is different at the chamber side. The first precursor and the plasma gas are fed separately to the chamber (Figure 2.1(b)).
Since mass flow controllers used in our system have a slow response time, maintaining a steady gas flow rate and hence plasma are little bit tricky. The required oxygen flow during plasma cycle is 50 sccm. For maintaining 50 sccm, the MFC1 in figure 2.1(b) is set to a lower value than 50 sccm which fills a gas tank at cycles other than the plasma cycle. The MFC1 flow and the tank pressure were adjusted to get a constant flow after the initial burst on opening the solenoid valve (SV3). The plasma strikes only

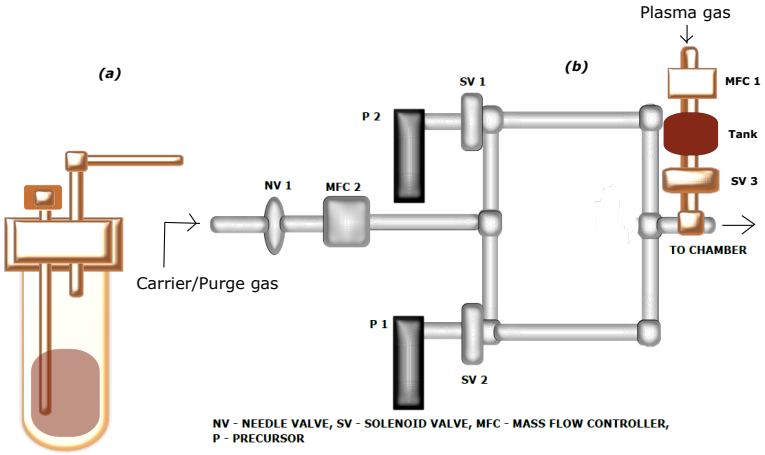

FIGURE 2.1: Schematic of the precursor bubbler and gas control lines for home made microwave plasma assisted ALD system

FIGURE 2.2: Photograph of ALD sequence controller.

after stabilization of the flow.

Figure 2.1(a) is schematic of the precursor bubbler. The chemical container of the bubbler is made of glass and stainless steel 316. The bubble gas entry line is kept closed. For Al_2O_3 deposition using trimethylaluminum (TMA), the TMA has a high enough vapour pressure and does not require bubbling. The capillary rise of TMA to the gas inlet tube and its bubbling back to the container is beneficial to get sufficient vapour pressure. In the present experiment TMA was kept at room temperature and the TMA precursor line at 100^0C to avoid precursor condensation.

The entire gas control unit is interfaced to a personal computer using

a home made electronics circuitry (ALD sequential controller), a photograph of which is shown in figure 2.2. The control is carried out using visual basic software. The solenoid valves used are low temperature ones and hence a regular periodic cleaning of the valves is necessary. Solenoid valves with short response time will help to avoid the chemical loss and they can provide better process efficiency (in terms of time). Similarly mass flow controllers with fast response are required. The use of 3/2 solenoid valves (for precursor and purge gas) can ensure complete precursor purge out. If there is a 3/2 solenoid valve together with a stop valve in precursor line, we can purge out the solenoid valve after the process. This will help to keep the solenoid valve intact.

2.4.2 ALD reactor

The ALD reactor contains the microwave plasma unit and a reaction chamber equipped with movable substrate holder with heater, exhaust port, view port and provision for insitu monitoring and characterization. The design of the chamber allows a laminar flow of gas through it. A schematic representation of the present ALD reactor is shown in figure 2.3. The substrate holder is able to hold wafers upto 2 inch diameter. It has a built in heater and a thermocouple attached to it. An additional thermocouple was inserted in to the chamber for measuring the temperature above substrate surface. The maximum possible temperature at the substrate surface is 500^0C. The substrate holder was inserted in to the chamber through a wilson seal like arrangement. The height of the substrate holder inside the chamber can be adjusted upto 15 cm. By adjusting the height of the substrate holder, the plasma to substrate distance can be varied from 40 cm to 25 cm. Heating tapes were used to heat the chamber walls and the precursor lines. This will help to avoid

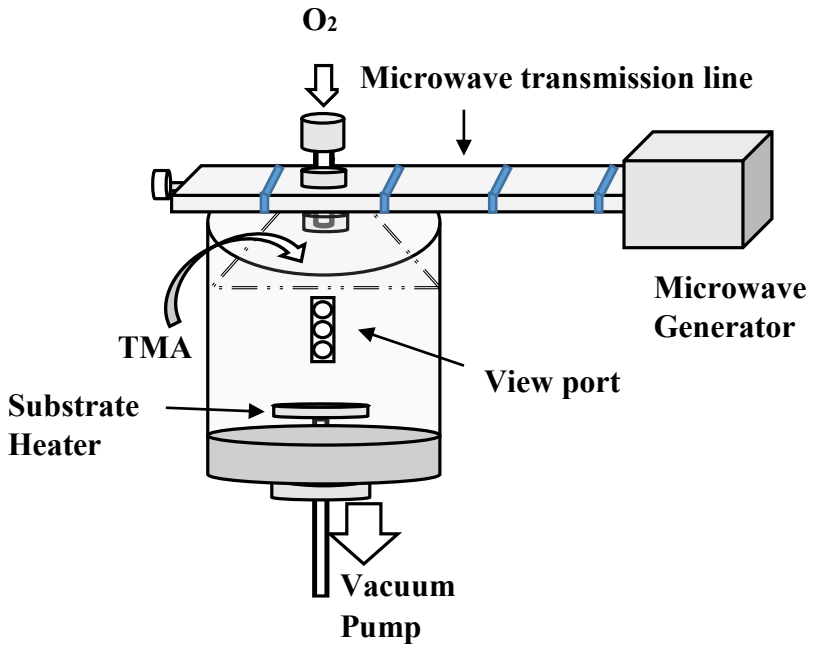

FIGURE 2.3: Schematic of the ALD reactor with microwave source on top.

unwanted precursor condensation at these areas. For deposition temperatures higher than 100 ^{0}C the chamber walls and precursor lines were kept at 100 ^{0}C and for deposition temperatures below 100 ^{0}C they were at the actual deposition temperature.

The reactor is a flow type one with a vertical flow. A flow reactor will enable speedy purging of the chamber in comparison with evacuation type reactor. The reactor was designed to operate in the viscous flow regime. During design and fabrication special care was taken to avoid sharp edges and air pockets inside the chamber. The precursor gas was delivered through top side of the reactor at an angle, so that the gas would reach the whole substrate surface. Cross flow type reactors are common in industries and in batch processing systems. A cross flow type reactor

is considered to be the best for ALD because of its lower chamber size requirement and easiness to purge out. In the present case, cross flow is not practical as it is required to have a sufficient plasma to substrate distance. The plasma gas is provided from the top side, which would pass through the microwave plasma column before entering the chamber. Inert gas is used as carrier and purge gas. The gas delivery line is divided into two at the source end. One line is used to carry TMA and the other for O_2. An inert purge gas is injected in to these lines just after the solenoid valve near to precursor. The inert gas supply is maintained throughout the process. This is essential for complete purge out of the precursor gases. In addition to the precursor delivery provisions, the reactor chamber has provisions for measuring the vacuum, a view port and a port for inserting the thermocouple. The pressure and flow inside the reactor is maintained at desired values by adjusting a butterfly valve in between the reactor and exhaust pump.

2.4.2.1 Microwave plasma unit

Microwave plasma has several exciting advantages for its use in thin film deposition. The microwave plasma can provide (1) a high degree of ionization of the working atmosphere, (2) a high concentration of active species such as atoms, radicals and/or excited molecules and photons in vacuum ultra violet (VUV), near ultra violet (UV), visible and infra red (IR) regions, (3) high density plasma and its electrode-less acceleration, (4) control of electron and ion energy distribution functions and (5) high deposition and etching rates [73]. These peculiarities make microwave plasma important for other applications like etching of thin films, surface treatments and chemical reaction activation.

There are two basic types of microwave plasma reactors used in thin film

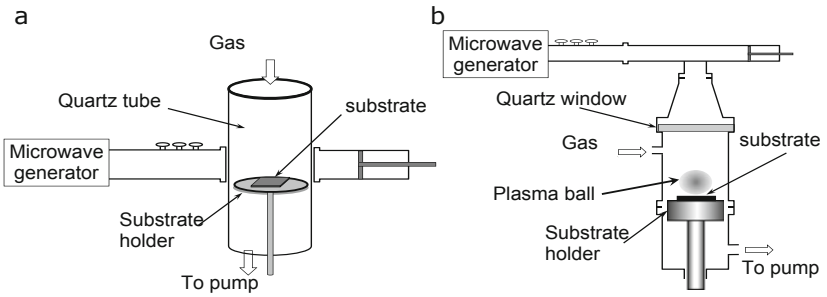

FIGURE 2.4: Schematic of (a) NIRIM type and (b) ASTeX type microwave plasma reactors.

systems: NIRIM (National Institute for Research in Inorganic Materials, Japan) type and the ASTeX (Applied Science and Technology Inc., presently a subsidiary of MKS Instruments) type. In NIRIM type reactor, plasma is generated in a cylindrical quartz tube which intersects the rectangular waveguide. Generally the waveguide is provided with a short circuit stub to arrange a standing wave maximum at the quartz tube and hence transfer maximum power to the gas load. In ASTeX type reactor an axial antenna is used for microwave power coupling. The microwave power is coupled to a quartz plate separated reaction chamber where it forms a spherical plasma column, the so called 'plasma ball'. Figure 2.4 shows schematic representation of both NIRIM type and ASTeX type microwave plasma reactors.

The microwave plasma unit can be described as a combination of three basic elements: (i) a microwave generator, (ii) a system of power delivery components and (iii) a plasma applicator. Figure 2.5 shows the block diagram of the microwave plasma reactor. It is a NIRIM type resonant cavity microwave plasma source. In resonant cavity structures high electric fields at resonance support plasma ignition and they generally produce high plasma densities. A 2.45 GHz microwave source with WR

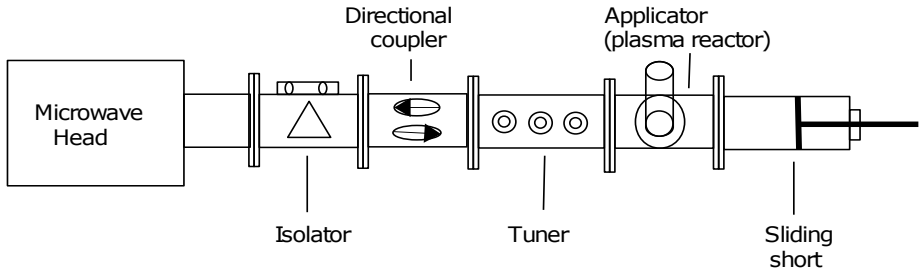

FIGURE 2.5: Schematic representation of microwave delivery system with plasma applicator.

340 waveguide was used in our system. In a WR340 waveguide the dominating mode is the TE_{10} mode [74]. A detailed description of the different components used in our microwave system is given in the following section. The picture of different components in the microwave unit is given in figure 2.6.

The resonance occurs if the waveguide has an approximate length of a few times the waveguide wavelength λ_g. The resonance frequency f_x is given by [74]

$$f_x = c_0\sqrt{(\frac{p}{2L})^2 + (\frac{m}{2a})^2 + (\frac{n}{2b})^2} \tag{2.1}$$

where c_0 is the speed of light, a is the wide side of the waveguide, b is the small side of the waveguide, L is the length of the waveguide resonator and m, n and p are mode coefficients. After plasma ignition the resonance is destroyed because the plasma acts as a complex load and it changes the impedance. The complex load of a plasma can be expressed by the impedance Z_p as

$$Z_p = \sqrt{\frac{\mu_0}{\varepsilon\varepsilon_0}} \tag{2.2}$$

μ_0 and ε_0 are the natural permeability and permittivity respectively. ε is complex permittivity of the plasma. For low temperature plasma it is given by

$$\varepsilon = 1 - \frac{(\omega_p/\omega)^2}{1 + (\nu/\omega)^2} - j(\frac{\nu}{\omega})\frac{(\omega_p/\omega)^2}{1 + (\nu/\omega)^2} \tag{2.3}$$

with ω is the excitation frequency, ω_p is the plasma frequency and ν is the collision frequency. The plasma frequency

$$\omega_p = \sqrt{\frac{n_e e^2}{\varepsilon_0 m_e}} \tag{2.4}$$

with n_e is the electron concentration, e is elementary charge and m_e is the electron mass [74]

2.4.2.2 Microwave unit components

The microwave source used in the present work is National Electronics (USA) MH1.2W-S microwave generator which produces microwaves of 2.45 GHz frequency at a maximum power of 1.2 kW. The power can be adjusted from 10 to 100% of the maximum power. A cooling water supply is necessary at a flow rate of 1.5 LPM at 25^0C. The maximum operating temperature is 58^0C. The waveguide used is rectangular type WR340 waveguide having 3.4 inch broad side and 1.7 inch narrow side.

The MH1.2W-S is controlled using SM-745 (Alter - Italy) switch-mode power supply. The power supply controls the power generation accurately and it monitors the generator temperature, current leakage, anodic over voltage, presence of any arc and over-current in real time. In case of any malfunction, the alarms will be activated together with LED indication. With SM-745, the MH1.2W-S can pulse upto 1 kHz frequency. The power supply can be operated either from front panel controls or by remote interface. We utilized an additional electronic circuitry (figure 2.7 and 2.8) to control and monitor the SM-745 power supply remotely using a personal computer.

If the microwave head is connected directly to the plasma source, there is a risk of reflected power going to the magnetron. The risk is maximum before the ignition of plasma and when the power absorption by plasma

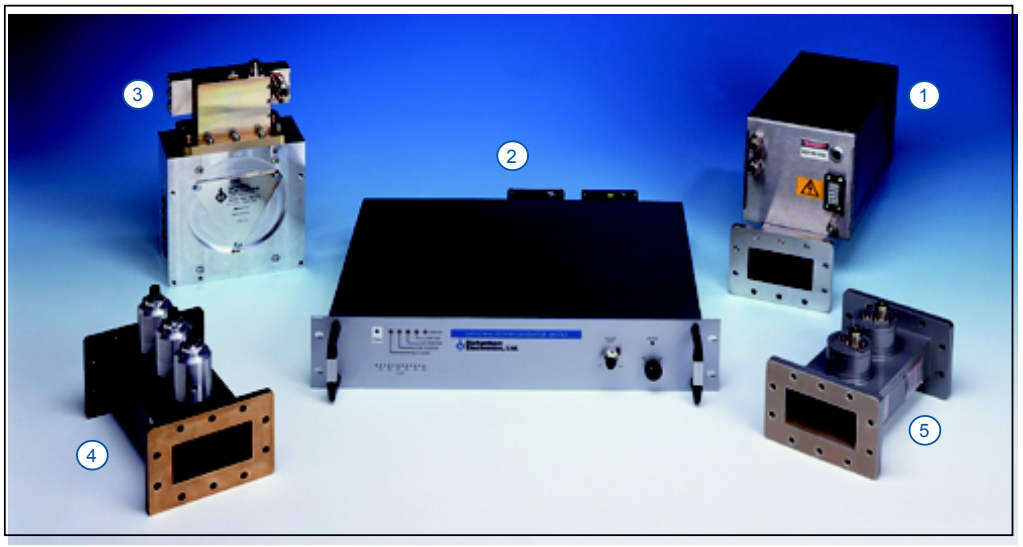

FIGURE 2.6: Picture of the major microwave plasma unit components. (1) Microwave generator MH1.2W-S (2)Alter SM-745 power supply (3) National Electronics Isolator (4) Alter 3-stub tuner (5) National electronics Dual Directional coupler.

source is low. The resonant cavity design minimises the risk of magnetron damage from reflected power. The resonance prior to ignition ensures that a major part of the microwave energy is absorbed inside the waveguide cavity even without plasma [74]. The use of an isolator further contributes to minimization of the risk. The function of isolator is to block all the reverse power reaching its output port and at the same time allow all the input to pass through the out put port. But every isolator inevitably varies from ideal case and there will be a small forward power absorption and reverse power transit. Our isolator is a water loaded isolator with 3.0 kW handling capacity.

The microwave power in a microwave circuit is measured using a power coupler. There are three types of power couplers; namely directional, non-directional and analytical. A directional coupler is used to measure the power propagating in a specific direction. We used one dual-directional

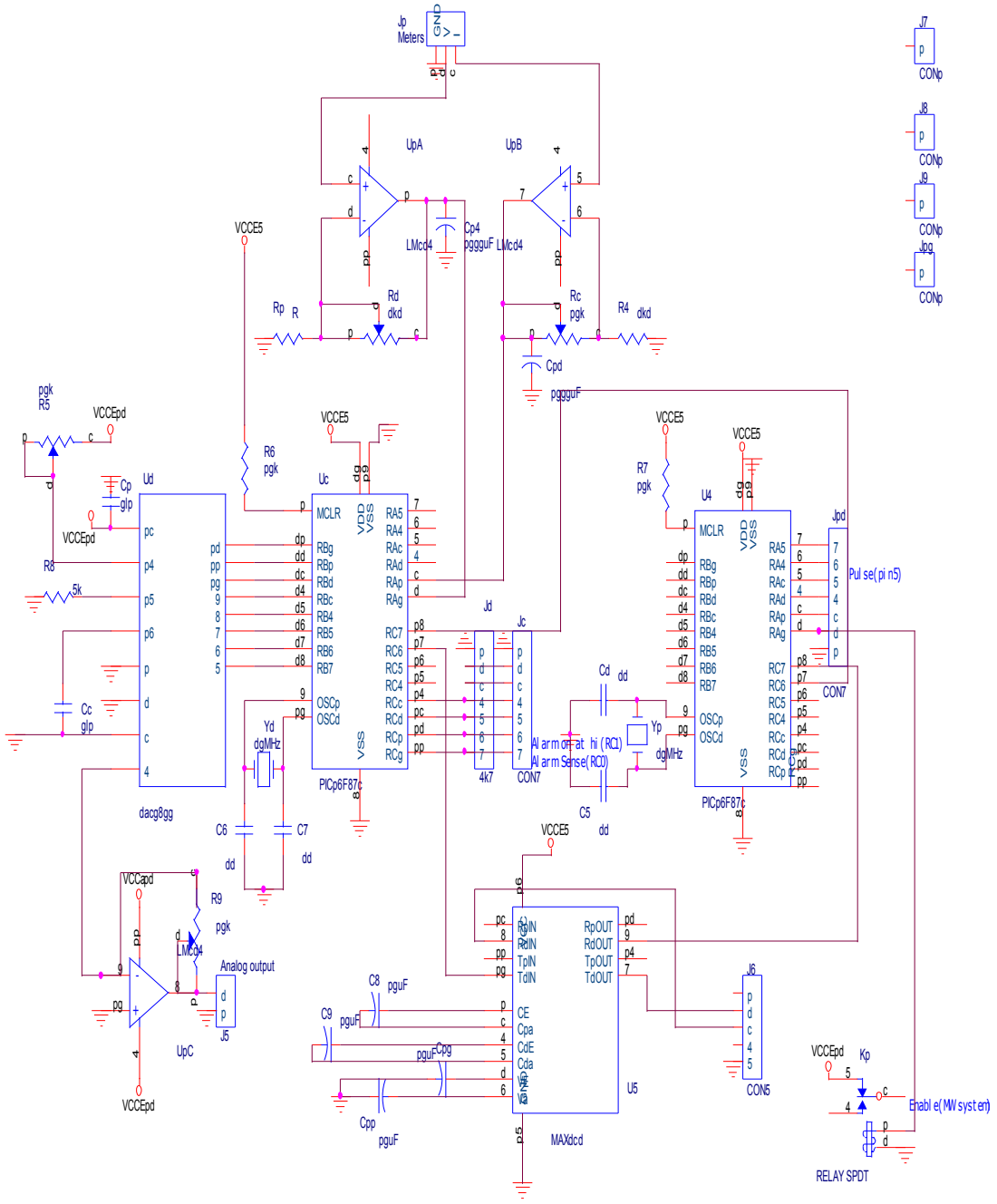

FIGURE 2.7: Circuit diagram of control unit for the microwave plasma unit in microwave plasma assisted ALD.

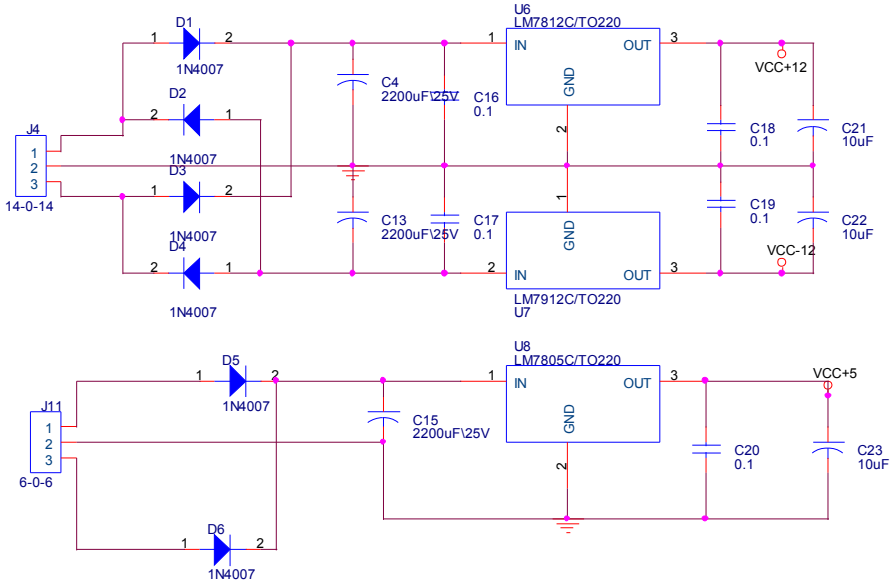

FIGURE 2.8: Circuit diagram of microwave plasma control unit power supply.

coupler to measure the forward and reflected power. A non-directional coupler cannot distinguish between the forward and reflected power. An analyser coupler can determine both phase and amplitude of forward and reverse microwaves [75].

For maximum power coupling, the impedance of the microwave and the gas load should be matched. The impedance has both amplitude and phase and hence the mismatch also has phase and amplitude components. The common method of impedance matching is by capacitive means. The capacitive matching is achieved by inserting metallic elements to the waveguide. For amplitude and phase matching, it is required to adjust the insertion position and depth. So multi stub tuners are best means of achieving impedance matching. A simple, economical design employs threaded stubs screwed directly through the broad wall of the

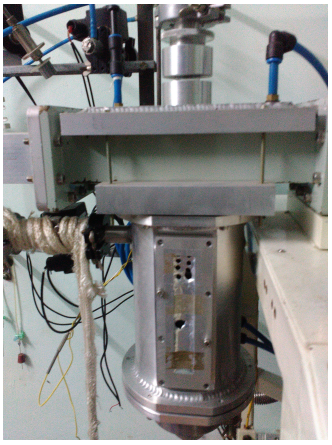

FIGURE 2.9: Photograph of plasma applicator in home made microwave plasma ALD system.

waveguide along its center line [75].

The plasma applicator is wave guide cavity type made by inserting quartz tube through the broad side of the WR340 waveguide. The photograph of the plasma applicator is shown in figure 2.9. The outer diameter of the inserted quartz tube is 1 inch. At bottom side, the lower end of the quartz tube extending out the wave guide is joined to top of reaction chamber through a cooling water assembly and a vacuum sealing arrangement. A mesh is placed inside the quartz tube at its lower end. On top, outside the wave guide the quartz tube is covered with a cut-off tube followed by a Wilson seal and plasma gas feed tubes. The cut-off tube is a cylindrical wave guide like structure which will not allow free flow of the microwave so that there will be attenuation of the microwave power. On reaching the cut-off tube the microwave will die out after passing a certain length which depends on the microwave power and cut-off tube dimension. The rate of power attenuation is given by the attenuation constant

$$\alpha = \sqrt{(\frac{2\pi}{\lambda_c})^2 - (\frac{2\pi}{\lambda})^2} \tag{2.5}$$

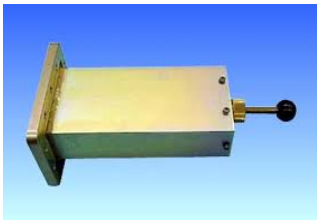

FIGURE 2.10: Photograph of sliding short used in MPALD system.

where λ_c equals 3.41 times the tube radius and λ is the microwave wavelength. The maximum leakage from industrial equipment and consumer appliances should be less than 25 mW cm^{-2} which yields the common regulatory limit of 1 mW cm^{-2} when measured at 5 cm from the source [76]. The attenuation constant is set to attain this condition. The size of the mesh in the bottom of quartz tube is carefully selected so that every hole in the mesh will act like a cut-off tube and prevent the microwave leak to the reaction chamber.
The waveguide terminates at a short circuit arranged at one end of the microwave unit. A sliding type short circuit is used in our plasma system. The sliding short allows us to change the length of the waveguide column and hence to achieve maximum power coupling. A fixed short circuit is suited only for specific process with known optimized short circuit position. Figure 2.10 shows the picture of a sliding short.

2.4.3 Exhaust unit

The exhaust unit contains two pumps: a molecular drag pump and a rotary pump. The molecular drag pump has a pumping speed of 7.5 litre/s (for nitrogen) and 10^{-5} mbar ultimate vacuum capability. It belongs to the special chemical inert series by Alcatel-Adixen. The molecular drag

FIGURE 2.11: Pumps and gauge used at the exhaust side of the home made ALD system. (a) molecular drag pump Adixen MDP5011, (b) capacitance diaphram gauge CDG0025 and (c) rotary pump

pump is backed by the rotary pump of 200 litre/minute capacity. Since the ALD system is a flow type reactor, rotary vacuum is sufficient for running the ALD cycles and the molecular drag pump is needed only for obtaining initial high vacuum. The chamber exhaust is connected to the molecular drag pump through a butterfly valve. There is a bypass connection to the rotary pump through another butterfly valve. This valve helps to control the chamber pressure during deposition. Figure 2.11 shows the pumps and capacitance diaphragm gauge used in the present ALD system. It is better to use a chemically inert and oil free low vacuum pump and an automatic pressure control valve in the system.

Two different gauges are used for measuring the pressure in the ALD reactor. A digital penning gauge is connected at the reaction chamber and a capacitance diaphragm gauge to the exhaust side of reaction chamber. The capacitance diaphram gauge (Infusil make) has a measuring range of 0.001 mbar to 10 mbar with 10 millisecond response time. It is interfaced to a computer using a locally made controller. The photograph of the control unit is given in figure 2.12 and the electronic circuit of the controller is shown in figure 2.13.

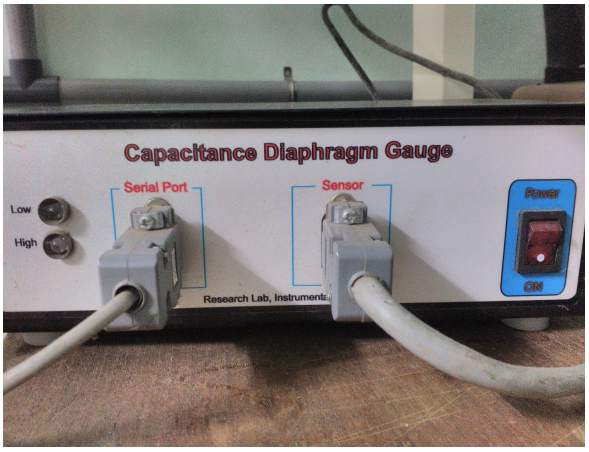

FIGURE 2.12: Photograph of the capacitance diaphragm gauge control unit.

2.5 Microwave plasma

The amount of reflected power shows how efficient is the microwave plasma system. The reflected power should be minimum in case of proper impedance matching. The impedance matching is achieved by adjusting both sliding short and the 3-stub tuner. Initially, the sliding short is adjusted to a point for standing wave pattern and then the stubs in the tuner are slowly inserted to the wave guide to get minimum reflected power. Successive readjustments of the sliding short and tuner will lead to the minimum reflected power at maximum impedance matching. The matching is a tedious process and a trade off should need to be reached between minimum reflected power and plasma initiation. It is also reported that an optimum tuning for initiation of breakdown generally does not correspond to the optimum tuning for sustaining the plasma [77]. The flow and gas pressure conditions are found critical in the microwave plasma system. The gas load pressure variations will affect the impedance matching and a pressure variation of around 2 mbar will extinguish the plasma. The ignition

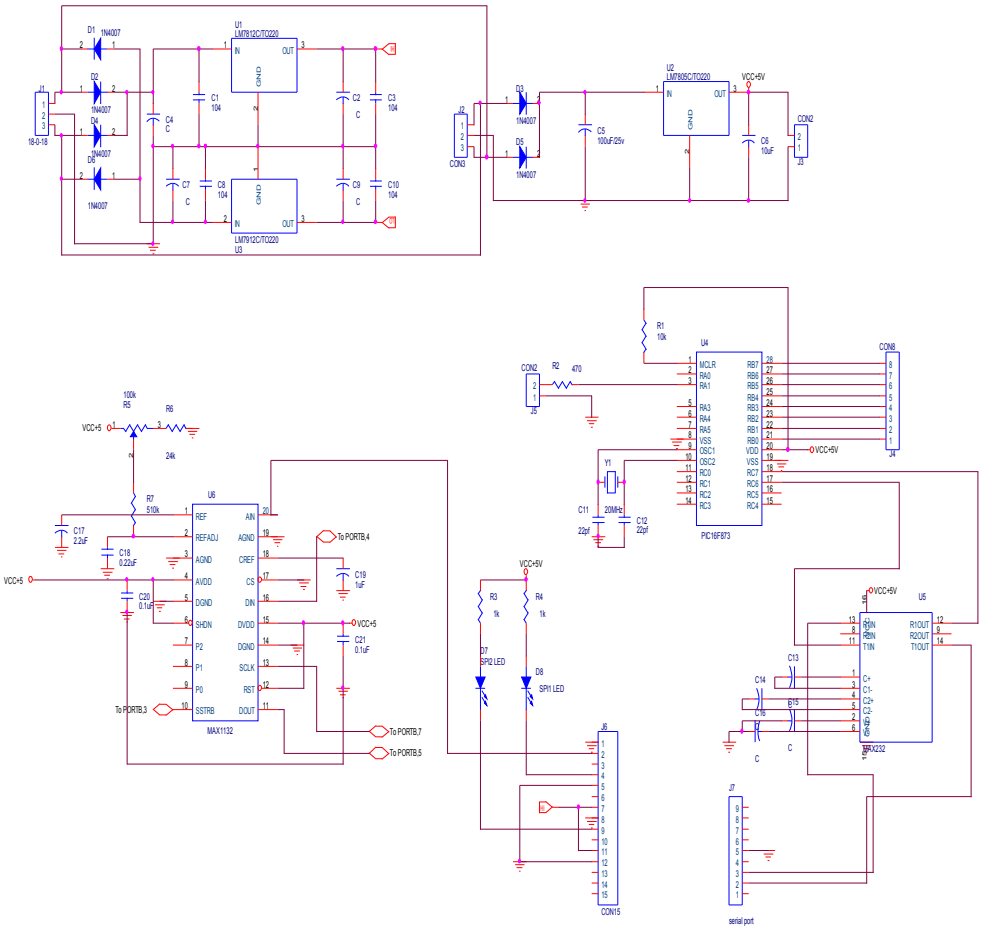

FIGURE 2.13: The electronic circuit for capacitance diaphragm gauge control unit.

of plasma in microwave system is not simple. In microwave plasma assisted ALD systems a background plasma is used at lower operating power [58]. This kind of background plasma will naturally add some CVD part to ALD. But in our case we have succeeded in generating plasma pulses without any background plasma sustaining throughout the process.

The Optical Emission Spectra (OES) of the microwave plasma recorded from the center of the plasma and from the substrate surface are given in figure 2.15. Ocean Optics HR 4000 Spectrometer was used for capturing

FIGURE 2.14: Photograph of home made microwave plasma assisted ALD system.

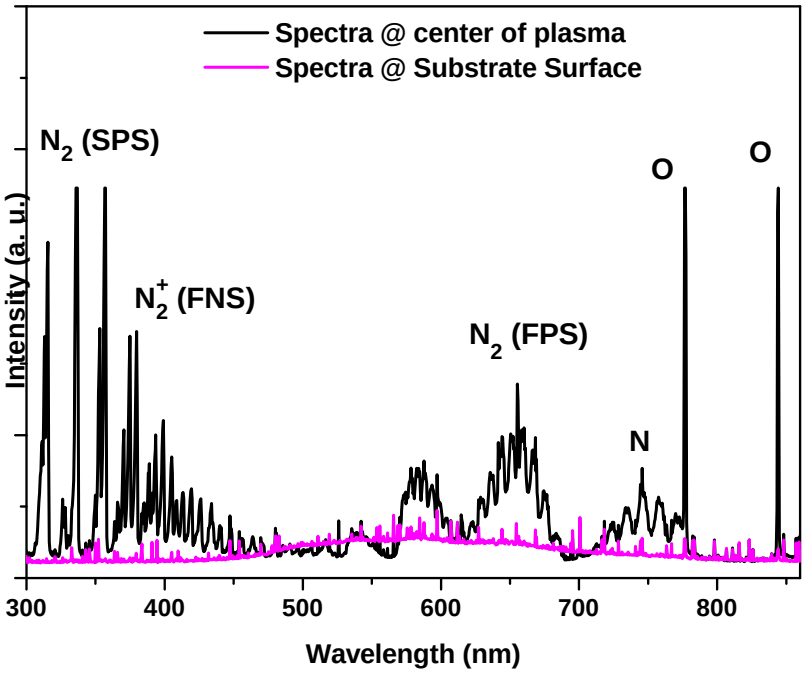

FIGURE 2.15: Emission spectra for N_2 + O_2 gas microwave spectra at 2.5 mbar recorded from the center of the plasma (dark) and from the substrate surface (fade).

the emission spectra. The microwave plasma was produced with O_2 (50 sccm) + N_2 (100 sccm) load gas at 2.5 mbar chamber pressure. The optical emission spectra can give information about the plasma composition by recording the de-excitation spectra. Emission spectra were recorded through a quartz window using optical fibre cables. At the center of the plasma, the presence of atomic oxygen is evident from peaks at 777 nm and 845 nm. The spectrum also consists of the second positive system (SPS), first positive system (FPS) and first negative system (FNS) of nitrogen plasma emissions. These emissions are transitions from the excited states of N_2 and N_2^+ respectively. Weak emission from excited nitrogen atoms (746 nm) is also present. OES recorded from the substrate surface

gives only a feeble broad spectrum that spreads over the entire visible spectrum. The broad peak was partially due to stray light and partially from nitrogen plasma reaching the substrate surface. The feeble spectra indicate less amount of energetic species reaching the substrate surface and hence the damage due to plasma on the depositing film would be less.

2.6 ALD process development

Since atomic layer deposition is a chemical method of thin film deposition, it is required to develop both the chemistry of the process and the system based process parameters for complete ALD process development. The atomic layer deposition of Al_2O_3 using trimethylaluminum (TMA) and water is considered as a model process for ALD. As discussed in the review, the reaction chemistry for thermal ALD-Al_2O_3 is well developed. Several groups have studied the underlying reaction kinetics also [3, 78–80]. The reaction chemistry and its kinetics studies were not a part of this work. We concentrated only on the ALD system and associated parameters by depositing Al_2O_3 from TMA and H_2O/O_2 plasma. Once if we have a definite ALD chemistry and predictable substrate surface composition, further if we kept the substrate at a constant temperature then the parameters with interest are the precursor dosing time and the purging time required for ALD growth. The minimum deposition time was one of the design goals during ALD system design. We conducted several kinds of studies on the system to optimize the process. The temperatures at different portions of the system are also important. The initial task was to assign and control the temperature on each part of the deposition system. The temperatures of various parts of the system are given in the table 2.1. Attempts were made to find out the precursor dosage pattern

Part of the ALD system	Temperature (^{0}C)	Accuracy (^{0}C)
Substrate holder	Variable from room temperature to 400	± 1
Precursor lines for TMA	100	± 5
Precursor lines for H_2O	100	± 5
Chamber wall	same as substrate holder temperature	± 5

TABLE 2.1: Distribution of temperature over different parts of the ALD system.

over the substrate surface by finding out areas of insufficient film formation on the substrate and hence tried to optimize the precursor dosage. If the precursor flow is not enough for complete reaction on the substrate surface, the sides of the substrate become deficient in film. We checked out for this kind of irregularities during film formation.

The valves used for the gas feed unit are Avcon vacuum compatible 2-way solenoid valves. The experimentally verified minimum response time for this valve is 300 milliseconds. Complete saturation of 2 inch silicon wafer is possible within 300 ms pulsing of either water or trimethylaluminum. The major disadvantages of using this kind of valve is the precursor wastage and decreased efficiency (in terms of time) of the process. The reactor pressure and gas flow were optimized by a careful examination of the film thickness profile. Several different working pressures were tried for the system for optimizing the pressure and flow conditions. The pressure condition and gas flow required for thermal ALD and for microwave plasma assisted ALD of Al_2O_3 are given in table 2.2 and 2.3 respectively.

The minimum possible 300 ms precursor pulsing was found to supply excess precursors. Usually the excess precursor dose not have major effect on the ALD film properties [81]. But it will naturally lead to higher purge time requirement. The precursor dosing and purge timings for thermal

ALD Sequence	Gas	Gas flow	Chamber Pressure (mbar)
Precursor 1	TMA+N_2	N_2 @ 100 sccm	2.3
Precursor 2	H_2O+N_2	N_2 @ 100 sccm	2.6
Purge	N_2	N_2 @ 100 sccm	1.8

TABLE 2.2: Precursor and carrier gas flow for thermal ALD process.

ALD Sequence	Gas	Gas flow	Chamber Pressure (mbar)
Precursor 1	TMA+N_2	N_2 @ 100 sccm	2.3
Precursor 2	O_2+N_2	O_2+N_2 @ 150 sccm	1.5
Purge	N_2	N_2 @ 100 sccm	1.8

TABLE 2.3: Precursor and carrier gas flow rate for microwace plasma assisted ALD process.

Temperature (T)(^{0}C)	TMA Purge (s)	H_2O Purge (s)	TMA pulse (ms)	H_2O pulse (ms)
T$\leq$ 100^{0}C	60	180	300	300
T$\geq$ 100^{0}C	60	60	300	300

TABLE 2.4: Precursor pulse and purge timings for thermal ALD-Al_2O_3 process.

ALD Al_2O_3 and microwave plasma ALD Al_2O_3 are given in table 2.4 and 2.5 respectively.

Temperature (^{0}C)	TMA Purge (s)	O_2 Purge (s)	TMA pulse (ms)	O_2 plasma (s)
All temperature	60	5	300	2

TABLE 2.5: Precursor pulse and purge timings for microwave plasma assisted ALD-Al_2O_3 process.

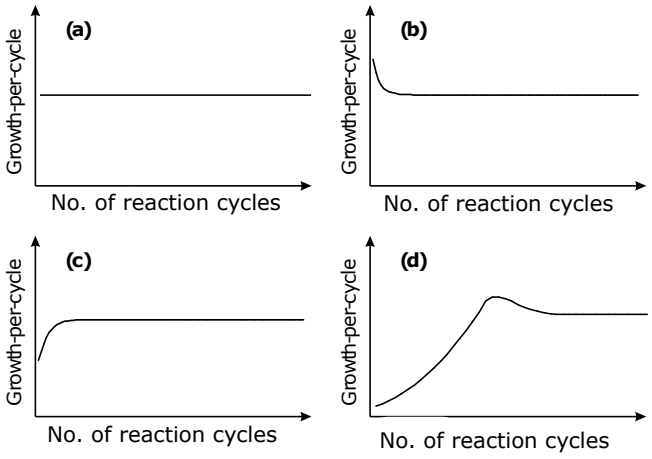

FIGURE 2.16: Dependence of GPC on number of cycles. (a) linear growth (b) substrate-enhanced growth (c) substrate-inhibited growth type 1 and (d) substrate-inhibited growth type 2.

2.6.1 Saturation & GPC

The basic feature of atomic layer deposition process is the self terminated gas solid reactions. For the gas solid reactions to be self saturated, the reaction should remain irreversible in the time scale of the ALD process [3]. The irreversible reaction should be chemisorption, which depends both on the adsorbent and the adsorbate surface. In the language of ALD the term monolayer for an ALD grown material MZ_X can be defined as one plane of MZ_X units in a crystalline face of the bulk MZ_X material in the preferred orientation of growth (for crystalline materials) [3]. The

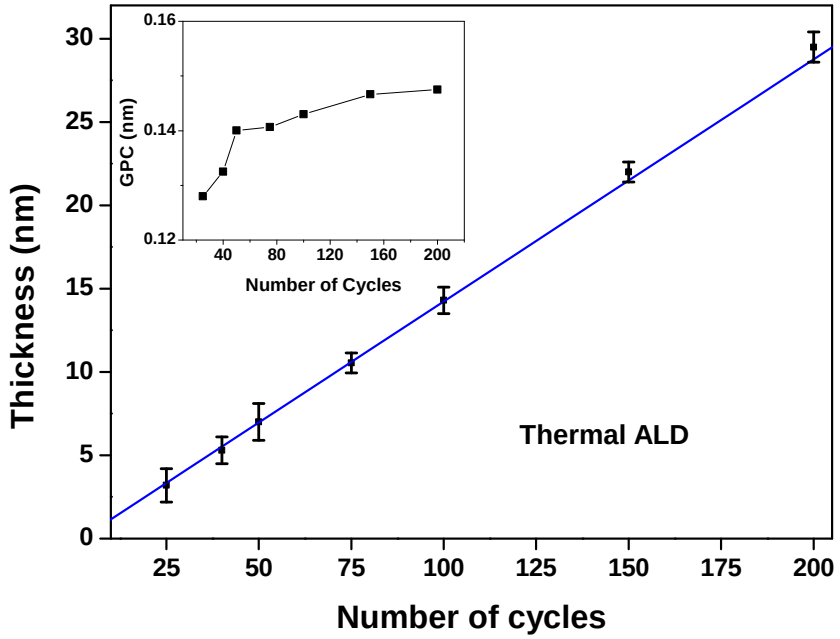

FIGURE 2.17: Thickness variation of thermal ALD-Al_2O_3 thin films with number of cycles of deposition. Inset figure shows the GPC with number of deposition cycles.

self saturation limits the ALD growth to one monolayer per cycle. The thickness of the monolayer in ALD is determined by available surface sites and steric hindrance of the precursor ligands. The steric hindrance usually limits the film growth to ALD-monolayer other than the actual monolayer.

The amount of material added to the surface on each reaction cycle is termed as growth per cycle (GPC) [3]. After few initial cycles the chemical composition of the substrate surface changes during deposition so that there should be a variation for GPC also. The GPC will set to a steady value after having initial variation. Based on the dependency of GPC on the number of reaction cycles, ALD process can be classified as (a) linear

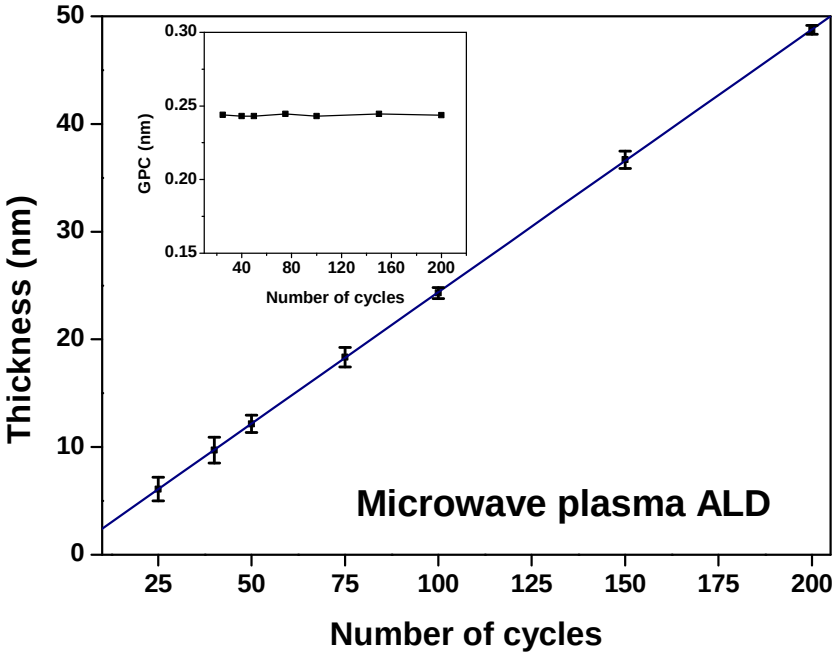

FIGURE 2.18: Thickness variation of microwave plasma assisted ALD-Al_2O_3 thin films with number of cycles of deposition. Inset figure shows the GPC with number of deposition cycles.

growth, (b) substrate-enhanced growth, (c) substrate-inhibited growth type 1 and (d) substrate-inhibited growth type 2. For linear growth the number of reactive sites on the surface does not change with number of cycles or the saturation is caused by steric hindrance [3]. The different types of GPC dependence on number of cycles is shown in figure 2.16. Figure 2.17 and figure 2.18 shows the thickness variation of the ALD grown Al_2O_3 thin films with number of deposition cycles. The inset figure shows the dependence of growth per cycle on number of deposition cycles. For both the cases, we obtained linearly increasing film thickness values with increasing number of deposition cycles. This consistent increase in film thickness with number of deposition cycles is a basic feature of atomic

layer deposition. So these curves confirm that the thin film deposition in home made ALD system is atomic layer deposition process. For thermal ALD, GPC vs number of cycles curve is substrate inhibited type and it is linear for microwave plasma assisted ALD. So steric hindrance is the limiting process that determines the 'monolayer' for microwave plasma assisted ALD process. But in the case of thermal ALD of Al_2O_3, the initial cycles were limited by both the number of available reaction sites and the steric hindrance. After a few cycles, the GPC curve was almost stabilized by initially grown Al_2O_3 layers.

2.7 Conclusions

A fully automated atomic layer deposition system was developed with an approximate cost of 12-13 lakhs. This home made system can work in plasma assisted mode and in conventional thermal mode ALD. The plasma used is a 2.45 GHz microwave based waveguide cavity plasma. The plasma is generated inside an applicator tube with a 1200 W microwave generator. An isolator, directional coupler, 3-stub tuner and sliding short are used for the efficient transmission and control of the microwave. The leakage of plasma is blocked with suitable cut-off tubes. A mesh is used to block the plasma from entering the deposition chamber and hence to keep the depositions remote from plasma. We succeeded to initiate and sustain the plasma only during oxygen precursor dosing. The ALD chamber is equipped with a movable 2 inch substrate holder. It is a top injection, flow type, medium vacuum, temporal ALD system. The ALD operates in rotary vacuum. Its ultimate vacuum capability is 10^{-5} mbar. The chamber wall and precursor lines are heated with heating tapes. The precursors are taken in bubblers. The precursor and purge gas lines are controlled with mass flow controllers, solenoid valves and needle valves.

The plasma was analysed using optical emission spectra. The broad and feeble spectrum observed near the surface of the substrate indicates that only less amount of energetic species reach the substrate surface. This is the expected desirable quality of a remote plasma system. The system parameters were optimized especially for Al_2O_3 thin films using TMA and H_2O/O_2 as the precursors. The optimum values of precursor pulse and purge timings for plasma assisted ALD and thermal ALD were found out for different substrate temperatures. The ALD nature of the thin film growth was identified from thickness versus number of cycle curve.

Chapter 3

Plasma assisted ALD-Al_2O_3 as a gate dielectric candidate

The present studies on atomic layer deposited Al_2O_3 dielectrics mainly focus on combinations with high mobility channels rather than with silicon [82, 83]. On silicon channel, Al_2O_3 is one of the most studied dielectric material. So by knowing the properties of ALD-Al_2O_3 as a gate dielectric material, it is easy to optimize the home made ALD system. Al_2O_3 is a material with variety of applications like solar cell passivation [84, 85], multilayer and compound dielectric materials for gate oxides [86, 87], encapsulation of organic & carbon based devices [88, 89], energy storage [90, 91], capacitors [92] etc. The essence of this chapter is the deposition and characterization of plasma assisted ALD-Al_2O_3 thin films in our home made ALD system and its comparison with Al_2O_3 film prepared in an industrial plasma assisted ALD system with emphasis on interfacial and bulk electrical characteristics of the thin films.

3.1 Short review on PALD-Al_2O_3 & reaction mechanisms

Trimethylaluminum and water based ALD is widely considered as a model system for atomic layer deposition. The surface chemistry and reaction mechanisms of ALD-Al_2O_3 was studied by several groups including our group [93, 94]. The binary reaction during ALD of Al_2O_3 is as follows

$$2Al(CH_3)_3 + 3H_2O \rightarrow Al_2O_3 + 6CH_4 \tag{3.1}$$

The reaction 3.1 can be divided in to two half reactions:

$$AlOH^* + Al(CH_3)_3 \rightarrow Al - O - Al(CH_3)_2^* + CH_4 \tag{3.2}$$

This is the first half cycle (reaction 3.2) of the reaction, by which $Al(CH_3)_3$ is chemisorbed by the surface -OH groups and form adsorbed $(\text{-O-})_n Al(CH_3)_{3-n}$ by releasing one CH_4.

$$Al(CH_3)^* + H_2O \rightarrow AlOH^* + CH_4 \tag{3.3}$$

During second half cycle(reaction 3.3), H_2O oxidises the metal and regenerates the -OH surface groups with the formation of CH_4. The initial works in this field was dominated by G. S. Higashi and C. G. Fleming [95], group of S. M. George [80, 96–99] and group of S. D. Elliot [100].
In 2003, S-W Choi et al. successfully deposited PALD Al_2O_3 with neutral oxygen atoms or oxygen ions from oxygen gas plasma. They noticed that the deposition rate increased more than 50% [35]. In the same year the usefulness of Al_2O_3 in a multilayer structure was studied by H B Park et al. They reported the dependence of fixed charges of the Al_2O_3/Si and HfO_2/Al_2O_3 interfaces greatly on the nitridation of the Al_2O_3 layer. Furthermore, they found that the interface trap density in the sample with

plasma-treated Al_2O_3 interlayer decreased from that of the nontreated sample by almost one order of magnitude [101]. Several compounds of aluminum like nitride, oxynitride and multilayer structures were studied during the initial period of PALD development [101, 102]. PALD was also done at different substrates and studied as follow ups of thermal ALD studies [103–106].

In the year 2006, the group lead by W. M. M. Kessels published their works on PALD-Al_2O_3 deposition for water permeation barriers [66]. They were interested in reaction mechanisms associated with the PALD-Al_2O_3. It is mainly because of their works the reaction mechanisms of the process was revealed upto the present level. In 2006, Kessels et al. reported their first work on PALD-Al_2O_3 reaction mechanism in a rapid communication. The precursors used were TMA and O_2 plasma. Quartz crystal microbalance, optical emission spectroscopy and quadrupole mass spectrometer were employed for studying the reaction mechanisms. They confirmed combustion like reactions by oxygen radical during the plasma half cycle and reaction similar to thermal ALD for the other half cycle. Evidences were also found for a concurrent thermal ALD like reaction pathway during plasma half cycle by formation of H_2O [107]. Again in 2008, they came with a better explanation of the PALD-Al_2O_3 reaction mechanism [108]. In this work, they utilized more in-situ tools such as spectroscopic ellipsometry, quartz crystal microbalance, quadrupole mass spectroscopy, optical emission spectroscopy and transmission infra-red spectroscopy. They confirmed the presence of H_2O, CO and CO_2 during the plasma half cycle. The presence of CH_4 and simultaneous reduction of O_2 represents the concurrent reaction pathway as suggested in their earlier work. They represented the complete reaction as follows

$$AlOH^* + Al(CH_3)_3(g) \rightarrow AlOAl(CH_3)_2^* + CH_4(g) \tag{3.4}$$

$$Al(CH_3)^* + 4O(g) \rightarrow AlOH^* + CO_2(g) + H_2O(g) \tag{3.5}$$

They identified the formation of increased number of -OH surface states with decreasing substrate temperature as the reason for higher growth per cycle at low temperature. A detailed account of the studies done by the group of Kessels to understand the reaction mechanisms are included in their Al_2O_3 case study paper [109].

Using ECR microwave plasma, room temperature Al_2O_3 deposition was facilitated by a Korean group on plastic substrates at a GPC of 2.2 A^0/cycle [110]. A capacitively coupled plasma assisted ALD-Al_2O_3 at room temperature was done by D.C. Cameron and T. O. Kaariainen [68]. In their study plasma was very close to the substrate surface and they used a grid to prevent film damage by the plasma. From their experiment, it was clear that an optimized plasma to substrate distance, O_2 pulse length and plasma power are essential to avoid the inclusion of reaction products like CO, CO_2, H_2O, CH_4 and to avoid the CVD like counter reaction originally proposed by Kessels group. They also reported incorporation of N_2 in to the film with increasing plasma power. In 2009, Kessels group together with NXP semiconductor deposited Al_2O_3 and TiN sequentially in a single reactor at the same temperature and studied the elecrical performance. From capacitance-voltage (C-V) measurements, a dielectric constant (κ) of 8.7$\pm$0.1 was extracted for Al_2O_3. Even though there was no direct dependence on the deposition temperature in the range 350 to 400^0C, the stack deposited at 400 ^{0}C demonstrated significantly lower C-V hysteresis of $\sim$50 mV. A negative fixed oxide charge density of 9.6$\pm$ 0.2 $\times 10^{12}$cm^{-2} was found to be present at the Al_2O_3/p-Si interface [111]. Dendoovan et al. made a detailed analysis on the conformality of the PALD-Al_2O_3 thin films deposited using inductively coupled plasma. The precursors were TMA and O_2 plasma. They conducted the study by depositing the films on macroscopic test structures with aspect ratios of $\sim$5, 10, and 22. Through comparison with the thermal TMA/H_2O process, they concluded that the conformality of the plasma based process

is more limited due to the surface recombination of the O-radicals during the plasma step. The conformality could be improved by raising the gas pressure or the RF power [112]. Group lead by Kessels also made process and simulation studies on conformality of PALD and they found aspect ratio >10 nm is challenging [113].

3.2 Preparation of plasma assisted ALD-Al_2O_3 thin films

Al_2O_3 thin films were deposited on Boron doped p-type silicon (100) wafer substrates (1-5 Ω cm) by Microwave Plasma assisted ALD (MPALD) and by inductively coupled Radio Frequency plasma assisted ALD (RFALD). Before deposition the silicon wafers were cleaned with standard RCA (Radio Corporation of America) procedure. The RCA cleaning includes standard cleaning 1 (SC1) followed by buffered hydrofluoric acid (HF) dip and standard cleaning 2 (SC2) again followed by buffered HF dip. After the final HF dip the substrates were loaded to the ALD chamber at the earliest. Microwave plasma assisted depositions were done with our home made ALD system and the properties of the deposited films were compared with RF plasma based depositions done using Cambridge NanoTech's Fiji F200. The microwave plasma system design, fabrication and process optimization are explained in chapter 2.

The Fiji F 200 is a modular high-vacuum ALD system that accommodates a wide range of deposition modes using a flexible system architecture and multiple configurations of precursors and plasma gases. The hyperboloid reactor geometry combined with the paraboloid substrate heater creates a laminar precursor and remote plasma generated radical flow [114]. The Fiji F 200 can work in conventional thermal mode ALD and in plasma assisted mode ALD (Inductively coupled radio frequency plasma). It can

handle 200 mm wafers. The maximum possible deposition temperature is 500^0C. In standard format it has 4 precursor lines with heatable (upto 200^0C) solenoid valves. The entire reaction chamber is covered with a heating jacket. It has integrated mass flow controllers for every gases in use. There are provisions for connecting in situ diagnostic tools. The entire system is interfaced using a Labview control [115].

Both microwave plasma assisted and RF plasma assisted modes of ALD depositions were carried out at different substrate temperatures to study the effect of deposition temperature on the film properties. In microwave plasma assisted ALD the temperature variation was from room temperature to 200^0C whereas in RF plasma assisted mode it was from 40^0C to 200^0C. The formation of native oxide was unavoidable in our experiments. For all Al_2O_3 depositions the precursors were Trimethylaluminum (TMA)

Temperature (^{0}C)	TMA Purge (s)	O_2 Purge (s)
300	5	5
250	8	5
200	10	5
150	20	5
100	30	5
75	60	5
50	120	5
25	180	5

TABLE 3.1: Standard precursor purge timings for Al_2O_3 deposition in Cambridge NanoTech's Fiji F200.

(Sigma-Aldrich) and plasma produced with high purity oxygen (5N purity). Standard recipe provided by Cambridge NanoTech was followed for RF plasma ALD depositions. The precursor dosage and purge timings by the Cambridge NanoTech's standard recipe are given in table 3.1. During microwave plasma assisted deposition, the chamber pressure was kept at 1 mbar. For microwave plasma assisted depositions up to 100^0C, the reactor wall was maintained at substrate temperature. For higher substrate

temperatures the reactor wall was kept at 100^0C. For RF plasma assisted depositions, the chamber pressure during deposition was kept around 0.1 mbar and the maximum chamber wall temperature was 150 ^{0}C.

3.3 Analysis of PALD-Al_2O_3 thin films

The dielectric constant (κ) for Al_2O_3 is 8.9, which is higher than that of the conventional oxide SiO_2. But it is less than that of HfO_2, which is the industrial standard for modern era microelectronics from 2007 onwards [116]. Al_2O_3 was studied heavily by the industry and research communities as an alternative gate dielectric material. Al_2O_3 thin films can remain in amorphous form even at semiconductor processing temperatures. In addition, Al_2O_3 satisfies most of the high-κ dielectric requirements like large band gap, good enough band offset values, kinetic stability, thermodynamic stability with silicon etc. [52, 117]. The major draw back of Al_2O_3 is its comparatively lower κ value.

3.3.1 Thickness, density & refractive Index

The thickness and refractive index of the deposited thin films were extracted from ellipsometric studies. The basics of ellipsometric technique is the measurement of polarization state of a reflected light. When light is reflected from a surface, it will undergo a phase shift and the reflected light will have a smaller amplitude. Spectroscopic ellipsometry is a non destructive contact less tool mainly used to measure the thickness and optical constants of thin films. The change in polarization during reflection or transmission on the sample surface is measured as follows in comparison

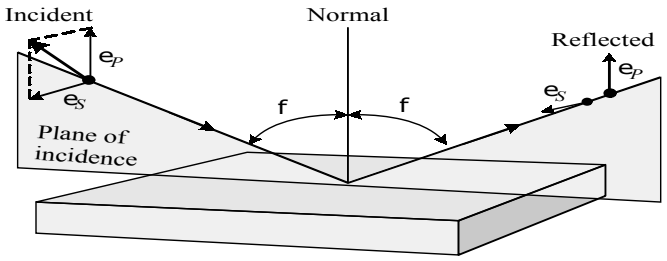

FIGURE 3.1: Configuration for ellipsometric measurements.

with a known initial polarization. The ratio of reflection coefficient,

$$\rho = \frac{R_p}{R_s} = \tan(\Psi)e^{i\Delta} \tag{3.6}$$

where R_p and R_s are the reflection coefficients for the parallel and perpendicular components of the electric field of the polarized light and Ψ and Δ are known as ellipsometric angles. Every spectroscopic ellipsometer requires one light source with polarization generator, sample, polarization analyser and a detector. The configuration of the incident and reflected beams is shown in figure 3.1. Presently, there are several kind of ellipsometric tools available in market like interferometric, variable angle and variable wavelength ellipsometry. In our study, we used the Sentech Ellipsometer SE800, for which the spectral range is 240 nm to 930 nm. All the measurements were done at a fixed incident angle of 70^0. The X-ray reflectivity (XRR) is another tool used for thickness measurements. XRR measurements will give the thickness, density and both surface and interfacial roughness. X-ray reflectivity, also known as X-ray reflectometry, is a non-destructive, non-contact method of film characterization. When X-rays are irradiated on to the sample at very low angles there will be total reflection of X-rays from the sample surface. As the angle of irradiation is gradually increased beyond a certain angle called critical angle, which is dependent on the material, X-rays are reflected from the interfaces of

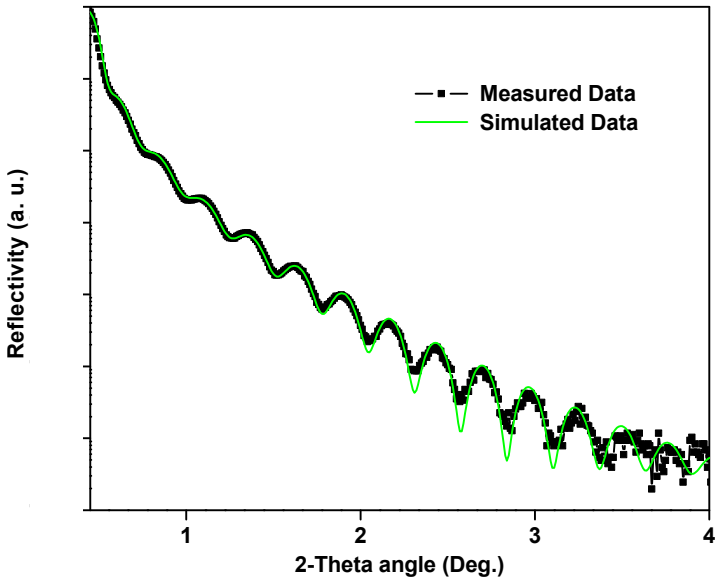

FIGURE 3.2: X-ray reflectivity spectra for MPALD thin film deposited at room temperature with the simulation fit over the measured data.

the sample and give rise to interference fringes. As the semiconductor industry is dealing with 22 nm technology and beyond, X-ray reflectivity is the only non-contact, non-destructive standardless technique to measure thickness, density and roughness of ultra thin amorphous, polycrystalline and single crystal metal films at this thickness range [118]. XRR can measure thickness in the range of 0.1 nm to 1000 nm, material density variation <1-2% and surface and interface roughness <3-5 nm. In our investigations we used two different XRR tools: (1) Rigaku Smartlab high resolution X-ray difractometer (2) PANalytical Xpert Pro materials research diffractometer. Both these use 3 kW solid state generator and the X-ray source is Cu K-α.

Figure 3.2 shows the measured X-ray reflectivity spectra for microwave

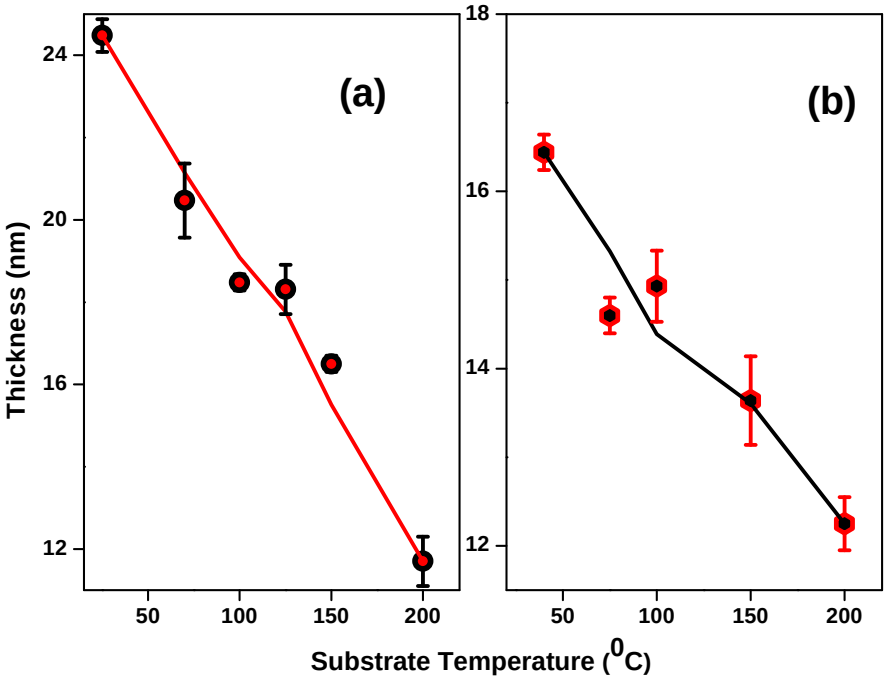

FIGURE 3.3: Thickness variation of Al_2O_3 thin films with substrate temperature for (a) Microwave plasma assisted ALD and (b) RF plasma assisted ALD.

plasma assisted ALD Al_2O_3 deposited at room temperature. The simulation fit over the measured data will give thickness, density and refractive index of the film. The periodicity of the fringes would be proportional to the thickness of the film, the fall of intensity would be proportional to the roughness of the film and amplitude of the fringes would be proportional to the density of the top and bottom layers. For room temperature MPALD-Al_2O_3, the measured thickness was 24.48 nm with 2.67 g/cm^3 density and have a refractive index of 1.5. With increasing deposition temperature the density of the deposited film was found to increase. At 200^{0}C, the density became 2.9 g/cm^3 and the film thickness reduced to

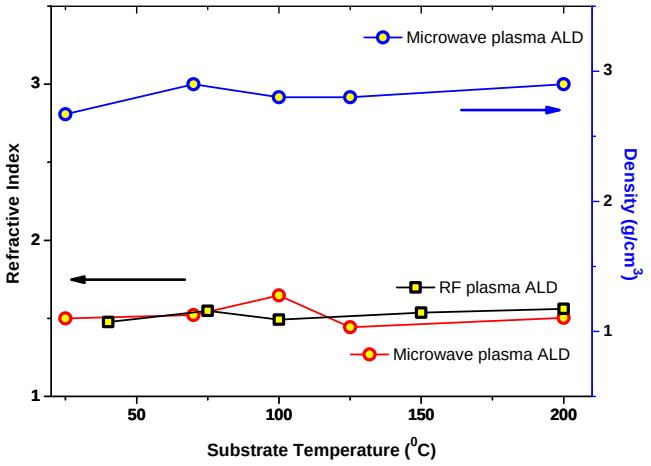

FIGURE 3.4: Substrate temperature dependence of refractive index for MPALD-Al_2O_3 & RFALD-Al_2O_3 and density dependence for MPALD-Al_2O_3 thin films.

11.7 nm. Similar behaviour was already reported for atomic layer deposited Al_2O_3 [36, 119].

Figure 3.3 shows the thickness variation of ALD-Al_2O_3 thin films with substrate temperature. The total number of deposition cycles was kept constant at 100 cycles for all the deposition temperatures. The ALD-Al_2O_3 film thickness was found to decrease with increasing substrate temperature. This remained valid for both microwave plasma and RF plasma modes of ALD. At lower temperatures the growth per cycle for MPALD-Al_2O_3 was greater than that for RFALD-Al_2O_3. The maximum growth per cycle of 2.4 A^0/cycle was obtained for MPALD at room temperature. This much growth is usually rare in ALD. At the maximum substrate temperature (200^0C), the film thickness was found to be around 12 nm for both modes of ALD. The decrease in thickness with temperature was noted earlier by other research groups working in ALD and the thickness reduction was attributed to reduced number of OH surface sites. At higher

temperatures dehydroxilation will take place and it will cause incomplete surface reactions [3, 80, 93, 120].
The refractive index for the crystalline hexagonal Al_2O_3 is 1.767 [68]. The reported refractive index value for atomic layer deposited Al_2O_3 for TMA and H_2O process is around 1.6 [98, 119]. But the reported refractive index value for plasma based method is around 1.5 [68]. Figure 3.4 shows the values of refractive index with varying substrate temperature. Similar to earlier reports for both plasma assisted modes of ALD-Al_2O_3 the obtained refractive index was more or less 1.5.

3.3.2 Film composition & morphology

The determination of crystal structure, surface morphology and composition are critical in understanding the electrical performance on the basis of its physical and chemical properties. A grain boundary in a crystalline dielectric can act as a source of leakage in the film, so it is necessary to know whether the film is crystalline or not. By knowing the composition we can correlate the chemical structure to device performance. The characterization of the surfaces is also crucial for electronic materials.

3.3.2.1 High resolution X-ray diffraction

X-ray diffraction is a non destructive technique used to obtain the structural information of materials. A monochromatic beam of X-rays having wavelength in the order of inter atomic distance is used for the structure determination. The sample scatters the X-ray in all directions. The periodic arrangement of atoms in crystallographic planes causes the X-ray beam to form diffracted beam in certain directions. The position of the diffracted beam is given by Bragg's law,

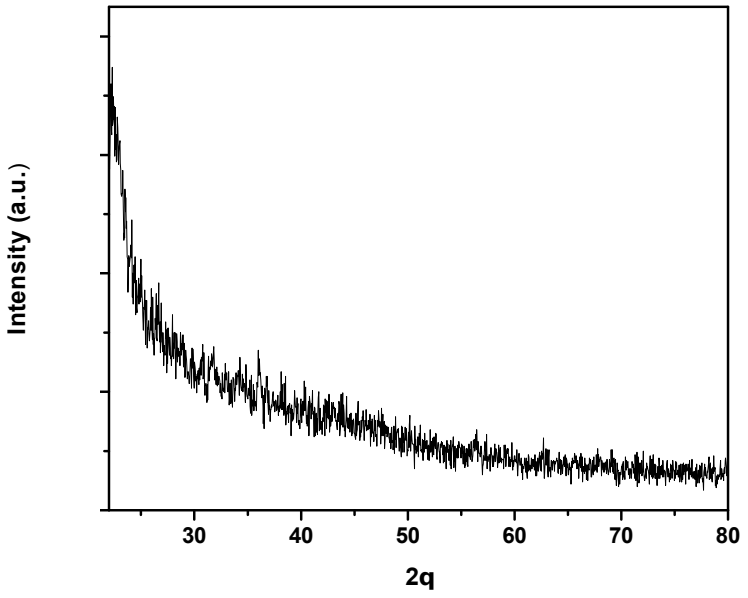

FIGURE 3.5: X-Ray diffraction spectra of MPALD-Al_2O_3 thin film deposited at room temperature

$$n\lambda = 2dsin\theta \tag{3.7}$$

where n is the order of diffraction, θ is the angle of incidence, λ is the X-ray wavelength and d is the distance between inter atomic planes from where the X-rays are scattering. Glancing angle X-ray diffraction (GXRD) is used to avoid the influences from the substrate. In GXRD, the X-ray beam is directed to the sample in a very small angle, below the critical angle. Hence it will penetrate only a minimum substrate.

The GXRD measuremets were done with Panalytical XPert Pro multipurpose diffractometer. Diffraction data is acquired by exposing samples to Cu-Kα radiation, which has a characteristic wavelength (λ) of 1.5405 A^0. X-rays were generated from a Cu anode supplied with 40 kV and a current of 40 mA. Figure 3.5 shows the GXRD spectra of MPALD-Al_2O_3 film deposited at room temperature. There is no specific peaks in the GXRD

spectrum. This indicates the amorphous nature of the MPALD-Al_2O_3 thin film deposited at room temperature.

3.3.2.2 X-ray photoelectron spectroscopy

XPS spectra are obtained by irradiating a solid surface with a beam of X-rays while simultaneously measuring the kinetic energy and electrons that are emitted from the top 1-10 nm of the material being analyzed. Using XPS, the electronic state and chemical state of the material can be analysed from the surface. To analyse the bulk of a material either etching or sputtering is usually incorporated with XPS. A photoelectron spectrum is recorded by counting ejected electrons over a range of electron kinetic energies. Peaks appear in the spectrum from atoms emitting electrons of a particular characteristic energy. The energies and intensities of the photoelectron peaks enable identification and quantification of all surface elements (except hydrogen) [121]. The chemical state of an atom alters the binding energy (BE) of a photoelectron which results a change in measured kinetic energy (KE). The binding energy is related to the measured photoelectron kinetic energy by the simple equation,

$$BE = h\nu - KE \tag{3.8}$$

where hν is the photon (X-ray) energy. The chemical or bonding information of the element is derived from these chemical shifts.

Kratos Analyticl's Amicus 3400 and ULVAC-PHI 5000 Versaprobe II systems were used for XPS measurements. The composition and chemical bonding states of the Microwave plasma assisted ALD-Al_2O_3 thin films were analysed using X-ray photoelectron spectroscopy. The C 1s hydrocarbon peak at 285 eV is used as the reference. Excess oxygen was detected in Al_2O_3 thin films deposited at various substrate temperatures. The O/Al ratio of the films are tabulated in table 3.2. Figure 3.6(a)

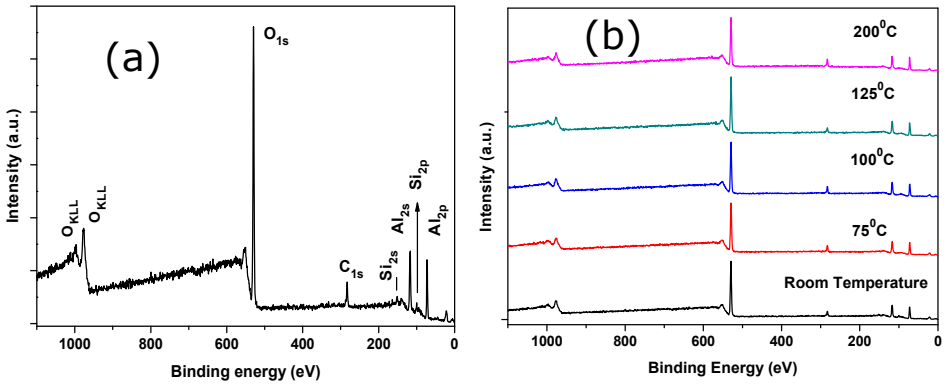

FIGURE 3.6: (a) XPS spectra of MPALD-Al_2O_3 deposited at room temperature (b) XPS spectra of MPALD-Al_2O_3 deposited at different substrate temperatures.

Substrate temperature(^{0}C)	O/Al Ratio
Room temperature	2.12
75	2.10
100	2.02
125	1.98
200	1.92

TABLE 3.2: O/Al ratio for microwave plasma assisted ALD-Al_2O_3 films for different substrate temperatures, as obtained from XPS.

shows the XPS spectra of MPALD-Al_2O_3 thin films deposited at room temperature and annealed at 400^{0}C for 30 minutes in a foaming gas ambient. Al 2s peak at 119.2 eV and Al 2p peak at 74.3 eV are present in the spectra. According to the data of NIST X-ray photoelectron spectroscopy database, the appearance of Al 2s at 119.2 eV and Al 2p at 74.3 eV confirms the formation of Al_2O_3 [122]. Al 2p at 74.3 eV belongs to oxidized aluminium and O 1s belongs to metal oxide. The peak positions of Al 2p and O 1s remain invariant with substrate temperature and hence their binding energy difference also remains the same, which indicates the

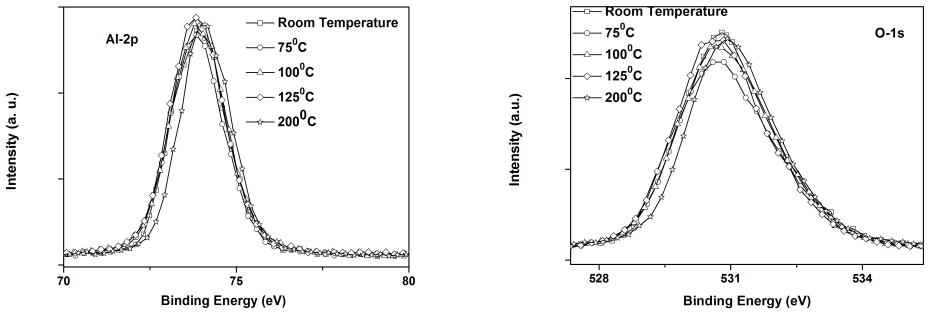

FIGURE 3.7: Photoelectron spectra for Al 2p & O 1s transitions obtained for MPALD-Al_2O_3 films deposited at different substrate temperatures.

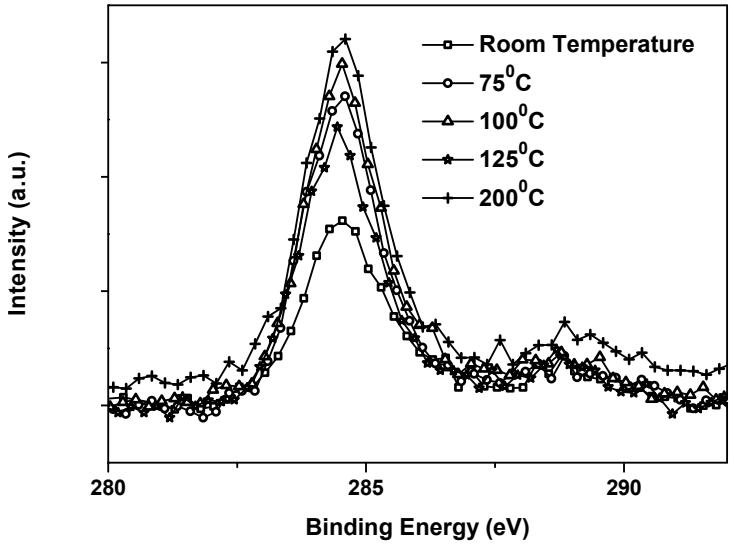

FIGURE 3.8: C-1s photoelectron spectra of MPALD-Al_2O_3 films deposited at different substrate temperatures.

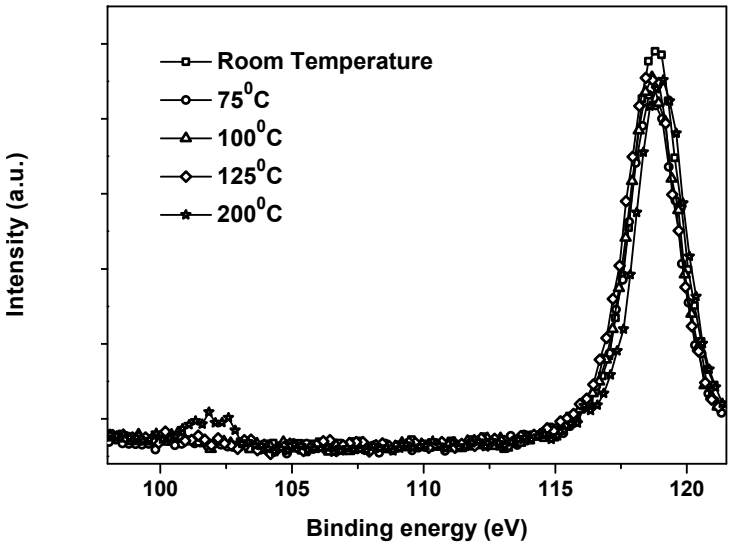

FIGURE 3.9: Al 2s photoelectron spectra of MPALD-Al_2O_3 prepared at different substrate temperatures.

existence of aluminium and oxygen only in one charge state irrespective of substrate temperature. Figure 3.6 (b) shows the XPS spectra recorded for MPALD-Al_2O_3 deposited at different substrate temperatures. No visible variation was noticed with varying substrate temperature. The O 1s and Al 2p peaks for the MPALD-Al_2O_3 at different substrate temperatures are shown in figure 3.7. No apparent broadening was observed for Al 2p curve at all deposition temperatures. The broadening at higher binding energy side of O 1s spectra indicates the formation of hydroxyl groups [123]. The MPALD-Al_2O_3 thin film deposited at 200^0C shows a shift towards the higher binding energy for both Al 2p and O1s spectra. This shift may be due to silicate formation at higher deposition temperature [124]. The C 1s and Al 2s peaks for MPALD-Al_2O_3 films deposited at varying substrate temperature are given in figure 3.8 and 3.9 respectively. The C 1s spectra shows a variation in carbon content with deposition temperature of MPALD-Al_2O_3 thin films. The small peak around 288

eV indicates carbonate formation [125]. In Al 2s spectra we can see the Si 2s peak at 102 eV and is prominent for high temperature deposition, representing the formation of SiO_2 interfacial layer over silicon wafer.

3.3.2.3 Field emission scanning electron microscopy

In scanning electron microscope (SEM) the sample surface is scanned using a finely focused electron beam. The electron beam scanning will generate secondary electrons, backscattered electrons and characteristic X-rays. These emissions are collected by the detector and analysed to get surface topography of the surface to be analysed. In field emission

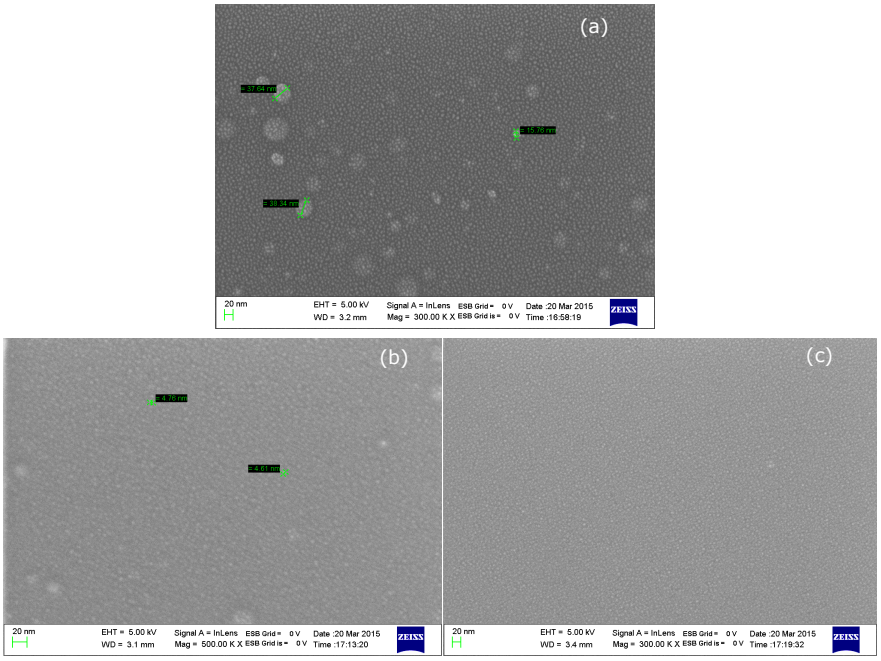

FIGURE 3.10: FESEM images of MPALD-Al_2O_3 films prepared at (a) room temperature, (b) 125^0C and (c)200^0C. (Scale 20 nm)

scanning electron microscopy (FESEM), a field emission cathode is used as the electron gun. The field emission cathode can provide narrow beam

of electrons having higher energy. SEM can be used to characterize the porosity, surface roughness, grain size and distribution of the film. FE-SEM can provide 3 to 6 times better resolution than conventional SEM. Reduced penetration of low kinetic energy electrons probes closer to the immediate material surface and electrocharging of the sample will be less in FESEM [126].

Figure 3.10 shows the FESEM images of MPALD-Al_2O_3 films deposited at different temperatures taken using Zeiss Ultra 55 FESEM instrument, which can provide 1nm SEM imaging resolution. The acceleration voltage range of Zeiss Ultra 55 FESEM is 0.1 - 30 kV. The FESEM images at higher temperatures show small island like structures distributed uniformly over the film, having feature size around 4 nm. The feature size and density of these islands were more (around 7 nm) for room temperature MPALD-Al_2O_3 deposition.

3.4 MOS capacitor (MOScap)

The study of MOS capacitor forms the best suited method for the MOS based system analysis. MOScap fabrication steps are similar to that used in integrated circuit fabrication. Therefore the MOScap provides direct measurement and monitoring of the MOS system as it is actually fabricated and used in the integrated circuit. Moreover the MOS capacitor has the advantage of simplicity of fabrication and analysis [127]. The insulator layer between the metal and the semiconductor acts like a big energy barrier between the metal and the semiconductor. Because of this energy barrier, the flow of carriers between metal and semiconductor is blocked. So the application of a bias across the MOS does not result in a current flow. But as the polarity and magnitude of the applied bias change, there will be a corresponding change in the carrier concentration

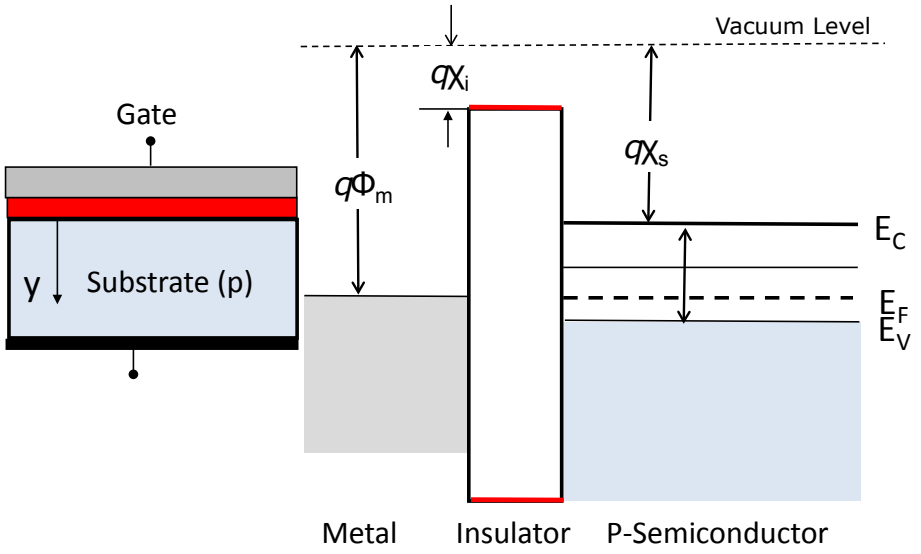

FIGURE 3.11: Cross sectional view of a MOS capacitor on the left and the band diagram for an ideal MOS at equilibrium on the right side.

and band structure of the semiconductor. These changes bring about the important electrical characteristics of MOScap. Figure 3.11 shows the cross sectional view of a MOS capacitor on the left and the band diagram for an ideal MOS at equilibrium on the right side. For an ideal MOS, the work function difference between the metal and semiconductor should be zero. The insulator should be perfect so that no dc current flows through it and there are no charged defects in the insulator. The change in carrier concentration can be determined with the help of band bending approximation. The band bending approximation assumes that the density of states in the conduction and valance bands is not changed by an electric field. In band bending approximation, the only effect of an electric field is to shift all the energy levels in the conduction and valance bands by a constant amount determined by the potential at a given point in the semiconductor [127]. Using the band bending approximation we can calculate the hole and electron density distribution as a function of position. For a p type semiconductor, the hole density in the valance band in the

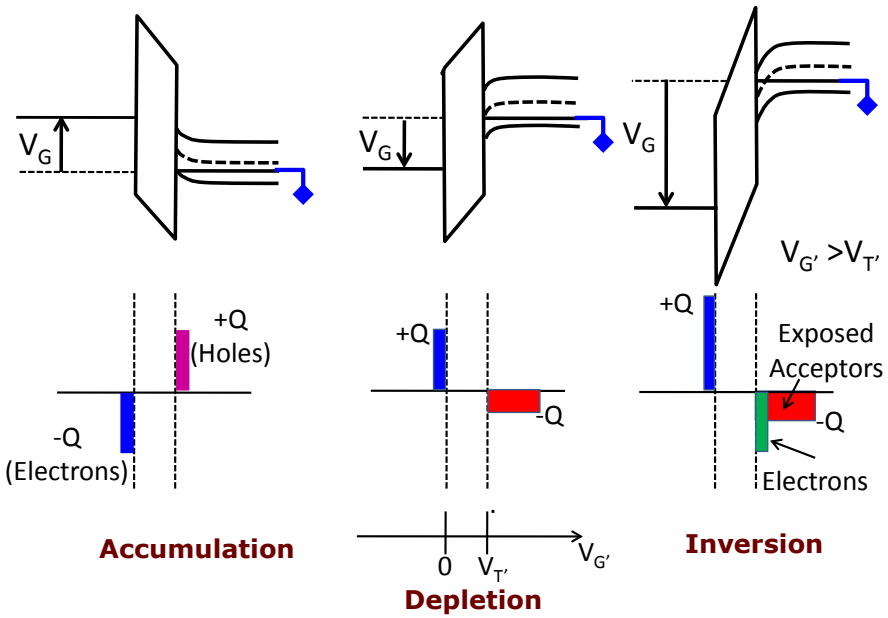

FIGURE 3.12: MOScap under different biasing conditions and the corresponding charge variation in the structure.

presence of an electric field is

$$p(x) = N_A \exp(-\frac{q\psi_x}{kT}) \tag{3.9}$$

where N_A is the acceptor concentration, q the elementary charge, kT is the energy equivalent of temperature T and ψ_x is the potential difference between valance band and the fermi level. Similarly for n type semiconductor,

$$n(x) = N_D \exp(\frac{q\psi_x}{kT}) \tag{3.10}$$

where N_D is the donor concentration. Under the ideal conditions, the work function difference between the metal and the semiconductor is given by

$$\phi_{ms} \equiv \phi_m - (\chi_s + \frac{E_g}{2q} + \phi_F) = 0 \tag{3.11}$$

where ϕ_{ms} is the metal-semiconductor work function difference, ϕ_m is the metal work function, χ_s is the electron affinity of semiconductor, E_g is the semiconductor band gap and ϕ_F is the bulk or fermi potential of semiconductor. For a p type semiconductor,

$$\phi_F = \frac{KT}{q} \ln \frac{N_A}{n_i} \tag{3.12}$$

where n_i is the intrinsic carrier concentration. Biasing a MOS capacitor gate with some voltage will give rise to three specific situations, namely-accumulation, depletion and inversion as shown in figure 3.12. In accumulation, the majority carriers from the semiconductor will get accumulated at the insulator-semiconductor interface. In depletion, the majority carriers are chased back by the applied potential and a charged region is formed by the uncompensated dopant atoms. A minority carrier layer will be formed at the insulator-semiconductor interface during the inversion. The variation of charges at the interface during accumulation, inversion and depletion is shown in figure 3.13. Under small signal ac, the depletion width expands and contract slightly. An ac charge appears at the bottom of the depletion layer as shown in figure 3.13(b). 3.13(c) shows the quasistatic case, i.e., the p-n junction act as the source of electron and the inversion charge can respond simultaneously to the ac signal. In high frequency case, there is no quick supply of electrons, the electron source is the slow thermionic generation, and the inversion charges cannot respond to the ac signal.

Another important term in MOS analysis is the flat band voltage. Flat band voltage is the voltage required to nullify internal electric fields in the MOScap. At flat band voltage there will be no net electric charge in the MOS capacitor. For an ideal MOScap, flat band voltage should be zero. For a real MOScap, in the absence of any oxide charges, flat band voltage will be equal to the work function difference between the metal gate and

semiconductor.

3.5 Characterizations of plasma assisted ALD-Al_2O_3 based MOScap

The major tool used in the characterization of a MOScap is the Capacitance-Voltage (C-V) characteristics. To a device specialist the MOScap C-V characteristics is like a picture window, a window revealing the internal nature of the structure [128]. The pioneering works by Grove et al. [129] developed the C-V measurement as a powerful tool for the evaluation of MOScap as an integral part of MOSFET. A MOScap is a non-linear capacitor, so the differential capacitance which gives the rate of change of charge with voltage is important, in comparison with the static capacitance for a normal capacitor. To measure the capacitance as a function of gate bias in steady state a small AC voltage is superimposed on the gate bias. The C-V measurements can give insulator layer thickness, semiconductor doping concentration, threshold voltage for inversion and the flat band voltage. In addition, a careful analysis of the C-V characteristics can give the defects in insulator layer and the interfacial layer traps present in the system.

The capacitance is usually measured with an LCR meter, which measure the differential capacitance:

$$C = \frac{dQ}{dV} \tag{3.13}$$

In a typical MOScap C-V characteristics, we can distinguish the accumulation, depletion and inversion regions. In an accumulated MOScap only majority carriers take part in the operation. The majority carriers can operate as fast as 10^{-10} to 10^{-13} second. So the MOScap can follow

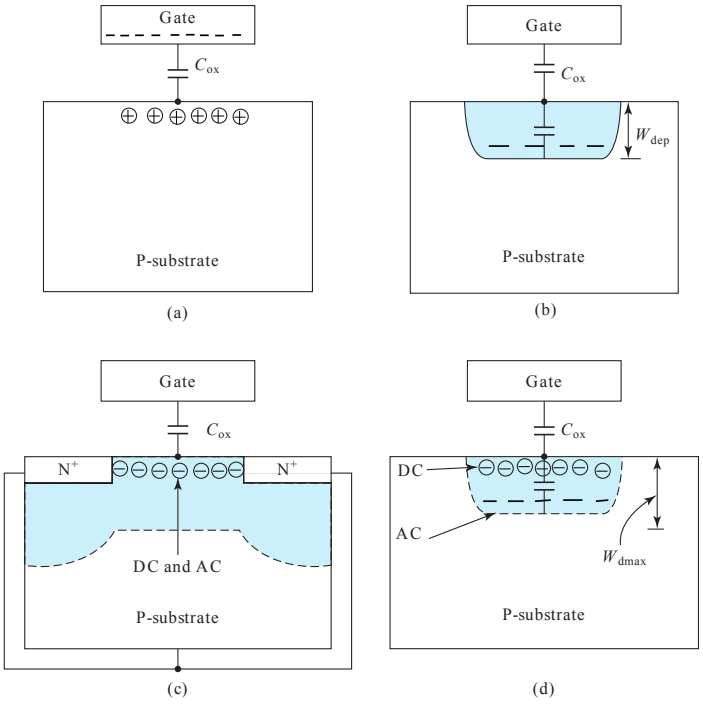

FIGURE 3.13: Illustration of the MOS capacitor in all bias regions with the depletion layers shaded. (a) Accumulation region (b) depletion region (c) inversion region with efficient supply of inversion electrons from the N region corresponding to the transistor C-V or the quasi-static C-V and (d) inversion region with no supply of inversion electrons (or weak supply by thermal generation) corresponding to the high-frequency capacitor C-V case. [130]

a usual small signal frequency of 1MHz or less quasistatically. Then,

$$C_{acc} = C_{oxide} = \frac{\kappa \varepsilon_0 A}{d} \tag{3.14}$$

where C_{acc} is the accumulation capacitance which would be equal to oxide capacitance (C_{oxide}), κ is the dielectric constant, ε_0 is the vacuum permittivity, A is the area of the MOS capacitor and d is the thickness of the dielectric layer. In depletion, only majority carriers will contribute to the process, but now the depletion layer width also widens with a quasistatic

variation with AC signal and the situation is like two parallel plate capacitors in series (C_{ox} and $C_{semiconductor}$). So we can write the capacitance of the MOS in the depletion region (C_{dep}) as

$$C_{dep} = \frac{C_{oxide}C_{semiconductor}}{C_{oxide} + C_{semiconductor}} \tag{3.15}$$

where $C_{semiconductor}$ is the capacitance due to depletion region in semiconductor. In inversion, for the semiconductor two alternative mechanisms are available to compensate the gate voltage: (1) fluctuate the depletion width and (2) minority carrier accumulation at the semiconductor surface. The second one is a slow process. So the MOScap will select in between these two based on the measurement frequency.

$$C_{inv} = C_{oxide} \quad \text{for} \quad \omega \to 0 \tag{3.16}$$

$$C_{inv} = \frac{C_{oxide}C_{semiconductor@Threshold}}{C_{oxide} + C_{semiconductor@Threshold}} \tag{3.17}$$

where $C_{semiconductor@Threshold}$ is the capacitance due to depletion region in semiconductor at the onset of inversion. Figure 3.13 shows the schematic representation of MOScap at different biasing regimes. A real MOScap will have some defect states like fixed charges in the oxide and interface trap charges. The interface states can change their charge on communication with the semiconductor. Any voltage applied to the gate will drop partially across the oxide and partially across the semiconductor, i.e.,

$$V_g = V_{FB} + V_{ox} + \phi_s \tag{3.18}$$

where V_{FB} is the flat band voltage, V_{ox} is the oxide voltage and ϕ_s is the surface potential. Flat band voltage is the voltage drop across the MOS at zero applied gate bias. The capacitance for a real MOS can be written as

$$C = -\frac{dQ_s + dQ_{it}}{dV_{ox} + d\phi_s} \tag{3.19}$$

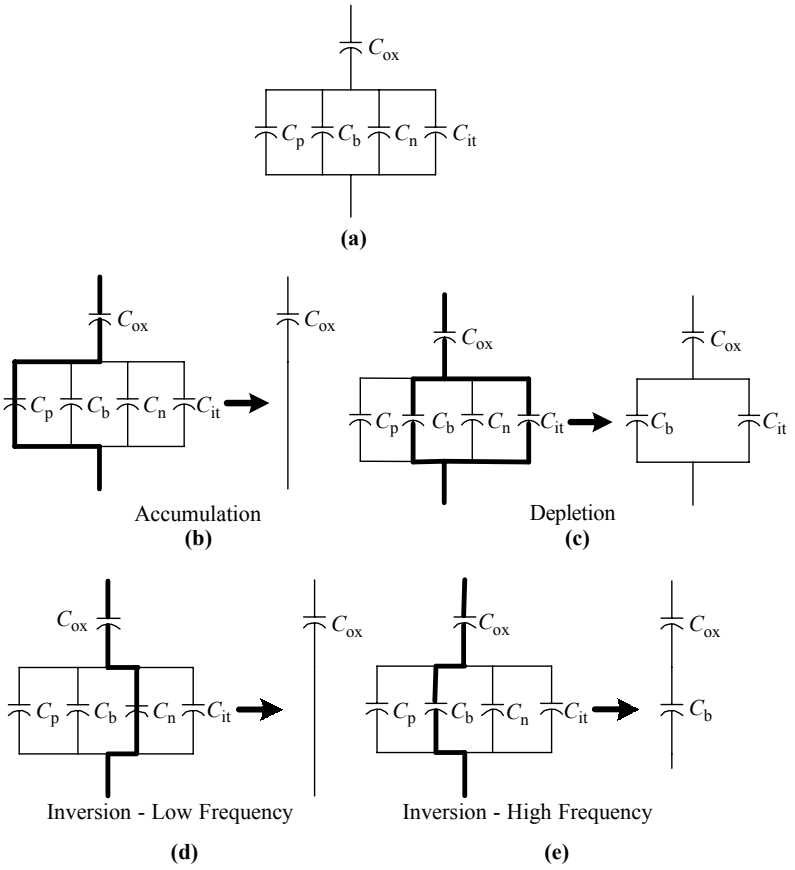

FIGURE 3.14: (a) Equivalent circuit of MOS capacitor represented in equation 3.20. (b) to (e) Illustration of the MOS capacitor in different bias regions.

where Q_s is the semiconductor charge density which consists of hole charge density Q_p, space charge region bulk charge density Q_b and electron charge density Q_n. Q_{it} is the interface trap state density. With $Q_s = Q_p + Q_b + Q_n$ the capacitance becomes [131]

$$C = \frac{C_{ox}(C_p + C_b + C_n + C_{it})}{C_{ox} + C_p + C_b + C_n + C_{it}} \tag{3.20}$$

The equation 3.20 can be represented by the equivalent circuit in figure 3.14(a). For negative gate voltages, the surface is heavily accumulated and

Q_p dominates. Now C_p should be very high and approach a short circuit (figure 3.14(b)). At small positive gate voltages the semiconductor surface becomes depleted and the space charge region and interface trap charge capacitance become important. In total, these two parallel capacitors act in series to the oxide capacitance (figure 3.14(c)). At inversion there would be accumulated electrons and for low ac frequencies they respond simultaneously to the signal and the effective capacitance becomes C_{ox} (figure 3.14(d)). Figure 3.14(e) is for the case when inversion charges can not follow the applied ac.

3.5.1 MOS fabrication

Al/Al_2O_3/p-Si MOS capacitors were fabricated using Al_2O_3 thin films prepared by microwave plasma assisted ALD and by RF plasma assisted ALD. The Al_2O_3 dielectric thin films deposited at different substrate temperatures were used for MOScap fabrication. Two different ALD systems were used for the deposition of the thin dielectric films: (1) Home made microwave plasma assisted ALD system and (2) Fiji F-200 RF plasma assisted ALD system by Ultratech (Cambridge NanoTech). Details regarding ALD systems and the thin film preparation conditions are already detailed in the previous sections of this thesis (microwave plasma assisted ALD in chapter 2 & RF plasma assisted ALD in section 3.2).
For all the depositions Boron doped p-type silicon (100) wafers with 1-5 Ω-cm resistivity were used as the substrate. Before depositions, the silicon wafers were cleaned by standard RCA procedure followed by hydrofluoric acid dip to remove the native oxides over the wafer. Electronic grade chemicals purchased from Sigma Aldrich were used for the silicon substrate cleaning. Al_2O_3 thin films were deposited over Si wafer at varying substrate temperatures. The silicon substrate and the deposited Al_2O_3 act as the semiconductor and oxide respectively for the MOS capacitor.

The gate metal of the MOS capacitor was made with aluminium in the form of small dots. Aluminium metal depositions were done using vacuum thermal evaporator at a vacuum better than 2×10^{-5} mbar. Shadow masks were used for the deposition of dot metal electrodes. Two different shadow masks were used through out this work. One of them has dots of three different sizes of 500 μm, 600 μm and 700 μm and the second mask has 400 μm and 1000 μm dots. The unpolished back side of the silicon wafer was cleaned with electronic grade buffered hydrofluoric acid (5:1) and then coated with 100 nm aluminium metal for back contact. The device was then annealed at 400^0C for 30 minutes in foaming gas (90% nitrogen and 10% hydrogen) ambient. Table 3.3 lists the different MOS capacitors fabricated for the study. Except the Al_2O_3 deposition conditions, all the fabrication and treatment steps done were similar for all the MOS capacitors.

MOS capacitor	Al_2O_3 deposition condition
MPALD-RT	Microwave plasma ALD @ room temperature
MPALD-75	Microwave plasma ALD @ 75^0C
MPALD-100	Microwave plasma ALD @ 100^0C
MPALD-125	Microwave plasma ALD @ 125^0C
MPALD-200	Microwave plasma ALD @ 200^0C
RFALD-40	RF plasma ALD @ 40^0C
RFALD-75	RF plasma ALD @ 75^0C
RFALD-100	RF plasma ALD @ 100^0C
RFALD-150	RF plasma ALD @ 150^0C
RFALD-200	RF plasma ALD @ 200^0C

TABLE 3.3: List of different MOS capacitors fabricated for the study.

3.5.2 Oxide capacitance & dielectric constant

The purpose of replacing SiO_2 based dielectric in microelectronics is to have a new material with high enough dielectric constant so that it can provide a lesser electrical thickness with the same physical thickness as that of SiO_2 (the equivalent oxide thickness). At accumulation the capacitance contribution is only from the dielectric and the accumulation capacitance can directly give the oxide capacitance and hence the dielectric constant. The capacitance-voltage characterizations of the MOS devices were done at equilibrium. For attaining the equilibrium, a pre-soak voltage equal to the initial value of the voltage ramp was applied and sufficient hold and delay times were given during the measurement. All the voltage sweeps were done from inversion to accumulation. All the high frequency MOS capacitor characterizations were done using Keithely semiconductor characterization system model 4200 with a 4210 capacitance-voltage unit integrated to it. Figure 3.15 shows the normalized capacitance-voltage

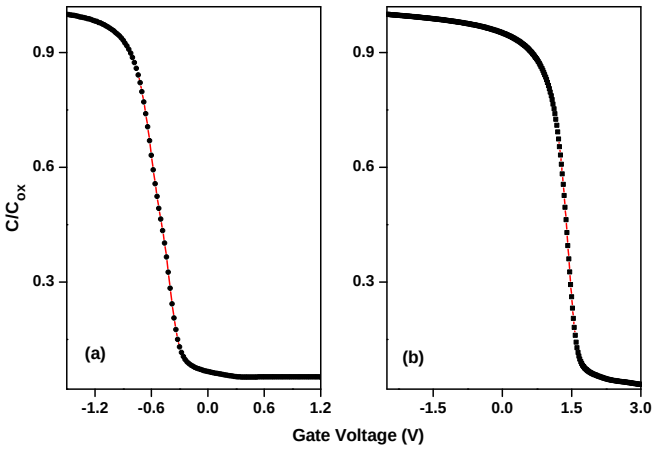

FIGURE 3.15: High frequency Capacitance-Voltage characteristics of MOS capacitor fabricated at room temperature with (a) Microwave plasma assisted ALD and (b)RF plasma assisted ALD.

curves for MOS capacitors fabricated using (a) microwave plasma assisted

ALD-Al_2O_3 and (b) RF plasma assisted ALD-Al_2O_3 deposited at room temperature. These measurements were done at room temperature at a frequency of 1 MHz. Amplitude of the AC signal was 30 mV and a 200 milliseconds sweep delay was applied to equilibrate the device. The dielectric constants of the Al_2O_3 thin films prepared at different plasma conditions and substrate temperatures were calculated from the 1 MHz C-V curves.

The C-V characteristics of the MOS devices were found to depend on the ac measurement frequency. Figure 3.16 shows the frequency dependent C-V of MOScap made with microwave plasma assisted ALD-Al_2O_3 deposited at room temperature (MPALD-RT). With varying frequency the C-V curves disperse from each other and dispersion becomes maximum at accumulation. The dispersion behaviour is due to the presence of interface state, which responds in time during lower frequency measurements and can contribute to the total capacitance [132, 133]. As the frequency decreases a step formation in C-V is evident from figure 3.16 which indicates the presence of slow states near the interface [134, 135]. The slow states can act as source of leakage in the MOS capacitor.

Al_2O_3 is a material with moderate dielectric constant; for bulk Al_2O_3 the κ value is 9. The κ value obtained with microwave plasma assisted ALD is slightly higher than the bulk κ value. Except the room temperature deposited film, all other films showed an increase in κ value with deposition temperature. For RF plasma ALD the κ value increased gradually from 5.86 to 9.89 as deposition temperature increased from 40^0C to 200^0C. This increase in κ value was in coincidence with earlier reports [36]. For Al_2O_3 thin films deposited with RF plasma assisted ALD, the dielectric values were slightly less than the MPALD Al_2O_3 thin films. The variation of the dielectric constant values with deposition temperature for microwave plasma assisted and RF plasma assisted ALD-Al_2O_3 are given in figure 3.17

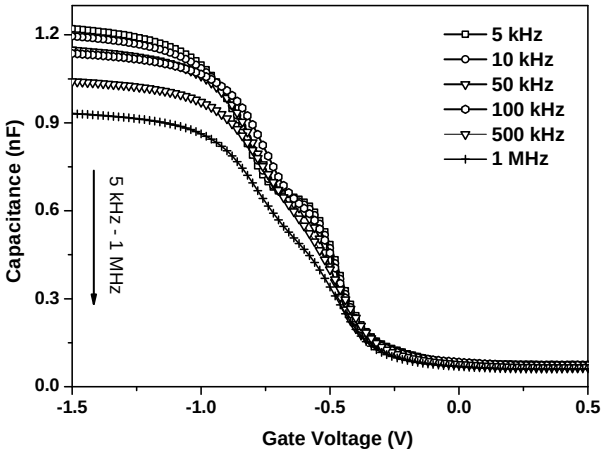

FIGURE 3.16: Frequency dispersion characteristics of MOS capacitor fabricated with microwave plasma assisted ALD-Al_2O_3 deposited at room temperature.

The equivalent oxide thickness of a material is defined as the thickness

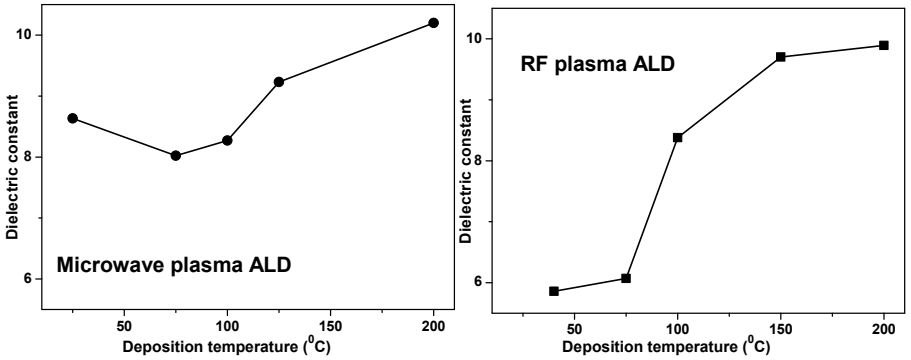

FIGURE 3.17: Variation in dielectric constant with deposition temperature for microwave plasma assisted ALD-Al_2O_3 and RF plasma assisted ALD-Al_2O_3.

of the SiO_2 layer that would be required to achieve the same capacitance density as the high-κ material in consideration [136]. The EOT can be calculated from physical thickness and dielectric constant of the thin films

as

$$EOT = \frac{\kappa_{SiO_2}}{\kappa_{high-\kappa}} \times t_{high-\kappa} \tag{3.21}$$

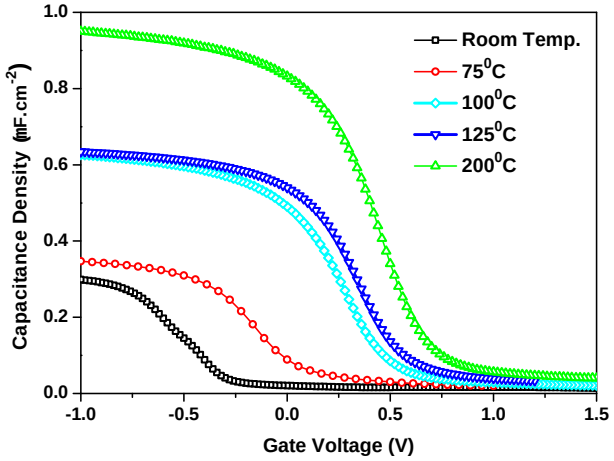

FIGURE 3.18: Capacitance - voltage curves for microwave plasma assisted ALD-Al_2O_3 based MOScaps by varying the Al_2O_3 deposition temperature. The C-V measurements were done at 1MHz probing frequency.

The EOT for Al_2O_3 thin film prepared at room temperature using MPALD system was 11.06 nm and that using RF plasma ALD system was 10.93 nm. For same number of deposition cycles, the thickness of the thin films prepared with microwave plasma ALD system was found to be higher than that using RF plasma based ALD. A complete saturation of the substrate surface caused by the presence of more reactive species can be the reason for higher growth rate and thickness for MPALD method. The growth per cycle for microwave plasma ALD at room temperature was 2.45 A^0/cycle. The growth rate curve for Microwave plasma ALD is given in section 2.6.1. The RF plasma deposition was done using the standard recipe by Cambridge NanoTech and the growth per cycle at 40^0C was 1.6 A^0/cycle.

Figure 3.18 and 3.19 show the effect of substrate temperature on C-V

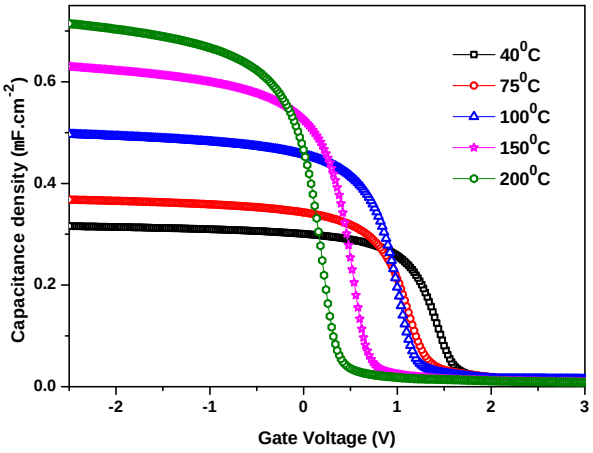

FIGURE 3.19: Capacitance - voltage curves for RF plasma assisted ALD-Al_2O_3 based MOScaps by varying the Al_2O_3 deposition temperature. The C-V measurements were done at 1MHz probing frequency.

characteristics of the MPALD-Al_2O_3 and RFALD-Al_2O_3 respectively. For MPALD-Al_2O_3 based MOScap, the capacitance value increases with increase in deposition temperature. For room temperature MPALD deposition, the C-V curve is on the negative side of the voltage axis and with increasing substrate temperature it shifts towards the positive side. This shift is caused by the presence of fixed oxide charges in the dielectric which will discuss detail in section 3.5.4. For RFALD, all the C-V curves are in the positive gate voltage side and with increase in deposition temperature the curve shifts to negative direction.

3.5.3 Doping profile

The dependence of capacitance on space charge width forms the basic of capacitance-voltage based doping profiling. Increasing the AC voltage from zero to a small positive voltage on the metal gate will add an

additional charge (dQ_m) on the metal. For maintaining the charge neutrality an additional charge (dQ_s) develops on the semiconductor. The semiconductor charge can be written as

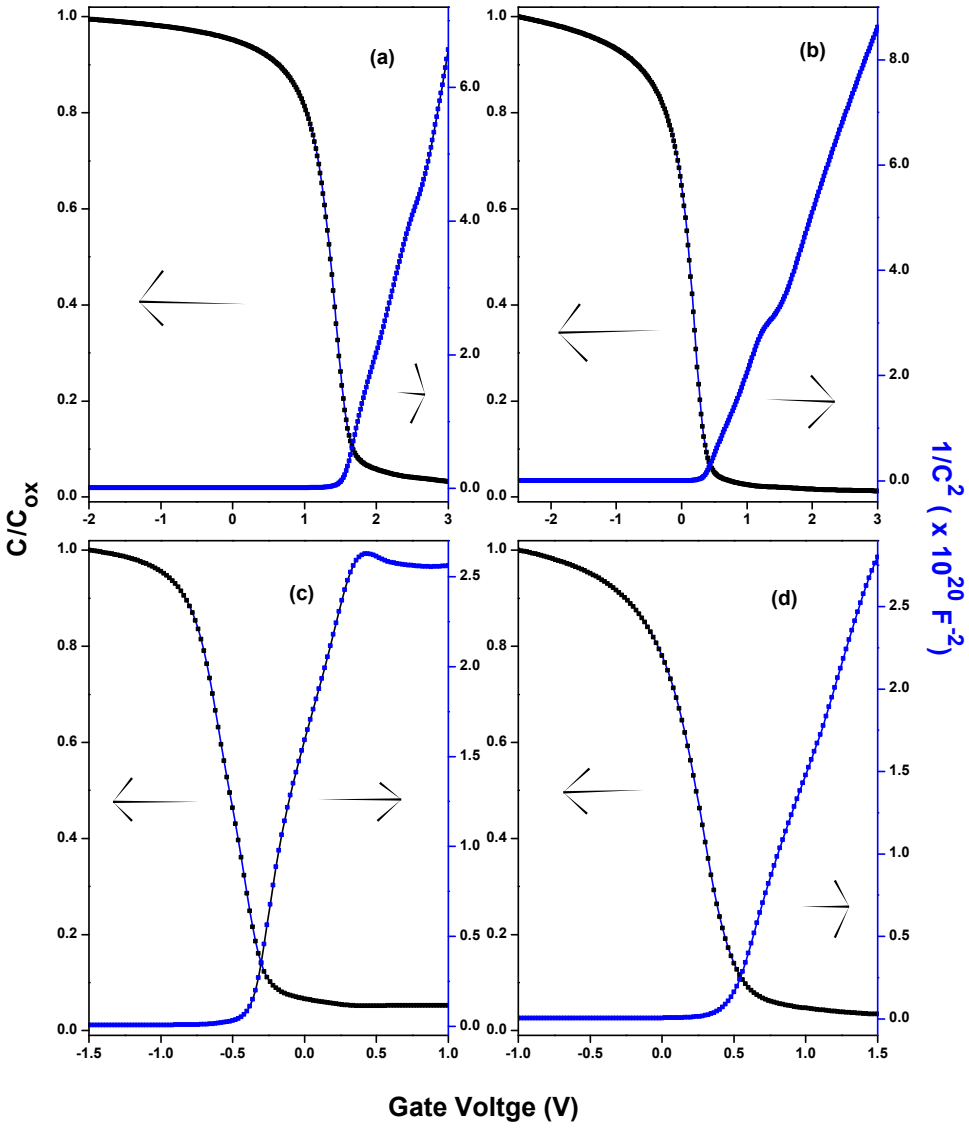

FIGURE 3.20: C-V and $1/C^2$ versus gate voltage curves for MOS capacitors fabricated with the minimum and maximum substrate temperatures for RF plasma assisted ALD (a & b) and for microwave plasma assisted ALD (c & d).

$$Q_s = qA \int_0^W (p - n + N_D^+ - N_A^-) dx \tag{3.22}$$

where q is the electronic charge, A is the area of the capacitor, n & p are electron and hole densities, N_D^+ & N_A^- are the number density of donor and acceptor ions and W is the depletion width. On application of the depletion approximation, the above equation can be written as

$$Q_s \approx -qA \int_0^W N_A dx \tag{3.23}$$

Accordingly the differential capacitance can be written as

$$C = qAN_A(W)\frac{dW}{dV} \tag{3.24}$$

When we compare the space charge region with a parallel plate capacitor, the capacitance can be written as

$$C = \frac{\kappa_s \varepsilon_0 A}{W} \tag{3.25}$$

where κ_s is the dielectric constant of the semiconductor and ε_0 is the permittivity of free space. Taking derivative of equation 3.25 with respect to voltage and substituting in equation 3.24 will give

$$N_A(W) = \frac{2}{q\kappa_s \varepsilon_0 A^2 d(1/C^2)/dV} \tag{3.26}$$

From equation 3.26, by knowing the slope of the Mott-Schottkey plot ($1/C^2$ vs gate voltage), the carrier density can be calculated at any depth inside the semiconductor. Figure 3.20 shows the combined C-V and Mott-Schottkey plot for MPALD and RFALD based MOScap at the minimum and maximum substrate temperatures used for Al_2O_3 deposition. The equation 3.26 is originally for metal-semiconductor contacts and if the interfacial layer thickness is small then the same equation can also be

used for carrier density calculation of MOS capacitors. For MOS capacitors, while taking the depletion width expression, we should consider the capacitance contribution by the oxide layer also i.e.,

$$W = \kappa_s \varepsilon_0 A(\frac{1}{C} - \frac{1}{C_{ox}}) \tag{3.27}$$

where C is the total capacitance and C_{ox} is the oxide capacitance. While applying an AC voltage the charges that actually move are the holes and not the doped ions, hence equation 3.26 actually measures the apparent carrier density instead of doping density [131]. But in the case of uniform doping the apparent carrier density, majority carrier density and the doping density will be practically the same. The majority carrier

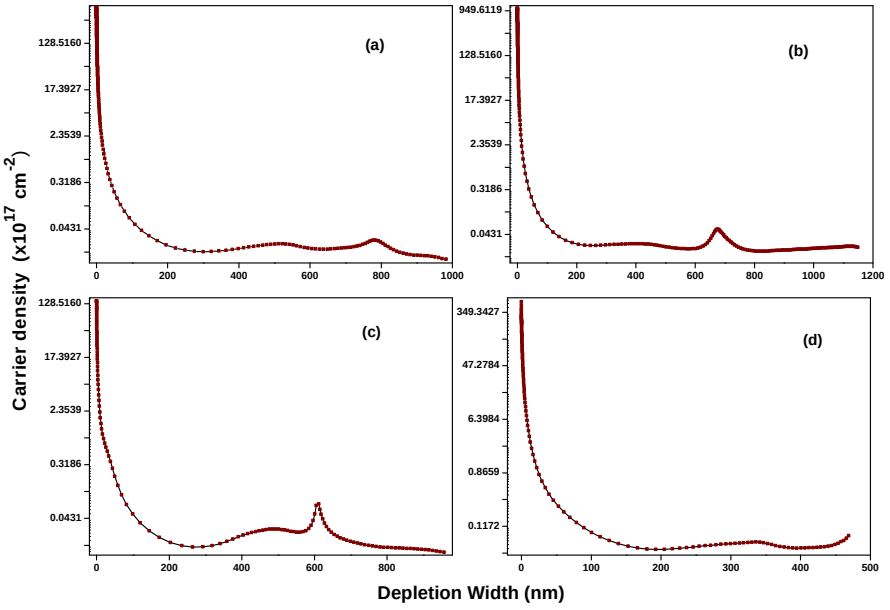

FIGURE 3.21: Doping profiles for MOScaps fabricated using MPALD & RFALD based Al_2O_3 at the maximum and minimum deposition temperatures. (a) & (b) RFALD based moscap, Al_2O_3 deposited at room temperature & 200^0C. (c)&(d) MPALD based moscap, Al_2O_3 deposited at 40^0C & 200^0C.

density's deviation from the doping density is governed by the extrinsic Debye length (λ),

$$\lambda = \sqrt{\frac{\kappa_s \varepsilon_0 kT}{q^2 N_A}} \tag{3.28}$$

more generally called the Debye length, is a measure of the distance over which a charge imbalance is neutralized by majority carriers under steady state or equilibrium conditions [131]. Figure 3.21 shows the doping concentration profiles for the ALD-Al_2O_3 based MOScaps.

3.5.4 Oxide charges

The oxide charges present in a gate dielectric can be classified into three different groups (1)mobile charges, (2) trapped oxide charges and (3) fixed oxide charges. Mobile charges are mainly due to Alkali metal ions. Mobile charges are harmful for the device and can be avoided by careful preparation and handling of the device. Trapped oxide charges seem to locate at the interface between the oxide and semiconductor or at the oxide metal interface. Trapped charges due to ion implantation is an exception and they can spread in the oxide. The oxide charges that remain after the annealing out of interface traps is known as fixed oxide charges [127]; they can not change their charge state and have no electrical communication with the semiconductor. The fixed oxide charge in a gate dielectric can change the threshold voltage of the MOSFET. The oxide charges alter the surface potential and it will affect the surface currents.

The amount of oxide charges present in a gate dielectric can be quantified by measuring the flat band voltage shift in MOScap characteristics. As the flat band voltage represents the voltage drop at zero applied gate voltage, from equation 3.18 it is clear that the flat band voltage can be written as a function of oxide charges and metal-semiconductor work function difference. A large quantity of interface state density will lead to erroneous

value of oxide charges. By using chemicals having sufficient purity for the desired purpose and by careful utilization of the present day sophistication available in deposition techniques one can easily avoid the presence of mobile carriers in gate dielectric. The trapped oxide charges can be reduced to a required extent by foaming gas annealing. From C-V characteristics the flat band voltage is measured as the voltage corresponding to the flat band capacitance. The flat band capacitance is given by

$$C_{FB} = \frac{C_{ox}\frac{\varepsilon_s A}{\lambda}}{C_{ox} + \frac{\varepsilon_s A}{\lambda}} \tag{3.29}$$

where λ is the extrinsic Debye length as specified by equation 3.28, A is the area of the MOScap, C_{ox} is the oxide capacitance and ε_s is the permittivity of the semiconductor.The fixed oxide charge density N_{ox} is given by

$$N_{ox} = \frac{C_{ox}(\phi_{ms} - V_{FB})}{qA}. \tag{3.30}$$

where V_{FB} is the flat band voltage and ϕ_{ms} is the metal-semiconductor workfunction difference. The ϕ_{ms} value is taken as -0.1 eV. The ϕ_{ms} is calculated by taking vacuum workfunction for aluminium as 4.2 eV, the electron affinity for silicon as 4.05 eV and by considering fermi level of silicon 250 meV below the conduction band minimum [137]. Figure 3.22 shows the C-V characteristics of the MOScap fabricated with RF plasma assisted ALD-Al_2O_3 with Al_2O_3 deposited at different substrate temperatures. For all MOScap the flat band shift is towards the positive gate voltage side, which indicates the presence of negative fixed oxide charges in the Al_2O_3 gate dielectric. The flat band voltage shift is maximum for MOScap fabricated at lower temperature. With increasing substrate temperature, the flat band shift reduces gradually and have minimum value for Al_2O_3 deposited at maximum substrate temperature. But from figure

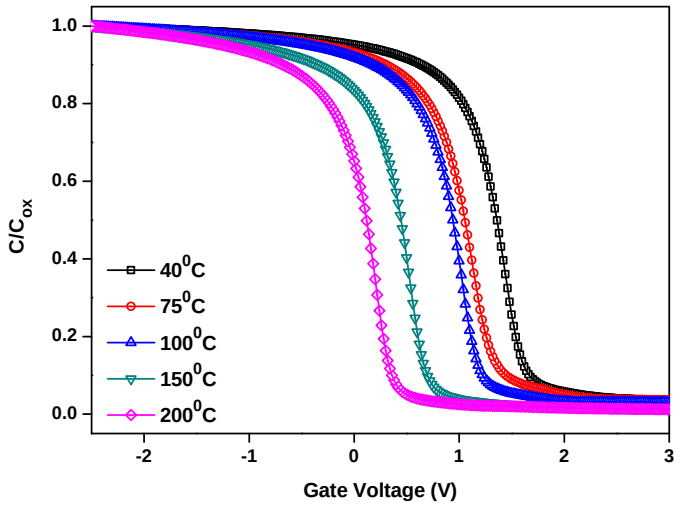

FIGURE 3.22: Normalized C-V curves for RF plasma assisted ALD-Al_2O_3, showing the variation in flat band voltage with substrate temperature.

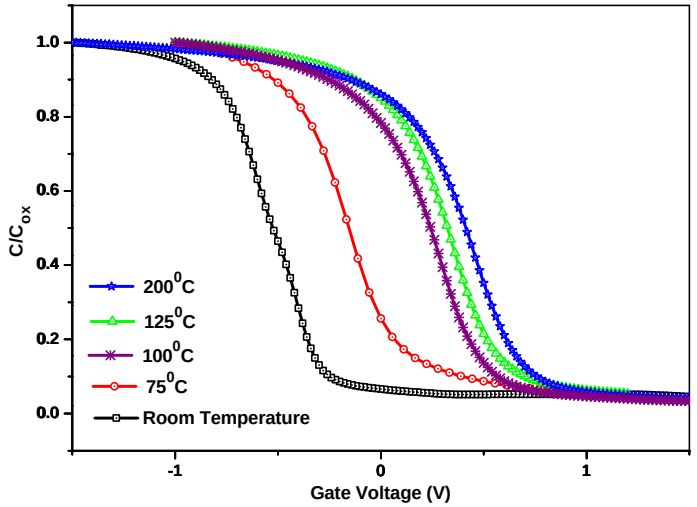

FIGURE 3.23: Normalized C-V curves for microwave plasma assisted ALD-Al_2O_3, showing the variation in flat band voltage with substrate temperature.

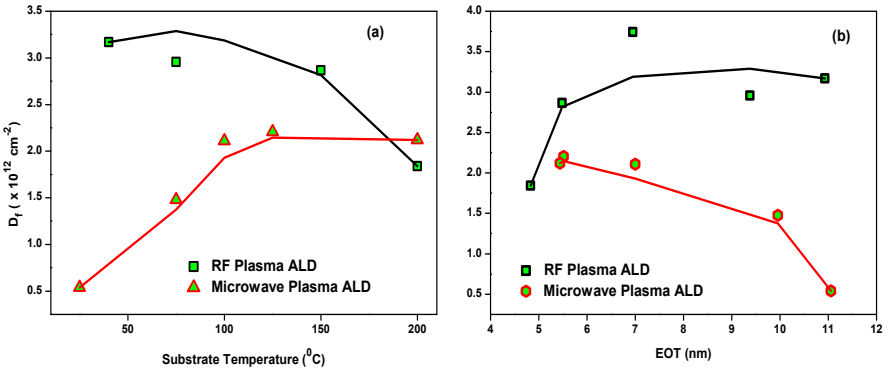

FIGURE 3.24: Number density of fixed oxide charges for microwave and RF plasma assisted ALD-Al_2O_3 as a function of (a) deposition temperature (b) variation with EOT.

3.18 it can be observed that the capacitance value also increases with deposition temperature due to thickness reduction. Hence the fixed oxide density remains almost constant with deposition temperature.

The sign of fixed oxide charges is assumed to be negative for Al_2O_3 thin films, irrespective of the deposition technique [8, 137–140]. Contrary to that for the room temperature MPALD deposition, the net polarity of the fixed oxide charges is positive as indicated by the negative shift in flat band voltage. The oxide charge polarity is reversed to negative at higher deposition temperatures and the flat band shift towards positive side increases gradually with substrate temperature. Even though it is very small, the higher capacitance and higher flat band voltage shift at higher deposition temperatures represent an increase in fixed oxide charges with deposition temperature. For MPALD-Al_2O_3 based MOScap, with increasing substrate temperature the flat band voltage shifts to the positive gate voltage side together with an increase in capacitance. This indicates an increase in fixed oxide density with increasing substrate temperature. Increasing fixed oxide density with deposition temperature is reported in literature for thermal ALD-Al_2O_3 [140]. For RF plasma assisted ALD the increase in flat band voltage and oxide capacitance are in opposite

directions with varying temperature. Hence the fixed oxide charge density remains constant irrespective of the deposition temperature. Figure 3.24(a) shows the variation of fixed oxide charge density with respect to substrate temperature. The oxide charge density remains in the same order of magnitude ($10^{12}cm^{-2}$) for all the depositions. Similar behaviour of fixed oxide charges with deposition temperature was reported in literature [137]. The variation of oxide charge density with equivalent oxide thickness is plotted in figure 3.24(b). Evidences were reported in literature for the existence of fixed oxide charges in the interface with the substrate [141–143] and figure 3.24(b) also supports this.

Since its birth, thermally grown silicon based oxides were the gate dielectric materials for MOSFETs. The oxide charges present in thermal oxides of silicon were positive in nature [131, 144]. Many experiments on plasma assisted ALD of Al_2O_3 reported negative fixed oxide charges in the oxide. Our present investigations on Microwave & RF plasma assisted depositions of Al_2O_3 also found to have negative fixed oxide charges. Out of the octahedral and tetrahedral bonding environments of Al atoms in Al_2O_3 the second type has a net negative charge and was assumed to cause a negative fixed charge density [145]. A constant value of fixed oxide density with respect to equivalent oxide thickness indicates that the fixed charges are located at the interface of Al_2O_3 for both microwave plasma and RF plasma assisted ALD. All the fixed oxide charge density calculations were done after post deposition foaming gas annealing. There are earlier reports of increase and decrease in fixed oxide density with post deposition annealing for plasma assisted ALD-Al_2O_3 thin films [8, 137, 146]. A soft control over fixed oxide density is beneficial to several electronic applications [8], even though some mechanisms are proposed for the formation of fixed oxides in dielectric structures, debates are still going on in this respect.

3.5.5 Interface defect studies

Due to the presence of interface defect states, the profiling and control of the oxide-semiconductor interfacial region is important for micro and nano electronics performance. Interface defect density can directly impact the device mobility [136]. As the device size shrinks more and more, the effect of interface become more critical. Even with the technological advances, a hetero dielectric/silicon interface can be made only with the presence of an interfacial layer. This interfacial layer would be either oxide of silicon or mixed oxide of silicon and hetero-dielectric. A hetero interface between high-κ and semiconductor is vulnerable to defect states (due to its bonding peculiarities and amorphous nature of high-κ) like (1) increased bond ionicity and oxygen atom coordination, (2) reduced conduction band offset energies as compared with Si-SiO_2, (3) interface trap associated with localized metal atom d states and (4) interfacial fixed charges associated with heterovalent character of interfaces [147]. In comparison with other high-κ materials Al_2O_3 is found to have higher density of interface and fixed charge densities [148].

The electrical properties of the interface states were characterized by their density, position in the silicon energy gap, and capture cross section [149]. There are several experimental methods for the characterization of the interface states. Stretch out in MOS capacitance due to interface states is utilized in Termann method [150]. But it is difficult to distil out other capacitance components (oxide and depletion capacitance). High-low frequency capacitance method developed by Kar and Dahlke is based on measuring the capacitance contribution by the interface states [145]. Charge pumping is another method of interface characterization, but it requires FET structure. For gate oxides having small thickness, the most accurate method for interface trap characterization is the conductance method.

The conductance method was developed by E. H. Nicollian and A. Goet-

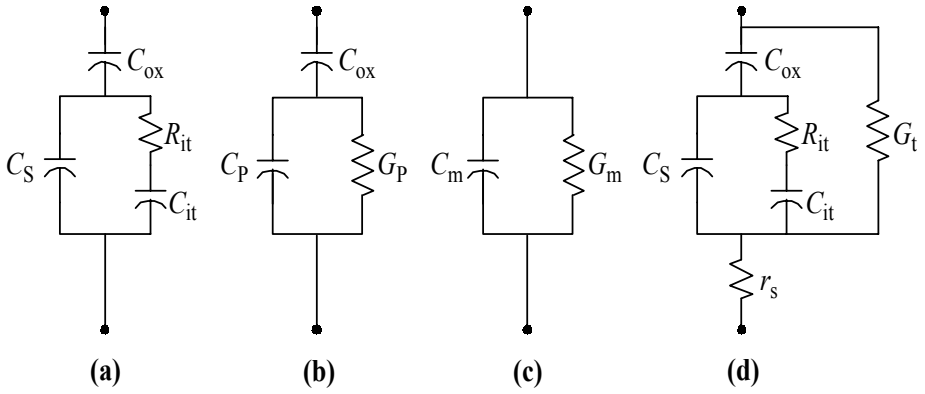

FIGURE 3.25: Equivalent circuits for conductance measurements (a) MOScap with interface trap time constant τ_{it}=$R_{it}C_{it}$, (b) Simplified circuit of (a), (c) measured circuit, (d) circuit including series resistance r_s and tunnel conductance G_t.

zberger in 1967 [149]. The equivalent circuits for conductance measurements of a MOS capacitor in the presence of interface charges are given in figure 3.25(a). By trapping and releasing the mobile carriers, the interface traps can contribute additional capacitance to the MOS. The conductance loss arising out of the capture and emission of carriers by interface states is measured in the conductance technique. The capture and emission of carriers by the interface states is a lossy process, represented by the resistance R_{it}. It is convenient to replace the circuit in figure 3.25(a) by 3.25(b), where C_p and G_p are given by[131]

$$C_p = C_s + \frac{C_{it}}{1 + (\omega\tau_{it})^2} \tag{3.31}$$

$$\frac{G_p}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1 + (\omega\tau_{it})^2} \tag{3.32}$$

where C_{it}=q^2D_{it}, ω=$2\pi f$ (f is the measurement frequency)and τ_{it}=$R_{it}C_{it}$. From equation 3.32, when $\omega\tau \ll 1$, $G_p/\omega \approx 0$ and for $\omega\tau \gg 1$, G_p/ω tends

to become zero. This gives the situation at which the interface traps cannot respond to ac signal and hence there is no energy loss. When $\omega\tau \approx 1$, G_p/ω has maximum value and then the time constant of the trap is comparable to time period of the interface trap states and the occupancy of the traps will change with a lag to ac signal. The equations 3.31 and 3.32 are for a single interface trap within the band gap of the semiconductor. In every C-V and G-V measurements there will be effects of series resistance (R_s). Figure 3.26 shows the measured conductance versus gate voltage curve at different frequencies for MOScap fabricated with MPALD-Al_2O_3 deposited at a substrate temperature of 200^0C. Conductance curves for all the MOS capacitors used in the present study show a similar behaviour as that of figure 3.26. The dispersion caused by series resistance is the reason for observed higher conductance at higher frequencies. The variation of series resistance with gate voltage as a function of frequency is shown in figure 3.27. The series resistance gives peaks due to conductance losses by interface traps. Hence the measurement of series resistance will give a peak at the depletion region and was found to decrease with increasing frequency. The nature of series resistance variation is the same for all MOScaps fabricated in this study. If there is conductance due to tunnelling of charge carriers, it will generate a linearly decreasing conductance curve in accumulation. After correcting for series resistance and tunnelling currents, we can isolate the interface trap effects in conductance [151]. This kind of corrected conductance curve are used for interface state density determination.

The major source of series resistance is the bulk of the wafer. The series resistance can cause deviations from actual behaviour while extracting interfacial characteristics and doping profiles [115, 127, 152, 153]. The series resistance can be deduced from capacitance and conductance values in the accumulation region as [127]

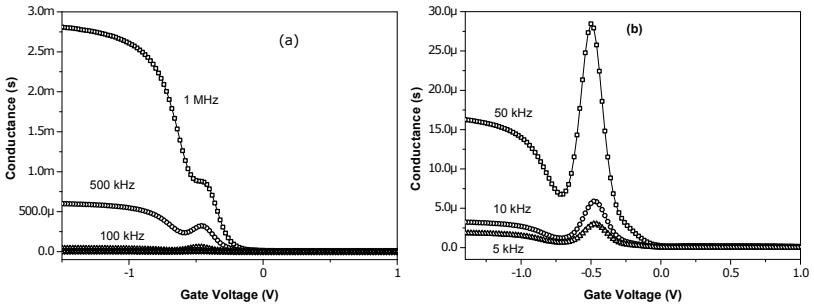

FIGURE 3.26: Measured conductance versus gate voltage curve for MOScapacitor fabricated with MPALD-Al_2O_3 deposited at room temperature (a) for higher measurement frequencies (b) low frequencies.

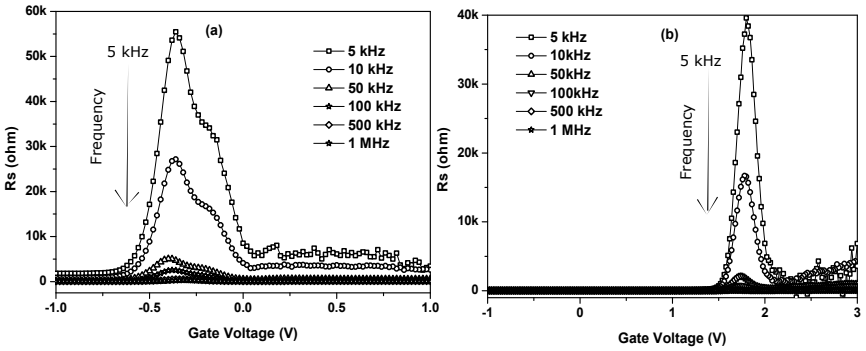

FIGURE 3.27: Frequency dispersion of series resistance for MOScapacitor fabricated with ALD-Al_2O_3 (a) MPALD-Al_2O_3 deposited at room temperature(b) RFALD-Al_2O_3 deposited at 40^0C.

$$R_s = \frac{G_m}{G_m^2 + \omega^2 C_m^2} \tag{3.33}$$

where G_m and C_m are the measured conductance and capacitance in accumulation. The corrected capacitance C and corrected conductance G are given by

$$C = \frac{(G_m^2 + \omega^2 C_m^2) C_m}{a^2 + \omega^2 C_m^2} \tag{3.34}$$

where $a = G_m - (G_m^2 + \omega^2 C_m^2) R_s$ and

$$G = \frac{(G_m^2 + \omega^2 C_m^2) a}{a^2 + \omega^2 C_m^2} \tag{3.35}$$

The effect of series resistance is critical for low interface trap level density

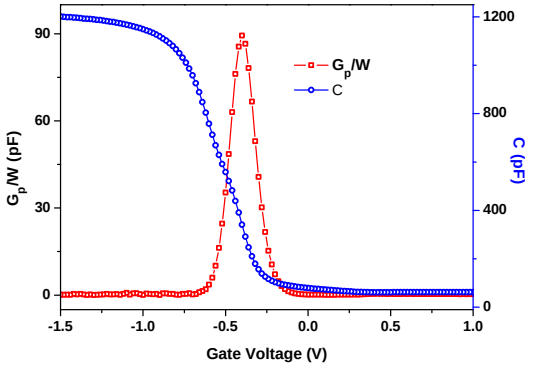

FIGURE 3.28: Combined Capacitance-Voltage (C-V) and Conductance-Voltage (G-V) characteristics (1 MHz) of MOScap based on MPALD-Al_2O_3 deposited at room temperature.

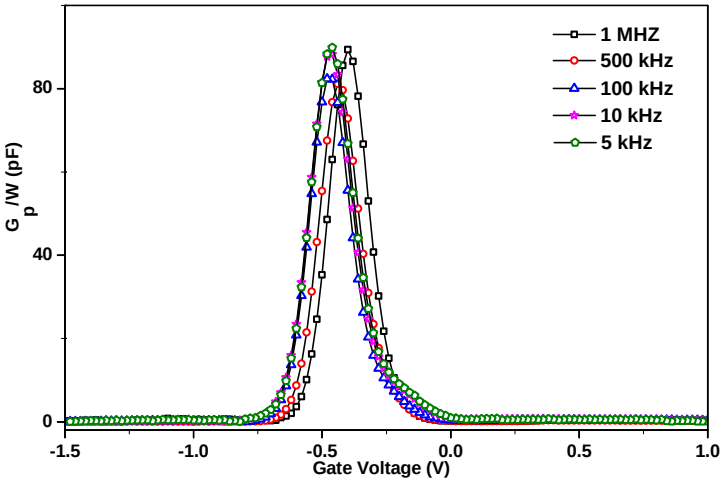

FIGURE 3.29: Frequency dependent corrected conductance vs gate voltage characteristics of MPALD-Al_2O_3 deposited at room temperature.

measurements [127].

Usually the interface states are distributed continuously throughout the

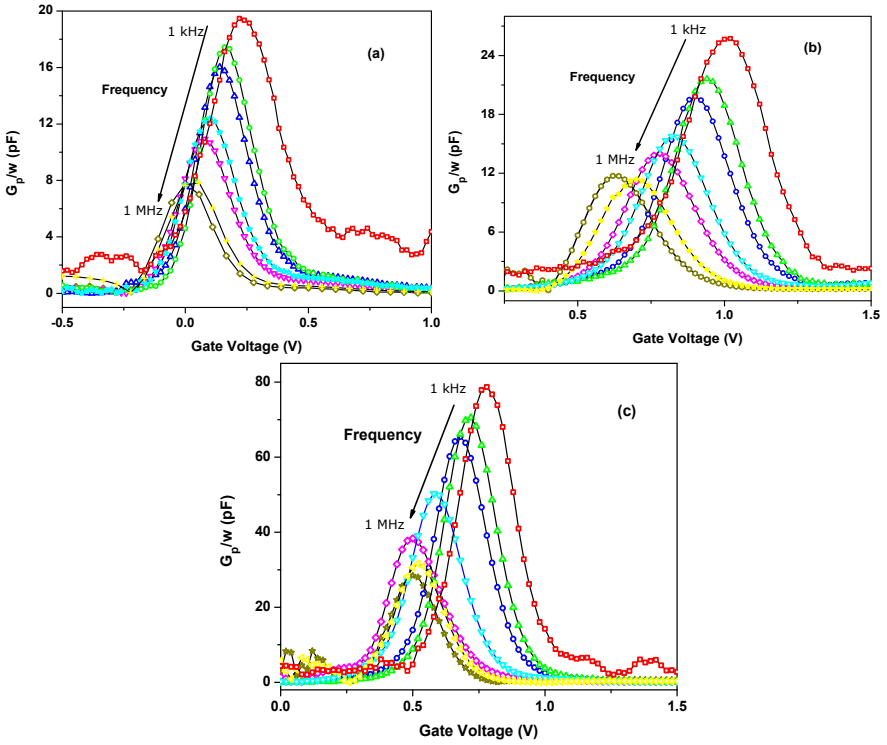

FIGURE 3.30: Frequency dependent corrected conductance-gate voltage characteristics of MPALD-Al_2O_3 prepared at different substrate temperature (a) 75^0C (b) 125^0C (c) 200^0C.

ALD Temperature (^{0}C)	D_{it} (MPALD) (cm^{-2} eV^{-1})	D_{it} (RFALD) (cm^{-2} eV^{-1})
Room Temperature	3.1716×10^{11}	
40		2.1696×10^{10}
75	5.589×10^{10}	2.436×10^{10}
100	4.141×10^{9}	2.2172×10^{10}
125	5.3714×10^{10}	
150		3.9982×10^{10}
200	1.9542×10^{11}	4.3347×10^{10}

TABLE 3.4: Interface trap level density values for plasma assisted ALD-Al_2O_3

bandgap of the material. For a distribution of interface trap levels over the semiconductor bandgap, transitions occur between the majority carrier band and interface trap levels in an energy interval of a few kT wide about the Fermi level. Each interface trap level in this energy interval contributes a different energy loss depending on its distance in energy from the Fermi level. As a result each interface trap level in this interval must have a different time constant [127]. So the normalized conductance becomes [131]

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} ln[1 + (\omega\tau_{it})^2] \tag{3.36}$$

The G_p/ω versus ω curve gives a peak at $\omega = 1/\tau_{it}$. For equation 3.36 $\omega \approx 2/\tau_{it}$ [149] and hence at maximum

$$D_{it} \approx \frac{2.5}{q}(\frac{G_p}{\omega})_{max} \tag{3.37}$$

The same equation can be used for G_p/ω versus gate voltage curves.

Figure 3.28 is the combined capacitance and corrected conductance versus gate voltage curve showing the conductance peak in depletion region of the C-V characteristics. From the peak of figure 3.28, the interface state density for room temperature MPALD-Al_2O_3 deposited over p-Si was calculated as 3.17×10^{11} cm^{-2} eV^{-1}. The frequency dependence of interface defects at MPALD-Al_2O_3/p-Si interface are shown in figures 3.29 and 3.30. Figure 3.29 represents the frequency dependence of room temperature MPALD-Al_2O_3/p-Si interface, for which the interface state respond almost independent of the frequency of applied ac voltage. Figure 3.30 shows the frequency dependence of high temperature deposited MPALD-Al_2O_3/p-Si interfaces. As expected the interface states become more active at lower frequencies. Figure 3.31 shows the frequency dependent corrected conductance-voltage characteristics of RFALD-Al_2O_3 based MOScap with RFALD-Al_2O_3 deposited at different substrate temperatures. The location of the charge can be established by varying the

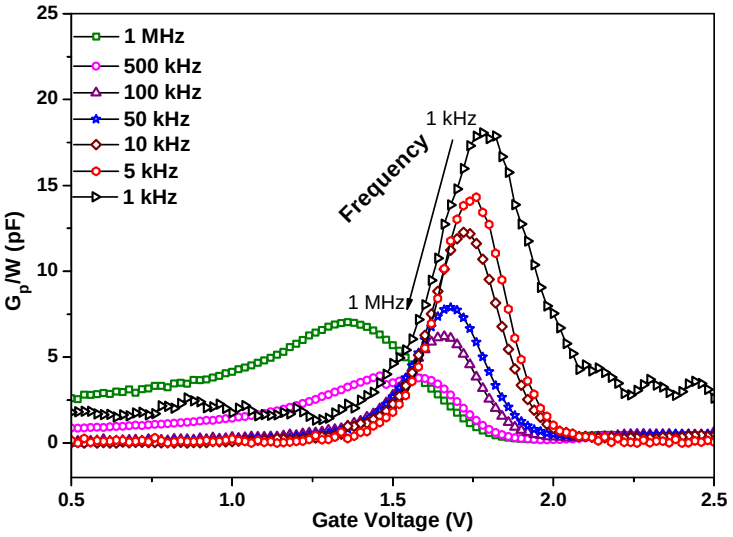

FIGURE 3.31: Frequency dependent conductance-Voltage characteristics of RFALD-Al_2O_3 prepared at 40^0C

thickness of the deposited oxide or etching it with repeated measurements.

3.5.6 Leakage characteristics

For scaling down the microelectronic device, it is necessary to reduce the gate oxide thickness. Increased leakage currents and higher power dissipation are the natural consequences of thickness reduction. The usage of high-κ materials provided a chance to reduce power loss by increasing the physical thickness of the gate dielectric material. At the same time aspects like barrier height reduction with silicon and reduced metal gate work function will lead to tunnelling through oxide and act as additional sources of leakage currents. The undesired leakage currents flowing through the MOS system and the corresponding conduction mechanisms can be evaluated using Current - Voltage measurements. Quantification

of the leakage current through a MOS device is a good measure of its reliability.

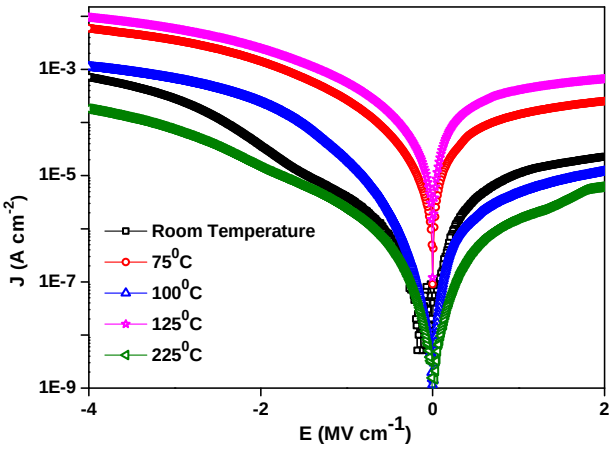

FIGURE 3.32: Leakage current density with electric field across the gate dielectric for MPALD-Al_2O_3 prepared at different substrate temperatures.

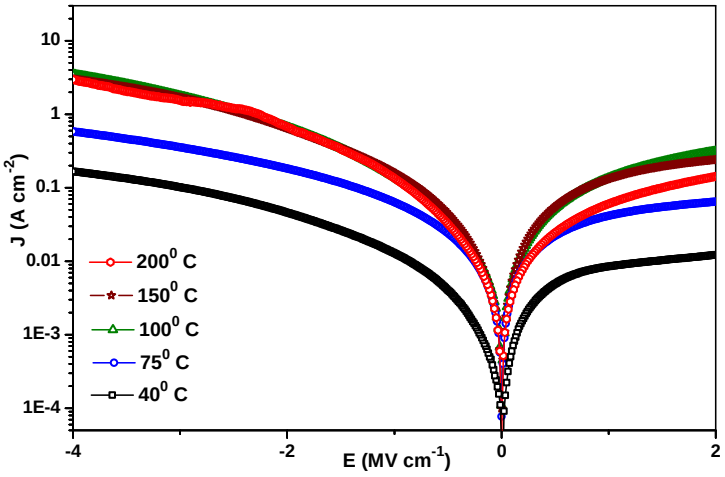

FIGURE 3.33: Leakage current density with electric field across the gate dielectric for RFALD-Al_2O_3 prepared at different substrate temperatures.

Figure 3.32 shows the current-voltage characteristics of Al/MPALD-Al_2O_3/p-Si MOS structures with MPALD-Al_2O_3 thin films deposited at different substrate temperatures. Figure 3.33 shows the similar characteristics for RF plasma assisted ALD-Al_2O_3 thin films. As similar to earlier reports the leakage characteristics almost remain unaffected by deposition temperature [119, 140]. In the present study, the thin films of Al_2O_3 prepared by both the plasma assisted modes of ALD were found to be leaky in nature. The large current values at negative bias is caused by the electrons injected from the aluminium electrode. On positive side the current value is less in comparison with the negative side and saturates early with gate bias because of the minority carriers injected from the p-type semiconductor substrate [154].

3.5.7 Conclusions

ALD-Al_2O_3 thin films were deposited using two different modes of plasma assisted ALD: Microwave plasma assisted ALD and RF plasma assisted ALD. The growth rate for microwave plasma assisted ALD was found to be higher than RF plasma ALD. The deposited thin films were amorphous in nature. The microwave plasma assisted ALD films were oxygen rich and the presence of hydroxyl group was identified from the XPS spectra. These films were found to have a little carbon incorporation in them. The density and refractive index for the plasma assisted ALD thin films are in agreement with earlier reports. Electrical characterization of the Al_2O_3 thin films were done by fabricating MOS structures using them. The growth rate of the MPALD thin films were found higher in comparison with RFALD films. The thickness of the thin films were found to decrease with increasing deposition temperature. The dielectric constant is also found better for the MPALD thin films. Frequency dispersion was observed in all the C-V characteristics due to the presence of interface

states. All the thin films were found to be little bit leaky from I-V characteristics. The fixed oxide charge density and the number density of interface states in Al_2O_3 thin films prepared in our home made MPALD system were found to be comparable to that prepared using commercial ALD system and are acceptable values for gate dielectric applications. Better understanding of the negative fixed charge density and their variation with substrate temperature will open door towards its application in solar cell passivation.

Chapter 4

Deposition and characterization of Thermal ALD-Al_2O_3

The energy enhanced forms of ALD like plasma assisted ALD came into scene only after 30 years of research and development of the conventional thermal ALD. Usually, there will be sufficient heating arrangement in every plasma assisted ALD system to incorporate the thermal mode along with plasma mode. Atomic layer deposition is a technique capable of achieving high film quality at moderate process temperatures [9, 14]. Thermal atomic layer deposition of Al_2O_3 thin films using trimethylaluminum and water is considered as a model system for ALD. The surface reaction during thermal ALD-Al_2O_3 is studied by several groups and the binary surface reactions included in this process are given by

$$AlOH^* + Al(CH_3)_3 \rightarrow AlOAl(CH_3)_2^* + CH_4 \tag{4.1}$$

$$AlCH_3^* + H_2O \rightarrow AlOH^* + CH_4 \tag{4.2}$$

where the asterisks represent the surface species [80, 96, 155–157]. This chapter deals with the thermal ALD deposition of Al_2O_3 thin films, fabrication of MOS structures using them and their characterizations.

4.1 Thermal ALD-Al_2O_3 over plasma ALD

The conformality of the deposited thin films and the possible thickness control are the key features that enabled the ALD technique to get credential over CVD and PVD. The plasma assisted atomic layer deposition has either scaled up some ALD features or added something additional. Even though the plasma assisted ALD has a number of advantages over the thermal ALD, there are some drawbacks also. The major drawback of plasma assisted ALD in comparison with thermal ALD is the limited conformality on high aspect ratio structures [19, 35, 112]. The conformality of the plasma based process is limited due to the surface recombination of radicals during the plasma step. Another possible drawback is collision induced defects by high energy species from plasma [58] and the complexity in reactor design. The reactive species from plasma can cause surface reactions including oxidation and nitridation of the top surface layers of the substrate [19, 68].

4.2 Atomic layer deposition of Al_2O_3 thin films

Al_2O_3 thin films were deposited over two inch p-type silicon(1 0 0) wafer having 1-5 Ω-cm resistivity. Before deposition, the silicon wafer was cleaned with standard RCA procedure followed by a hydrofluoric acid dip. The RCA cleaned silicon wafers were transferred to the reaction chamber

at the earliest. 100 ALD cycles were used for the deposition of Al_2O_3 thin films. Two different ALD systems were used for the deposition: home made ALD system and Fiji F 200 ALD system of Cambridge NanoTech.

ALD system	Temperature (^{0}C)	TMA purge(s)	H_2O purge (s)
Home made	150	40	180
	175	40	180
	200	20	60
	225	20	60
	250	20	60

TABLE 4.1: Optimized purge timings for thermal ALD-Al_2O_3 deposition in home made ALD system

ALD system	Temperature (^{0}C)	TMA purge(s)	H_2O purge (s)
Fiji	100	30	30
	150	20	20
	200	10	10
	250	8	8
	300	5	5

TABLE 4.2: Standard precursor purge timings for thermal mode Al_2O_3 deposition in Cambridge NanoTech's Fiji F200.

Deposition was carried out using both these systems at different substrate temperatures. In home made ALD system, deposition temperature was varied from 150^0C to 250^0C with 25^0C interval. In Fiji ALD system the deposition temperature variation was from 100^0C to 300^0C with 50^0C interval. Trimethylaluminum (TMA)($Al(CH_3)_3$) and water (H_2O) were the precursors used for deposition of Al_2O_3 thin films. For the home made ALD system the pulse time for both TMA and water was 300 milliseconds. In this system 300 millisecod is the minimum possible pulse time. For Fiji F 200 ALD system the pulse time was 60 millisecond for both the precursors. The purge time required for Al_2O_3 deposition is not the same

for all substrate temperatures, because at higher deposition temperatures the residual species after deposition can be desorbed easily [158]. For lower deposition temperatures the desorption and hence the removal of residual un-reacted precursor molecules and reaction by products will take more time. The table 4.1 and 4.2 show the purge timings corresponding to different deposition temperatures in the two ALD systems.

4.3 Film growth rate & density

Figure 4.1 shows the thickness reduction of ALD-Al_2O_3 thin film with increase in deposition temperature. Similar nature of thickness reduction was reported by several groups and the reduced number of available OH reaction sites is attributed as the reason for this thickness reduction with substrate temperature [3, 80, 81, 93, 120]. The ALD growth on a substrate surface is governed by available surface reaction sites and by the reaction kinetics [80, 96, 119]. At higher temperatures partial self-decomposition of TMA may also affect the growth rate [81]. Almost same behaviour of thickness reduction was observed in Fiji ALD system and is shown in figure 4.2.

While comparing with the plasma assisted ALD results obtained in the previous chapter, we can see that the thermal ALD-Al_2O_3 also shows thickness reduction with increasing deposition temperature. But the thickness reduction for plasma assisted ALD (figure 3.3) was more linear than the thermal ALD case. From figure 2.17 and 2.18 we can see that the GPC vs number of cycles is a straight line for plasma assisted ALD even for few numbers of deposition cycles. So there is a chance that the growth in plasma assisted ALD is limited only by the number of OH sites. But for thermal ALD the growth may be limited by the presence of OH sites and by steric hindrance.

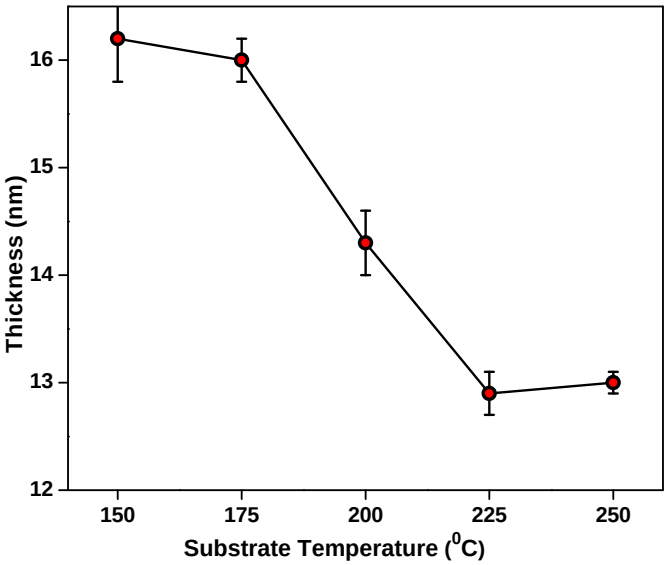

FIGURE 4.1: Thickness variation of thermal ALD-Al_2O_3 thin films deposited using home made ALD system.

The growth rate of plasma assisted ALD thin films were found to be higher than thermal ALD films. This is a well established result with a number of supporting literature reports [35, 109]. In home made ALD system the maximum thickness obtained at the minimum 150^0C substrate temperature with 100 deposition cycles is 16.2 nm. In Fiji ALD system, 12.23 nm Al_2O_3 was deposited at the minimum 100^0C deposition temperature for the same number of ALD cycles. A minimum film thickness of 12 nm was recorded at 150^0C. But for plasma assisted ALD the maximum thickness in home made ALD system at room temperature was 24.4 nm and at 100^0C was 18.48 nm. In RF plasma assisted mode of Fiji F 200 ALD system, the maximum thickness was 16.44 nm at 40^0C substrate temperature. The Fiji ALD system has given a maximum thickness of 12.3 nm at 200^0C for thermal ALD. In Fiji thermal ALD the film thickness remained almost constant for temperatures up to 250^0C, after which

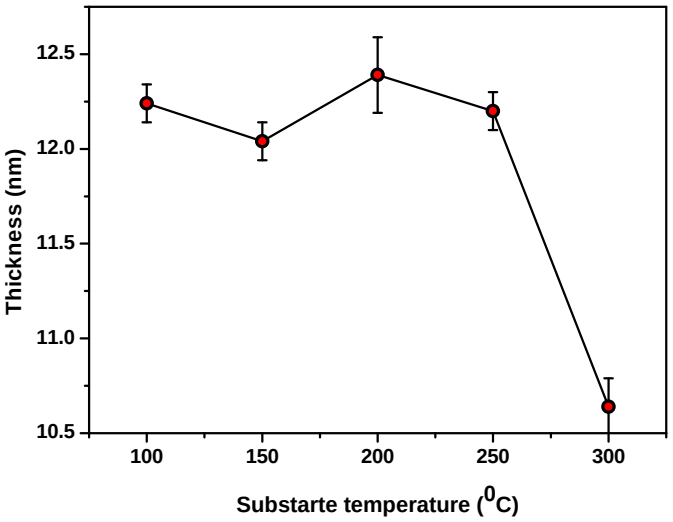

FIGURE 4.2: Thickness variation of thermal ALD-Al_2O_3 thin films deposited using Fiji F 200 ALD system.

it reduced to 10.6 nm at 300^0C.

The density of thermal ALD thin films deposited at different temperatures in the home made ALD system was obtained from X-ray reflectivity measurements and is plotted in figure 4.3. A reduction in film density was observed with decrease in deposition temperature. Similar results are reported in literature [119, 155]. The refractive index value of all the thermal ALD-Al_2O_3 thin films measured using XRR or ellipsometry are shown in figure 4.3. The average refractive index value of thermal ALD-Al_2O_3 thin films was around 1.6. But for plasma assisted ALD-Al_2O_3, the refractive index was slightly less (Figure 3.4). This variation in refractive index between plasma assisted ALD-Al_2O_3 and thermal ALD-Al_2O_3 was already noted and reported by researchers [68, 98, 119, 120].

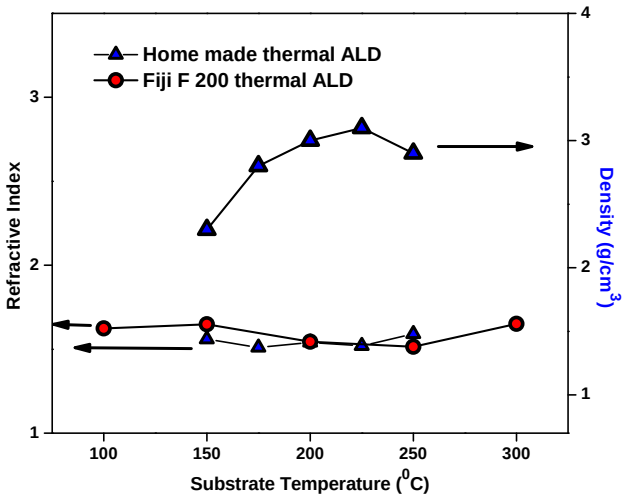

FIGURE 4.3: Substrate temperature dependence of refractive index for thermal ALD-Al_2O_3 using home made and FIji ALD systems and density dependence for home made thermal ALD-Al_2O_3.

4.4 Morphology & composition

Surface morphology and composition of the thermal ALD-Al_2O_3 thin films deposited in our home made ALD system was studied using FESEM and X-ray photoelectron spectroscopy respectively.

4.4.1 FESEM

As in the case of microwave plasma assisted films some island like structures are visible in the thermal ALD-Al_2O_3 films also. The FESEM images for samples deposited at 150^{0}C, 200^{0}C and 250^{0}C are given in figure 4.4(a), 4.4(b) and 4.4(c) respectively. A small increase in the size of the island like structure was found in microwave plasma assisted ALD films. But for the TALD films the size of the island like structures remains al-

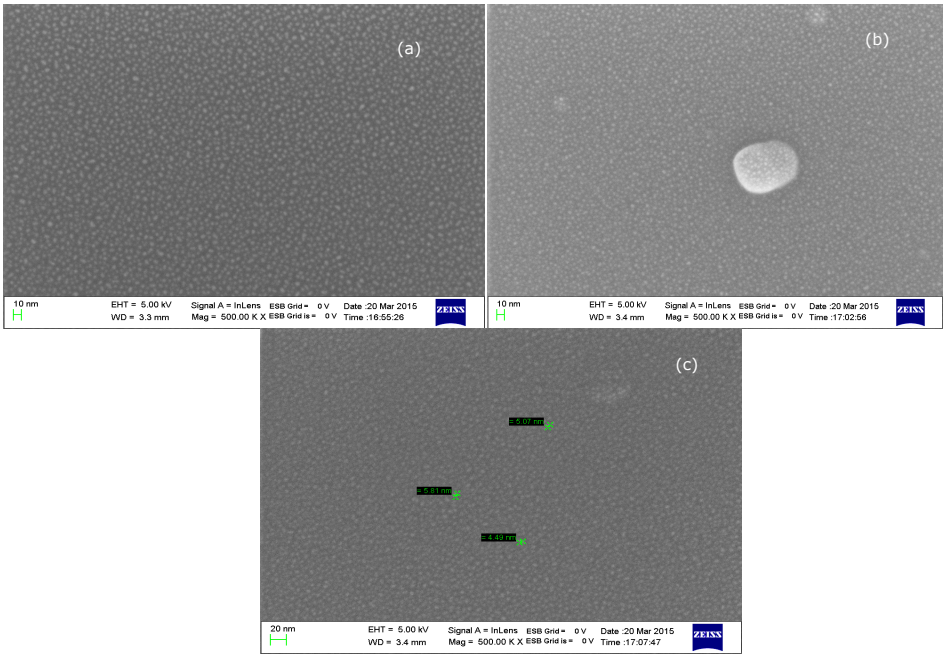

FIGURE 4.4: FESEM images of TALD-Al_2O_3, deposited at different substrate temperatures (a)150^0C, (b)200^0C and (c) 250^0C.

most the same irrespective of the deposition temperature (images 4.4(a) and 4.4(b) are at 20 nm scale and 4.4(c) at 10 nm scale).

4.4.2 X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy measurements were done to study the elemental composition and the chemical structure of the Al_2O_3 thin films. The presence of Al 2s, Al 2p and O 1s spectra reveals the Al_2O_3 deposition. For lower deposition temperatures the Al 2p peak is around 74.17 eV, while for 200^0C the Al 2p peak is around 74.65 eV. O 1s spectra also show a similar kind of shift with deposition temperature. The Al 2p spectra and the O 1s spectra are shown in figure 4.5 and 4.6 respectively. The energy difference between Al 2p and O 1s remains around 456.85 eV for all deposition temperatures and this value is close to earlier reports for

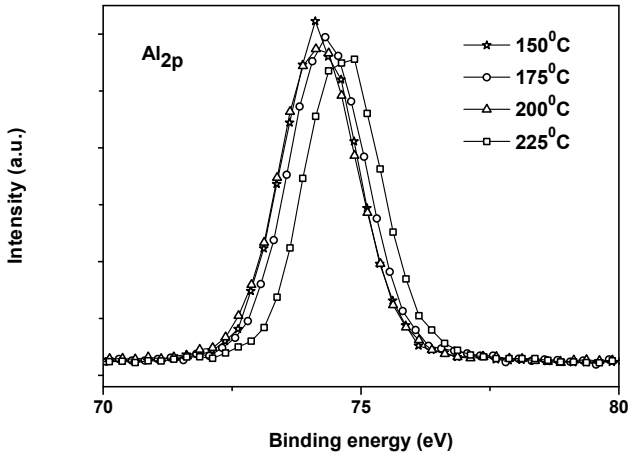

FIGURE 4.5: Al 2p spectra for thermal ALD-Al_2O_3 deposited at different substrate temperatures.

aluminium oxide and nitride [159, 160]. Similar to the microwave plasma assisted ALD-Al_2O_3, the thermal ALD-Al_2O_3thin films also remain in only one charge state.

Figure 4.7 gives a comparison between O 1s spectra of Al_2O_3 thin films prepared by MPALD and thermal ALD. As in the case of plasma assisted ALD-Al_2O_3, we can see a broadening at higher binding energy side of O 1s spectra of the thermal ALD-Al_2O_3. The broadening indicates the presence of hydroxyl group and is present in samples prepared at all deposition temperatures. In comparison, more hydroxyl group formation is evident for MPALD samples.

C 1s spectra centered around 284 eV is an indication of adsorbed methyl species [161], which seems to vary with deposition temperature; but the variation is not regular with substrate temperature. Peak around 288 eV corresponds to carbonate species [125]. A small peak which correspond to silicate formation is found around 104 eV in the Al 2s spectra. This peak is prominent only for high temperature deposition.

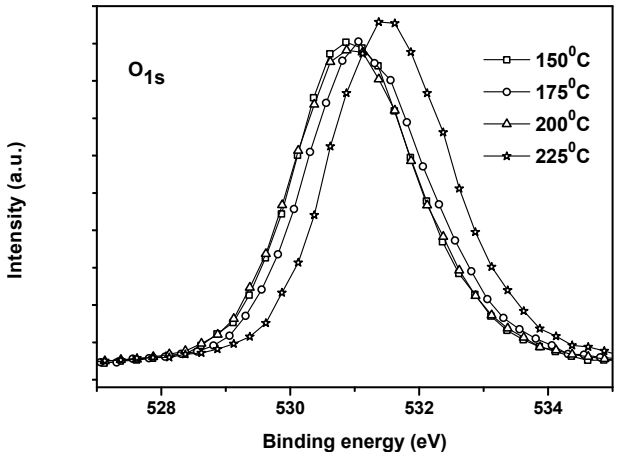

FIGURE 4.6: O 1s spectra for thermal ALD-Al_2O_3 deposited at different substrate temperatures.

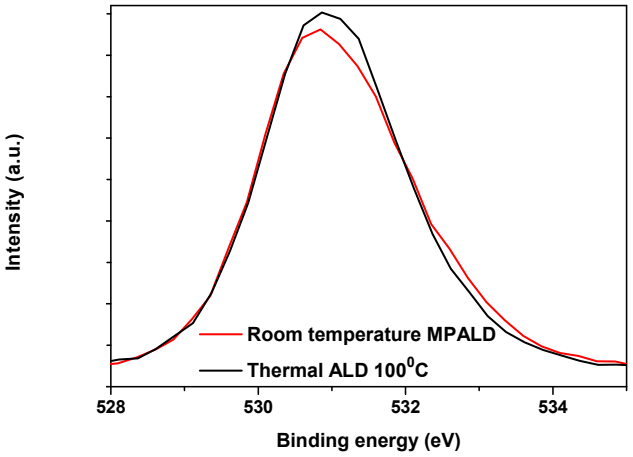

FIGURE 4.7: Comparison of O 1s spectra for thermal ALD and microwave plasma assisted ALD

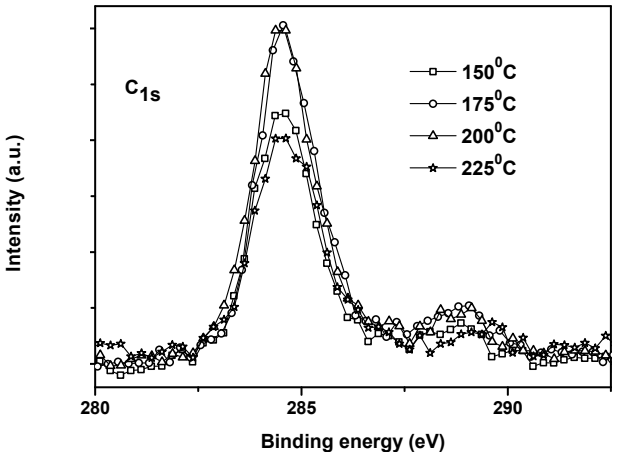

FIGURE 4.8: C 1s spectra for thermal ALD-Al_2O_3 deposited at different substrate temperatures.

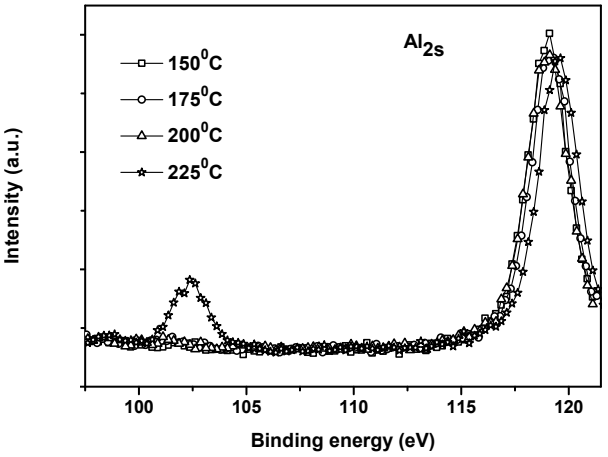

FIGURE 4.9: Al 2s spectra for thermal ALD-Al_2O_3 deposited at different substrate temperatures.

4.5 Electrical characteristics of thermal ALD-Al_2O_3

The electrical characterizations of thermal ALD-Al_2O_3 thin films were done by fabricating MOS capacitor structures. A number of Al/Al_2O_3/p-Si MOS capacitors were fabricated with thermal ALD-Al_2O_3 thin films deposited at different substrate temperatures. Similar to microwave plasma assisted ALD-Al_2O_3 based MOS capacitors, thermal ALD-Al_2O_3 based MOS capacitors were fabricated in three different sizes (500, 600 & 700 μm diameter). 100 nm thick top and bottom aluminium electrodes were deposited using vacuum thermal evaporator. The MOS capacitors were annealed at 400^0C for 30 minutes in foaming gas ambient.

4.5.1 Oxide charges

Figure 4.10 and 4.11 show the variation in flat band voltage with deposition temperature for MOS capacitors fabricated with ALD-Al_2O_3 deposited using the home made system and Fiji F 200 ALD system respectively. The determination of fixed oxide charge density was done after a post deposition foaming gas anneal using the same methodology mentioned in section 3.5.4. For the home made ALD samples, the flat band voltage is on the positive side of the applied gate voltage which indicates the presence of negative fixed oxide charges. The variation in flat band voltage is not regular with deposition temperatures. Al_2O_3 thin films deposited using Fiji F 200 ALD system show a regular variation in flat band voltage to the positive side with decreasing deposition temperature. The variation of flat band voltage with deposition temperature exhibits similar trend for both plasma assisted and thermal ALD using the Fiji ALD system. Thin film deposited at 300^0C using Fiji ALD system show

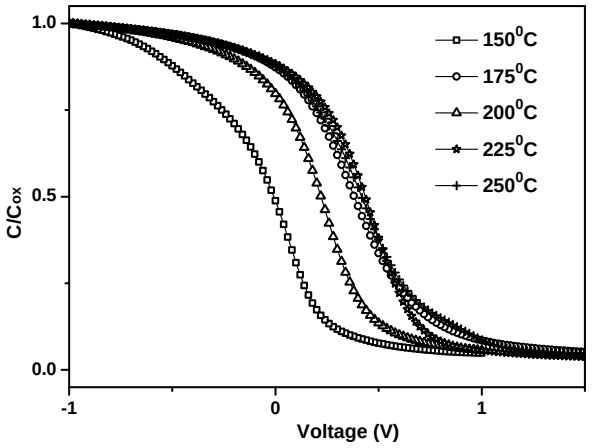

FIGURE 4.10: Normalised C-V characteristics showing the flat band voltage shift of MOS capacitors with thermal ALD-Al_2O_3 deposited at different substrate temperatures in home made ALD system.

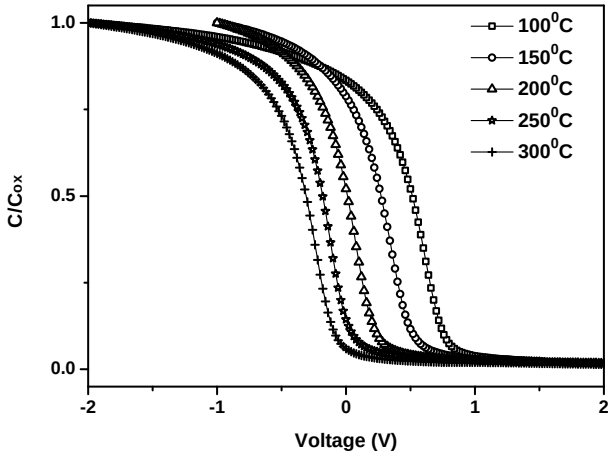

FIGURE 4.11: Normalised C-V characteristics showing the flat band voltage shift of MOScaps with thermal ALD-Al_2O_3 deposited at different substrate temperatures in Fiji F 200 ALD system.

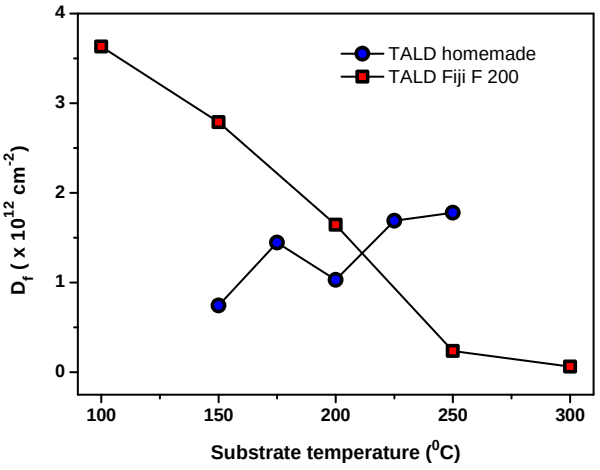

FIGURE 4.12: Variation in fixed oxide charge density with deposition temperature for homemade ALD-Al_2O_3 & for Fiji F 200 ALD-Al_2O_3.

negative flat band voltage shift, which indicates net positive fixed oxide charge in this film.

Figure 4.12 shows the fixed oxide charge density with varying deposition temperature. The fixed oxide charge density remains within same order of magnitude ($10^{12}cm^{-2}$) for thermal ALD-Al_2O_3 thin films prepared using the home made ALD system and Fiji ALD system in thermal mode. Fixed oxide charge density in the order of $10^{11}cm^{-2}$ and $10^{12}cm^{-2}$ for thermal ALD-Al_2O_3 were reported in the literature [137, 162]. Section 3.5.4 of this thesis is about the oxide charges in ALD-Al_2O_3 thin films prepared in plasma mode ALD. On a comparison it is clear that there is no distinct variation of fixed oxide charge density between the thermal and plasma assisted ALD-Al_2O_3 thin films.

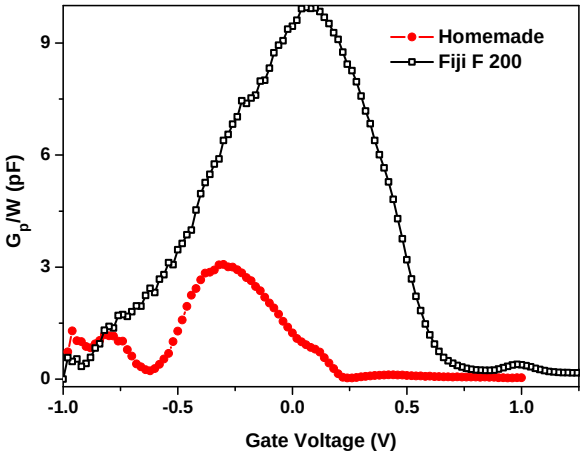

FIGURE 4.13: Comparison of corrected conductance curves for ALD-Al_2O_3 deposited at 150^0C using home made ALD system and Fiji F 200 ALD system.

4.5.2 Interface trap states

The number density of interface trap states was determined from conductance method. Figure 4.13 shows the corrected conductance vs gate voltage curve for ALD-Al_2O_3 thin film based MOS capacitor, where the samples were prepared using the home made ALD system and Fiji F 200 ALD system at 150^0C in thermal mode. Interface state density was calculated from the conductance maximum using equation 3.37. A higher peak of G_p/ω curve represents an increased density of interface states. For thermal mode ALD, the interface state density for the deposited thin films using the home made ALD system has a lower value in comparison with Fiji F ALD system. The interface state density values of thermal ALD-Al_2O_3 thin films deposited at different substrate temperatures are tabulated in table 4.3. The obtained interface state density values for home made thermal ALD films is in the $10^9 cm^{-2}$ eV^{-1} order. But thermal ALD films in Fiji system have interface state density of the order of

ALD Temperature (^{0}C)	D_{it} for Home made (cm^{-2} eV^{-1})	D_{it} for Fiji F 200 (cm^{-2} eV^{-1})
100	-	2.29×10^{10}
150	2.35×10^{9}	1.86×10^{10}
175	4.77×10^{9}	-
200	3.21×10^{9}	3.31×10^{10}
250	1.47×10^{10}	4.77×10^{9}
300	-	2.69×10^{10}

TABLE 4.3: Interface trap level density for thermal ALD-Al_2O_3 films deposited at different substrate temperatures.

$10^9 cm^{-2}$ eV^{-1}. Both these values are in the acceptable limit for gate dielectric application. While comparing the interface state density values of thermal ALD samples with that of plasma ALD samples (section 3.5.5), we can see that the interface state density values are lower for thermal ALD depositions.

4.5.3 Leakage current

Figure 4.14 shows the leakage current density as a function of applied electric field for thermal ALD-Al_2O_3 thin films deposited using home made ALD system at different substrate temperatures. Thin films deposited at all substrate temperatures exhibited similar behaviour of leakage. The leakage current is measured using MOS capacitor structure made out of ALD-Al_2O_3 thin films. The leakage is more in the forward bias region of the applied voltage. The sharp increase in the leakage with applied voltage in the negative gate voltage side is expected to be due to the Fowler-Nordheim tunnelling.

Figure 4.15 is the leakage current density vs applied electric field curve for thermal ALD-Al_2O_3 thin film deposited in Fiji ALD system at different substrate temperatures. The curves represent an irregular variation in

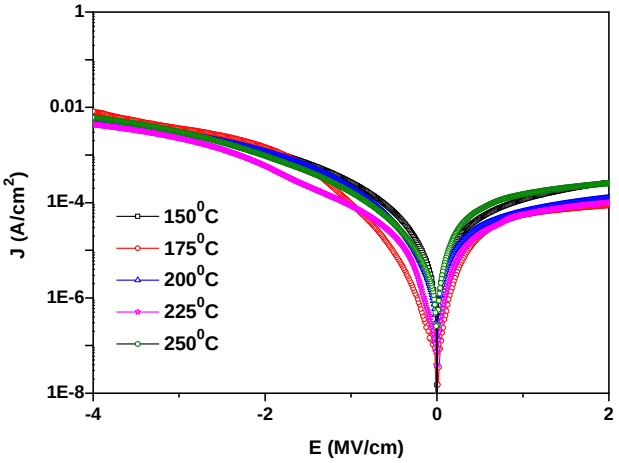

FIGURE 4.14: Leakage current density for ALD-Al_2O_3 thin films deposited at different substrate temperatures using home made ALD system

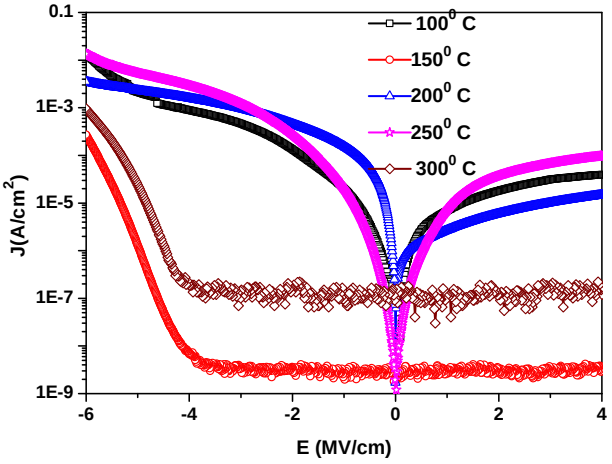

FIGURE 4.15: Leakage current density for ALD-Al_2O_3 thin films deposited at different substrate temperatures using Fiji F 200 ALD system

leakage current with respect to deposition temperature. Films deposited at 150^0C and 300^0C have fairly good leakage current values but the leakage characteristics of all the other thin films are not as good for gate dielectric applications. Any how the leakage current density values are better than leakage values of plasma assisted ALD-Al_2O_3 thin films discussed in section 3.5.6.

4.6 Conclusions

Atomic layer deposition has emerged and grown in the initial period as a temperature assisted method of thin film deposition having a number of advantages over chemical vapour deposition and any forms of physical vapour deposition. Plasma assisted ALD was developed as a modified form of conventional thermal mode ALD and now dominates over thermal ALD. But still the conventional thermal ALD has a favourable position in terms of conformality and defect less nature. In the present work thermal ALD-Al_2O_3 thin films were deposited at different deposition temperatures in two different ALD systems: a home made ALD system and Fiji F 200 ALD system by Cambridge NanoTech. The deposition time for thermal ALD at lower deposition temperatures is higher due to lengthy purge requirement. In home made ALD system, the minimum possible pulse time is 300 millisecond. This will allow excess precursor to the deposition chamber than it required for surface saturation. The excess H_2O precursor will increase the purge time requirement. The growth rate of films in the home made ALD system is higher than that in Cambridge NanoTech's Fiji F 200 ALD system. The structural and compositional characterizations confirmed the formation of ALD-Al_2O_3 thin films. MOS capacitors were fabricated with deposited thin films for their electrical characterizations. The oxide charge density remains invariant with temperature in a 10^{12}

cm^{-2} order for deposition in both the ALD systems. The interface state density is found to be almost an order of magnitude less for ALD-Al_2O_3 depositions in the home made ALD system. The thermal ALD-Al_2O_3 films have all the necessary qualities required for industrial gate oxide purpose except the higher leakage current values. The interface state density values are much better in comparison with the plasma assisted ALD-Al_2O_3 thin films described in the previous chapter.

Chapter 5

Plasma assisted ALD of Higher-κ $HfZrO_2$ thin films

5.1 Introduction

After dominating for around four decades, the SiO_2 dielectric in MOS devices has been replaced by hafnium based dielectrics. The introduction of high-κ/metal gate devices enabled the effective reduction of equivalent oxide thickness without compromise in leakage current. This rendered the microelectronics industry to continue the historical scaling trends as proposed by Gordon E Moore. The non planar device architecture was in production from 22 nm node technology [163]. The experimental efforts to reduce the EOT further beyond 1 nm or less has been diluted by the invention of non planar device architectures. According to 2013 ITRS the scaling technologies based on equivalent scaling (like strained silicon and high-κ/metal gate) will be the supporting technique for microelectronics scaling upto the end of this decade and beyond [48]. So any advancement

in the direction of equivalent scaling can contribute towards further developments in microelectronics industry. HfO_2 is the widely used high-κ dielectric material having a κ value around 20 [164]. Any material having a κ value higher than that of HfO_2 can be called as higher-κ material. The work included in this chapter deals with the efforts to increase the dielectric constant of HfO_2 thin films by structural phase transformations.

5.2 Higher-κ gate dielectrics: A tool for future scaling

The equivalent oxide thickness (EOT) for the first generation high-κ/ metal- gate device was approximately 1 nm [116]. An increased thickness of the high-κ layer can cause mobility degradation by charge trapping [2], remote phonon scattering or by remote charge scattering [165]. The high-κ layer is in the limits of physical thickness scaling in the first high-κ/metal gate devices itself [164]. A further reduction in physical thickness will cause unacceptable leakage currents. By reviewing the scaling approaches researchers in this field suggest three possible fostering routes for further scaling of CMOS devices as (1) introduction of new high-κ material, (2) increase the κ-value of the interfacial layer and (3) reduction in physical thickness of the interfacial layer [164, 166].

In CMOS, HfO_2 based dielectrics are used in its amorphous form. The suitability and performance improvements by crystalline form of HfO_2 are still under debate [167]. There are inspiring reports on electrical properties of the crystalline HfO_2. Negligible effects on gate leakage currents with crystallization was reported by Kim et al. They also found that the additional trap states formed by grain boundary have also negligible effects on conduction [168]. Perkin et al. reported comparable or lower EOT for crystalline ZrO_2 [169]. On both these cases they have

done their experiments with 1.5 nm SiO_2 interfacial layer. At the same time the crystalline HfO_2 with issues on EOT scaling and reliability were also reported. Studies show that boron can diffuse through a thin HfO_2 polycrystalline film via grain boundary diffusion, but not by bulk diffusion [170]. The crystalline portion of HfO_2 in hafnium silicate found to degrade the electron mobility due to additional coloumb scattering other than the substrate impurity scattering [171]. The thermodynamically stable form of HfO_2 at typical CMOS relevant deposition and post deposition annealing (PDA) temperatures is monoclinic [172]. Monoclinic HfO_2 has the minimum dielectric constant compared to the tetragonal and cubic phases [167]. The distinguishable feature of HfO_2 in comparison with other high-κ dielectric candidates is its good thermodynamic stability on silicon [173]. Researchers have made several attempts to stabilize HfO_2 in its higher-κ phases, but could not achieve it yet. The introduction of some suitable dopant material to HfO_2 for improving the κ value seems to be promising and is a hot research topic now.

Interfacial scavenging reactions introduced by Kim et al. [174] can be used to reduce the interfacial layer thickness and hence to reduce the EOT for the future generation of electronic devices with small feature size. Scavenging approaches can be divided into direct and remote scavenging. In direct scavenging the high-κ layer is directly involved in the scavenging reaction and in remote scavenging an additional layer of material that is isolated from the high-κ is used for the reaction [175]. But the interfacial layer reduction beyond a certain limit will introduce some mobility degradation [164, 175]. So a controlled scavenging of the SiO_2 layer together with some higher-κ dielectric layer is the most preferred mechanism for further developments in EOT reduction.

5.3 $HfZrO_2$ as a higher-κ dielectric

HfO_2 and ZrO_2 are two dielectrics having similar properties; they have resemblance in many chemical and physical properties. The resemblance is attributable to the structural similarity between the two oxides, which can in turn be explained by the chemical similarity of Hf and Zr, which have similar atomic and ionic radii (ionic radii for Hf^{4+} and Zr^{4+} are 0.78 and 0.79 A^0 respectively) as a result of the so-called lanthanide contraction[176]. Both HfO_2 and ZrO_2 have well known applications in optics and electronics. They are high band gap materials with fairly good transmission ranging from UV to IR and relatively higher refractive index [177]. Before entering to the microelectronic scenario they were used in buffer layer for supercapacitors [178], in gas sensors [179] and as solid electrolyte [180]. In microelectronics, HfO_2 is preferred over ZrO_2 as gate dielectric, because HfO_2 is little more stable with silicon than ZrO_2. ZrO_2 has the ability to form higher-κ crystallographic phases even at low temperatures. In combination with other dielectric materials ZrO_2 will prompt them to crystallize to higher-κ phases [181] At ambient pressure the oxides of hafnium and zirconium are monoclinic at low temperature and transform to tetragonal structure and then to cubic structure as temperature increases [176]. ZrO_2 is slightly unstable and can react with Si to form the silicide [182–184].

Both HfO_2 and ZrO_2 exist in different crysatlline phases. Bulk ZrO_2 has three crystalline phases at normal pressure: cubic (2300^0C-2680^0C), tetragonal (1170^0C-2300^0C), and monoclinic ($<1170^0$C). Bulk HfO_2 has only two crystalline structures: tetragonal (1750^0C-2800^0C), and monoclinic ($<1750^0$C) [127]. According to theoretical predictions, at elevated temperatures thin film of HfO_2 can stabilize in cubic or tetragonal phase other than monoclinic, which is preferred thermodynamically at ambient conditions. The κ value for tetragonal, cubic and monoclinic phases are

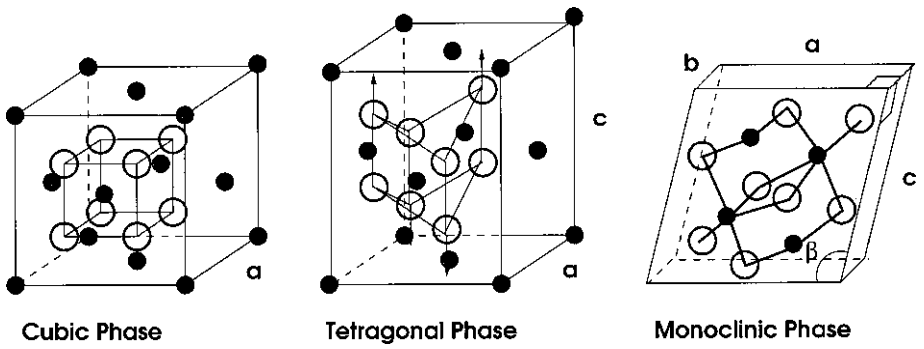

FIGURE 5.1: Structure of three different phases of hafnium oxide . Dark circles are hafnium and open circles are oxygen. HF-O bonds are shown for monoclinic HfO_2 [176].

70,29 and 16 respectively [176]. For amorphous HfO_2, the κ value is almost equal to that of monoclinic phase [185].

The effect of post deposition thermal treatments on the crystallization behaviour and microstructure of the $HfZrO_2$ was studied by glancing angle XRD (GXRD). Unannealed thin films were found to be in amorphous form. For pure HfO_2 with RTA at 500^0C, GXRD evidenced the crystalline nature with monoclinic phase.

There are two ways of achieving higher-κ crystallographic phases of HfO_2: (1) structural phase transformation by doping metal oxide to the HfO_2 (2) controlling the timing of annealing process of amorphous HfO_2 [186]. An oxide matrix of Hafnium and Zirconium, with potential for phase transformation, is tried to grow by sequential atomic layer deposition of hafnium oxide HfO_2 and zirconium oxide ZrO_2. Role of Zr in the crystallization behaviour of $HfZrO_2$ was investigated together with the effects of annealing treatments.

5.4 Review of $HfZrO_2$ as a gate dielectric

The very first paper published on $HfZrO_2$ gate dielectrics had reported a number of advantages over the HfO_2 gate dielectrics. Compared to HfO_2, the $HfZrO_2$ gate dielectric exhibited: (1) higher transconductance, (2) less charge trapping, (3) higher drive current, (4) lower NMOS V_t, (5) reduced C-V hysteresis, (6) lower interface state density, (7) superior wafer-level thickness uniformity and (8) longer Positive Bias Temperature Instability (PBTI) lifetime. They found a 0.4 eV reduction in band gap and noticed the tendency to form smaller grains than HfO_2 [51]. Way Kuo et al. prepared zirconium doped HfO_2 by co-sputtering Hf and Zr [187]. Electrical properties including the equivalent oxide thickness, flat band voltage, interface state density, and the oxide trapped charge density of the MOS capacitors were investigated with respect to fabrication parameters such as Zr doping condition, post deposition annealing ambient and type of bottom interface layer. For similar physical structure they got lower EOT for Zr doped film. They attributed this behaviour to higher thermal stability and hence lower interfacial layer formation in Zr doped HfO_2 film. They deposited both HfO_2 and Zr doped HfO_2 film over SiO_2/Si and SiO_xN_y/Si. The SiO_2/Si intreface exhibited better electrical properties. The lowest interface state density achieved was 1.91×10^{12} cm^{-2} eV^{-1}. The flat band voltage varied its polarity with Zr sputtering power and with post deposition anneal ambient. Way Kuo et al. also studied the breakdown mechanism in Zr doped HfO_2 thin films [134].
D. H. Triyoso et al. have done a number of works on $HfZrO_2$ gate dielectrics; they attained a $\sim2A^0$ increase in capacitance equivalent thickness (CET) [188, 189]. They studied $HfZrO_2$ thin films prepared in different precursor combinations. T. Kelwing et. al. studied physical and electrical properties of metal organic chemical vapour deposited (MOCVD)

and ALD deposited $HfZrO_4$ gate dielectrics for 32 nm CMOS high performance logic silicon on insulator (SOI) technologies. The interface trap charge density and the time dependent dielectric break down reliability were found similar for films made with both the deposition techniques and hence concluded MOCVD as the feasible technique [190]. K. Tapily et al. studied the phase stabilization possibilities by depositing $HfZrO_2$ at varying Zr content and by cyclical deposition and annealing scheme [191]. They obtained monoclinic phase for low zirconium content and tetragonal phase with preferred (111) orientation for increased zirconium content. Relja Vasic et al. had used a multi technique X-ray and optical characterisation to determine the crystal phase of $HfZrO_2$ high-κ dielectric deposited using atomic layer deposition in combination with a cyclic deposition and annealing scheme [192]. They identified an onset of tetragonal phase formation in their method for $\frac{Zr}{Zr+Hf}\% = 58\%$ with a concomitant increase in tetragonal phase with further increase in Zr content.

In 2014, M. N. Bhuyian et al. deposited $HfZrO_2$ thin films by using Ar plasma in the slot plane antenna system by using a cyclical deposition and plasma treatment process termed as DSDS [193]. They studied the gate stack reliability using $HfZrO_2$ as the dielectric by understanding the charge trapping behaviour of the dielectric and its response to electrical stress. $Pt/Al_2O_3/Hf_{0.5}Zr_{0.5}O_2/Al_2O_3$/p-Si memory structure was fabricated and studied by W. Lu et al [194] and they found that the major defects in the system were positively charged ones.

Jae Ho Lee et. al. made attempts to stabilize the tetragonal phase by depositing HfO_2 in an HfO_2 seed layer formed by plasma assisted O_2 and O_3 based ALD followed by post deposition annealing (PDA) treatments [172]. They also attempted alloying of HfO_2 with ZrO_2 thin films. The seed layer approach was not effective in transforming the phase. But the κ

value is found to be tuned with Zr concentration and with PDA temperature. They observed compositional segregation for PDA temperatures higher than 800^0C, which leads to high leakage currents. Several research groups have tried phase stabilization of doped HfO_2 thin films with several dopants in order to achieve ferroelectric behaviour for memory applications [195–199]

5.5 Atomic layer deposition of $HfZrO_2$ thin films

$HfZrO_2$ thin films were deposited over four inch boron doped p-type silicon (100) wafer having 1-5 Ωcm resistivity. Before deposition the silicon wafer was cleaned with standard RCA procedure followed by buffered HF dip. After RCA cleaning the silicon wafer was loaded in to the deposition chamber at the earliest. All the depositions were done at RF plasma assisted Fiji F 200 ALD system by Cambridge NanoTech. Tetrakis(Dimethylamido)Hafnium ($Hf(NMe_2)_4$), Tetrakis(Dimethylamido) Zirconium ($Zr(NMe_2)_4$) and O_2 plasma were the precursors used for the deposition. All the samples were deposited at a substrate temperature of 200^0C. The precursors were kept at 75^0C. The precursor lines and the ALD valves for precursor pulsing were maintained at 150^0C. 50 sccm flow of O_2 was maintained in the chamber and an RF power of 300 W was applied to generate the plasma column. The chamber pressure during deposition was 0.15 mbar. We prepared $HfZrO_2$ thin films at four different ratios by varying zirconium content from zero to 80%. The composition of the prepared thin films are given in table 5.1.

The incorporation of zirconium was exercised by utilizing ALD supercycles. $4HfO_2$+$1ZrO_2$ forms one ALD supercycle for $Hf_{1-0.2}Zr_{0.2}O_2$. The

Film	Hf:Zr Ratio	Thickness (nm)
HfO_2	1:0	2.7
$HfZrO_2$	4:1	2.7
$HfZrO_2$	3:2	2.7
$HfZrO_2$	2:3	2.7
$HfZrO_2$	1:4	2.7

TABLE 5.1: Composition and thickness of the $HfZrO_2$ thin films prepared.

precursor	pulse time(s)	purge time(s)
$Hf(NMe_2)_4$	0.25	5
$Zr(NMe_2)_4$	0.25	5
O_2 plasma	20	5

TABLE 5.2: Precursor exposure time & purge time for plasma assisted ALD-$HfZrO_2$.

Hf:Zr Ratio	ALD supercycle	Film thickness (nm)
4:1	$(4HfO_2+1ZrO_2)\times6$	2.7
3:2	$(3HfO_2+2ZrO_2)\times6$	2.7
2:3	$(2HfO_2+3ZrO_2)\times6$	2.7
1:4	$(1HfO_2+4ZrO_2)\times6$	2.7

TABLE 5.3: ALD supercycle configurations for $HfZrO_2$ thin film deposition.

precursor exposure and purge time for various precursors are given in table 5.2. In supercycle ALD, two different ALD cycles were involved in one complete ALD cycle for $HfZrO_2$. i.e., For depositing 4:1 thin film of $HfZrO_2$ ($Hf_{1-0.2}Zr_{0.2}O_2$) one complete supercycle ALD consists of 4 HfO_2 cycles and one ZrO_2 cycle. The ALD supercycles used for different $HfZrO_2$ films are summarised in table 5.3.

After deposition the thin films were cut into pieces and undergone 30 seconds rapid thermal annealing at 500^0C, 700^0C and 900^0C. Structure and

composition of these $HfZrO_2$ thin films were studied with high resolution X-ray diffraction and X-ray photoelectron spectroscopy.

5.6 Structural and compositional characterization of plasma assisted ALD-$HfZrO_2$

The thermodynamically stable phase of HfO_2 at typical post deposition annealing temperatures is monoclinic [200]. The phase stabilization to higher-κ phases is possible but it is difficult to differentiate between the tetragonal and cubic phases using laboratory X-ray diffraction. In addition the κ value of the two phases are also dependent on the crystallographic directions [172]. So the higher-κ phase is considered as tetragonal , even if it is either tetragonal, cubic or mixture of cubic and tetragonal.

5.6.1 High resolution XRD

Figure 5.4 (a), (b) and (c) show XRD pattern of $HfZrO_2$ thin films with varying Hf:Zr ratio annealed at 500^0C, 700^0C and 900^0C The GXRD was carried out using PANalytical X-pert pro HRXRD system with 0.3 radian incident angle. Figure 5.2 shows the XRD spectrum of HfO_2 thin films subjected to rapid thermal annealing at 500^0C. The peak positions of monoclinic, tetragonal and hafnium silicate are also included in the figure for reference. From the XRD spectra, we can see that the pure HfO_2 is in monoclinic phase after 500^0C anneal. The variation of the crystalline nature with rapid thermal annealing is shown in figure 5.3. Samples annealed at higher temperatures have some tetragonal phase in it. The major peak of tetragonal phase is at 30^0; this peak together with monoclinic peaks at 28^0 and 32^0 has given a broad peak around 30^0.

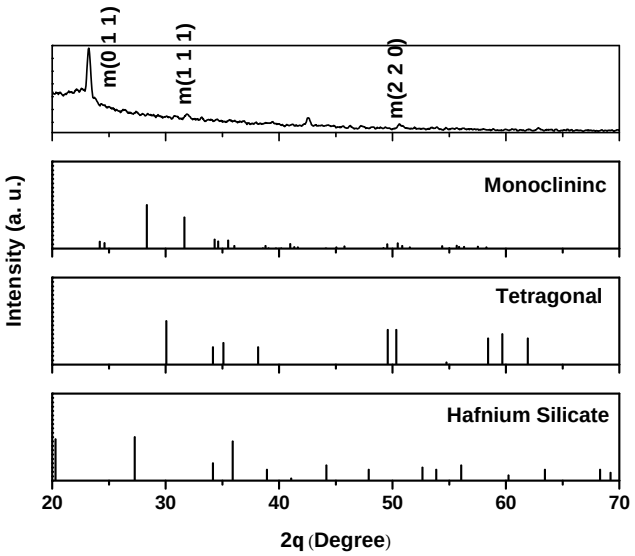

FIGURE 5.2: XRD of pure HfO_2 thin film rapid thermal annealed at 500^0C

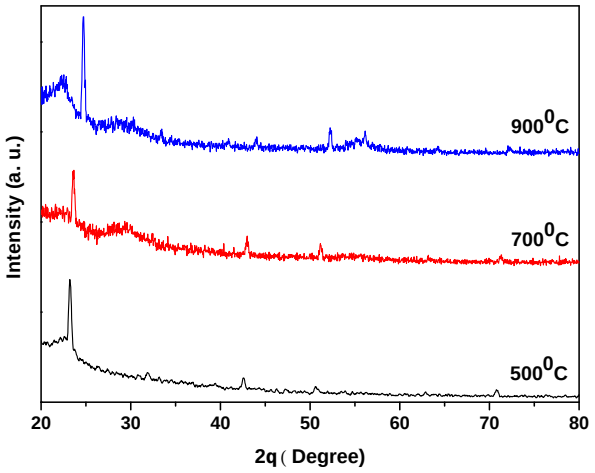

FIGURE 5.3: XRD of pure HfO_2 thin films annealed at different temperatures.

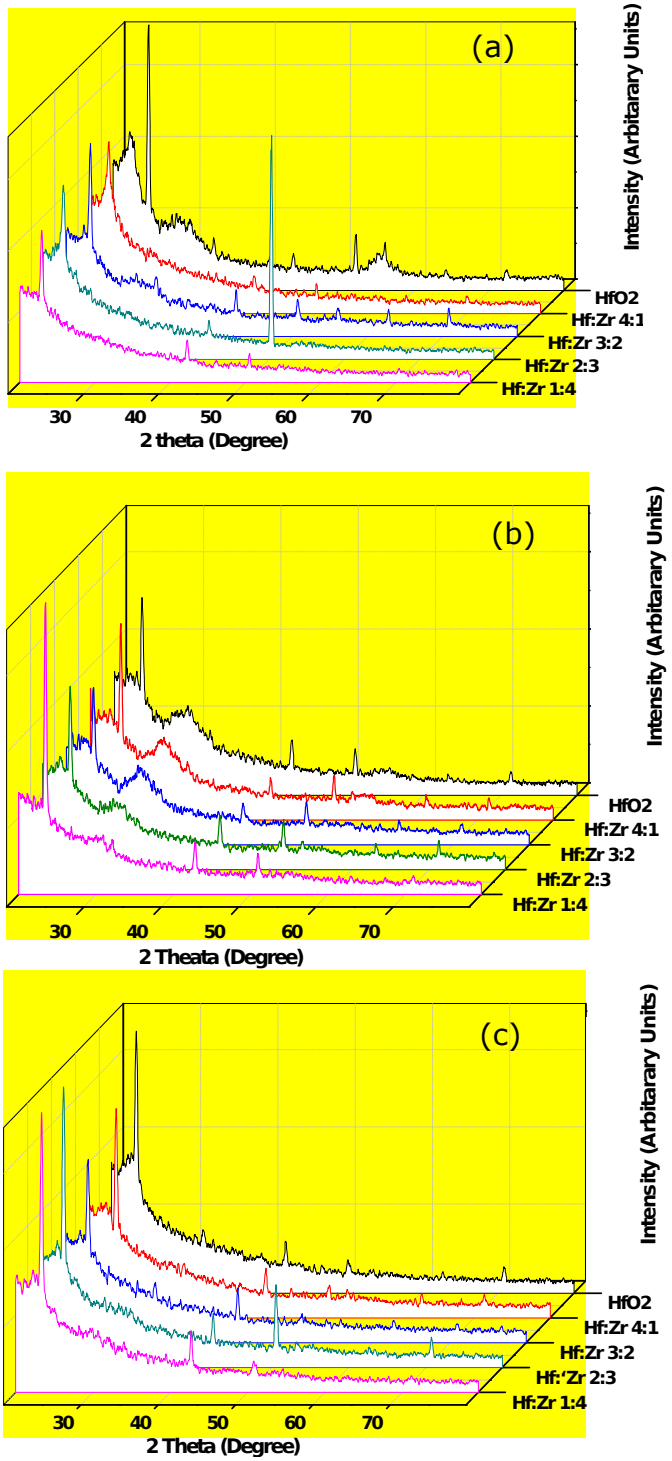

FIGURE 5.4: XRD of $HfZrO_2$ thin films with different Hf:Zr ratio and rapid thermal annealed at (a) 900^0C (b) 700^0C and (c) 500^0C.

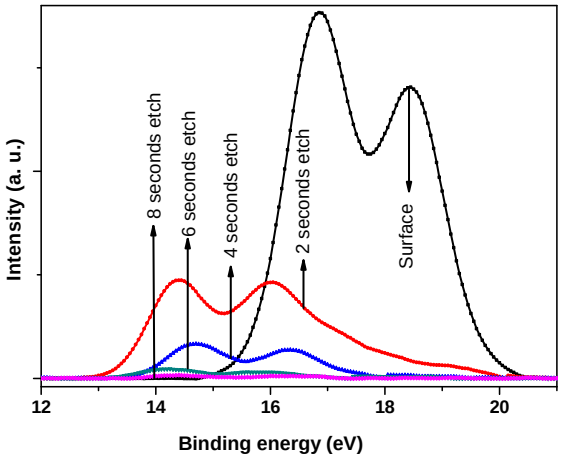

FIGURE 5.5: XPS depth profile of Hf 4f core level spectra for $HfZrO_2$ thin film with Hf:Zr ratio 3:2.

The peak around 42^0 indicates the unwanted silicide formation due to the interaction between HfO_2 and the silicon substrate.

5.6.2 X-Ray photoelectron spectroscopy

X-Ray photoelectron spectroscopy (XPS) measurements were done with Kratos Analyticl's Amicus 3400. XPS meausrement was done on un-annealed $HfZrO_2$ thin film with Hf:Zr ratio 3:2, which is the sample optimized to have maximum tetragonal phase after the rapid thermal anneal. To study the composition of this thin film XPS measurements were done at different depth in this film. The non-stoichiometric $HfSi_xO_y$ structure could be a random mixture of Hf-Si (silicide), HfO_4 (hafnium oxide) and SiO_4 (silicon oxide) tetrahedral and excess Hf and Si atoms [201].

Figure 5.5 shows the depth profile of the Hf 4f core level spectra. The Hf 4f core level spectra from the film surface has doublet feature due to Hf $4f_{7/2}$ and Hf $4f_{5/2}$ spin. The doublet separation for the Hf 4f doublet

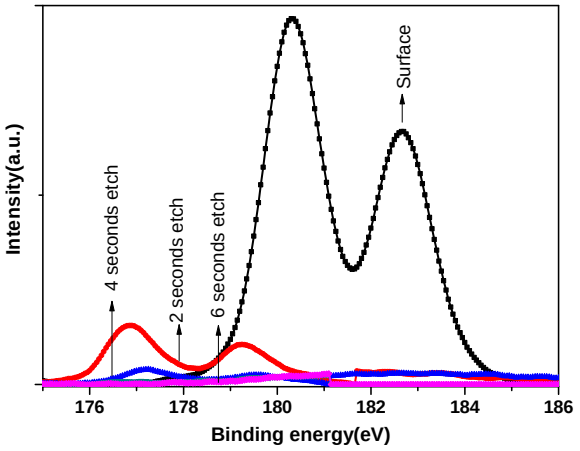

FIGURE 5.6: XPS depth profile of Zr 3d core level spectra for $HfZrO_2$ thin film with Hf:Zr ratio 3:2.

is measured as 1.6 which is close to earlier reports on doublet separation [202]. The measured binding energies are similar to earlier reports on HfO_2 [203]. With etching at different depths the Hf 4f doublet shifts to 14.3 eV to 16.4 eV range. This shift corresponds to silicide (Hf-Si) formation as reported in scientific literature [201, 204]. The binding energy of the Hf 4f peak for Hf silicate shifts to a higher binding energy than that for HfO_2 [205]. So the broadening at the higher binding energy side of the spectra taken from surface and after 2 seconds etch film represents the presence of silicate species. Wilk et al. calculated the difference in binding energy between Hf 4f spectra with and without Hf silicate formation as 1 eV [206]. An unusual shift to the hafniuum core level spectra may also happen by adsorbed organometallic species on the surface [207].

The binding energy of Zr 3d electrons in pure zirconium films are around 178.8 eV for Zr $3d_{5/2}$ and 181.1 eV for Zr $3d_{3/2}$ [203, 208]. For ZrO_2, the 3d doublets have peaks reported at 182.3 ($3d_{5/2}$) and 184.7 ($3d_{3/2}$) [203, 209, 210]. Zr 3d core level spectra for the deposited film is shown in figure 5.6. The Zr 3d doublet peaks for the deposited $HfZrO_2$ thin film

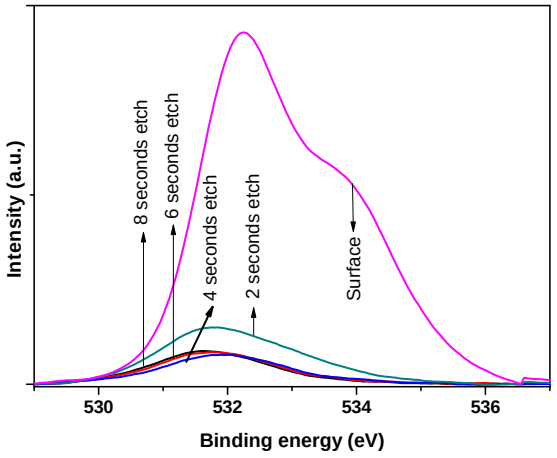

FIGURE 5.7: Depth profile of the O 1s spectra for $HfZrO_2$ thin film with Hf:Zr ratio 3:2.

was at 180.3 ($3d_{5/2}$) and 182.7 ($3d_{3/2}$) for spectra taken from the surface. The magnitude of spin orbit splitting constant for zirconium 3d is found to be 2.4 eV which represents the formation of sub oxides [203]. The Zr 3d core level spectra taken from depth of the $HfZrO_2$ thin films indicate formation of more sub-oxides.

Figure 5.7 shows the O 1s spectra depth profile of the $HfZrO_2$ thin film. The O 1s spectra is expected to have peaks centered around 530 eV and 532.5 eV [211–213] corresponding to Hf-O or Zr-O and Si-O bonds respectively. Hf-O peak is expected to dominate in spectra taken from the surface. But peaks at 532.2 eV and 533.9 eV were dominant in the surface O 1s spectra. The thin films were found to have excess oxygen in their composition. A 2.6 eV shift in Hf-O peak and associated hydroxyl peak was reported by J. P. Lehan et al. [212]. So the peaks at 532.2 eV and 533.9 eV were attributed to Hf-O and to hydroxyl group. After 2 seconds etch, the O 1s spectra has only one peak in binding enrgy centered around 531.6 eV and it can be attributed to Hf-O-Si bonds. Wong et al. describes the chemical shift of O 1s spectra in terms of Hf/Si ratio [201].

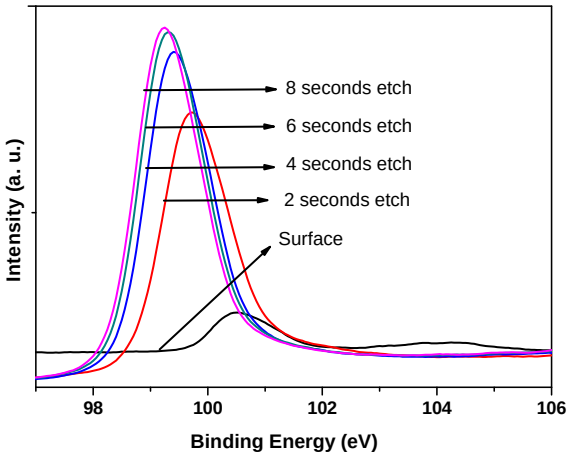

FIGURE 5.8: Depth profile of the Si 2p spectra for $HfZrO_2$ thin film with Hf:Zr ratio 3:2.

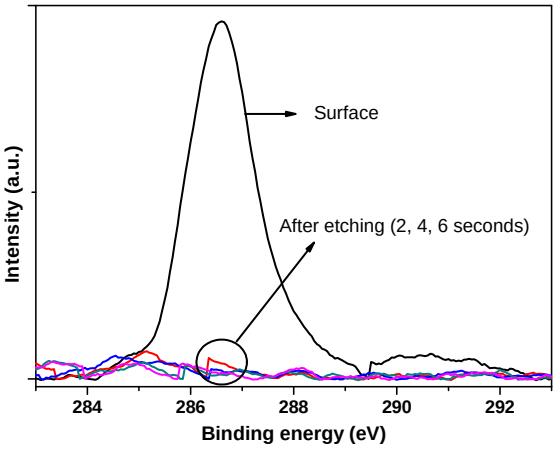

FIGURE 5.9: The C 1s core level XPS depth profile spectra for $HfZrO_2$ thin film with Hf:Zr ratio 3:2.

The irregular shift of O 1s spectra with further etching can be assumed as the effect of the variations in elemental compositions.
The Si 2p core level spectra is shown in figure 5.8. For XPS spectra taken after higher etching (6 & 8 seconds) of the film gave peak around 99.4 eV, representing the silicon substrate [203, 214]. The Si 2p depth profile with 2 to 4 second etching reveals the silicide formation [213]. The Si 2p spectra for stoichiometric SiO_2 is reported to have 103.5 eV binding energy [203, 208, 215]. The binding energy for Si 2p peak in hafnium silicate is at 102.7 eV [215]. In the un-etched spectra, the Si 2p core level has two distinct peaks at 104.2 eV and 100.5 eV. The peak at 104.2 indicates the non-stoichiometric SiO_2 [208]. Figure 5.9 shows the carbon contamination levels with depth in the thin film.

5.7 Electrical characterizations

Al/$HfZrO_2$/p-Si metal oxide semiconductor structures were fabricated for electrical characterizations of the $HfZrO_2$ thin films. MOS capacitors having 500, 600 & 700 μm diameter were fabricated. 100 nm thick top aluminium gate electrodes were deposited using vacuum thermal evaporator. A shadow mask is used for the Al electrode deposition. The backside of the silicon wafer is etched with buffered hydrofluoric acid solution and aluminium back electrode is deposited. MOS capacitors were fabricated with $HfZrO_2$ thin films which were prepared at different HF:Zr ratio followed by rapid thermal annealing at different temperatures (500, 700 & 900^0C). MOS capacitors were subjected to post metallization annealing at 400^0C under foaming gas ambient for 30 minutes.

All MOS capacitors failed to achieve the capacitance saturation at the accumulation region of the capacitance-voltage characteristics. This was same for MOS capacitors with both annealed and un-annealed $HfZrO_2$

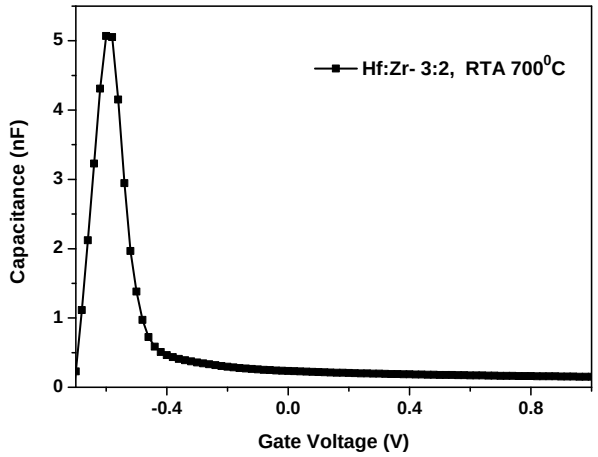

FIGURE 5.10: C-V characteristics of $HfZrO_2$ thin film with 3:2 Hf:Zr ratio and annealed at 700^0C.

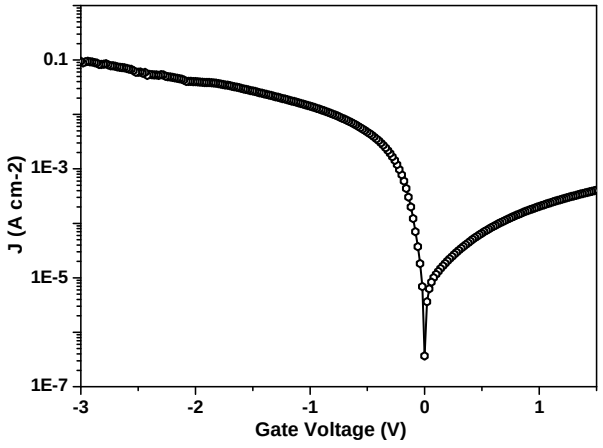

FIGURE 5.11: Leakage current density vs gate voltage for $HfZrO_2$ thin film with 3:2 Hf:Zr ratio and annealed at 700^0C.

thin films. This descending nature of C-V charactristics at the accumulation is due to higher leakage current flowing through the dielectric. Large leakage currents will affect the reliability of the MOS structure. The C-V characteristics and the leakage current characteristics of the $HfZrO_2$ thin films prepared at 3:2 Hf:Zr ratio is given in figure 5.10. Figure 5.11 shows the leakage characteristics of this film. The large value of leakage current flowing through the dielectric is the reason for sudden drop in capacitance during C-V measurements. This prevented us from measuring the electrical parameters like dielectric constant, fixed oxide charge density and interface trap state density.

5.8 Strategy to reduce leakage current

From the electrical characteristics, we can summarise that an interfacial layer requirement is critical for this work. The oxide and oxy-nitride of the wafer are the preferred interfacial layer for silicon wafer based devices. The interfacial layer usually has a lower dielectric constant value and it is favoured to be at its minimum thickness. Chemical oxide formation is the best method for interfacial layer formation because it will provide better control [216] and higher surface OH concentration [194]. For interfacial layer formation we followed the methodology by M. L. Green et al. [194]. They found that for early stages of growth, HfO_2 coverage per cycle is highest for the chemical oxide underlayer in comparison with HF-last case and with the thermal oxide.

For the chemical oxide formation, initially the silicon wafer was cleaned with standard RCA procedure followed by hydrofluoric (HF) acid dip. This last HF dip will remove the unwanted native oxide from the silicon surface. After hydrofluoric acid dip a separate SC1 step was used to grow better SiO_2 layer in preffered thickness (0.5 nm). The SC1 was done at

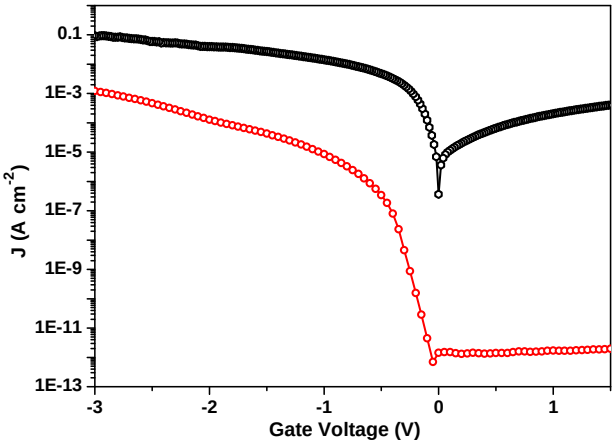

FIGURE 5.12: Leakage current density vs gate voltage for $HfZrO_2$ thin film with and without chemical oxide layer (Hf:Zr ratio 3:2, rapid thermal annealing at 700^0C).

45^0C for 10 minutes. The composition of the SC1 is given below.
$200H_2O + 4H_2O_2(30\%) + 1NH_4OH(29\%)$
A 0.5 nm SiO_2 growth is expected as in the case reported by M. L. Green et al [194].

The substrate is loaded into the ALD chamber immediately (within 5 minutes) after the chemical oxide growth. The $HfZrO_2$ thin films with a 3:2 Hf:Zr ratio were deposited over the SiO_2 interfacial layer by employing super ALD cycles. The deposited films were annealed at 700^0C using rapid thermal annealing process. Al dot electrodes (700 μm) were deposited to form MOS structure with this $SiO_2/HfZrO_2$ combination as the dielectric. The MOS structure was subjected to undergo foaming gas annealing (10% H_2 and 90% Ar) at 400^0C for 30 minutes. The I-V characteristics of the device is shown in figure 5.12. $HfZrO_2$ thin films with intentionally grown SiO_2 showed better leakage characteristics while comparing with $HfZrO_2$ thin films prepared without focussing on interfacial layer growth. Still the gate injection leakage hikes exponentially and soon reaches a higher value.

From this result we conclude the attempt to make the interface between high-k dielectric and silicon better has succeeded to an extent. Further characterizations and optimization of the interfacial layer is required and thereafter $HfZrO_2$ can be subjected to further study.

5.9 Conclusions

An attempt is made to exploit the potential of plasma assisted ALD by using its supercycle formation, to deposit the $HfZrO_2$ thin films and then by stabilizing the tetragonal phase. $HfZrO_2$ thin films were deposited in four different Hf:Zr ratio by simply varying the number of atomic layer deposition cycles in supercycle ALD. Depositions were carried out on H-terminated Si wafers. Post deposition annealing treatments were done at three different temperatures and the change in phase and chemical structure were analysed using XRD and XPS. Unwanted hafnium silicide formation was identified from XPS measurements. 3:2, Hf:Zr ratio $HfZrO_2$ thin film annealed at 700^0C had the maximum tetragonal phase. $HfZrO_2$ thin films were deposited again in the same 3:2 Hf:Zr ratio with intentionally grown SiO_2 interfacial layer. Even though the new method could improve the leakage characteristics, still the $HfZrO_2$ withheld from saturating at the accumulation due to the high flat band voltage shifts.

Chapter 6

Summary & Concluding remarks

6.1 Summary of the thesis

Atomic Layer Deposition (ALD) is emerging with extensive technological applications, which spans diverse areas. ALD market is expected to grow at a CAGR (Compound Annual Growth Rate) of 36.10% from 2013 to 2018. For the same period, the projected growth rate for crystalline silicon solar cell is only 7.82%. This enumerates the growth trend followed by ALD in comparison with other technically relevant fields. The wide acceptance of ALD is attributed two facts: (1) the need for extremly thin films with technological advancement and (2) possible thickness control with conformality and uniformity. In semiconductor industry ALD market is going to overtake the broader equipment market.

ALD is the thin film deposition method in which the precursors are pulsed alternately to the substrate surface and the cyclic repetition of these pulses leads to self limiting surface reactions between gas phase precursor

molecules and a suitable solid surface. In ALD, the substrate surface is initially exposed to the first reactant. After purging out the first reaction by-products the substrate is exposed to the second reactant. This is followed by the purge out of the second reaction by-products. The film is thus grown to desired thickness by repeating this sequential steps and these steps together constitute one ALD cycle.

During the 1990s, development of the ALD stagnated mainly due to slowness of the process. However the newly emerging industrial requirements of ultra thin, defect free films and the large area and batch processing capabilities of ALD made the slowness insignificant for its current applications.

Thermal activation was the only method of initiating ALD reaction in the initial periods of ALD. Later it followed the trend of low temperature activation like plasma activation as in case of CVD. Plasma assisted ALD developed as a low temperature ALD process in which the potential of plasma in generating energetic species is made use of. In PALD at least one of the precursors should be a plasma species or it should be activated with plasma. On comparing with thermal ALD, plasma assisted ALD has the advantages of low temperature growth, increased process versatility, possibility for plasma treatments and a higher throughput.

ALD became popular after its success in deposition of high-κ dielectric thin films for microelectronic application, where the dielectric is a critical operational layer and its modification has remained a hot research topic for the last few decades. The initial big step towards the use of high-κ dielectric was taken by Intel and further studies are still going on. The possible higher physical thickness of high-κ material will help to reduce the tunnelling and reliability issues and will provide a similar electrical performance as that of scaled SiO_2. In future, ALD will be the central thin film deposition tool in industries where thickness, conformality, and/or interface control are key criteria.

As part of this study we developed an atomic layer deposition system, which can work in plasma assisted mode of ALD using its microwave plasma source and in thermal mode ALD. The microwave source and the components for delivering the microwave to plasma applicator were purchased and assembled locally. We have succeeded in alternate generation of microwave plasma during ALD sequence. Generally, the alternate generation of microwave plasma is tedious and hence its use is limited among the ALD community. The plasma applicator, the atomic layer deposition chamber, the gas delivery lines for sequential precursor pulsing and the precursor bubblers were designed and developed indigenously. Maximum power coupling to the plasma and prevention of microwave leakage were ensured during the applicator design. The plasma is arranged in a remote configuration with the deposition chamber. Special care was given to line up the gas flow dynamics and hence to reduce the deposition timings. ALD chamber has provisions for pressure and temperature monitoring, subatrate heating, varying substrate distance from plasma and provisions for using insitu diagnostic tools. In the exhaust side two pumps are connected to the ALD system and the system is generally operated in rotary vacuum. The precursor lines can handle two liquid precursors and one gaseous precursor (other than carrier or purge gas) for a single ALD process. The precursor bubblers can handle low and high vapour pressure precursors.

Atomic layer deposition process in the home made ALD system was optimized by deposition and characterisation of Al_2O_3 thin films using trimethylaluminum and H_2O/O_2 plasma. A linear increase in Al_2O_3 film thickness with deposition cycles was observed for both thermal and plasma assisted ALD, which indicates the true ALD nature of the depositions. A linear GPC vs number of ALD cycles curve was obtained for microwave plasma assisted ALD. A comparatively higher GPC was obtained for microwave plasma assisted ALD. The thermal mode ALD is less efficient (in

terms of time) in comparison to an industrial system but the microwave plasma assisted ALD system is either equally efficient or better.

By varying the substrate temperature, plasma assisted ALD-Al_2O_3 thin films were deposited by the home made ALD system and by a commercial research level ALD system, the Fiji F 200 of Cambridge Nanotech. The Fiji F 200 is a RF plasma assisted ALD system. A decrease in film thickness was observed with increasing deposition temperature. Density, refractive index, composition and morphology of the microwave plasma assisted ALD-Al_2O_3 films were studied.

Al/Al_2O_3/p-Si MOS capacitors were fabricated using both microwave plasma assisted and RF plasma assisted ALD-Al_2O_3 as the dielectric layer. The electrical characteristics of these MOS capacitors were studied to evaluate the ALD-Al_2O_3 as a gate dielectric layer for MOSFET applications. The dielectric constant was fairly good and the number density of fixed oxide charges and interface state density were found to be in the acceptable range for gate oxide applications. The leakage current density is excess than that expected for a gate oxide. In a similar manner thermal ALD-Al_2O_3 films deposited using both the systems were characterised. The dielectric constant was less for thermal ALD thin films. In comparison with plasma assisted ALD-Al_2O_3 thin films, the fixed oxide charges remain almost invariant. The interface state density and the leakage current density for the thermal ALD films were found to be better than plasma assisted ALD thin films.

In 2007, the conventional gate oxide SiO_2 was replaced with HfO_2 by Intel Corporation. The physical thickness of HfO_2 dielectric used in the first device itself was 2 nm and the EOT was 1 nm. Non planar device architectures were introduced with 22 nm feature size electronic devices. A better dielectric can make productive changes even to non planar devices. The stable form of HfO_2 at low temperature is monoclinic. The high temperature tetragonal and cubic phases of HfO_2 have higher dielectric

constant values and can provide better EOT. The stabilization of HfO_2 to its higher dielectric constant phases is a feasible approach for EOT reduction.

The addition of zirconium to hafnium is a method to stabilise the higher-κ HfO_2 phase. Zirconium will tempt the HfO_2 to crystallise with small crystallite sizes. In small crystallites, HfO_2 naturally tend to become tetragonal. $HfZrO_2$ thin films were deposited with different HF:Zr ratio. Supercycle ALD was used for $HfZrO_2$ thin film deposition. XRD studies revealed that $HfZrO_2$ with Hf:Zr ratio of 3:2 subjected to rapid thermal annealing at 700^0C had maximum tetragonal phase. The electrical performance parameters were unable to be calculated due to the higher leakage current. Unintentional Interfacial compound formation was identified as the source of high leakage current. Later an interfacial layer of 0.5 nm SiO_2 was grown intentionally to avoid the formation of unwanted interfacial layers and hence to reduce the leakage current.

6.2 Highlights of the work

- Design and development of a microwave plasma assisted atomic layer deposition system for around 10% cost of a commercial research level ALD system.
- Optimization of ALD process in the home made ALD system.
- Deposition of gate dielectric quality thin films in the home made ALD system both in thermal mode and plasma assisted mode.
- Comparison of the home made ALD-Al_2O_3 film quality with commercial ALD thin film.
- Deposition and studies of higher-κ $HfZrO_2$ thin films for gate oxide application.

6.3 Potential and possibilities

The number of industries that are familiar with and using ALD are very few. According to the 'ALDPulse', a forum for supporting ALD community, the only factor that limits the industrial use of ALD is the lack of information about it. Anyhow the situation is changing at a noticeable speed since the last decade. Over 250 ALD units were dispensed during this period and people are working on a variety of applications using these systems [16]. A few modifications will stimulate the possibilities and capabilities of the home made atomic layer deposition system. Thermally withstanding fast responding 3/2 solenoid valves will make the ALD fast and it will allow the use of more vigorous precursors. An automatic gate valve is useful to adjust the process parameters. The exhaust side need to be replaced with a dry pump rather than rotary pump. An in depth study of plasma is required to coordinate the plasma parameters with film properties. The effect of plasma species on the surface and interfacial properties of the thin film can be studied by varying the distance from the center of the plasma to the substrate. The fixed oxide charge variation in the case of microwave plasma assisted ALD-Al_2O_3 is promising for applications like solar cell passivation. The negative fixed oxide charges and their control using the microwave plasma parameters is a field which requires keen attention for the field effect passivation of solar cells. The highly reactive nature of microwave plasma allows the deposition even on plastic substrates. In addition to the conventional applications of Dynamic Random Accesss Memory (DRAM) and Complementary Metal Oxide Semiconductor (CMOS) electronics, high-κ materials now have a number of emerging applications like Resistive Random Access Memory (RRAM), Metal Insulator Metal (MIM) capacitor, ferroelectric logic & memory devices and mask layers for nanoscale patterning etc [217]. Since Al_2O_3 is a stable material on most of the semiconductor substrates, it acts

as the interfacial layer for many high-κ based applications, especially in high mobility channels.

The use of higher-κ materials together with interfacial layer scaling has current relevance among high-κ dielectric community. HfO_2 films prepared with O_2 plasma assisted atomic layer deposition usually have small crystallite sizes due to the carbon incorporation and seems to form tetragonal phase in post deposition annealing (PDA) treatments [172]. The oxygen vacancies in high-k dielectrics play a crucial role in their flat band voltage and hence in threshold voltage stabilization [210]. Varying the oxygen vacancy levels in $HfZrO_2$ films will provide the role of oxygen vacancies in structural transformation of $HfZrO_2$ during PDA. Formation of a remote scavenging structure over the optimized thin film followed by PDA treatments will provide a higher-κ dielectric based MOS structure with minimum EOT. In hafnium and zirconium based high-κ dielectrics, oxygen vacancies play a crucial role in interfacial scavenging by acting as oxygen transportation sites in the case of a remote scavenging structure and they themselves can act as scavengers to reduce the EOT [164]. On this aspect, we are continuing the study of $HfZrO_2$ thin films by varying the level of oxygen and the carbon contamination. A study of this process may reveal some vital information regarding the phase stabilization in $HfZrO_2$ thin films. A remote scavenging type structure together with these optimized $HfZrO_2$ thin films is expected to give good enough scaling in EOT.

Appendix A

List of publications

A.1 Journal publications

- Subin Thomas, Anu Philip, Nisha R and K Rajeev Kumar. Effect of frequency and bias voltage on the electrical and dielectric properties of atomic layer deposited $Al/Al_2O_3/$ p-Si MOS structure at room temperature. Indian Journal of Pure and Applied Physics, **Accepted (2015)**.

- A Philip, S Thomas and K R Kumar. Calculation of growth per cycle (GPC) of atomic layer deposited aluminium oxide nanolayers and dependence of GPC on surface OH concentration. Pramana, **82(3)**, 2014, pp. 563-569.

- Anu Philip, Subin Thomas and K Rajeev Kumar. Compositional characterization of atomic layer deposited alumina. AIP Conference Proceedings, **183**, 2014, pp. 1576-1578.

- Anu Philip, Subin Thomas, K Rajeev Kumar. Explanation for the appearance of alumina nanoparticles in a cold wall Atomic Layer Deposition system and their characterization. Vacuum, **85**, 2010, pp. 368-372.

- Subin Thomas, Savitha Nalini, SasankaKumar S., K Rajeev Kumar. Substrate temperature dependence of oxide and interfacial characteristics in Microwave plasma assisted ALD-Al_2O_3 thin films (Under review)

A.2 Conference publications

- Measurement of Oxide Charges Present in Alumina Thin Films Prepared by Microwave Plasma Assisted Atomic Layer Deposition, International Conference on Energy harvesting, storage and conversion, held at Cochin University of Science and Technology, Cochin, India during 5-7 February 2015.

- Morphological and compositional characterization of zirconium oxide thin films prepared by atomic layer deposition, Materials and Characterization: Emerging trends held at KKTM college, Kodungalloor during 17-18 December 2013.

- Compositional characterization of atomic layer deposited alumina, OMTAT 2013 held at Cochin University of Science and Technology, Cochin, India during 2-5 January 2013.

- Structural and optical studies of atomic layer deposited Alumina, NSI-37 held at CSIR-CSIO, Chandigarh during October 30-November 1, 2012.

- Dielectric studies of Microwave Plasma Polymerized Allylamine thin films, NSI -37 held at CSIR-CSIO, Chandigarh during October 30-November 1, 2012.

- Effects of temperature and frequency on the dielectric properties of Al/Al_2O_3/p-Si structures, by Atomic layer Deposition, ICMAT 2011 held at Singapore during 26 June - 2 July 2011.

- Remote Plasma ALD - An Advanced Atomic Layer Deposition, National seminar on Recent trends in Nanotechnology held at St. Josephs College Alappuzha, Kerala during September 30- October 1, 2011.

- Influence of frequency on the dielectric properties and ac conductivity of Al/Al_2O_3/P-Si (MOS) capacitor DAE - SSPS 2010 held at Manipal University during 2630 December 2010.

Bibliography

[1] Gregory N. Parsons, Steven M. George, and Mato Knez. Progress and future directions for atomic layer deposition and ALD-based chemistry. *MRS Bulletin*, 36:865, 2011.

[2] Riikka L. Puurunen. A short history of atomic layer deposition: Tuomo Suntola's atomic layer epitaxy. *Chemical Vapor Deposition*, 20(10-11-12):332, 2014.

[3] Riikka L. Puurunen. Surface chemistry of atomic layer deposition: A case study for the trimethylaluminum/water process. *Journal of Applied Physics*, 97(12):121301, 2005.

[4] Markku Leskelä and Mikko Ritala. Atomic layer deposition (ALD): from precursors to thin film structures. *Thin Solid Films*, 409(1): 138, 2002.

[5] M. Knez, K. Nielsch, and L. Niinist. Synthesis and surface engineering of complex nanostructures by atomic layer deposition. *Advanced Materials*, 19(21):3425, 2007.

[6] Delphine Longrie, Davy Deduytsche, and Christophe Detavernier. Reactor concepts for atomic layer deposition on agitated particles: A review. *Journal of Vacuum Science and Technology A*, 32(1): 010802, 2014.

[7] G.L. Doll, B.A. Mensah, H. Mohseni, and T.W. Scharf. Chemical vapor deposition and atomic layer deposition of coatings for mechanical applications. *Journal of Thermal Spray Technology*, 19 (1-2):510, 2010.

[8] G. Dingemans and W. M. M. Kessels. Status and prospects of Al_2O_3-based surface passivation schemes for silicon solar cells. *Journal of Vacuum Science and Technology A*, 30(4):040802, 2012.

[9] Richard W. Johnson, Adam Hultqvist, and Stacey F. Bent. A brief review of atomic layer deposition: from fundamentals to applications. *Materials Today*, 17(5):236, 2014.

[10] Global Atomic Layer Deposition Market 2014-2018. Research and markets website. http://www.researchandmarkets.com/reports/2735170/global_atomic_layer_deposition_market_20142018.

[11] All About ALD. Asm website. http://www.asm.com/technology/key-technologies/all-about-ald.

[12] J. Malm. Surface functionalization by atomic layer deposited binary oxide thin films. *Doctoral Dissertations 57/2013, Aalto University publication series*, 2013.

[13] Atomic Layer Deposition. Beneq website. http://www.beneq.com/atomic-layer-deposition.html.

[14] Anthony C. Jones and Michael L. Hitchman. *Chemical Vapour Deposition : Precursors, Processes and Applications*. The Royal Society of Chemistry, 2009.

[15] Z. Karim T. Seidel, G. Y. Kim and A. Srivastava. Crucial applications addressed via fundemental ALD advances. *Solid State Technology*, 48(2):138, 2005.

[16] ALD in Industry. ALD pulse website. http://www.aldpulse.com/node/16.

[17] Markku Leskelä and Mikko Ritala. Atomic layer deposition chemistry: Recent developments and future challenges. *Angewandte Chemie International Edition*, 42(45):5548, 2003.

[18] J. Schmidt, F. Werner, B. Veith, D. Zielke, R. Bock, V. Tiba, P. Poodt, F. Roozeboom, T.A. Li, A. Cuevas, and R. Brendel. Industrially relevant Al_2O_3 deposition techniques for the surface passivation of Si solar cells. *25th European Photovoltaic Solar Energy Conference and Exhibition / 5th World Conference on Photovoltaic Energy Conversion,Valencia, Spain*, 5:1130, 2010.

[19] H. B. Profijt, S. E. Potts, M. C. M. van de Sanden, and W. M. M. Kessels. Plasma-assisted atomic layer deposition: Basics, opportunities, and challenges. *Journal of Vacuum Science and Technology A*, 29(5):050801, 2011.

[20] 2015 PEALD Publication Review. plasma-ald website. http://www.plasma-ald.com/2015YIR.php.

[21] W. J. Maeng, Sang-Joon Park, and H. Kim. Atomic layer deposition of Ta-based thin films: Reactions of alkylamide precursor with various reactants. *Journal of Vacuum Science and Technology B*, 24 (5):2276, 2006.

[22] Oh-Kyum Kwon, Se-Hun Kwon, Hyoung-Sang Park, and Sang-Won Kang. PEALD of a ruthenium adhesion layer for copper interconnects. *Journal of The Electrochemical Society*, 151(12):C753, 2004.

[23] G.A. Ten Eyck, J.J. Senkevich, F. Tang, D. Liu, S. Pimanpang, T. Karaback, G.-C. Wang, T.-M. Lu, C. Jezewski, and W.A. Lanford. Plasma-assisted atomic layer deposition of palladium. *Chemical Vapor Deposition*, 11(1):60, 2005.

[24] Jin-Seong Park, Min-Jung Lee, Choon-Soo Lee, and Sang-Won Kang. Plasma-enhanced atomic layer deposition of tantalum nitrides using hydrogen radicals as a reducing agent. *Electrochemical and Solid-State Letters*, 4(4):C17, 2001.

[25] Jin-Seong Park, Hyung-Sang Park, and Sang-Won Kang. Plasma-enhanced atomic layer deposition of Ta-N thin films. *Journal of The Electrochemical Society*, 149(1):C28, 2002.

[26] Yangdo Kim, Jaehyoung Koo, Jiwoong Han, Sungwoo Choi, Hyeongtag Jeon, and Chan-Gyung Park. Characteristics of ZrO_2 gate dielectric deposited using Zr t-butoxide and $Zr(NEt_2)_4$ precursors by plasma enhanced atomic layer deposition method. *Journal of Applied Physics*, 92(9):5443, 2002.

[27] Jung Wook Lim, Sun Jin Yun, and Jin Ho Lee. Characteristics of TiO_2 films prepared by ALD with and without plasma. *Electrochemical and Solid-State Letters*, 7(11):F73, 2004.

[28] Jaehyoung Koo, Yangdo Kim, and Hyeongtag Jeon. ZrO_2 gate dielectric deposited by plasma-enhanced atomic layer deposition method. *Japanese Journal of Applied Physics*, 41(5R):3043, 2002.

[29] Kai-Erik Elers, Jerry Winkler, Keith Weeks, and Steven Marcus. $TiCl_4$ as a precursor in the TiN deposition by ALD and PEALD. *Journal of The Electrochemical Society*, 152(8):G589, 2005.

[30] S. E. Potts, W. Keuning, E. Langereis, G. Dingemans, M. C. M. van de Sanden, and W. M. M. Kessels. Low temperature plasma-enhanced atomic layer deposition of metal oxide thin films. *Journal of The Electrochemical Society*, 157(7):P66, 2010.

[31] Jung Wook Li, Sun Jin Yun, and Jin Ho Lee. Low-temperature growth of SiO_2 films by plasma-enhanced atomic layer deposition. *ETRI Journal*, 27(1):118, 2005.

[32] S. E. Potts, L. Schmalz, M. Fenker, B. Daz, J. wiatowska, V. Maurice, A. Seyeux, P. Marcus, G. Radnczi, L. Tth, and W. M. M. Kessels. Ultra-thin aluminium oxide films deposited by plasma-enhanced atomic layer deposition for corrosion protection. *Journal of The Electrochemical Society*, 158(5):C132, 2011.

[33] Sun Jin Yun, Young-Wook Ko, and Jung Wook Lim. Passivation of organic light-emitting diodes with aluminum oxide thin films grown by plasma-enhanced atomic layer deposition. *Applied Physics Letters*, 85(21):4896, 2004.

[34] Hu Young Jeong, Yong In Kim, Jeong Yong Lee, and Sung-Yool Choi. A low-temperature-grown TiO_2 -based device for the flexible stacked RRAM application. *Nanotechnology*, 21(11):115203, 2010.

[35] S.-W. Choi, C.-M. Jang, D.-Y. Kim, J.-S. Ha, H.-S. Park, W. Koh, and C.-S. Lee. Plasma enhanced atomic layer deposition of Al_2O_3 and TiN. *Journal of the Korean Physical Society*, 42(SUPPL.2): S975, 2003.

[36] A. Niskanen, K. Arstila, M. Ritala, and M. Leskelä. Low temperature deposition of aluminum oxide by radical enhanced atomic layer deposition. *Journal of the Electrochemical Society*, 152(7):F90, 2005.

[37] Yujin Lee, Seokhoon Kim, Jaehyoung Koo, Inhoe Kim, Jihoon Choi, Hyeongtag Jeon, and Youngdo Won. Effect of nitrogen incorporation in HfO_2 films deposited by plasma-enhanced atomic layer deposition. *Journal of The Electrochemical Society*, 153(4):G353, 2006.

[38] Woo-Hee Kim, W.J. Maeng, Kyeong-Ju Moon, Jae-Min Myoung, and Hyungjun Kim. Growth characteristics and electrical properties of La_2O_3 gate oxides grown by thermal and plasma-enhanced atomic layer deposition. *Thin Solid Films*, 519(1):362, 2010.

[39] A. Niskanen, K. Arstila, M. Leskelä, and M. Ritala. Radical enhanced atomic layer deposition of titanium dioxide. *Chemical Vapor Deposition*, 13(4):152, 2007.

[40] W. J. Maeng and H. Kim. Thermal and plasma-enhanced ALD of Ta and Ti oxide thin films from alkylamide precursors. *Electrochemical and Solid-State Letters*, 9(6):G191, 2006.

[41] Michael A. Lieberman and Alan J. Lichtenberg. *Principles of plasma discharges and materials processing.* John Wiley and Sons, 2005.

[42] Scott E. Thompson and Srivatsan Parthasarathy. Moore's law: the future of Si microelectronics. *Materials Today*, 9(6):20, 2006.

[43] G. E Moore. Cramming more components onto integrated circuits. *Electronics*, 38(8), 1965.

[44] G.E. Moore. Progress in digital integrated electronics. *International Electron Devices Meeting, 1975*, 21:11, 1975.

[45] C. A. Mack. The end of the semiconductor industry as we know it. *The proceedings of Optical Microlithography XVI, SPIE*, 5040:xxi, 2003.

[46] Robert H. Dennard, Fritz H. Gaensslen, Hwa-Nien Yu, V.Leo Rideout, Ernest Bassous, and Andre R. LeBlanc. Design of ion-implanted mosfet's with very small physical dimensions. *IEEE Journal of Solid-State Circuits*, SC-9(5):256, 1974.

[47] Hei Wong and Hiroshi Iwai. On the scaling of subnanometer EOT gate dielectrics for ultimate nano CMOS technology. *Microelectronic Engineering*, 138:57, 2015.

[48] Executive summary. *2013 International Technology Roadmap for Semiconductors*.

[49] J. Maria A. I. Kingson and S. K. Streiffer. Alternative dielectrics to silicon dioxide for memory and logic devices. *Nature*, 406:1032, 2000.

[50] Supratik Guha and Vijay Narayanan. High-k/metal gate science and technology. *Annual Review of Materials Research*, 39(1):181, 2009.

[51] R.I. Hegde, D.H. Triyoso, P.J. Tobin, S. Kalpat, M.E. Ramon, H.-H. Tseng, J.K. Schaeffer, E. Luckowski, W.J. Taylor, C.C. Capasso, D.C. Gilmer, M. Moosa, A. Haggag, M. Raymond, D. Roan, J. Nguyen, L.B. La, E. Hebert, R. Cotton, X.-D. Wang, S. Zollner, R. Gregory, D. Werho, R.S. Rai, L. Fonseca, M. Stoker, C. Tracy, B.W. Chan, Y.H. Chiu, and Jr. White, B.E. Microstructure modified HfO_2 using Zr addition with Ta_xC_y gate for improved device performance and reliability. *IEEE International Electron Devices Meeting, 2005. IEDM Technical Digest.*, page 35, 2005.

[52] G. D. Wilk, R. M. Wallace, and J. M. Anthony. High-k gate dielectrics: Current status and materials properties considerations. *Journal of Applied Physics*, 89(10):5243, 2001.

[53] E. Eisenbraun. ALD developments, challenges and emerging applications for current and advanced technologies. *Semiconductor fabtech*, 37:73, 2008.

[54] Atomic Layer Deposition (ALD) is a true nanotechnology allowing ultra-thin films of a few nanometres to be deposited in a precisely controlled way. Oxford instruments ald website. http://www.oxford-instruments.com/products/etching-deposition-and-growth/plasma-etch-deposition/atomic-layer-deposition.

[55] Paul Poodt, Adriaan Lankhorst, Fred Roozeboom, Karel Spee, Diederik Maas, and Ad Vermeer. High-speed spatial atomic-layer deposition of aluminum oxide layers for solar cell passivation. *Advanced Materials*, 22(32):3564, 2010.

[56] David Munoz-Rojas and Judith MacManus-Driscoll. Spatial atmospheric atomic layer deposition: a new laboratory and industrial tool for low-cost photovoltaics. *Materials Horizons*, 1:314, 2014.

[57] Tuomo Suntola. Atomic layer epitaxy. *Materials Science Reports*, 4 (5):261, 1989.

[58] Antti Niskanen, Antti Rahtu, Timo Sajavaara, Kai Arstila, Mikko Ritala, and Markku Leskelä. Radical-enhanced atomic layer deposition of metallic copper thin films. *Journal of the Electrochemical Society*, 152(1):G25, 2005.

[59] Ernst Granneman, Pamela Fischer, Dieter Pierreux, Herbert Terhorst, and Peter Zagwijn. Batch aLD: Characteristics, comparison with single wafer ALD, and examples. *Surface and Coatings Technology*, 201(22):8899, 2007.

[60] W. R. Grove. On the electro-chemical polarity of gases. *Philosophical Transactions of the Royal Society London*, 142:87, 1852.

[61] M. de Keijser and C. van Opdorp. Atomic layer epitaxy of gallium arsenide with the use of atomic hydrogen. *Applied Physics Letters*, 58(11):1187, 1991.

[62] Gregory N. Parsons, Jeffrey W. Elam, Steven M. George, Suvi Haukka, Hyeongtag Jeon, W. M. M. (Erwin) Kessels, Markku Leskelä, Paul Poodt, Mikko Ritala, and Steven M. Rossnagel. History of atomic layer deposition and its relationship with the American Vacuum Society. *Journal of Vacuum Science and Technology A*, 31(5):050818, 2013.

[63] S. M. Rossnagel, A. Sherman, and F. Turner. Plasma enhanced atomic layer deposition of Ta and Ti for interconnect diffusion barriers. *Journal of Vacuum Science and Technology B*, 18(4):2016, 2000.

[64] H. Kim and S. M. Rossnagel. Growth kinetics and initial stage growth during plasma-enhanced Ti atomic layer deposition. *Journal of Vacuum Science and Technology A*, 20(3):802, 2002.

[65] H. Kim. Atomic layer deposition of metal and nitride thin films: Current research efforts and applications for semiconductor device processing. *Journal of Vacuum Science and Technology B*, 21(6): 2231, 2003.

[66] E. Langereis, M. Creatore, S. B. S. Heil, M. C. M. van de Sanden, and W. M. M. Kessels. Plasma-assisted atomic layer deposition of Al_2O_3 moisture permeation barriers on polymers. *Applied Physics Letters*, 89(8):081915, 2006.

[67] Yong Ju Lee and Sang-Won Kang. Study on the characteristics of alumdinum thin films prepared by atomic layer deposition. *Journal of Vacuum Science and Technology A*, 20(6):1983, 2002.

[68] Tommi O. Kääriäinen and David C. Cameron. Plasma-assisted atomic layer deposition of Al_2O_3 at room temperature. *Plasma Processes and Polymers*, 6(S1):S237, 2009.

[69] Antti Niskanen, Ulrich Kreissig, Markku Leskelä, and Mikko Ritala. Radical enhanced atomic layer deposition of tantalum oxide. *Chemistry of Materials*, 19(9):2316, 2007.

[70] Woong-Sun Kim, Dae-Yong Moon, Byoung-Woo Kang, Jong-Wan Park, and Jae-Gun Park. Deposition of Al_2O_3 by using ECR-ALD for organic substrate devices. *Journal of the Korean Physical Society*, 55(1):55, 2009.

[71] H. Ishizaki, M. Iida, Y. Otani, Y. Fukuda, T. Sato, T. Takamatsu, and T. Ono. Formation of Al_2O_3 film on Si substrate by microwave generated remote plasma assisted atomic layer deposition technique. *ECS Transactions*, 33(6):227, 2010.

[72] Yukio Fukuda, Hiroki Ishizaki, Yohei Otani, Chiaya Yamamoto, Junji Yamanaka, Tetsuya Sato, Toshiyuki Takamatsu, Hiroshi Okamoto, and Hidehumi Narita. Spontaneous formation of aluminum germanate on Ge(100) by atomic layer deposition with trimethylaluminum and microwave-generated atomic oxygen. *Applied Physics Letters*, 102(13):132904, 2013.

[73] J. Musil. Deposition of thin films using microwave plasmas: present status and trends. *Vacuum*, 47(2):145, 1996.

[74] A. Muller, M. Emme, D. Korzec, and J. Engemann. Direct power coupling into a waveguide cavity plasma source. *Surface and Coatings Technology*, 116-119:674, 1999.

[75] John F. Gerling. Waveguide components and configurations for optimal performance in microwave heating systems. *Technical note, Gerling Applied Engineering, Inc.*, pages 1–8, 2000.

[76] John F. Gerling. Cut-off tube design. *Application Bulletin, Gerling Applied Engineering, Inc.*, 960005:1, 2009.

[77] F. C. Fehsenfeld, K. M. Evenson, and H. P. Broida. Microwave discharge cavities operating at 2450 MHz. *The Review of Scientific Equipments*, 36(3):294, 1965.

[78] L. Hiltunen, H. Kattelus, M. Leskel, M. Mkel, L. Niinist, E. Nyknen, P. Soininen, and M. Tiittad. Growth and characterization of aluminium oxide thin films deposited from various source materials by atomic layer epitaxy and chemical vapor deposition processes. *Materials Chemistry and Physics*, 28(4):379, 1991.

[79] E-L. Lakomaa, A. Root, and T. Suntola. Surface reactions in Al_2O_3 growth from trimethylaluminium and water by atomic layer epitaxy. *Applied Surface Science*, 107:107, 1996.

[80] A.W. Ott, J.W. Klaus, J.M. Johnson, and S.M. George. Al_3O_3 thin film growth on Si(100) using binary reaction sequence chemistry. *Thin Solid Films*, 292(12):135, 1997.

[81] Raija Matero, Antti Rahtu, Mikko Ritala, Markku Leskelä, and Timo Sajavaara. Effect of water dose on the atomic layer deposition rate of oxide thin films. *Thin Solid Films*, 368(1):1, 2000.

[82] L.S. Liyanage, D.J. Cott, A. Delabie, S.V. Elshocht, Z. Bao, and H.-S. Philip Wong. Atomic layer deposition of high-k dielectrics on

single-walled carbon nanotubes: A raman study. *Nanotechnology*, 24(24):245703, 2013.

[83] J. Yang, S. Kim, W. Choi, S.H. Park, Y. Jung, M.-H. Cho, and H. Kim. Improved growth behavior of atomic-layer-deposited high-k dielectrics on multilayer MoS_2 by oxygen plasma pretreatment. *ACS Applied Materials and Interfaces*, 5(11):4739, 2013.

[84] W. Liang, K.J. Weber, D. Suh, S.P. Phang, J. Yu, A.K. McAuley, and B.R. Legg. Surface passivation of boron-diffused p-type silicon surfaces with (1 0 0) and (1 1 1) orientations by ALD Al_2O_3 layers. *IEEE Journal of Photovoltaics*, 3(2):678, 2013.

[85] Baochen Liao, Rolf Stangl, Thomas Mueller, Fen Lin, Charanjit S. Bhatia, and Bram Hoex. The effect of light soaking on crystalline silicon surface passivation by atomic layer deposited Al_2O_3. *Journal of Applied Physics*, 113(2):024509, 2013.

[86] Andrey M. Markeev, Anna G. Chernikova, Anastasya A. Chouprik, Sergey A. Zaitsev, Dmitry V. Ovchinnikov, Holger Althues, and Susanne Drfler. Atomic layer deposition of Al_2O_3 and $Al_xTi_{1-x}O_y$ thin films on N_2O plasma pretreated carbon materials. *Journal of Vacuum Science and Technology A*, 31(1):01135, 2013.

[87] J. W. Liu, M. Y. Liao, M. Imura, H. Oosato, E. Watanabe, A. Tanaka, H. Iwai, and Y. Koide. Interfacial band configuration and electrical properties of $LaAlO_3/Al_2O_3$/hydrogenated-diamond metal-oxide-semiconductor field effect transistors. *Journal of Applied Physics*, 114(8):084108, 2013.

[88] H.-Y. Li, Y.-F. Liu, Y. Duan, Y.-Q. Yang, and Y.-N. Lu. Method for aluminum oxide thin films prepared through low temperature atomic layer deposition for encapsulating organic electroluminescent devices. *Materials*, 8(2):600, 2015.

[89] K. Hong, M. Cho, and S.O. Kim. Atomic layer deposition encapsulated activated carbon electrodes for high voltage stable supercapacitors. *ACS Applied Materials and Interfaces*, 7(3):1899, 2015.

[90] C. Guan, Z. Zeng, X. Li, X. Cao, Y. Fan, X. Xia, G. Pan, H. Zhang, and H.J. Fan. Atomic-layer-deposition-assisted formation of carbon nanoflakes on metal oxides and energy storage application. *Small*, 10(2):300, 2014.

[91] A.L. Lipson, K. Puntambekar, D.J. Comstock, X. Meng, M.L. Geier, J.W. Elam, and M.C. Hersam. Nanoscale investigation of solid electrolyte interphase inhibition on Li-ion battery MnO electrodes via atomic layer deposition of Al_2O_3. *Chemistry of Materials*, 26(2), 2014.

[92] J.L. Van Hemmen, S.B.S. Heil, J. Klootwijk, F. Roozeboom, C.J. Hodson, M.C.M. Van De Sanden, and W.M.M. Kessels. Remote plasma and thermal ALD of Al_2O_3 for trench capacitor applications. *ECS Transactions*, 3(15):67, 2007.

[93] Anu Philip and K. Rajeev Kumar. On adsorption of aluminium and methyl groups on silica for TMA/H_2O process in atomic layer deposition of aluminium oxide nano layers. *Bulletin of Materials Science*, 33(2):97, 2010.

[94] Anu Philip, Subin Thomas, and K Rajeev Kumar. Calculation of growth per cycle (GPC) of atomic layer deposited aluminium oxide nanolayers and dependence of GPC on surface OH concentration. *Pramana*, 82(3):563, 2014.

[95] G. S. Higashi and C. G. Fleming. Sequential surface chemical reaction limited growth of high quality Al_2O_3 dielectrics. *Applied Physics Letters*, 55(19):1963, 1989.

[96] A.C. Dillon, A.W. Ott, J.D. Way, and S.M. George. Surface chemistry of Al_2O_3 deposition using $Al(CH_3)_3$ and H_2O in a binary reaction sequence. *Surface Science*, 322(13):230, 1995.

[97] A.W. Ott, J.W. Klaus, J.M. Johnson, S.M. George, K.C. McCarley, and J.D. Way. Modification of porous alumina membranes using Al_2O_3 atomic layer controlled deposition. *Chemistry of Materials*, 9(3):707, 1997.

[98] A.W. Ott, K.C. McCarley, J.W. Klaus, J.D. Way, and S.M. George. Atomic layer controlled deposition of Al_2O_3 films using binary reaction sequence chemistry. *Applied Surface Science*, 107:128, 1996.

[99] S.M. George, A.W. Ott, and J.W. Klaus. Surface chemistry for atomic layer growth. *Journal of Physical Chemistry*, 100(31):13121, 1996.

[100] S.D. Elliott and J.C. Greer. Simulating the atomic layer deposition of alumina from first principles. *Journal of Materials Chemistry*, 14 (21):3246, 2004.

[101] H.B. Park, M. Cho, J. Park, C.S. Hwang, J.-C. Lee, and S.-J. Oh. Effects of plasma nitridation of Al_2O_3 interlayer on thermal stability, fixed charge density, and interfacial trap states of HfO_2 gate dielectric films grown by atomic layer deposition. *Journal of Applied Physics*, 94(3):1898, 2003.

[102] J.W. Lim and J.Y. Sun. Characterization of AlON-TiON stacked insulators for ZnS:Mn thin film electroluminescent devices. *Electrochemical and Solid-State Letters*, 7(9):H33, 2004.

[103] S.J. Yun, J.W. Lim, and J.-H. Lee. Low-temperature deposition of aluminum oxide on polyethersulfone substrate using plasma-enhanced atomic layer deposition. *Electrochemical and Solid-State Letters*, 7(1):C13, 2004.

[104] K.-Y. Park, H.-I. Cho, J.-H. Li, S.-B. Bae, C.-M. Jeon, J.-L. Lee, D.-Y. Kim, C.-S. Lee, and J.-H. Lee. Fabrication of AlGaN/GaN MIS-HFET using an Al_2O_3 high-k dielectric. *Physica Status Solidi C: Conferences*, (7):2351, 2003.

[105] Th. Seyller, K. Gao, L. Ley, F. Ciobanu, G. Pensl, A. Tadich, J.D. Riley, and R.C.G. Leckey. Structural and electronic properties of the 6H-SiC(0001)/Al_2O_3 interface prepared by atomic layer deposition. *Materials Science Forum*, 457-460(II):1369, 2004.

[106] S.-C. Ha, E. Choi, S.-H. Kim, and J.S. Roh. Influence of oxidant source on the property of atomic layer deposited Al_2O_3 on hydrogen-terminated Si substrate. *Thin Solid Films*, 476(2):252, 2005.

[107] S. B. S. Heil, P. Kudlacek, E. Langereis, R. Engeln, M. C. M. van de Sanden, and W. M. M. Kessels. In situ reaction mechanism studies of plasma-assisted atomic layer deposition of Al_2O_3. *Applied Physics Letters*, 89(13):131505, 2006.

[108] E. Langereis, M. Bouman, J. Keijmel, S.B. S. Heil, M. C. M. Van de Saden, and W. M. M. Kessels. Plasma-assisted ALD of Al_2O_3 at low temperatures: Reaction mechanism and material properties. *ECS Transactions*, 16(4):247, 2008.

[109] S. B. S. Heil, J. L. van Hemmen, M. C. M. van de Sanden, and W. M. M. Kessels. Reaction mechanisms during plasma-assisted atomic layer deposition of metal oxides: A case study for Al_2O_3. *Journal of Applied Physics*, 103(10):103302, 2008.

[110] W.-S. Kim, D.-Y. Moon, B.-W. Kang, J.-W. Park, and J.-G. Park. Deposition of Al_2O_3 by using ECR-ALD for organic substrate devices. *Journal of the Korean Physical Society*, 55(1):55, 2009.

[111] D. Hoogeland, K. B. Jinesh, F. Roozeboom, W. F. A. Besling, M. C. M. van de Sanden, and W. M. M. Kessels. Plasma-assisted atomic layer deposition of TiN/Al_2O_3 stacks for metal-oxide-semiconductor capacitor applications. *Journal of Applied Physics*, 106(11):114107, 2009.

[112] J. Dendooven, D. Deduytsche, J. Musschoot, R.L. Vanmeirhaeghe, and C. Detavernier. Conformality of Al_2O_3 and AlN deposited by plasma-enhanced atomic layer deposition. *Journal of the Electrochemical Society*, 157(4):G111, 2010.

[113] H.C.M. Knoops, E. Langereis, M.C.M. Van De Sanden, and W.M.M. Kessels. Conformality of plasma-assisted ALD: Physical processes and modeling. *Journal of the Electrochemical Society*, 157 (12):G241, 2010.

[114] Fiji F200 series is the Cambridge NanoTech's most advanced ALD research and development system. Annealsys website. http://www.annealsys.com/ultratech-products/ald-plasma/fiji.html.

[115] Fiji Generation 2 (G2) Technical Specifications. Annealsys website. http://www.annealsys.com/docs/Fiji-G2-spec-sheet-Rev-2-22-04-14-00.pdf.

[116] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, C.-H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu,

J. Maiz, B. McIntyre, P. Moon, J. Neirynck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes, M. Prince, P. Rarade, T. Reynolds, J. Sandford, L. Shifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S. Williams, and K. Zawadzki. A 45nm logic technology with high-k+ metal gate transistors, strained silicon, 9 Cu interconnect layers, 193 nm dry patterning, and 100 percent Pb-free packaging. *Technical Digest - International Electron Devices Meeting, IEDM*, page 247, 2007.

[117] J. A. Aboaf. Deposition and properties of aluminum oxide obtained by pyrolytic decomposition of an aluminum alkoxide. *Journal of The Electrochemical Society*, 114(9):948, 1967.

[118] X ray Reflectivity (XRR): The technology. Bruker website. https://www.bruker.com/products/x-ray-diffraction-and-elemental-analysis/x-ray-metrology/d8-fabline/metrology-knowledge/x-ray-metrology-knowledge/xrr.html.

[119] M. D. Groner, F. H. Fabreguett, and J. W. Elam amd S. M. George. Low temperature Al_2O_3 atomic layer deposition. *Chemistry of Materials*, 16:639, 2004.

[120] K. Kukli, M. Ritala, M. Leskelä, and J. Jokinen. Atomic layer epitaxy growth of aluminum oxide thin films from a novel $Al(CH_3)_2Cl$ precursor and H_2O. *Journal of Vacuum Science and Technology A*, 15:2214, 1997.

[121] What is X-Ray Photoelectron Spectroscopy (XPS)? Thermoscientific website. http://xpssimplified.com/whatisxps.php.

[122] L. Zhang, H. C. Jiang, C. Liu, J. W. Dong, and P. Chow. Annealing of Al_2O_3 thin films prepared by atomic layer deposition. *Journal of Physics D: Applied Physics*, 40:3707, 2007.

[123] Fu Guang-Sheng, Ding Wen-Ge, Song Wei-Cai, Zhang Jiang-Yong, and Yu Wei. Microstructure modification of silicon nanograins embedded in silicon nitride thin films. *Chinese Physics Letters*, 23(7): 1926, 2006.

[124] Seong Keun Kim and Cheol Seong Hwang. Atomic-layer-deposited Al_2O_3 thin films with thin SiO_2 layers grown by in situ O_3 oxidation. *Journal of Applied Physics*, 96(4):2323, 2004.

[125] Byeong-Ok Cho, Sandy Lao, Lin Sha, and Jane P. Chang. Spectroscopic study of plasma using zirconium tetra-tert-butoxide for the plasma enhanced chemical vapor deposition of zirconium oxide. *Journal of Vacuum Science and Technology A*, 19(6):2751, 2001.

[126] Field Emission Scanning Electron Microscopy (FE-SEM). Photometrics website. http://photometrics.net/field-emission-scanning-electron-microscopy-fesem/.

[127] J. R. Brews E. H. Nicollian. *MOS (Metal Oxide Semiconductor) Physics and Technology*. John Wiley and Sons Inc., 2002.

[128] Robert F. Pierret. *Semiconductor Device Fundamentals*. Pearson Education, 1996.

[129] A.S. Grove, B.E. Deal, E.H. Snow, and C.T. Sah. Investigation of thermally oxidised silicon surfaces using metal-oxide-semiconductor structures. *Solid-State Electronics*, 8(2):145, 1965.

[130] Chenming Calvin Hu. *Modern Semiconductor Devices for Integrated Circuits*. Pearson Education, 2009.

[131] Dieter K. Schroder. *Semiconductor Material and Device Characterization*. Wiley-IEEE Press, 2006.

[132] A. Tataroğlu, Ş. Altındal, and M.M. Bülbül. Temperature and frequency dependent electrical and dielectric properties of $Al/SiO_2/p$-Si (MOS) structure. *Microelectronic Engineering*, 81(1):140, 2005.

[133] Wen Luo, Tao Yuan, Yue Kuo, Jiang Lu, Jiong Yan, and Way Kuo. Breakdown phenomena of zirconium-doped hafnium oxide high-k stack with an inserted interface layer. *Applied Physics Letters*, 89 (7):072901, 2006.

[134] Wen Luo, Tao Yuan, Yue Kuo, Jiang Lu, Jiong Yan, and Way Kuo. Breakdown phenomena of zirconium-doped hafnium oxide high-k stack with an inserted interface layer. *Applied Physics Letters*, 89 (7):072901, 2006.

[135] D.M. Fleetwood, M.R. Shaneyfelt, W.L. Warren, J.R. Schwank, T.L. Meisenheimer, and P.S. Winokur. Border traps: Issues for MOS radiation response and long-term reliability. *Microelectronics Reliability*, 35(3):403, 1995.

[136] M. Houssa. *High-k Gate Dielectrics*. Institute of Physics Publishing, 2003.

[137] Karsten Henkel, Hassan Gargouri, Bernd Gruska, Michael Arens, Massimo Tallarida, and Dieter Schmeißer. Capacitance and conductance versus voltage characterization of Al_2O_3 layers prepared by plasma enhanced atomic layer deposition at $25°C \leq$ to $\leq 200°C$. *Journal of Vacuum Science and Technology A*, 32(1):01107, 2014.

[138] B. Hoex, J. J. H. Gielis, M. C. M. van de Sanden, and W. M. M. Kessels. On the c-Si surface passivation mechanism by the negative-charge-dielectric Al_2O_3. *Journal of Applied Physics*, 104(11):113703, 2008.

[139] S. Dueñas, H. Casťan, H. García, A. de Castro, L. Bailón, K. Kukli, A. Aidla, J. Aarik, H. Mändar, T. Uustare, J. Lu, and A. Hårsta. Influence of single and double deposition temperatures on the interface quality of atomic layer deposited Al_2O_3 dielectric thin films on silicon. *Journal of Applied Physics*, 99(5):054902, 2006.

[140] J. Buckley, B. De Salvo, D. Deleruyelle, M. Gely, G. Nicotra, S. Lombardo, J.F. Damlencourt, Ph. Hollinger, F. Martin, and S. Deleonibus. Reduction of fixed charges in atomic layer deposited Al_2O_3 dielectrics. *Microelectronic Engineering*, 80:210, 2005.

[141] J. A. Aboaf, D. R. Kerr, and E. Bassous. Charge in SiO_2 - Al_2O_3 double layers on silicon. *Journal of The Electrochemical Society*, 120 (8):1103, 1973.

[142] Robert S. Johnson, Gerald Lucovsky, and Isreal Baumvol. Physical and electrical properties of noncrystalline Al_2O_3 prepared by remote plasma enhanced chemical vapor deposition. *Journal of Vacuum Science and Technology A*, 19(4):1353, 2001.

[143] Sang Yong No, Dail Eom, Cheol Seong Hwang, and Hyeong Joon Kim. Property changes of aluminum oxide thin films deposited by atomic layer deposition under photon radiation. *Journal of The Electrochemical Society*, 153(6):F87, 2006.

[144] Armin G. Aberle, Stefan Glunz, and Wilhelm Warta. Impact of illumination level and oxide parameters on Shockley-Read-Hall recombination at the Si/SiO_2 interface. *Journal of Applied Physics*, 71(9):4422, 1992.

[145] S. Kar and W.E. Dahlke. Interface states in MOS structures with 20-40 Å thick SiO_2 films on nondegenerate Si. *Solid-State Electronics*, 15(2):221, 1972.

[146] G. Dingemans, N. M. Terlinden, D. Pierreux, H. B. Profijt, M. C.M. van de Sanden, and W. M.M. Kessels. Influence of the oxidant on the chemical and field-effect passivation of Si by ALD Al_2O_3. *Electrochemical and Solid-State Letters*, 14(1):H1, 2011.

[147] V. Misra, G. Lucovsky, and G. Parsons. Issues in high-k gate stack interfaces. *MRS Bulletin*, 27(3):212, 2002.

[148] H. Wong and H. Iwai. On the scaling issues and high-k replacement of ultrathin gate dielectrics for nanoscale MOS transistors. *Microelectronic Engineering*, 83:1867, 2006.

[149] E. H. Nicollian and A. Goetzberger. The Si-SiO_2 interface - electrical properties as determined by the metal insulator silicon conductance technique. *The Bell System Technical Journal*, XLVI(6):1055, 1967.

[150] L.M. Terman. An investigation of surface states at a silicon/silicon oxide interface employing metal-oxide-silicon diodes. *Solid-State Electronics*, 5(5):285, 1962.

[151] Eric M. Vogel and George A. Brown. Challenges of electrical measurements of advanced gate dielectrics in metaloxidesemiconductor devices. *AIP Conference Proceedings*, 683(1):771, 2003.

[152] C.K. Maiti, G.K. Dalapati, S. Chatterjee, S.K. Samanta, S. Varma, and S. Patil. Electrical properties of high permittivity ZrO_2 gate dielectrics on strained-Si. *Solid-State Electronics*, 48(12):2235, 2004.

[153] S. Kaya and E. Yilmaz. A comprehensive study on the frequency-dependent electrical characteristics of Sm_2O_3 MOS capacitors. *IEEE Transactions on Electron Devices*, 62(3):980, 2015.

[154] Yu. N. Novikov, V. A. Gritsenko, and K. A. Nasyrov. Charge transport mechanism in amorphous alumina. *Applied Physics Letters*, 94 (22):222904, 2009.

[155] Steven M. George. Atomic layer deposition: An overview. *Chemical Reviews*, 110(1):111, 2010.

[156] Riikka L. Puurunen. Correlation between the growth-per-cycle and the surface hydroxyl group concentration in the atomic layer deposition of aluminum oxide from trimethylaluminum and water. *Applied Surface Science*, 245(14):6, 2005.

[157] R.L. Puurunen. Formation of metal oxide particles in atomic layer deposition during the chemisorption of metal chlorides: A review. *Chemical Vapor Deposition*, 11(2):79, 2005.

[158] Sun Jin Yun, Kyung-Ho Lee, Jarmo Skarp, Hae-Rim Kim, and Kee-Soo Nam. Dependence of atomic layer-deposited Al_2O_3 films characteristics on growth temperature and Al precursors of $Al(CH_3)_3$ and $AlCl_3$. *Journal of Vacuum Science and Technology A*, 15(6): 2993, 1997.

[159] E. Ghiraldelli, C. Pelosi, E. Gombia, G. Chiavarotti, and L. Vanzetti. ALD growth, thermal treatments and characterisation of Al_2O_3 layers. *Thin Solid Films*, 517(1):434, 2008.

[160] O. Böse, E. Kemnitz, A. Lippitz, and W. E. S. Unger. C_{1s} and Au $_{4f_{7/2}}$ referenced XPS binding energy data obtained with different aluminium oxides, -hydroxides and -fluorides. *Fresenius' Journal of Analytical Chemistry*, 358(1):175, 1997.

[161] Riikka L. Puurunen, Andrew Root, Suvi Haukka, Eero I. Iiskola, Marina Lindblad, , and A. Outi I. Krause. IR and NMR study of the chemisorption of ammonia on trimethylaluminum-modified silica. *The Journal of Physical Chemistry B*, 104(28):6599, 2000.

[162] Carey M. Tanner, Ya-Chuan Perng, Christopher Frewin, Stephen E. Saddow, and Jane P. Chang. Electrical performance of Al_2O_3 gate

dielectric films deposited by atomic layer deposition on 4H-SiC. *Applied Physics Letters*, 91(20):203510, 2007.

[163] Over 6 decades of continued transistor shrinkage innovation. Intel website. http://www.intel.com/content/www/us/en/silicon-innovations/standards-22-nanometers-technology-backgrounder.html.

[164] Takashi Ando. Ultimate scaling of high-k gate dielectrics: Higher-k or interfacial layer scavenging? *Materials*, 5(3):478, 2012.

[165] M. A. Negara, K. Cherkaoui, P. K. Hurley, C. D. Young, P. Majhi, W. Tsai, D. Bauza, and G. Ghibaudo. Analysis of electron mobility in HfO_2/TiN gate metal-oxide-semiconductor field effect transistors: The influence of HfO_2 thickness, temperature, and oxide charge. *Journal of Applied Physics*, 105(2):024510, 2009.

[166] Martin M. Frank, SangBum Kim, Stephen L. Brown, John Bruley, Matthew Copel, Marco Hopstaken, Michael Chudzik, and Vijay Narayanan. Scaling the MOSFET gate dielectric: From high-k to higher-k? *Microelectronic Engineering*, 86(79):1603, 2009.

[167] Yi Zhao. Design of higher-k and more stable rare earth oxides as gate dielectrics for advanced CMOS devices. *Materials*, 5(8):1413, 2012.

[168] Hyoungsub Kim, Paul C. McIntyre, and Krishna C. Saraswat. Effects of crystallization on the electrical properties of ultrathin HfO_2 dielectrics grown by atomic layer deposition. *Applied Physics Letters*, 82(1):106, 2003.

[169] Charles M. Perkins, Baylor B. Triplett, Paul C. McIntyre, Krishna C. Saraswat, Suvi Haukka, and Marko Tuominen. Electrical and materials properties of ZrO_2 gate dielectrics grown by atomic

layer chemical vapor deposition. *Applied Physics Letters*, 78(16): 2357, 2001.

[170] Chun-Li Liu, Z. X. Jiang, R. I. Hegde, D. D. Sieloff, R. S. Rai, D. C. Gilmer, C. C. Hobbs, P. J. Tobin, and Shifeng Lu. Theoretical and experimental investigation of boron diffusion in polycrystalline HfO_2 films. *Applied Physics Letters*, 81(8):1441, 2002.

[171] T. Yamaguchi, R. Iijima, T. Ino, A. Nishiyama, H. Satake, and N. Fukushima. International electron devices meeting, 2002. iedm '02. page 621, 2002.

[172] Jae Ho Lee, Il-Hyuk Yu, Sang Young Lee, and Cheol Seong Hwang. Phase control of HfO_2-based dielectric films for higher-k materials. *Journal of Vacuum Science and Technology B*, 32(3):03109, 2014.

[173] Gang He, Zhaoqi Sun, Guang Li, and Lide Zhang. Review and perspective of Hf-based high-k gate dielectrics on silicon. *Critical Reviews in Solid State and Materials Sciences*, 37(3):131, 2012.

[174] Hyoungsub Kim, Paul C. McIntyre, Chi On Chui, Krishna C. Saraswat, and Susanne Stemmer. Engineering chemically abrupt high-k metal oxidesilicon interfaces using an oxygen-gettering metal overlayer. *Journal of Applied Physics*, 96(6):3467, 2004.

[175] Takashi Ando, Martin M. Frank, Kisik Choi, Changhwan Choi, John Bruley, Marinus J. Hopstaken, Richard Haight, Matthew Copel, Hiroaki Arimura, Heiji Watanabe, and Vijay Narayanan. Ultimate EOT scaling (< 5Å) using Hf-based high-k gate dielectrics and impact on carrier mobility. *ECS Transactions*, 28(1):115, 2010.

[176] Xinyuan Zhao and David Vanderbilt. First-principles study of structural, vibrational, and lattice dielectric properties of hafnium oxide. *Physical Review B*, 65:233106, 2002.

[177] I.P. Studenyak, M. Kranjec, O.T. Nahusko, and O.M. Borets. Influence of HfZr substitution on optical and refractometric parameters of $Hf_{1-x}Zr_xO_2$ thin films. *Thin Solid Films*, 476(1):137, 2005.

[178] H. Wendel, H. Holzschuh, H. Suhr, G. Erker, S. Dehnicke, and M. Mena. Thin zirconium dioxide and yttrium oxide-stabilized zirconium dioxide films prepared by plasma-CVD. *Modern Physics Letters B*, 04(19):1215, 1990.

[179] Mikko Ritala and Markku Leskelä. Zirconium dioxide thin films deposited by ALE using zirconium tetrachloride as precursor. *Applied Surface Science*, 75(14):333, 1994.

[180] K. Sasaki and J. Maier. Re-analysis of defect equilibria and transport parameters in Y_2O_3-stabilized ZrO_2 using EPR and optical relaxation. *Solid State Ionics*, 134(34):303, 2000.

[181] Michael A. Lieberman and Alan J. Lichtenberg. *Principles of plasma discharges and materials processing.* John Wiley and Sons, 2005.

[182] M. Copel, M. Gribelyuk, and E. Gusev. Structure and stability of ultrathin zirconium oxide layers on Si(001). *Applied Physics Letters*, 76(4):436, 2000.

[183] Maciej Gutowski, John E. Jaffe, Chun-Li Liu, Matt Stoker, Rama I. Hegde, Raghaw S. Rai, and Philip J. Tobin. Thermodynamic stability of high-k dielectric metal oxides ZrO_2 and HfO_2 in contact with Si and SiO_2. *Applied Physics Letters*, 80(11):1897, 2002.

[184] Robertson, J. High dielectric constant oxides. *The European Physical Journal Applied Physics*, 28(3):265, 2004.

[185] Davide Ceresoli and David Vanderbilt. Structural and dielectric properties of amorphous ZrO_2 and HfO_2,. *Physical Review B*, 74: 125108, 2006.

[186] Akira Toriumi, Yasuhiro Nakajima, and Koji Kita. Opportunity for phase-controlled higher-k HfO_2. *ECS Transactions*, 41(7):125, 2011.

[187] Yue Kuo, Jiang Lu, Jiong Yan, Tao Yuan, Hyun Chul Kim, Jeff Peterson, Mark Gardner, S. Chatterjee, and W. Luo. Sub 2 nm thick zirconium doped hafnium oxide high-k gate dielectrics. *ECS Transactions*, 1(5):447, 2006.

[188] D. H. Triyoso, R. I. Hegde, J. K. Schaeffer, D. Roan, P. J. Tobin, S. B. Samavedam, B. E. White, R. Gregory, and X.-D. Wang. Impact of Zr addition on properties of atomic layer deposited HfO_2. *Applied Physics Letters*, 88(22):222901, 2006.

[189] D. H. Triyoso, R. I. Hegde, J. K. Schaeffer, R. Gregory, X.-D. Wang, M. Canonico, D. Roan, E. A. Hebert, K. Kim, J. Jiang, R. Rai, V. Kaushik, S. B. Samavedam, and N. Rochat. Characteristics of atomic-layer-deposited thin $Hf_xZr_{1-x}O_2$ gate dielectrics. *Journal of Vacuum Science and Technology B*, 25(3):845, 2007.

[190] Torben Kelwing, Sergej Mutas, Martin Trentzsch, Andreas Naumann, Bernhard Trui, Lutz Herrmann, Falk Graetsch, Christoph Klein, Lutz Wilde, Susanne Ohsiek, Martin Weisheit, Anita Peeva, Inka Richter, Hartmut Prinz, Alexander Wuerfel, Rick Carter, Rolf Stephan, Peter Kcher, and Walter Hansch. Physical and electrical properties of MOCVD and ALD deposited $HfZrO_4$ gate dielectrics for 32nm CMOS high performance logic SOI technologies. *ECS Transactions*, 33(3):3, 2010.

[191] Kandabara Tapily, Steven Consiglio, Robert D. Clark, Relja Vasić, Eric Bersch, Jean Jordan-Sweet, Ilyssa Wells, Gert J. Leusink, and Alain C. Diebold. Texturing and tetragonal phase stabilization of ALD $Hf_xZr_{1-x}O_2$ using a cyclical deposition and annealing scheme. *ECS Transactions*, 45(3):411, 2012.

[192] Relja Vasić, Steven Consiglio, Robert D. Clark, Kandabara Tapily, Shawn Sallis, Bo Chen, David Newby, Manasa Medikonda, Gangadhara Raja Muthinti, Eric Bersch, Jean Jordan-Sweet, Christian Lavoie, Gert J. Leusink, and Alain C. Diebold. Multi-technique x-ray and optical characterization of crystalline phase, texture, and electronic structure of atomic layer deposited $Hf_{1-x}Zr_xO_2$ gate dielectrics deposited by a cyclical deposition and annealing scheme. *Journal of Applied Physics*, 113(23):234101, 2013.

[193] M. N. Bhuyian, D. Misra, K. Tapily, R. D. Clark, S. Consiglio, C. S. Wajda, G. Nakamura, and G. J. Leusink. Cyclic plasma treatment during ALD $Hf_{1-x}Zr_xO_2$ deposition. *ECS Journal of Solid State Science and Technology*, 3(5):N83, 2014.

[194] M. L. Green, M.-Y. Ho, B. Busch, G. D. Wilk, T. Sorsch, T. Conard, B. Brijs, W. Vandervorst, P. I. Räisänen, D. Muller, M. Bude, and J. Grazul. Nucleation and growth of atomic layer deposited HfO_2 gate dielectric layers on chemical oxide (SiOH) and thermal oxide (SiO_2 or SiON) underlayers. *Journal of Applied Physics*, 92(12): 7168, 2002.

[195] Johannes Müller, Patrick Polakowski, Stefan Müller, and Thomas Mikolajick. Ferroelectric hafnium oxide based materials and devices: Assessment of current status and future prospects. *ECS Transactions*, 64(8):159, 2014.

[196] Chi-Chou Lin and Yue Kuo. Memory functions of nanocrystalline cadmium selenide embedded ZrHfO high-k dielectric stack. *Journal of Applied Physics*, 115(8):084113, 2014.

[197] Chi-Chou Lin, Yue Kuo, and Shumao Zhang. Nonvolatile memory devices with AlO_x embedded Zr-doped HfO_2 high-k gate dielectric

stack. *Journal of Vacuum Science and Technology B*, 32(3):03116, 2014.

[198] Dominik Fischer and Alfred Kersch. Stabilization of the high-k tetragonal phase in HfO_2: The influence of dopants and temperature from ab initio simulations. *Journal of Applied Physics*, 104(8): 084104, 2008.

[199] S. Govindarajan, T. S. Böscke, P. Sivasubramani, P. D. Kirsch, B. H. Lee, H.-H. Tseng, R. Jammy, U. Schröder, S. Ramanathan, and B. E. Gnade. Higher permittivity rare earth doped HfO_2 for sub-45-nm metal-insulator-semiconductor devices. *Applied Physics Letters*, 91(6):062906, 2007.

[200] Hiroya Ikeda, Satoru Goto, Kazutaka Honda, Mitsuo Sakashita, Akira Sakai, Shigeaki Zaima, and Yukio Yasuda. Structural and electrical characteristics of HfO_2 films fabricated by pulsed laser deposition. *Japanese Journal of Applied Physics*, 41(4S):2476, 2002.

[201] Hei Wong, K. L. Ng, Nian Zhan, M. C. Poon, and C. W. Kok. Interface bonding structure of hafnium oxide prepared by direct sputtering of hafnium in oxygen. *Journal of Vacuum Science and Technology B*, 22(3):1094, 2004.

[202] Ralf Nyholm, Anders Berndtsson, and Nils Mårtensson. Core level binding energies for the elements Hf to Bi. *Journal of Physics C: Solid State Physics*, 13:L1091, 1980.

[203] Hei Wong. Material and interface instabilities of hafnium gate oxide. *7th International Conference on Solid-State and Integrated Circuits Technology, 2004.*, 1:378, 2004.

[204] M.-H. Cho, Y. S. Roh, C. N. Whang, K. Jeong, S. W. Nahm, D.-H. Ko, J. H. Lee, N. I. Lee, and K. Fujihara. Thermal stability

and structural characteristics of HfO_2 films on Si (100) grown by atomic-layer deposition. *Applied Physics Letters*, 81(3):472, 2002.

[205] Jihoon Choi, Seokhoon Kim, Jinwoo Kim, Hyunseok Kang, Hyeongtag Jeon, and Choelhwyi Bae. Characteristics of remote plasma atomic layer-deposited HfO_2 films on O_2 and N_2 plasma-pretreated Si substrates. *Journal of Vacuum Science and Technology A*, 24(3): 678, 2006.

[206] G. D. Wilk, R. M. Wallace, and J. M. Anthony. Hafnium and zirconium silicates for advanced gate dielectrics. *Journal of Applied Physics*, 87(1):484, 2000.

[207] Paul G. Gassman and Charles H. Winter. Understanding electronic effects in organometallic complexes. Influence of methyl substitution on hafnocene dihalides. *Organometallics*, 10(5):1592, 1991.

[208] T. Yamauchi, H. Kitamura, N. Wakai, S. Zaima, Y. Koide, and Y. Yasuda. Photoelectron spectroscopic studies on interfacial reactions in Zr/2x1(100)Si and Zr/SiO_2/(100)Si systems. *Journal of Vacuum Science and Technology A*, 11(5):2619, 1993.

[209] S. Ardizzone, M.G. Cattania, and P. Lugo. Interfacial electrostatic behaviour of oxides: correlations with structural and surface parameters of the phase. *Electrochimica Acta*, 39(1112):1509, 1994.

[210] Eduard A. Cartier. The role of oxygen in the development of Hf-base high-k/metal gate stacks for CMOS technologies. *ECS Transactions*, 33(3):83, 2010.

[211] Alexander V. Naumkin, Anna Kraut-Vass, Stephen W. Gaarenstroom, and Cedric J. Powell. NIST X-ray photoelectron spectroscopy database. *NIST Standard Reference Database*, 20(4.1), 2012.

[212] J.P. Lehan, Y. Mao, B.G. Bovard, and H.A. Macleod. Optical and microstructural properties of hafnium dioxide thin films. *Thin Solid Films*, 203(2):227, 1991.

[213] Anand Deshpande, Ronald Inman, Gregory Jursich, and Christos G. Takoudis. Annealing behavior of atomic layer deposited hafnium oxide on silicon: Changes at the interface. *Journal of Applied Physics*, 99(9):094102, 2006.

[214] A Tabata, S Fujii, Y Suzuoki, T Mizutani, and M Ieda. X-ray photoelectron spectroscopy (XPS) of hydrogenated amorphous silicon carbide (a-Si_xC_{1-x} :H) prepared by the plasma CVD method. *Journal of Physics D: Applied Physics*, 23(3):316, 1990.

[215] Hei Wong, K. L. Ng, Nian Zhan, M. C. Poon, and C. W. Kok. Characterization of high-k dielectric materials on silicon using angle resolved XPS. *Thermo Scientific application note*, 31021:1, 2004.

[216] F. De Smedt, C. Vinckier, I. Cornelissen, S. De Gendt, and M. Heyns. A detailed study on the growth of thin oxide layers on silicon using ozonated solutions. *Journal of The Electrochemical Society*, 147(3):1124, 2000.

[217] Robert D. Clark. Emerging applications for high-k materials in VLSI technology. *Materials*, 7(4):2913, 2014.