An Improved Design of Combinational Digital Circuits with Multiplexers using Genetic Algorithm

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***Abstract*—This paper presents a new approach to the design of combinational digital circuits with multiplexers using Evolutionary techniques. Genetic Algorithm (GA) is used as the optimization tool. Several circuits are synthesized with this method and compared with two design techniques such as standard implementation of logic functions using multiplexers and implementation using Shannon's decomposition technique using GA. With the proposed method complexity of the circuit and the associated delay can be reduced significantly.**

***Keywords*— Optimization; Logic synthesis; Binary multiplexers Shannon's decomposition technique; Genetic Algorithm**

I. INTRODUCTION

Genetic algorithm (GA) is a powerful tool which can be used for many of the optimization problems. Conventional GA takes in a linear set of chromosomes on which one dimensional crossover and mutation operators are applied to get an optimal solution [1]. The speed of convergence and the quality of the solutions are influenced by these operators.

Majority of electronic systems with any level of complexity were designed by specialized designers having a complete knowledge of operation of the system and designing rules. Such design methods are obviously limited by the experience and knowledge of the designer [2]. In evolutionary design, knowledge and experience of the designer are replaced by evolution process which has comparatively less constraints. Designers are not only limited by technology but also by their own habits, imagination and creative thinking [3]. By applying evolutionary methods to the design of digital circuits, the above mentioned constraints do not come into picture. The main goal of evolutionary algorithm is to evolve a functional circuit with the least possible complexity.

Gate level design of logic functions using GA has been done using a set of gates (AND, OR, NOT, XOR) [4].Here gates have been substituted by binary multiplexers. Any Boolean function can be realized using 1- control line multiplexers.

In VLSI design, importance must be given to reduce the whole manufacturing cost. Here the elemental binary multiplexer is replicated for the synthesis of logic circuits, thereby minimizing the cost. Only 1's and 0's are fed to the multiplexers and the variables are used as control signals of the multiplexers [5]. A logic function with n variables can be realized by using 2^n-1, 1 control line multiplexers. Any implementation using less than 2^n-1units can be considered as an improvement in cost and speed.

Desired logic function specified by the truth table has been realized by 1-control line multiplexers using genetic Programming in [5-6]. Here a procedure based on the residue of a Boolean Function combined with Shannon's decomposition technique produced a circuit that used only binary multiplexers. In [5], circuits with only one output have been evolved with binary multiplexers using Genetic Programming approach. A considerable reduction in the number of multiplexers has been obtained with this technique, thereby reducing the cost and delay.

The problem is to evolve combinational digital circuits with least possible number of universal logic module, 2-1 multiplexer. Here, GA is used as the optimization tool. In [5] Genetic programming has been used for the evolution of Boolean functions with binary multiplexers. In this paper, evolution of digital circuits using Shannon's decomposition technique and GA is presented. Circuits have been evolved with lesser number of multiplexers than standard implementation. A modification has been made on this method by which the circuit complexity was reduced further.

Fitness for each individual in the population is calculated based on the proximity to the target truth table. The best fit circuits are selected by any suitable standard selection procedure and cross over and mutations are done. A fit circuit which exactly matches with the user defined truth table may be evolved in a few runs of the GA.

The paper is organized as follows: Section II describes the representation of chromosomes for the circuit, section III deals with implementation of logic circuit using Shannon's decomposition technique and the modified method, section IV gives the results and comparison with the existing methods.

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II. REPRESENTATION OF CHROMOSOMES FOR THE CIRCUIT

The chromosomes for GA is coded in a 1 dimensional pattern where each bit or a group of bit combination represents a particular input or control in the circuit.[7-9].Any combinational digital circuit can be realized using a cascade of multiplexers [10]. For an n variable function there will be n levels. Fig.1 represents the chromosome used to represent a multiplexer in the first level of implementation (starting from bottom) of a three variable circuit. Bit X1 is used to check the presence of the multiplexer, and bit X2 represents the different input conditions to the multiplexer and X3 and X4 combinations check the control input to the multiplexer. Here if X2='0', then the input to the multiplexer is considered as '1,0' otherwise it is '0,1'. Also if the X3X4="00" then the control input is taken as 'a',"01" is taken as 'b' and so on.

X1	X2	X3	X4

Figure 1.Chromosomal representation for a multiplexer in the first level

Fig.2 shows the chromosomal representation of a multiplexer in the second level.

X1	X2	X3	X4	X5	X6	X7

Figure 2.Chromosomal representation of the multiplexer in the second level

Here bit X1 checks the presence of multiplexer in the second level. Bits X2-X5 combinations represent different input conditions into the multiplexer. For example, if "X2X3X4X5"="0000", then input is considered as '0,1' and if "X2X3X4X5"="1111",then input is 'output of multiplexer1,0' and so on. Combinations of bits X6X7 determines the different control input to the multiplexer for example, if "X6X7"="00", then control input is 'a'. The same 7 bit chromosomal representation is followed for the final/third level of the circuit.

III. IMPLEMENTATION USING SHANNON'S DECOMPOSITION TECHNIQUE

A multiplexer is a combinational circuit whose output is obtained from the 2^n input lines according to the value in the select lines. Multiplexers are of "active low" or "active high" denoted as Class A and Class B multiplexers. For a class A multiplexer, when the control input is high, input labeled as '1' is directed to the output and the input labeled as '0' is directed to the output when the control is low [5]. Here we use the class A multiplexer representation of the circuit [5,11]. For a function $f(x_1,x_2,x_3,\ldots\ldots x_n)$, its residue with respect to a variable x_j is the value of the function for a specific value of x_j .Its Shannon's expansion is [8-9].

$$f = \overline{x_j} f|_{\overline{xj}} + x_j f|_{xj} \qquad (1)$$

In this reduction technique, same variable is fed as control input for a particular level, starting from top to bottom levels. Realization of the full adder function F(a,b,c)= ∑(1,2,4,7) using Shannon's decomposition technique is shown in Fig 3.

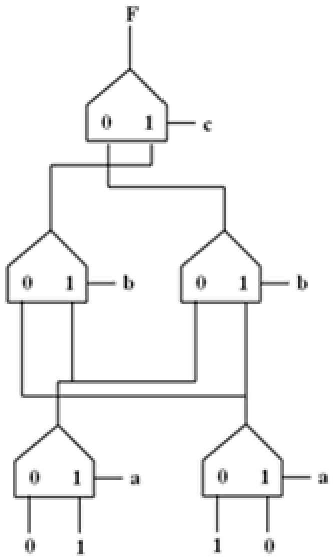

Figure 3.Full adder circuit using Shannon's technique

A. Modified method

Using Shannon's decomposition technique, same variable is used as the control signal for all the multiplexers in a level. Here a modification has been made such that the control signal is also generated at random using GA. The same variable need not be applied as control signals in a level. The flexibility for the circuit is achieved by coding the chromosomes such that for a multiplexer in a particular level receives input from all possible combinations of previous level outputs and control input is also made flexible for all possible combinations. Circuits have been evolved for 2, 3 and 4 variable functions using this technique with reduced number of units.

Delay for all the evolved circuits have been obtained by simulation using QUARTUS II software using VHDL codes. Delay for the circuits generated using modified method have been compared with the circuits obtained by standard implementation, and by Shannon's decomposition method using GA.

IV. RESULTS

The parameters selected for GA were population size=100, number of generations=150, crossover rate=0.7, mutation rate=0.3, Roulette wheel selection technique has been used for selecting the individuals for crossover. The simulation was done in MATLAB R2011a and QUARTUS II design software version 9 is used for the delay analysis of the evolved circuit using the proposed method. The program was run in Intel core2 duo processor (2.00 GHz).

Example 1. F(a,b,c)=∑(0,4,6,7)

The optimized circuit evolved from Shannon's decomposition method using GA is shown in Fig 4 and its convergence graph is shown in Fig 5.

Table I. Comparison between different implementations

Function	Standard Implementation		Shannon's implementation & GA			Using GA & flexibility in giving control signal (modified method)		
	No: of Multiplexers	Delay(ns)	No: of Multiplexers	% Saving	Delay(ns)	No: of Multiplexers	% Saving	Delay(ns)
F(a,b)=∑(1,2,3)	3	7.103	3	0	7.103	3	0	7.103
F(a,b,c)=∑(0,4,6,7)	7	8.495	4	43	8.035	3	57	7.995
F(a,b,c,d)= ∑(0,4,6,7,8,12,14,15)	15	8.613	4	73	8.085	3	80	7.337

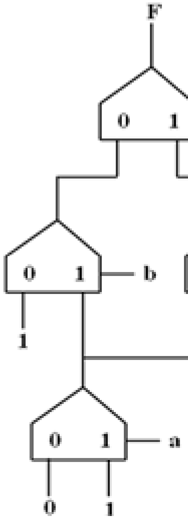

Figure 4.Evolved circuit

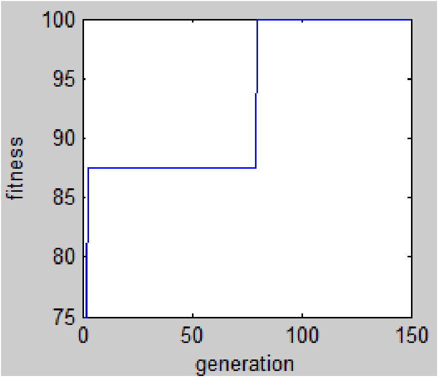

Figure 5. Convergence curve

Using standard implementation, for a three variable function, 7, (2^3-1) multiplexers are needed. Here the circuit was converged with 4 multiplexers, a 43% saving in the modules for implementation.

The Fig. 6 shows the optimized circuit evolved for the same three variable function F(a,b,c)=∑(0,4,6,7) with the modified method using GA.

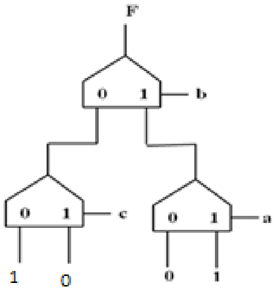

Figure 6. Evolved circuit

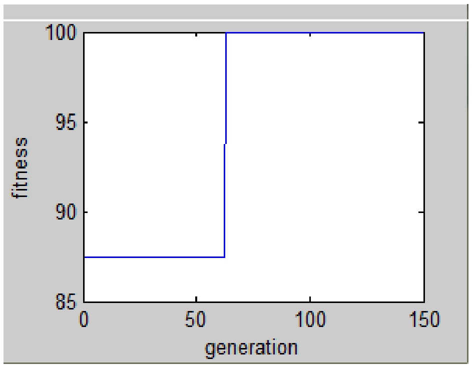

Figure 7 .Convergence curve

The function was realized in just three multiplexers. Thus with the proposed design, there is a saving of 57% compared to standard implementation and 25% compared to Shannon's technique. Fitness was achieved in 62 generations and the time for convergence of the circuit was found to be 23.065 seconds.

Example 2. F(a,b,c,d)= Σ(0,4,6,7,8,12,14,15)

The optimized circuit evolved from Shannon's decomposition method using GA is illustrated in Fig 8

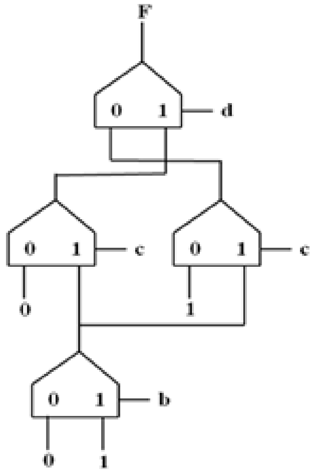

Figure 8.Evolved circuit

The evolved circuit needed only 4 multiplexers to implement the required function compared to the standard implementation, which requires 15 multiplexers. The circuit was 100% fit at the 110th generation and the time for convergence was found to be 162.448 seconds. Fig 9 shows the convergence curve for the evolved circuit.

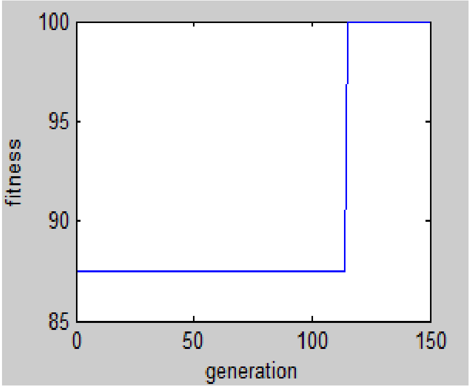

Figure 9.Convergence curve

The Fig 10 shows the circuit evolved for the same four variable function F(a,b,c,d)= Σ(0,4,6,7,8,12,14,15) with modified method using GA and Fig 11 shows its convergence curve. With the modified method, the same circuit was implemented using just 3 multiplexers, obtaining 80% saving in the number of multiplexers compared to the standard implementation and 25% compared to Shannon's decomposition technique using GA.Fig.11 shows its convergence graph.100% fitness was obtained in less than 20 generations.

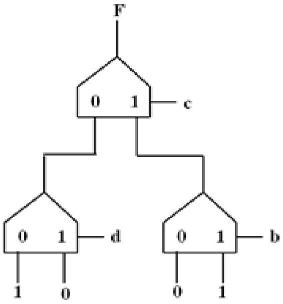

Figure 10.Evolved circuit

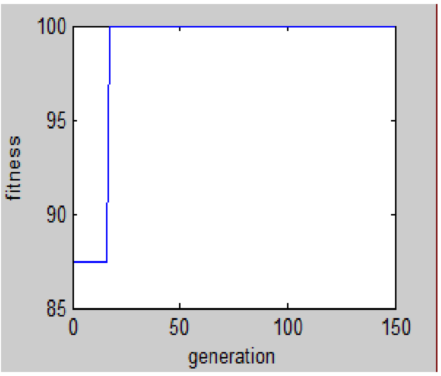

Figure 11.Convergence curve

B. *Comparison of realisation of Boolean functions using multiplexer by various methods*

Comparison was made between different types of implementations of Boolean functions. The Shannon's decomposition technique and the modified method using GA needed lesser number of multiplexers than the standard implementation techniques.. The proposed method was found to be more efficient than the Shannon implementation technique in terms of multiplexer count and area requirement. Delay analysis was also done for the evolved circuits using Quartus II design software for the Stratix II EP2S15F672C3 device. The program was tested for more than 100 functions. The delay was considerably reduced with the proposed design for two, three, and four variable functions. Also as the number of multiplexers is reduced, the cost of realization reduced.

Table 1 shows the comparison between the various implementation techniques in terms of % saving in number of multiplexers and the delay involved in all the three case for two, three and four variable functions.

V. CONCLUSION

A new method for implementation of combinational logic circuit is proposed with 2-1 multiplexers using GA. Its performance was compared with the existing standard implementation technique and Shannon's decomposition technique. It is found that the number of units required is reduced considerably thereby reducing the cost .The delay incurred by various schemes have been simulated and is found to reduce considerably with the proposed technique.

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