GA-based Optimization of a Fourth-order Sigma-delta Modulator for WLAN

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***Abstract*- Over-sampling sigma-delta analogue-to-digital converters (ADCs) are one of the key building blocks of state of the art wireless transceivers. In the sigma-delta modulator design the scaling coefficients determine the overall signal-to-noise ratio. Therefore, selecting the optimum value of the coefficient is very important. To this end, this paper addresses the design of a fourth-order multi-bit sigma-delta modulator for Wireless Local Area Networks (WLAN) receiver with feed-forward path and the optimum coefficients are selected using genetic algorithm (GA)-based search method. In particular, the proposed converter makes use of low-distortion swing suppression SDM architecture which is highly suitable for low oversampling ratios to attain high linearity over a wide bandwidth. The focus of this paper is the identification of the best coefficients suitable for the proposed topology as well as the optimization of a set of system parameters in order to achieve the desired signal-to-noise ratio. GA-based search engine is a stochastic search method which can find the optimum solution within the given constraints.**

I. INTRODUCTION

Genetic algorithms (GAs) have been successfully applied to a wide range of optimization problems including design, scheduling, routing, and signal processing. In Sigma delta (∑Δ) modulator design, GA [1,2] can be effectively used to optimize the scaling coefficients in order to achieve the desired signal-to-noise ratio. ∑Δ modulators were traditionally used for audio applications where the oversampling ratio is high and a high resolution can be achieved with a realizable clock frequency. Recently ∑Δ modulators are exploited for wideband applications like WLAN, thus preventing the excess increase in the OSR and resorting to higher order modulators. Higher order modulators with low OSR requires the optimization of system parameters in order to achieve the required dynamic range

The requirements that the ADC has to fulfill are set by both the standard characteristics and the receiver architecture. This work focuses on a zero-IF WLAN 802.11b receiver, presented in Fig. 1 [3]. The zero-IF architecture shows excellent multi-standard capabilities, making our system easy to upgrade to multi-mode operation. The radio specifications of WLAN 802.11b [4] are summarized in Table I. This together with the link budget, sets the minimum requirements for the ADC. Our architecture choice leads to a minimum dynamic range of 50dB for the ADC for a 10 MHz bandwidth.

This paper presents the design and optimization of a highly linear sigma-delta modulator for wireless applications. The proposed architecture employs a multi-bit 2-2 modified cascaded sigma-delta modulator suitable for WLAN receivers. The paper is organized as follows: Section I is the introduction. Section II presents the modified cascaded sigma-delta modulator architecture and discusses the design issues in arriving at the topology. Section III describes the genetic optimization algorithm used to find the optimal values for the proposed modulator. The simulation results are presented in Section IV. Finally, Section V concludes the paper.

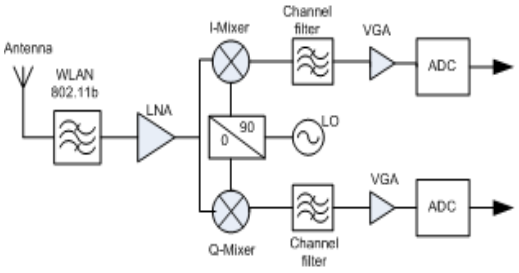

Figure 1. Zero-IF Receiver Architecture

TABLE I. RADIO SPECIFICATIONS FOR WLAN 802.11b

Frequency Band	2.412-2.484 GHz
Channel Spacing	25 MHz
Channel Bandwidth	20 MHz
Sensitivity	-76 dBm
Maximum Input Signal	-10 dBm
Input Noise	-104 dBm
Required SNR	14 dB

II. MODULATOR ARCHITECTURE

This Section explores tradeoffs among the wide variety of ∑-Δ modulator architectures that can be used to implement a ∑-Δ A/D converter suitable for low power and high integration WLAN standard receiver. The search for an optimal wideband ∑-Δ topology has been performed by varying the order L, the oversampling ratio M and the number of bits B in the quantizer.

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The target specifications for the ∑-Δ modulator were defined to be 50dB DR over 10MHz bandwidth at minimum power dissipation. For signals of very wide bandwidth, such as in WLAN receiver, oversampling ratio cannot be very high (4 or 5) because the achievable clock frequency is constrained by the process technology. Therefore the only solution is by increasing the order L and quantizer bits B in order to achieve the required resolution. The dynamic range DR [5] of a ∑Δ modulator is given by

$$DR = \frac{3}{2}\frac{2L+1}{\pi^{2L}} M^{2L+1}.(2^B - 1)^2 \qquad (1)$$

For low-data rate applications, such as GSM receiver, where bandwidth is relatively smaller, over-sampling ratio (M) can be made higher, which will increase the circuit complexity and power consumption. For higher order or multi-bit modulators the complexity becomes higher, and for higher sampling frequency the requirements of analog building blocks becomes more demanding. Alternatively, the increased quantizer resolution enables us to use a lower over-sampling ratio or a lower noise-shaping order for a given dynamic range bandwidth target. Unfortunately, the higher quantizer resolution will lead to a large area of internal flash ADC and switched-capacitor DAC and increased power consumption. An OSR of 8 has been chosen as a compromise between the technologically feasibility sampling frequency and bandwidth requirements. Once the OSR was established, a 2-2 modified cascaded modulator architecture has been adopted which can provide comparable dynamic ranges. The next key issue in the design of a low-power ∑-Δ modulator is the quantizer resolution. Thus B plays an important role in the power-performance design of the modified cascaded sigma-delta modulator. A multibit quantizer with multi-bit feedback digital-to-analog converter (DAC) has to be used to attain the WLAN specifications. The main drawback of multi-bit ∑-Δ modulator is the high linearity that is required of the feedback DAC. Thus the overall sigma-delta converter linearity and resolution are limited by the precision of the multi-bit DAC. Reducing the quantizer's resolution to 1 bit may eliminate the dependence on feedback DAC linearity. One way to achieve further reduction of quantization noise is to use a multi-bit quantizer only in the final stage to eliminate the necessity of DEM techniques to improve the linearity of multi-bit DAC. Therefore we have adopted a single bit quantizer in the first stage and 4-bit quantizer in the second stage.

Figure 2 shows the block diagram of the proposed modified cascaded sigma-delta modulator. The 4th order modified cascaded ∑-Δ modulator architecture employs two key design approaches. One is the 2nd order sigma-delta modulator with feedforward signal path [6, 7], which has a high linearity even at low OSR. The other is the structural approach, which combines the merits of modified cascaded topology and multibit quantization in the last stage to make all quantization noise sources negligible at low oversampling (OSR). The scaling coefficients have been used to achieve the peak signal-to-noise and distortion ratio (SNDR), to control the input of the second stage and to utilize the full dynamic range of the next stage. By combining these techniques the performance improvements of the ∑-Δ modulator are significant.

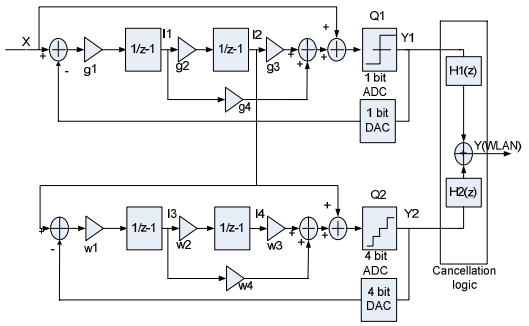

Figure 2. Modified cascaded sigma-delta modulator for WLAN

The output of the first stage of the modulator is given by

$$Y_1(z) = X(z) + \frac{(1-z^{-1})^2}{1+(g_1g_4-2)z^{-1}+(1+g_1g_2g_3-g_1g_4)z^{-2}} Q_1(z) \qquad (2)$$

The output of the integrators, I_1 and I_2 are given by

$$I_1(z) = \frac{g_1 z^{-1}(1-z^{-1})}{1+(g_1g_4-2)z^{-1}+(1+g_1g_2g_3-g_1g_4)z^{-2}} Q_1(z) \qquad (3)$$

$$I_2(z) = \frac{g_1g_2z^{-2}}{1+(g_1g_4-2)z^{-1}+(1+g_1g_2g_3-g_1g_4)z^{-2}} Q_1(z) \qquad (4)$$

From equations (3) and (4), it is observed that the integrators process only the quantization noise. Therefore, the integrator output swings of the proposed architecture are reduced compared with the traditional one and then the operational amplifier requirements are greatly relaxed. Since the output of the second integrator (I_2) contains only quantization noise, this output has been used as input for the second stage. Therefore, the output of the second stage is given by

$$Y_2(z) = \frac{g_1g_2z^{-2}}{1+(g_1g_4-2)z^{-1}+(1+g_1g_2g_3-g_1g_4)z^{-2}} Q_1(z) + \frac{(1-z^{-1})^2}{1+(w_1w_4-2)z^{-1}+(1+w_1w_2w_3-w_1w_4)z^{-2}} Q_2(z) \qquad (5)$$

where $Q_1(z)$, $Q_2(z)$ are the quantization errors of the first and second stages respectively and $g_1, g_2, g_3, g_4, w_1, w_2, w_3, w_4$ are

the analog coefficients. The final modulator output after the cancellation logic is given by

$$Y(z)=z^{-2}X(z)+\frac{1}{g_1g_2}\frac{(1-z^{-1})^4}{1+(w_1w_4-2)z^{-1}+(1+w_1w_2w_3-w_1w_4)z^{-2}}Q_2(z) \quad (6)$$

where the digital coefficient is $g_5=1/g_1g_2$ and the digital transfer functions are $H_1(z)=z^{-2}$ and $H_2(z)=g_5(1-z^{-1})^2$. The coefficients selected randomly for generating the maximum peak signal to noise and distortion ratio (SNDR) were: $g_1=g_2=w_1=w_2=0.5$, $g_3=g_4=w_3=w_4=4$.

III. GA-BASED COEFFICIENT OPTIMIZATION

A. GENETIC ALGORITHM

GAs are search and optimization algorithms based on the mechanics of natural selection and natural genetics [8]. They make use of structured but randomized information exchange and concept of the survival of the fittest. The algorithm starts with an initial population which consists of a collection of chromosomes i.e. possible solutions coded in the form of strings. The chromosome which produces the minimum error function value represents the best solution. The chromosomes which represent the better solutions are selected using roulette wheel selection technique. Genetic operators like crossover, mutation, elitism etc are applied over the selected chromosomes. As a result a new set of chromosome is produced. This process is repeated until a fit solution appears. In essence, a population of chromosomes is always available to get the desired result. Occasionally a new part is added to a chromosome to make it more robust. Genetic algorithms exploit past to extrapolate new search points to provide improved performance.

A robust method like GA works well across a wide range of problems and also is more efficient. The traditional derivatives based approach, enumerative schemes and simple random walks are not that good for all classes of problems. On the other hand, heuristics approaches, such as genetic algorithms (GAs), differ from the traditional ones in that there exists a high probability that the global optimal solution will be reached. Fig. 3 shows the flowchart of the binary GA.

B. GA IN ∑Δ ADC DESIGN

In the design of ∑Δ ADCs, we need to optimize a large set of parameters including the overall structures and the performance of the building blocks to achieve the required signal-to-noise ratio. Therefore, behavioral simulations were carried out using a set of Simulink models [9,10] in MATLAB Simulink environment in order to verify the performance for a WLAN system, to investigate the circuit non-idealities effect, to optimize the system parameters and to establish the specifications for the analog cells. The most important parameter to be optimized in a sigma-delta modulator are the gain coefficients in order to achieve the desired signal-to-noise ratio. GA is one of the best optimization technique which finds a global optimum solution without taking much of the computational power.

The steps involved in the process of optimization using GA is shown in Fig. 4 There are two general schemes for coding the solutions: (i) binary coding (ii) decimal coding. In our work, binary coding has been used where '0's and '1's are used to form a chromosome of length 'l' depending on the precision needed. After defining the chromosome, an initial population is obtained by randomly producing N number of chromosomal solutions called the first generation.

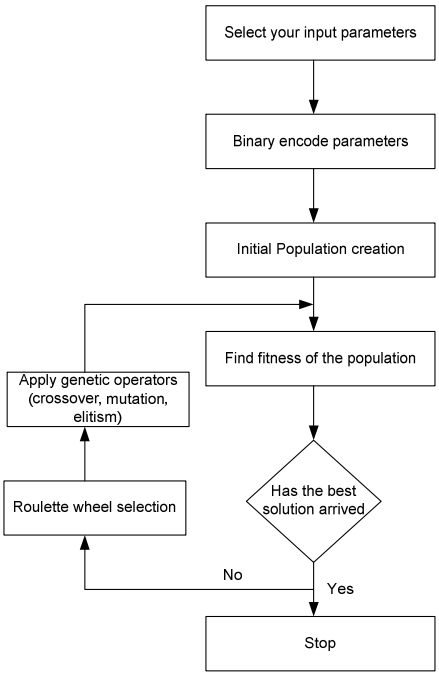

Figure 4. Flow chart of binary GA.

The next step, called pairing, consists of selecting the chromosomes that will pair together to reproduce the offsprings. This is done by using roulette wheel selection technique. These pairs will be used for reproduction. Reproduction ensures that chromosomes with higher fitness will have a higher probability of reproduction than chromosomes with lower fitness. Reproduction is the application of crossover, mutation and elitism operators over the selected chromosomes. In this work single point crossover has been used as shown in Fig. 5.

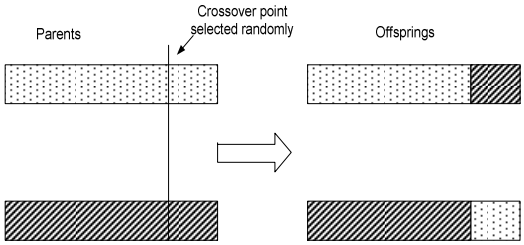

Figure 5. Single-point crossover process

Mutation rate (MR) is set to a very low value of 0.08. A high MR introduces high diversity but might cause instability. However, a very low MR makes it difficult for the GA to find a global optimal solution. In addition to crossover and mutation the best chromosome present in a particular generation is passed on to the next generation so that it will not be lost until the next best arrives. In this way the stability of the GA is improved. A fitness function or objective function has to be obtained to evaluate the performance of the chromosomes and compare their performance. In the design of sigma-delta modulator we need to optimize the coefficients for a maximum signal-to-noise ratio (SNR). Hence the fitness function is formulated as

$$fitness = \left(\frac{1}{Error}\right) \quad (7)$$

where

$$Error = DesiredSNR - ObtainedSNR \quad (8)$$

After evaluating the fitness function, fitness values will be assigned to each chromosome. If the best fit chromosome has arrived, the GA can be stopped and the coefficient values can be decoded. Else the chromosomes are sent back to the selection module and the whole procedure is repeated again until the best arrives or the maximum number of generation set is reached.

It is to be noted that the number of chromosomes should not be very small or very high. Too small a population size will lead to very fast convergence of GA and thus one may not obtain an optimum solution. Too high a population size will take a lot of computation time for the GA to converge which needs sufficient computing power.

IV. SIMULATION RESULTS

Simulations were performed for both using ideal and real integrator blocks. Real integrator block takes into account the main circuit non-idealities like opamp finite dc gain, slew rate, gain-bandwidth product and amplifier saturation voltage. In this work a population of 20 binary chromosomes for a precision of 3 decimal places has been run for 20 generations to get the optimum value of the coefficients. Crossover rate and mutation rate were chosen as 0.7 and 0.8/l respectively where 'l' is the length of the chromosome. At the end of the 20th generation, the optimum values of the coefficients were obtained as g1=0.325, g2=0.7646, g3=4.023, g4=6.1538. Figure 6 shows the convergence plot for the first coefficient g1 which is the most critical one. After 20 generations, the optimum value for g1 was found to be 0.325 for which the peak SNDR was 64 dB. Table II shows there is an improvement of almost 6dB after using GA-based optimization technique.

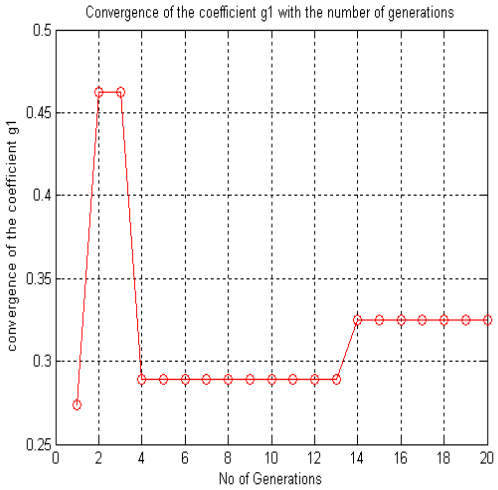

Figure 6. Convergence of coefficient g1 with number of generations

Table II. Comparison of gain coefficients with and without GA

	Coefficients	Peak SNR	Peak SNDR
Without GA	g1=0.5, g2=0.5 g3=4, g4=4	64 dB	59 dB
With GA	g1=0.325, g2=0.7646, g3=4.023, g4=6.1538	69 dB	64 dB

Simulations were performed using an OSR of 8 for a bandwidth of 10 MHz. Fig 7 shows the modulator output spectrum for a 0.5V/2.5MHz input signal. As shown in Fig 7, the peak SNDR achieved was found to be 64 dB with a finite dc gain of 60 dB, slew rate of at least 300V/us and a gain-bandwith product of 350 MHz.

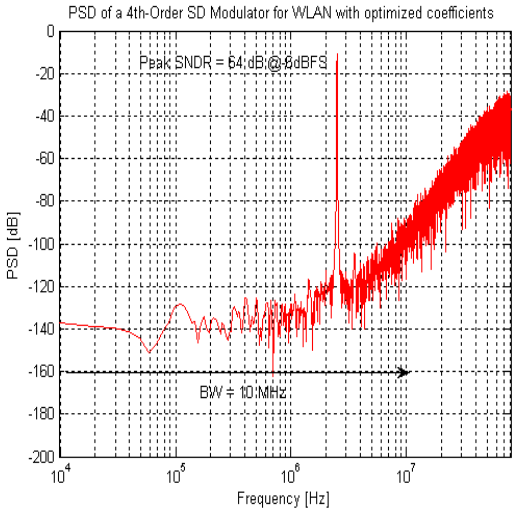

Figure 7. Modulator Output Spectrum for WLAN

Fig 8 presents the simulated SNR and SNDR versus input signal amplitude for WLAN. Simulation results show a peak SNDR of 59 dB@-6dBFS without using GA and 64 dB@-4dBFS after optimizing the coefficients using GA in the WLAN mode.

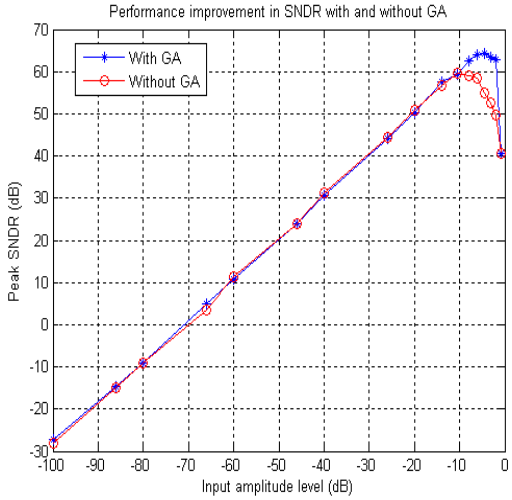

Figure 8. SNR and SNDR versus input signal amplitude

The performance summary of the modulator is shown in Table III. The overall performance demonstrates the efficiency of the proposed architecture for WLAN operation.

TABLE III. PERFORMANCE SUMMARY OF THE MODULATOR

Process Supply voltage	TSMC 0.18um CMOS (@1.8V)
Architecture	(2-2) modified cascaded ∑Δ modulator
Sampling frequency	160 MHz
Signal Bandwidth	10 MHz
OSR	8
DR	71 dB
Peak SNR	69 dB@-4dBFS
Peak SNDR	64dB@-6dBFS
Estimated Power	42 mW

V. CONCLUSIONS

Genetic algorithm has been successfully used to improve the performance of a sigma-delta ADC which is proposed for WLAN applications. It employs a 2-2 modified cascaded architecture with a single bit in the first stage and 4 bit in the second stage. The low-distortion topology has reduced sensitivity to OTAs nonlinearity effects and simplifies the implementation of cascaded architecture. The coefficients were optimized using GA to extend the dynamic range. It achieves a peak SNDR of 59/64 dB over 10MHz signal bandwidth with/without using GA. Simulation results show there is almost a 6 dB improvement which corresponds to 1-bit resolution after the GA-based optimization technique.

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