J Sign Process Syst (2011) 62:117–130
DOI 10.1007/s11265-008-0326-z

A Multi-Mode Sigma-Delta ADC for GSM/WCDMA/ WLAN Applications

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Received: 28 September 2008 / Revised: 23 November 2008 / Accepted: 25 November 2008 / Published online: 6 January 2009

Abstract The demand for new telecommunication services requiring higher capacities, data rates and different operating modes have motivated the development of new generation multi-standard wireless transceivers. In multi-standard design, sigma-delta based ADC is one of the most popular choices. To this end, in this paper we present cascaded 2-2-2 reconfigurable sigma-delta modulator that can handle GSM, WCDMA and WLAN standards. The modulator makes use of a low-distortion swing suppression topology which is highly suitable for wide band applications. In GSM mode, only the first stage (2nd order $\sum$-Δ ADC) is used to achieve a peak SNDR of 88dB with over-sampling ratio of 160 for a bandwidth of 200KHz and for WCDMA mode a 2-2 cascaded structure (4th order) is turned on with 1-bit in the first stage and 2-bit in the second stage to achieve 74 dB peak SNDR with over-sampling ratio of 16 for a bandwidth of 2MHz. Finally, a 2-2-2 cascaded MASH architecture with 4-bit in the last stage is proposed to achieve a peak SNDR of 58dB for WLAN for a bandwidth of 20MHz. The novelty lies in the fact that unused blocks of second and third stages can be made inactive to achieve low power consumption. The modulator is designed in TSMC 0.18um CMOS technology and operates at 1.8 supply voltage.

Keywords Triple mode · Feed-forward path · Multi-standard receiver · Sigma-delta modulator

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1 Introduction

Mobile Telecommunication has experienced tremendous growth since the progressive development of wireless communication systems. Several mobile telecommunications standards are used worldwide in the transition from the second generation (2G) digital system into the third generation (3G) system. The most popular standard for 3G systems is WCDMA, supported by the third generation partnership project (3GPP). 4G mobile systems will be further integrated with Wireless Local Area Networks (WLAN). A user will employ the WLAN mode whenever the mobile terminal is within range of a WLAN access point [1]. WLAN-enabled cell phones are expected to contain multimode cellular capability. A suggestion is to encompass GSM and WCDMA operation, in addition to WLAN [2].

Sigma-delta modulator is the most promising candidate to achieve high resolution over a wide variety of bandwidth requirements in multi-mode receivers. The advantage of sigma-delta ADCs in providing high resolution with low precision components lies on the use of over-sampling and noise shaping. As bandwidth requirement increases, the over-sampling ratio decreases which results in a decrease in the resolution. Designing sigma-delta modulators that can achieve high resolution and wide bandwidth remains challenging. Sigma-delta A/D converters suitable for dual-mode receivers have already been published in the literature

Table 1 Performance summary of the published multi-standard ∑-Δ ADCs.

	Dual-mode ∑-Δ ADCs				Triple-mode ∑-Δ ADCs		
	[3]	[4]	[5]	[6]	[7]	[8]	[9]
Order	3	2	2	2/(2-1)	2-1-1	2-1-1-1	2-2
No. of bits	1	2.5	6	1/2.3	1/1/1	1/1.5/3	2.5/2.5
Fs (MHz)	104/184.32	26/46	23/46	39/38.4	138/245/320	51.2/100/100	23/46
BW (MHz)	0.2/3.84	0.2/2	0.2/1.92	0.1/1.92	0.271/3.84/20	0.2/5/20	0.2/1.5/1.92
DR (dB)	86/54	79/50	81/70	82/70	103/82/66	94/88/56	70/51/50
CMOS Process	0.25 um	0.13 um	0.18 um	0.13 um	0.35 um	0.18 um	0.18 um
Power (mW)	11.5/13.5	2.4/2.9	30/50	2.4/4.3	58/82/128	-	5.8/5/11

[3–6]. These solutions of switched-capacitor (SC) ∑Δ modulators that cover GSM and WCDMA standards are presented in Table 1.

A triple-mode cascaded ∑Δ architecture for GSM/UMTS/WLAN has been reported in [7] whose wide range of programmability of input frequency and dynamic range descends from modulator order programmability. Another reconfigurable ∑Δ modulator for a triple standard receiver has been introduced in [8] where a feedback path from the last stage to the third stage is done in order to further suppress the quantization noise power. Yet another triple mode sigma-delta ADC has been explored in [10] which uses low-distortion architecture and Pseudo-Data-Weighted-Averaging technique to attain high linearity over a wide bandwidth. Traditional topology is increasingly sensitive to circuit imperfections, especially at very low over-sampling ratios. In this work, we present a triple-mode low-distortion swing suppression (feed-forward) cascaded topology which uses multi-bit quantizer in the last stages in order to eliminate the necessity of DEM techniques to improve the linearity of multi-bit DAC, for use in wideband applications like WLAN.

Based on the triple-standard Zero-IF/Low-IF approach, GSM/WCDMA/WLAN triple-mode receiver architecture is proposed in Fig. 1. In this architecture, three sets of band filters and LNAs are required for GSM/WCDMA/WLAN selection. The multi-standard ADC is shared by these three standards. Table 2 summarizes the channel bandwidth and dynamic range requirements of the base-band ADC for the three standards, obtained from the Simulink™ model of the receiver.

The paper is organized as follows. Section 1 is the introduction. Section 2 focuses on selecting the appropriate architecture for the multi-standard ∑Δ modulator given the wireless receiver specifications. Section 3 explains the various ∑Δ modulator non-idealities and their analysis. Section 4 describes the circuit-level implementation which uses a switched-capacitor (SC) ∑-Δ modulator operating from 1.8V supply and implemented in TSMC 0.18um CMOS technology. Section 5 provides the simulation results. Finally, Section 6 concludes the paper.

2 Modulator Architecture

This Section explores tradeoffs among the wide variety of ∑-Δ modulator architectures that can be used to implement a ∑-Δ A/D converter suitable for low power

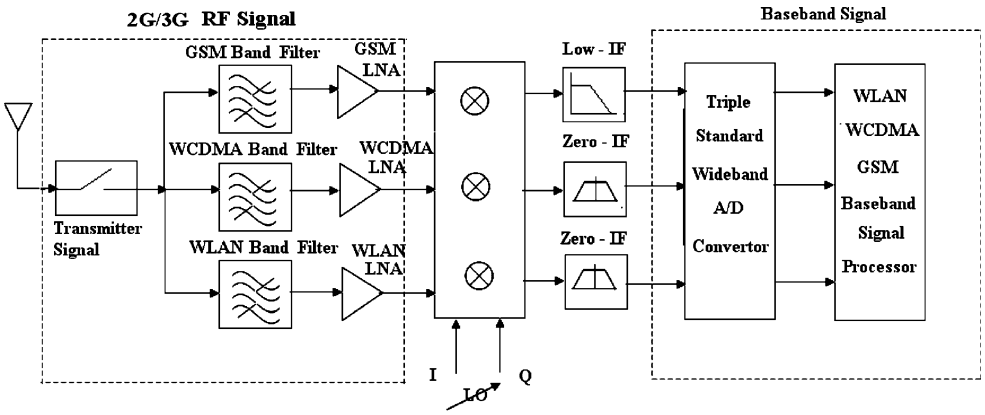


Figure 1 Triple standard wideband receiver architecture.

Table 2 ADC requirements for multi-standard receiver.

Wireless Standard	Frequency (MHz)	Channel Bandwidth	Dynamic Range
GSM	890–915(Tx) 935–960 (Rx)	200 kHz	>80 dB
WCDMA	1850–1910 (Tx)1920–1980 (Rx)	5 MHz	>60 dB
WLAN	2401–2473	20 MHz	>50 dB

and high integration triple-standard receiver. The search for an optimal wideband ∑-Δ topology has been performed by varying the order L, the over-sampling ratio (OSR) M and the number of bits B in the quantizer as shown in Table 3.

For signals of very wide bandwidth, such as in WLAN receiver, over-sampling ratio (OSR) cannot be very high (4 or 5) because the achievable clock frequency is constrained by the process technology. Therefore the only solution is by increasing the order L and quantizer bits B in order to achieve the required solution. The dynamic range of a ∑Δ modulator is given by

$$DR = \frac{3}{2}\frac{2L+1}{\pi^{2L}} M^{2L+1}.\left(2^B - 1\right)^2 \tag{1}$$

For low-data rate applications, such as GSM receiver, over-sampling ratio (M) can be made higher, due to much smaller signal bandwidth. For higher order or multi-bit modulators the complexity becomes higher, and for higher sampling frequency the requirements of analog building blocks becomes more demanding.

Taking into account the above considerations, a cascaded 2-2-2 structure with multi-bit quantizer is proposed which is shown in Fig. 2. A second order single bit ∑Δ modulator has been selected as the first stage in order to meet the specifications of GSM mode. Here, we choose a low-distortion swing suppression topology [11], which is highly suitable for wide band applications because of its relaxed requirements on the analog building blocks. The unused blocks in the second and third stages are switched off while working in the GSM mode, taking into account the design considerations like power consumption. In the WCDMA mode, the 4th order modulator (2-2 cascaded) is switched to operation by closing the switch labeled W thus making it programmable. In the WLAN mode, a sixth order modulator (2-2-2 cascaded) is switched to operation by closing the switches labeled S, in order to get more than 50 dB SNDR. The novelty lies in the fact that the input to the second and third stages can be directly taken from the output of the second integrator of the preceding stages, since the integrators are only processing the quantization noise.

The modulator output in GSM mode is the output of the first stage

$$Y_{GSM}(z) = X(z) + \left(1 - z^{-1}\right)^2 Q_1(z) \tag{2}$$

and the output of the second stage is given by

$$Y_2(z) = I_2(z) + \left(1 - z^{-1}\right)^2 Q_2(z) \tag{3}$$

where

$$I_2(z) = -g_1 g_2 z^{-2} Q_1(z) \tag{4}$$

The modulator output in W-CDMA mode is given by the output of the modified cascaded modulator.

$$Y_{CDMA}(z) = z^{-2}X(z) + g_5\left(1 - z^{-1}\right)^4 Q_2(z) \tag{5}$$

where $g_5 = \frac{1}{g_1 g_2}$ the digital coefficient and the digital transfer functions are

$$H_1(z) = z^{-2} \text{ and } H_2(z) = g_5\left(1 - z^{-1}\right)^2 \tag{6}$$

Proceeding in this manner, we have the modulator output in the WLAN mode as

$$Y_{WLAN} = z^{-4}X(z) + g_6\left(1 - z^{-1}\right)^6 Q_3(z) \tag{7}$$

where $g_6 = \frac{1}{(g_1 g_2)(w_1 w_2)}$ is the gain coefficient in the digital cancellation filter and the digital transfer functions are

$$H_3(z) = z^{-2} \text{ and } H_4(z) = g_6\left(1 - z^{-1}\right)^2 \tag{8}$$

The optimal set of coefficient for the three standards are given in Table 4

3 ∑Δ Modulator Non-Idealities and Analysis

In the design of ∑Δ ADCs, we need to optimize a large set of parameters including the overall structures and the performance of the building blocks to achieve the required

Table 3 Comparison of ∑Δ modulator architectures.

Wireless Standard	Order	OSR	F_{CLK} (MHz)	Bits B	SNR (dB)
GSM	2	64	25.6	1	78
	2	128	51.2	1	80
	2	160	64	1	88
	3	64	25.6	1	105
WCDMA	3	16	80	2	68
	4	16	64	2	73
	4	20	100	1	88
	5	16	80	1	94
WLAN	4	5	100	4	52
	5	4	80	4	50
	6	5	100	3	64
	6	8	160	4	65

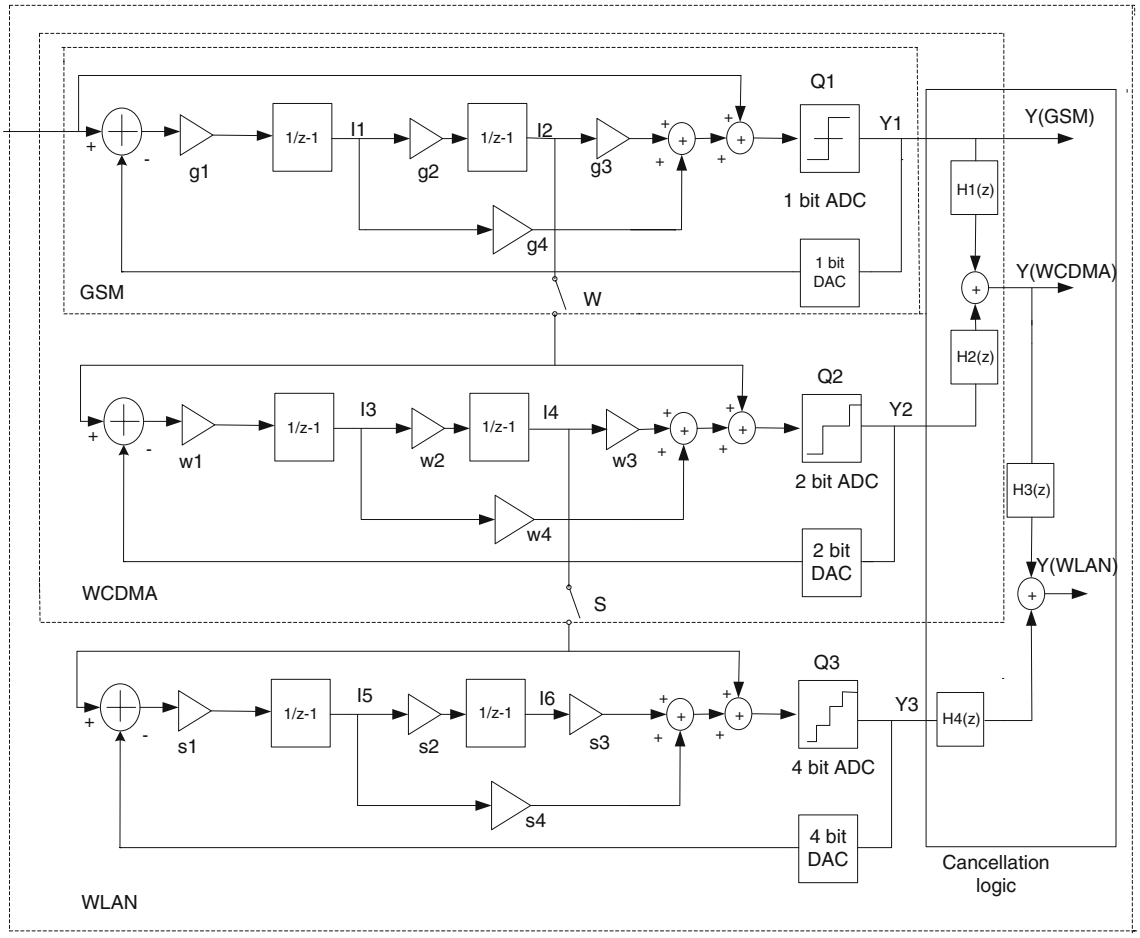


Figure 2 Programmable sigma-delta modulator for GSM/WCDMA/WLAN.

signal-to-noise ratio. Therefore, behavioral simulations were carried out using a set of Simulink™ models [12, 13] in MATLAB Simulink™ environment in order to verify the performance of GSM/WCDMA/WLAN system, to investigate the circuit non-idealities effect, to optimize the system parameters and to establish the specifications for the analog cells. The most important building block of a ∑Δ ADCs is the switched-capacitor (SC) integrator which is shown in Fig. 9. The z-domain transfer function of the integrator in Fig. 9 is $H(z) = \frac{C_s}{C_i}\frac{z^{-1}}{1-z^{-1}}$.

Table 4 Coefficients of the triple-mode sigma-delta modulator.

GSM		WCDMA		WLAN	
Coefficients	Value	Coefficients	Value	Coefficients	Value
G1	0.5	W1	0.5	S1	0.5
G2	0.5	W2	0.5	S2	0.5
G3	4.0	W3	4.0	S3	4.0
G4	4.0	W4	4.0	S4	4.0

The main non-idealities considered here are finite and nonlinear dc gain, slew rate and gain-bandwidth limitations, amplifier saturation voltage, capacitor mismatch, opamp input referred noise, kT/C noise, clock jitter and DAC capacitor mismatch [12, 13]. The most important building block in switched-capacitor (SC) ∑Δ ADC is operational

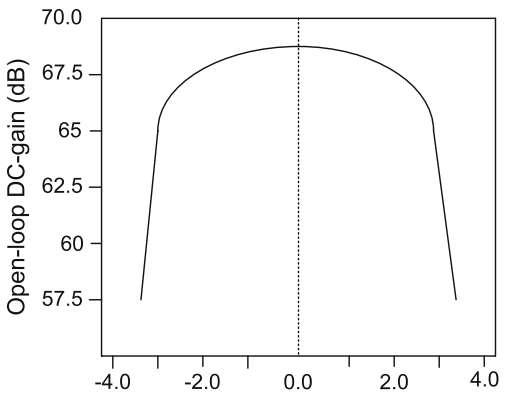


Figure 3 Open loop DC gain as a function of the output voltage.

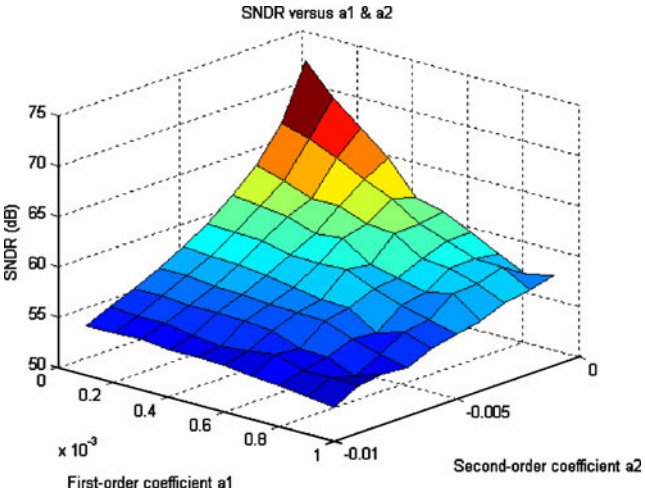


Figure 4 Degradation of SNDR with nonlinear dc gain.

trans-conductance amplifier (OTA). So the modeling of its non-idealities becomes critical. Among all the performance, finite and nonlinear dc gain, finite BW and slew rate and output swing are the most limiting non-idealities of OTA.

3.1 Effect from Finite and Non-Linear DC Gain

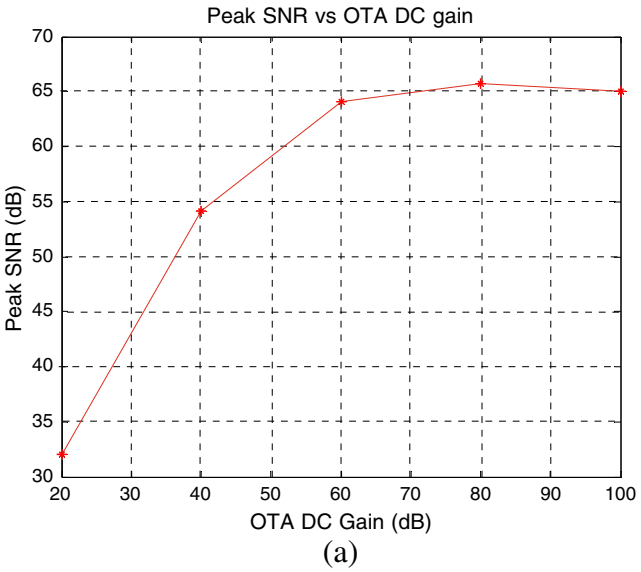
The open-loop dc gain of the amplifier is not only finite but can be nonlinear also. Such non-linearities occur, when the integrator implementation is based on an amplifier with input-dependent gain as shown in Fig. 3. The consequence of these non-linearities is harmonic distortion that limits the peak SNR achievable at large signal levels.

The non-linear open loop gain of the amplifiers introduces error components as harmonic distortion in the modulator output spectrum. The non-linearity of the gain is manifested by its dependency on the amplifier output. In reality, all the amplifiers experience a non-linear gain because the transition between the linear and saturation output region is gradual. The dependency of the open-loop gain of the amplifier in the first integrator on the output voltage can be approximated by the polynomial as follows :-

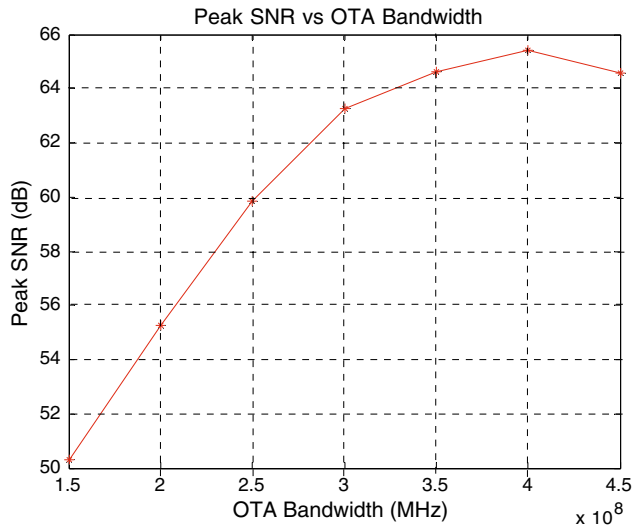
$$A_v = A_0(1 + a_1 v + a_2 v + \ldots\ldots) \quad (9)$$

where the second-order nonlinear coefficient is negative and of a module quite large than that of the first order.

Figure 4 shows the 3D simulation result where the first-order coefficient (a_1) changes from 0.01% to 0.1% and second-order coefficient (a_2) changes from 0.1% to 1%, keeping the DC gain at 1000. The performance degradation



(a)



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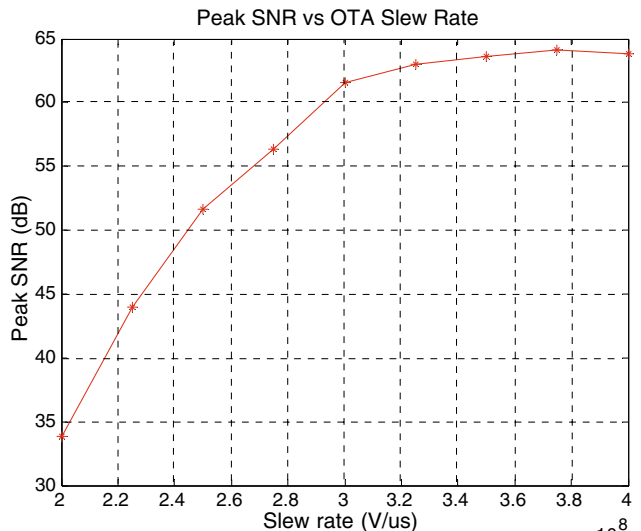


(c)

Figure 5 Peak SNR for **a** OTA DC gain; **b** OTA Bandwidth; **c** OTA Slew Rate.

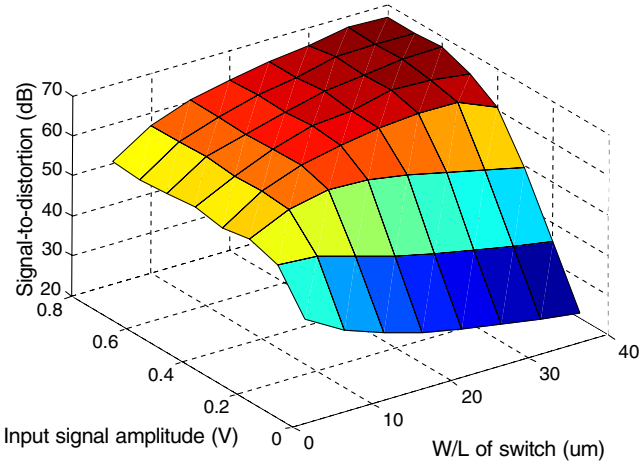


Figure 6 Distortion of the sampling phase of an integrator.

is a consequence of harmonic distortion, rather than an increase in quantization noise

3.2 Effect from Incomplete Settling of OTA

Slew rate (SR) and Bandwidth (BW) limitation [12,13] can lead to a non-ideal transient response within each clock cycle, thus producing an incomplete or inaccurate charge transfer to the output at the end of the integration period. In other words, the time constant of the integrator which is given by $1/2\pi GBW$ should be kept smaller than the sampling period T_s for the modulator to be stable. But it is found that this constraint for the settling of the integrator output is acceptable, provided that the settling process is linear. That is, the settling must not be slew-rate limited. The SR and BW limitations produce harmonic distortion reducing the total SNDR of the $\Sigma\Delta$ modulators.

MATLAB simulations were carried out to determine the requirements of OTA to meet the specifications of GSM/WCDMA/WLAN applications. Figure 5 shows the peak SNR for various OTA DC gain, bandwidth and slew rate. Based on these results, OTA needs to have more than 60 dB DC gain, at least 350 MHz closed loop bandwidth and more than 300 V/us slew rate. The SNRs are then checked with OTA gain of 1000, bandwidth of 350 MHz and slew rate of 300 V/us in the WLAN mode which is the most critical one.

3.3 Effects from Switch Non-Linearity

The input signal amplitude, switch size and harmonic distortion statistics are compiled to minimize the distortion introduced by the switches. Figure 6 shows the statistical result of the signal to distortion ratio (SDR) vs. switch size with various input signal amplitudes. SDR can be increased either by increasing the switch size or by reducing the input signal amplitude. Although increasing the switch can reduce the harmonic distortion, it causes the parasitic capacitance to increase and thus the clock feed-through noise is increased. There is a trade off between the switch size and the distortions. It is found that the optimum value of the switch size can be chosen as 30 um without much degradation in SDR.

3.4 Effect of Capacitor Mismatch

MASH (Multi-stage Noise Shaping) $\sum\Delta$ modulators are sensitive to coefficient mismatches. Those coefficients are implemented in the switched-capacitor (SC) $\sum\Delta$ modulator by capacitor ratios. This necessitates the study of sensitivity analysis of matching error between analog and digital gain coefficients. Figure 7 depicts the sensitivity of matching between analog and digital gains on the performance of the modulator. The 3-D plot shows the influence in signal-to-noise ratio as the percentage of mismatch between the analog (g_1) and digital (g_5) coefficients which are varied from 0 to 10%, both in the positive and negative direction. It is observed that there is a degradation of more than 20 dB in the peak signal-to-noise ratio.

4 Circuit-Level Design

The configurable sigma-delta modulator has been designed in TSMC 0.18um CMOS technology, operating from 1.8V supply voltage. The circuit-level implementation of the 2nd order $\sum\Delta$ modulator with feed forward signal path used in the first stage is shown in Fig. 8.

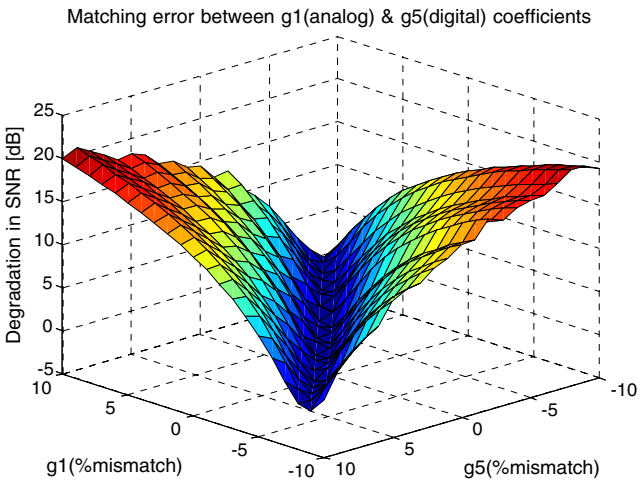


Figure 7 Degradation of SNR with coefficient mismatch.

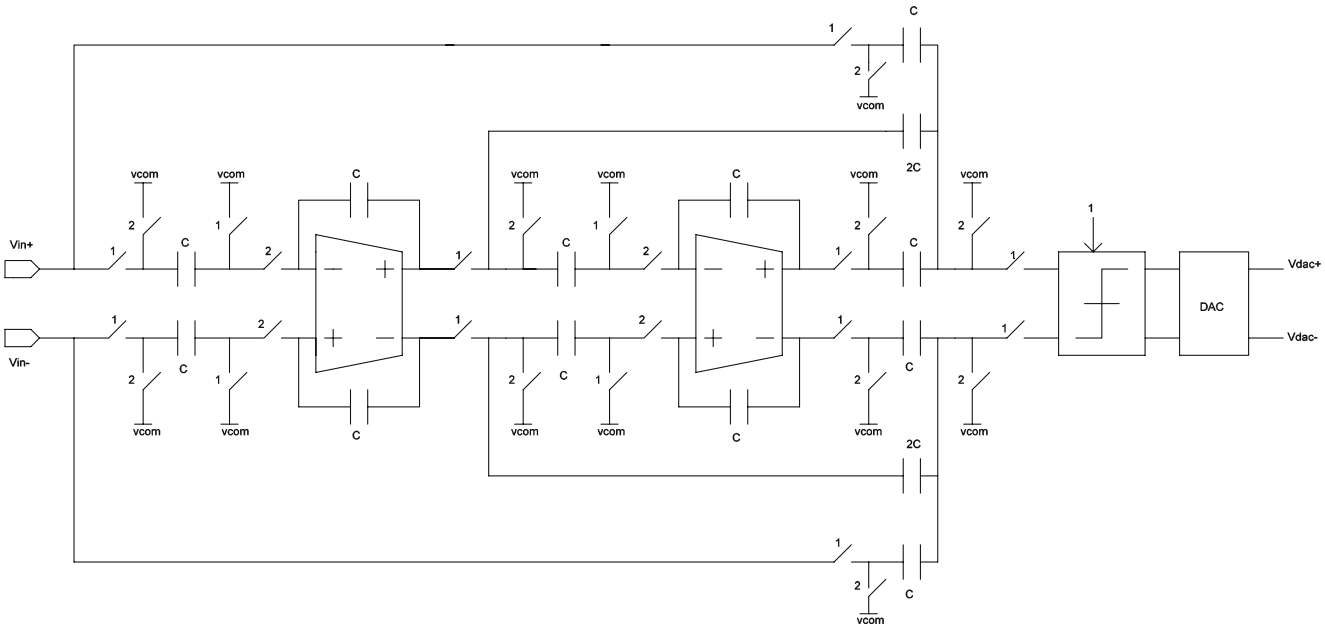


Figure 8 The first stage 2nd order feed forward single-bit ∑Δ modulator.

The proposed sigma-delta modulator for GSM/WCDMA/WLAN receiver was implemented as a fully-differential switched-capacitor (SC) circuit, which has been simulated using Cadence/Spectre. The design of the individual circuit blocks like operational transconductance amplifier (OTAs), switches, capacitors and comparators has been done based on the behavioral simulation results. The forward signal path was implemented by connecting a passive SC network to the input of the quantizer. The integrators were implemented in a fully differential configuration as shown in Fig. 9 and employ the bottom-plate sampling technique to minimize signal-dependent charge-injection and clock feed through. The basic blocks are dealt in detail.

The integrator is implemented in a fully differential configuration and employs a two-phase non-overlapping clock as shown in Fig. 9. The input is sampled during phase 1 (F_1 and F_{1d}). During phase 2, the charge is transferred from the sampling capacitor (Cs) to the integrating capacitor (Ci). At the same time, depending on the output value, the appropriate DAC reference level is applied by closing either switches labelled F_{2d1} or F_{2d2}, thus performing the subtraction operation and the results are being accumulated in the integration capacitors.

The integrator employs the bottom-plate sampling technique to minimize signal-dependent charge-injection and clock-feed through. This is achieved through delayed

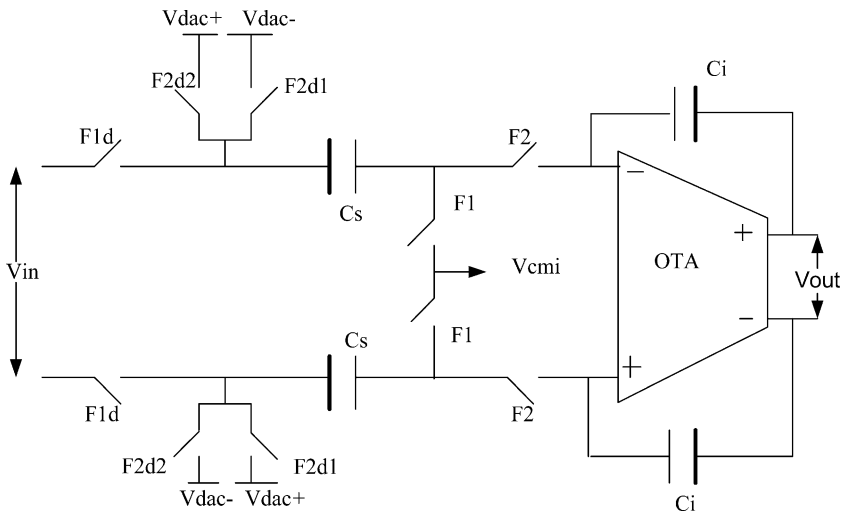


Figure 9 Fully-differential switched-capacitor integrator.

clocks: F_{1d}, F_{2d1} and F_{2d2}. When switches labelled F_1 are first turned off, the charge injection from those switches remains, to a first order, independent of the input signal. Because one of plates is now floating, turning off switches labelled F_{1d} shortly after does not introduce charge-injection errors. Further the switches F_{1d}, F_{2d1} and F_{2d2} are implemented as CMOS transmission gates in order to ensure a small variation in on-resistance across the full input signal range. This also serves to reduce signal-dependent charge injection from the switches to Cs and Ci to a negligible level.

4.1 Switches

Linearity is an important factor in the design of switches. It is desirable to operate in a region where the on resistance of the switch is independent of the input voltage. Figure 10 shows the switch on-resistance as a function of input voltage. The switches used in the integrator are implemented with complementary MOS devices because the DC voltages are biased at mid-supply. In CMOS switches, the sizing of the NMOS and PMOS devices is critical. Figure 11 shows the on-resistance of the CMOS switch for varying widths of NMOS and PMOS transistors. The parallel combination of the NMOS and PMOS devices yields an effective resistance given by

$$R_{ON,CMOS} = \left[\begin{array}{l}\mu_N C_{ox}\left(\frac{W}{L}\right)_N (V_{GSN} - V_{THN}) \\ +\mu_p C_{ox}\left(\frac{W}{L}\right)_p (V_{GSP} - |V_{THP}|)\end{array}\right]^{-1} \quad (10)$$

For linearity reasons, the input switches, labeled F_{1d}, F_{2d1} and F_{2d2} in Fig. 9 should be designed for equal impedances. This means the PMOS should be made larger than the NMOS by a factor equal to the ratio μ_N/μ_P as shown below.

$$\frac{\left(\frac{W}{L}\right)_P}{\left(\frac{W}{L}\right)_N} = \frac{\mu_N}{\mu_P} \quad (11)$$

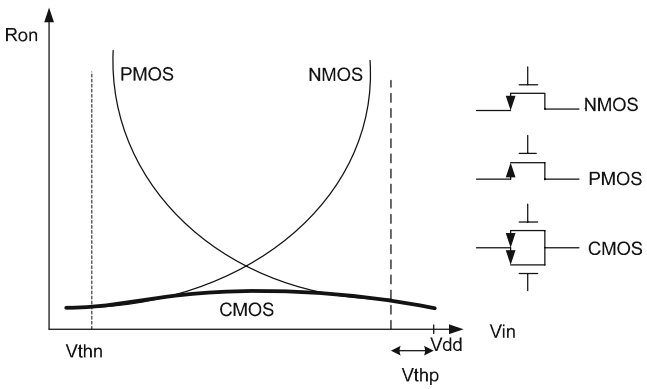


Figure 10 Switch on-resistance as a function of the input voltage.

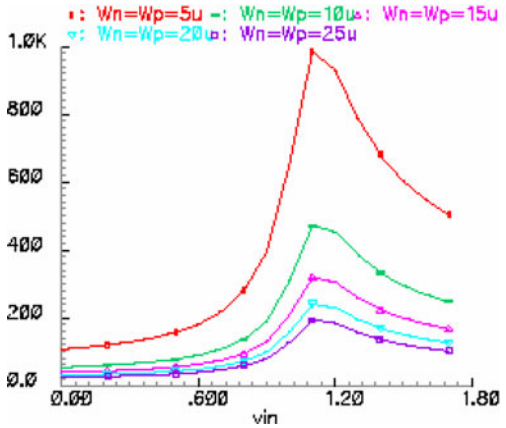


Figure 11 On-resistance of the sampling switch.

A switch size of 10/0.18 µm for NMOS and 40/0.18 µm for PMOS is chosen for F_{1d}, F_{2d1}, and F_{2d2} as shown in the Table 5. The bottom-plate switches, labelled F_1 and F_2 should be designed for a first-order cancellation of charge-injection errors. The error is given by

$$\begin{aligned}\Delta V_{OUT} &= -\tfrac{1}{2}\cdot\frac{(Q_{chan})_N}{C_s} + \tfrac{1}{2}\cdot\frac{(Q_{chan})_P}{C_s} \\ &= -\tfrac{1}{2}\cdot\frac{C_{ox}}{C_s}\cdot\{W_N L_N(V_{DD} - V_{IN} - V_{THN}) \\ &\quad - W_P L_P(V_{IN} - V_{THP})\}\end{aligned} \quad (12)$$

For a partial cancellation of charge-injection error, the NMOS and PMOS devices should be designed to have equal sizes.

$$W_N L_N = W_P L_P \quad (13)$$

A switch size of 10/0.18 µm is selected for F_1 and F_2 as from the Table 5 which has an on-resistance of 500 ohm. The fully-differential configuration of the integrator further mitigates the effects of signal-dependent charge injection. The values of sampling and integration capacitors are 2pF, 1pF, 0.5pF, 0.2pF and 4pF, 2pF, 1pF, 0.4pF respectively.

4.2 Operational Trans-conductance Amplifier (OTA)

The goal in selecting OTA was to choose a topology, which can meet the integrator requirements at minimum power dissipation. Reduced integrator output swings allowed us to

Table 5 Switches and capacitors in the integrator.

Switch	Size	Switch	Size	Capacitor	Size
F_1	N: 10/0.18 µm P: 10/0.18 µm	F_{1d}	N: 10/0.18 µm P: 40/0.18 µm	C_s	2 pF
F_2	N: 10/0.18 µm P: 10/0.18 µm	F_{2d1}, F_{2d2}	N: 10/0.18 µm P: 40/0.18 µm	C_i	4 pF

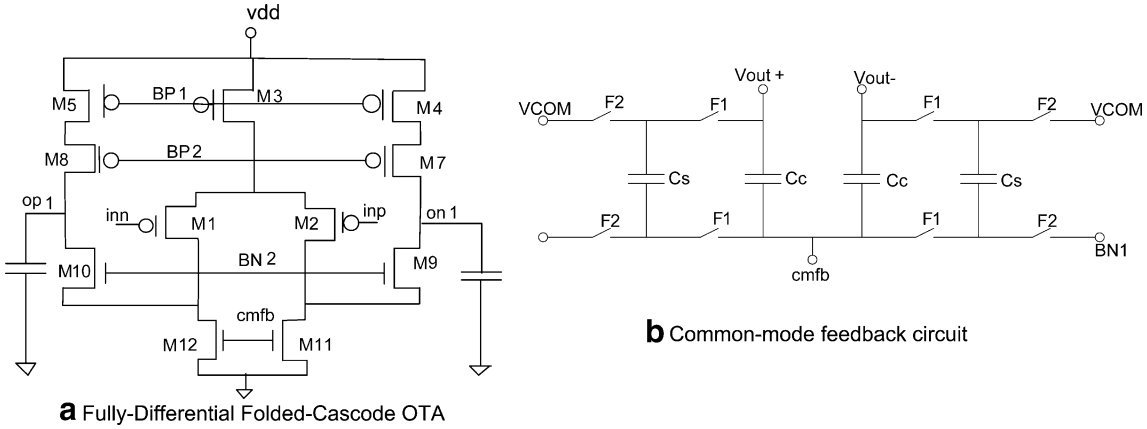


Figure 12 Fully-differential folded-cascode OTA and CMFB circuit.

choose the fully differential folded-cascode OTA for all integrators. Since the DC gain requirement is not so demanding, this is a good selection because of its high operation speed / power consumption ratio. The output common-mode voltage was also stabilized using a dynamic switched-capacitor common-mode feedback (CMFB) circuit whose linearity is good enough for this application and does not require extra power consumption. Figure 12 shows the schematic of the fully differential folded-cascode OTA and the SC common-mode feedback (CMFB) circuit. The load capacitances and the OTAs have been scaled down to minimize the power. The transistor sizes and the performance summary of the front-end OTA is presented in Table 6.

4.3 Comparator

The single-bit quantizer is implemented with a regenerative latch followed by an SR latch as shown in Fig. 13. The comparator hysteresis is 7.9mV and the comparator offset is 3.8mV, which is less than 0.5LSB. The single-bit DAC is a simple switch network connected to reference voltages. The 4-bit quantizer from the third stage is implemented with a 4-bit flash A/D converter and the 4-bit D/A converter is implemented in a fully differential SC configuration as shown in Fig. 14. The sampling capacitances are combined with sixteen small unit capacitance to realize the 4-bit DAC. No DEM circuit is used because the behavioral simulations suggested that there are no distortions associated with the 4-bit DAC nonlinearity. Table 7 gives the transistor sizes used in the regenerative latch.

4.4 The Clocks

In switched-capacitor circuit two non-overlap clock phases are needed. In order to reduce the influence of charge injection (also called clock feed through), a delayed version is needed for each clock phase. A complement version is also needed for each clock phase when a transmission gate is used. Normally 4–8 clock phases are needed in a sigma delta modulator. These clock phases are usually generated on-chip. In a normal signal generator the delayed version clock phase has a same delay at both rising edge and falling edge. However in most modulators only the falling edge needs to be delayed in order to reduce the signal-dependent charge injection. The rising edge does not have to be delayed. The advantage of non-delayed rising edge is that the settling time can be increased, which reduces the requirement on the OTA driving capability. The rising edges of the delayed clocks should be lined up with the rising edges of the non-delayed versions to increase the amount of available settling time for the OTA, which is given by

$$T_{settle,available} = \frac{T_s}{2} - t_{nol} - t_r - t_f \tag{14}$$

Table 6 Transistor sizes and the performance summary of the folded-cascode OTA.

OTA Specification	Value
DC Gain	63.7 dB
GBW (C_L = 2pF)	442 MHz
SR (C_L = 2pF)	300 V/us
Phase Margin	62 degree
Output Swing	2 V (differential)
Maximum Current	2.1 mA
Power dissipation	3.78 mW
Technology	0.18 um CMOS
Transistor	Size (μm)
M_1, M_2	720/0.48
M_3	432/0.48
M_4, M_5, M_7, M_8	216/0.48
M_9, M_{10}	144/0.48
M_{11}, M_{12}	72/0.48

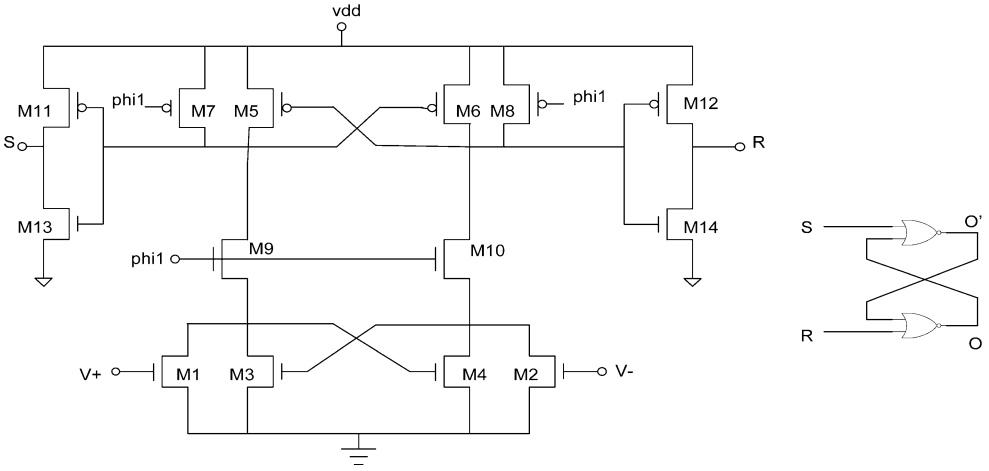
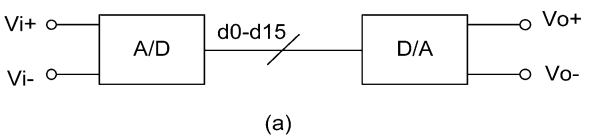


Figure 13 Regenerative comparator.

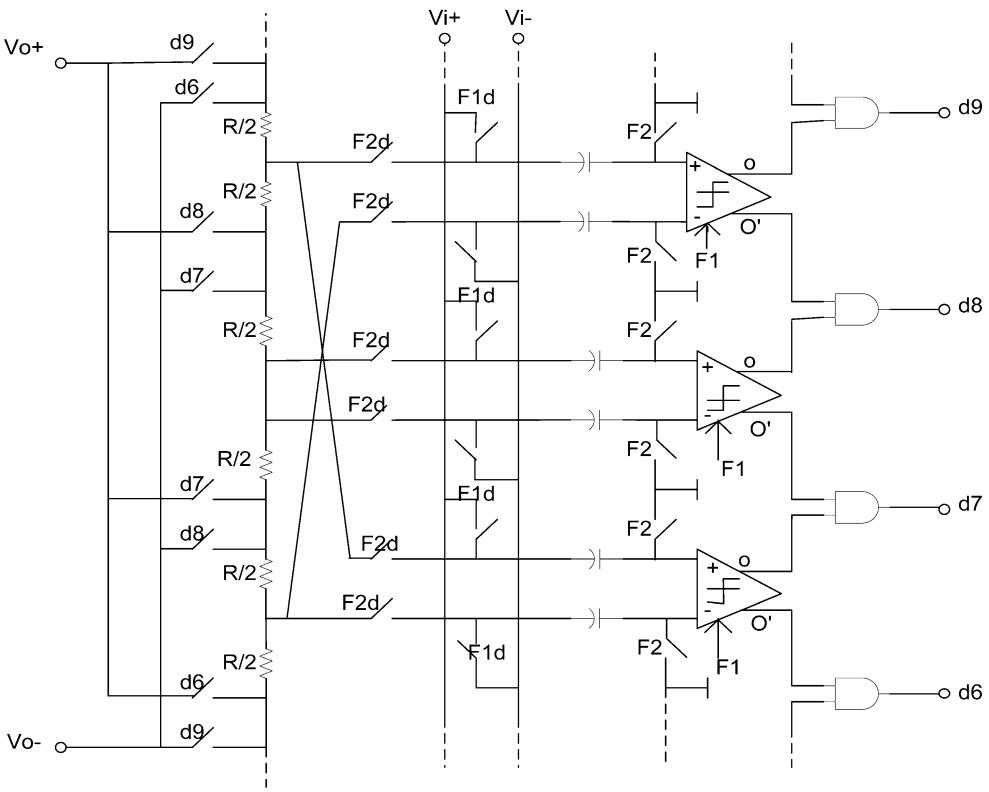
where

T_s	Sampling period
t_{nol}	Nonoverlap Time
t_r	Rise Time
t_f	Fall Time

A circuit to realize two-phase non-overlapping clocks is shown in Fig 15. The two basic non-overlap phases F_1 and F_2 are generated by latches. The delayed versions of these two phases are generated by inverters working as delay-line. The complement versions of these phases are also generated by inverters, but these inverters are large and cause very



(a)



(b)

Figure 14 **a** Block diagram of the A/D/A system **b** Partial view of its SC implementation.

Table 7 Transistor sizes in the regenerative latch.

Transistors	Size (μm)
M_1, M_3, M_2, M_4	0.9/0.45
M_9, M_{10}	2.25/0.45
M_5, M_6, M_7, M_8	2.25/0.45
M_{11}, M_{12}, M_{13}, M_{14}	1.2/0.18

short extra delay. The special two-input "inverter" guarantees that the delay happens only at falling edges.

5 Simulation Results

Figure 16 shows the modulator output spectrum for GSM/WCDMA/WLAN modes for a 0.5V,0.2/2/20MHz input signal at a sampling frequency of 64/64/200 MHz respectively. These results show that a high linearity can be achieved due to the low-distortion sigma-delta modulator architecture, multi-bit quantization and modified cascaded architecture.

Figure 17 presents the simulated Signal-to-Noise plus Distortion Ratio (SNDR) versus input signal amplitude, for GSM/WCDMA/WLAN standards. Simulation results show a peak SNDR of 88 dB@-4dBFS in GSM mode a peak SNDR of 73 dB@-6dBFS in WCDMA mode, and a peak SNDR of 58 dB@-6dBFS in the WLAN mode. Table 8 summarizes simulated performance of this multi-standard ∑Δ modulator.

6 Conclusions

A GSM/WCDMA/WLAN multi-standard sigma-delta modulator has been proposed in this paper. This programmable sigma-delta ADC uses a low-distortion swing suppression topology to achieve high linearity in wideband applications. This architecture is effective for low OSR and imperfect components of the modulator, and it can simplify the circuit complexity. Simulation

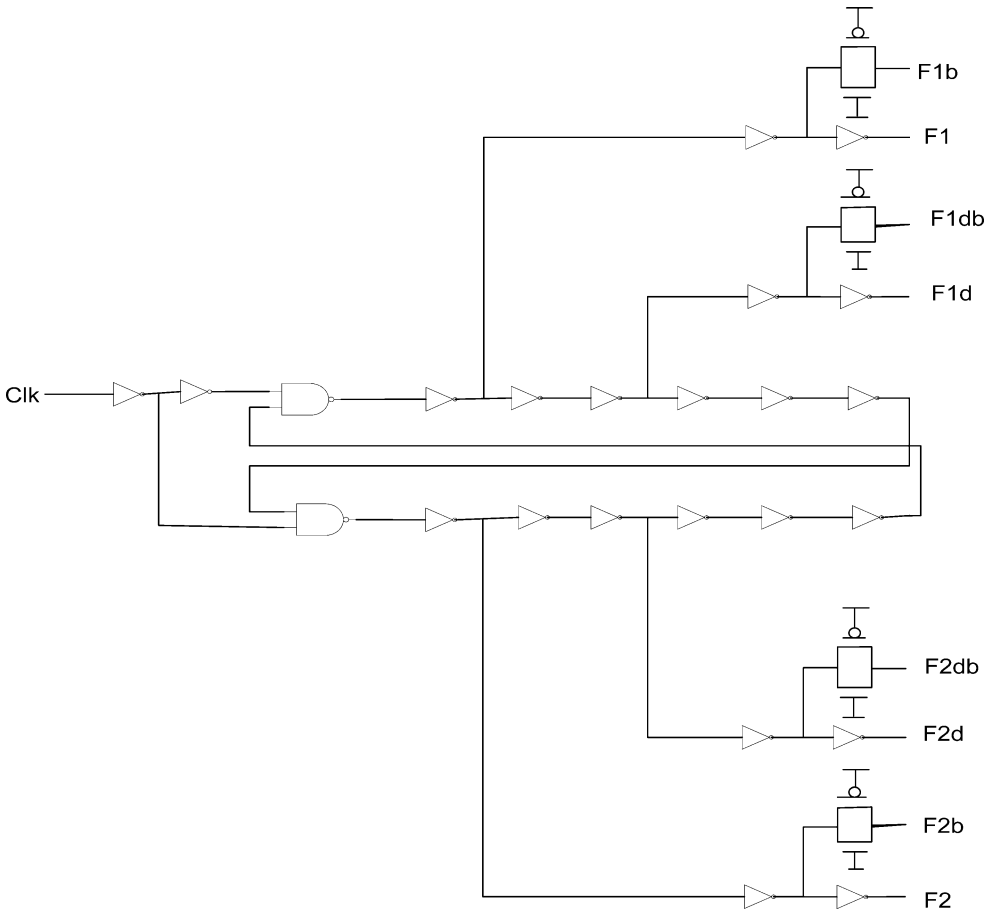


Figure 15 Two-Phase Clock Generator Schematic.

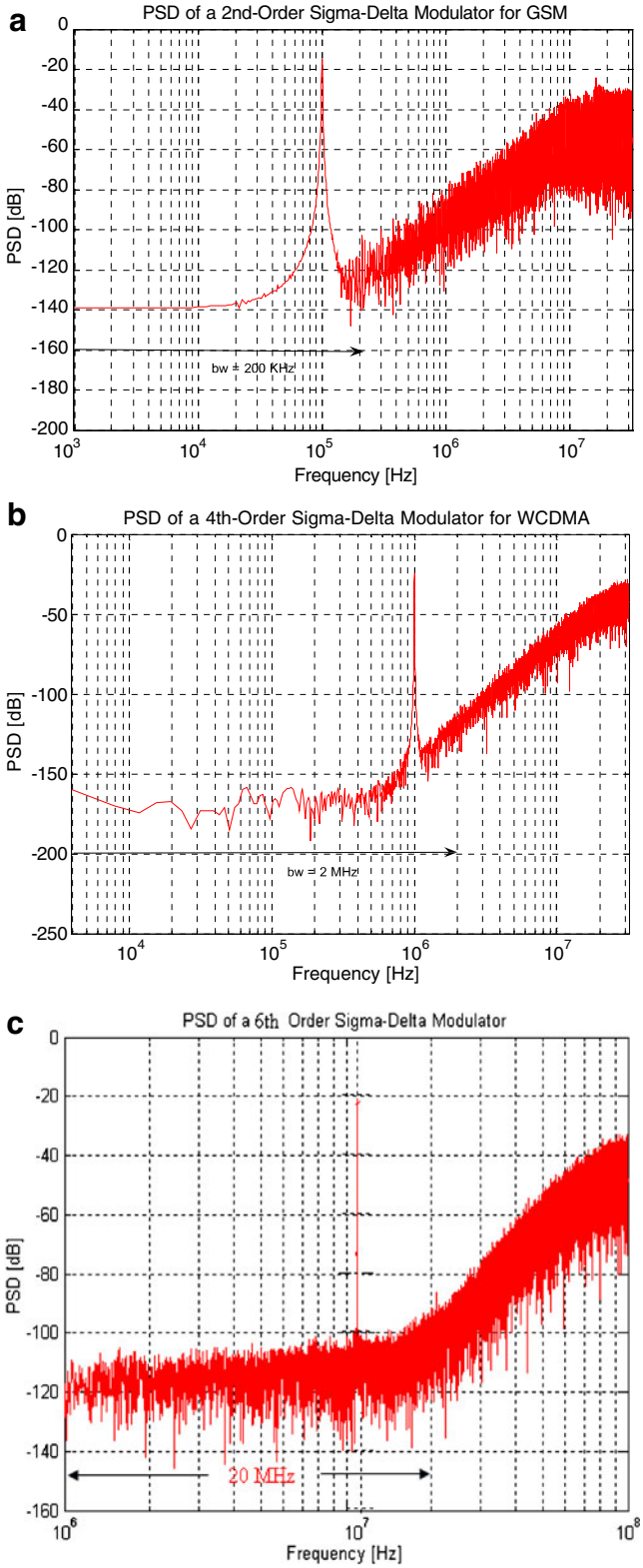


Figure 16 Modulator output spectrum in **a** GSM mode **b** WCDMA mode **c** WLAN mode.

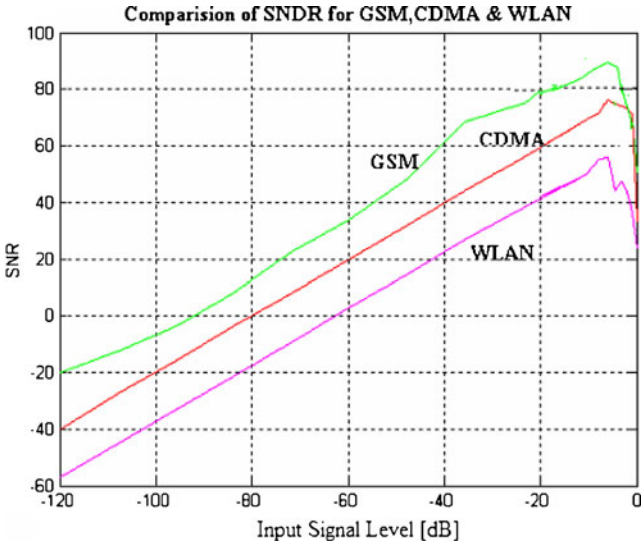


Figure 17 SNDR versus input level for GSM/WCDMA/WLAN mode.

results indicate that a 4th order modified cascaded modulator with single-bit in the first stage and 2-bit in the second stage can be used to achieve the required dynamic range for WCDMA mode and a 2-2-2 cascaded MASH architecture can be adopted for the WLAN standard. The circuit-level design and implementation were carried out using TSMC 0.18 um CMOS technology at 1.8 V supply.

Table 8 Summary of the performance of the multi-standard ∑Δ modulator.

Process Supply voltage	TSMC 0.18um CMOS process 1.8 V		
Mode Architecture	GSM Feed forward 2nd order	WCDMA 2-2 modified cascaded	WLAN 2-2-2 modified cascaded
Sampling frequency	64 MHz	64 MHz	200 MHz
Signal Bandwidth	200 kHz	2 MHz	20 MHz
OSR	160	16	5
Peak SNDR	88 dB	73 dB	58 dB

Acknowledgments A preliminary version of this paper has appeared at the IEEE International Conference on System on Chip Design (IEEE SOC ' 07) in September, 2007 as "A triple-mode feed-forward sigma-delta modulator design for GSM / WCDMA / WLAN applications."

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