Wideband Low-Distortion Sigma-Delta ADC for WLAN

Babita R. Jose, Mythili P
Department of Electronics and Communication
Cochin University of Science and Technology
Kochi, Kerala, India

Jimson Mathew, D.K. Pradhan
Department of Computer Science
University of Bristol, UK.

Abstract- **This work presents a wideband low-distortion sigma-delta analog-to-digital converter (ADC) for Wireless Local Area Network (WLAN) standard. The proposed converter makes use of low-distortion swing suppression SDM architecture which is highly suitable for low oversampling ratios to attain high linearity over a wide bandwidth. The modulator employs a 2-2 cascaded sigma-delta modulator with feedforward path with a single-bit quantizer in the first stage and 4-bit in the second stage. The modulator is designed in TSMC 0.18um CMOS technology and operates at 1.8V supply voltage. Simulation results show that, a peak SNDR of 57dB and a spurious free dynamic range (SFDR) of 66dB is obtained for a 10MHz signal bandwidth, and an oversampling ratio of 8.**

***Keywords* – dual-band, feedforward path, multistandard receiver, sigma-delta modulator**

I. INTRODUCTION

The demand for higher system capacity and data rate of the cellular phone leads us to move beyond 3G and the development of 4G wireless systems [1] where cellular and Wireless Local Area Network (WLAN) coexist in the same handheld devices like mobile phones and PDAs. WLAN-enabled cell phones are expected to contain multimode cellular capability. To achieve higher data rates in emerging wireless generations such as IEEE 802.11b, the analog front-end must be able to handle wider bandwidths at lower noise and power levels. The sigma-delta (∑-Δ) analog-to-digital converters (ADCs) are widely used in wireless systems because of their superior linearity, robustness to circuit imperfections, inherent resolution-bandwidth trade off and increased programmability in digital domain.

The requirements that the ADC has to fulfill are set by both the standard characteristics and the receiver architecture. This work focuses on a zero-IF WLAN 802.11b receiver, presented in Fig. 1 [2]. The zero-IF architecture shows excellent multi-standard [3] capabilities, making our system easy to upgrade to multi-mode operation. The radio specifications of WLAN 802.11b [4] are summarized in Table I [5]. This together with the link budget, sets the minimum requirements for the ADC. Our architecture choice leads to a minimum dynamic range of 50dB for the ADC for a 10 MHz bandwidth.

This paper presents the design of a highly linear sigma-delta modulator for wireless applications. The proposed architecture employs a multibit 2-2 modified cascaded sigma-delta modulator suitable for WLAN receivers. The paper is organized as follows: Section I is the introduction. Section II presents the modified cascaded sigma-delta modulator architecture and discusses the design issues in arriving at the topology. Section III provides the simulation results. The circuit design considerations are discussed in Section IV. Finally, Section V concludes the paper.

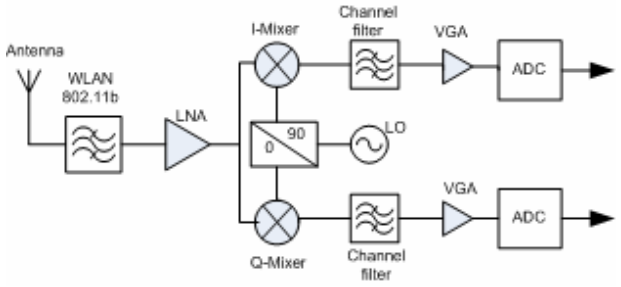


Figure 1. Zero-IF Receiver Architecture

TABLE I. RADIO SPECIFICATIONS FOR WLAN 802.11b

Frequency Band	2.412-2.484 GHz
Channel Spacing	25 MHz
Channel Bandwidth	20 MHz
Sensitivity	-76 dBm
Maximum Input Signal	-10 dBm
Input Noise	-104 dBm
Required SNR	14 dB

II. MODULATOR ARCHITECTURE

This Section explores tradeoffs among the wide variety of ∑-Δ modulator architectures that can be used to implement a ∑-Δ A/D converter suitable for low power and high integration WLAN standard receiver. The search for an optimal wideband ∑-Δ topology has been performed by varying the order L, the oversampling ratio M and the number of bits B in the quantizer.

The target specifications for the ∑-Δ modulator were defined to be 50dB DR over 10MHz bandwidth at minimum power dissipation. For signals of very wide bandwidth, such as in WLAN receiver, oversampling ratio cannot be very high (4 or 5) because the achievable clock frequency is constrained by the process technology. Therefore the only solution is by increasing the order L and quantizer bits M in order to achieve the required solution. The dynamic range DR [6] of a ∑Δ modulator is given by

$$DR = \frac{3}{2}\frac{2L+1}{\pi^{2L}} M^{2L+1}.(2^B - 1)^2 \qquad (1)$$

For low-data rate applications, such as GSM receiver, where bandwidth is relatively smaller, oversampling ratio (M) can be made higher, which will increase the circuit complexity and power consumption. For higher order or multi-bit modulators the complexity becomes higher, and for higher sampling frequency the requirements of analog building blocks becomes more demanding. Alternatively, the increased quantizer resolution enables us to use a lower oversampling ratio or a lower noise-shaping order for a given dynamic range bandwidth target. Unfortunately, the higher quantizer resolution will lead to a large area of internal flash ADC and switched-capacitor DAC and increased power consumption. An OSR of 8 has been chosen as a compromise between the technologically feasibility sampling frequency and bandwidth requirements. Once the OSR was established, a 2-2 modified cascaded modulator architecture has been adopted which can provide comparable dynamic ranges. The next key issue in the design of a low-power ∑-Δ modulator is the quantizer resolution. Thus B plays an important role in the power-performance design of the modified cascaded sigma-delta modulator. A multibit quantizer with multibit feedback digital-to-analog converter (DAC) has to be used to attain the WLAN specifications. The main drawback of multibit ∑-Δ modulator is the high linearity that is required of the feedback DAC. Thus the overall sigma-delta converter linearity and resolution are limited by the precision of the multibit DAC. Reducing the quantizer's resolution to 1 bit may eliminate the dependence on feedback DAC linearity. One way to achieve further reduction of quantization noise is to use a multibit quantizer only in the final stage to eliminate the necessity of DEM techniques to improve the linearity of multibit DAC. Therefore we have adopted a single bit quantizer in the first stage and 4-bit quantizer in the second stage.

Fig 2 shows the block diagram of the proposed modified cascaded sigma-delta modulator. The 4th order modified cascaded ∑-Δ modulator architecture employs two key design approaches. One is the 2nd order sigma-delta modulator with feedforward signal path [8], which has a high linearity even at low OSR. The other is the structural approach, which combines the merits of modified cascaded topology and multibit quantization in the last stage to make all quantization noise sources negligible at low oversampling (OSR). The scaling coefficients have been used to achieve the peak signal-to-noise and distortion ratio (SNDR), to control the input of the second stage and to utilize the full dynamic range of the next stage. By combining these techniques the performance improvements of the ∑-Δ modulator are significant.

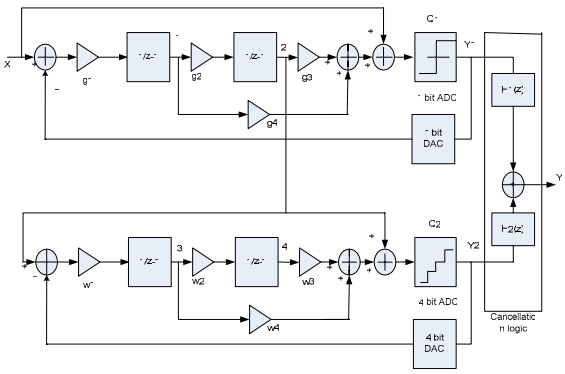


Figure 2. Modified cascaded sigma-delta modulator for WLAN

The output of the first stage of the modulator is given by

$$Y_1(z) = X(z) + \frac{(1-z^{-1})^2}{1+(g_1g_4-2)z^{-1}+(1+g_1g_2g_3-g_1g_4)z^{-2}} Q_1(z) \qquad (2)$$

The output of the integrators, I_1 and I_2 are given by

$$I_1(z) = \frac{g_1 z^{-1}(1-z^{-1})}{1+(g_1g_4-2)z^{-1}+(1+g_1g_2g_3-g_1g_4)z^{-2}} Q_1(z) \qquad (3)$$

$$I_2(z) = \frac{g_1g_2z^{-2}}{1+(g_1g_4-2)z^{-1}+(1+g_1g_2g_3-g_1g_4)z^{-2}} Q_1(z) \qquad (4)$$

From equations (3) and (4), it is observed that the integrators process only the quantization noise.
Therefore, the integrator output swings of the proposed architecture are reduced compared with the traditional one and then the operational amplifier requirements are greatly relaxed. Since the output of the second integrator contains only quantization noise, this output has been used as input for the second stage. Therefore, the output of the second stage is given by

$$Y_2(z) = \frac{g_1g_2z^{-2}}{1+(g_1g_4-2)z^{-1}+(1+g_1g_2g_3-g_1g_4)z^{-2}} Q_1(z) + \frac{(1-z^{-1})^2}{1+(w_1w_4-2)z^{-1}+(1+w_1w_2w_3-w_1w_4)z^{-2}} Q_2(z) \qquad (5)$$

where $Q_1(z)$, $Q_2(z)$ are the quantization errors of the first and second stages respectively and g_1, g_2, g_3, g_4, w_1, w_2, w_3, w_4 are the analog coefficients.

The final modulator output after the cancellation logic is given by

$$Y(z) = z^{-2}X(z) + \frac{1}{g_1 g_2}\frac{(1-z^{-1})^4}{1+(w_1w_4-2)z^{-1}+(1+w_1w_2w_3-w_1w_4)z^{-2}}Q_2(z) \quad (6)$$

where the digital coefficient is $d=1/g_1g_2$ and the digital transfer functions are $H_1(z)=z^{-2}$ and $H_2(z)=d\,(1-z^{-1})^2$.

The optimal coefficients for generating the maximum peak signal to noise and distortion ratio (SNDR) are: $g_1=g_2=w_1=w_2=0.5$, $g_3=g_4=w_3=w_4=4$.

The simulated integrator outputs histograms of the 4th order cascaded sigma-delta modulator with -4dB/2.5 MHz sine wave input is shown in Fig. 3.

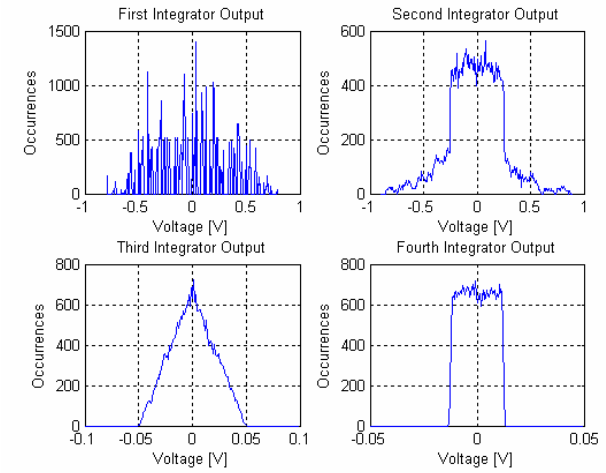


Figure 3. Integrator Output Swings

III. SIMULATION RESULTS

Behavioral simulations were carried out using behavioral models [9,10] in MATLAB Simulink environment in order to verify the performance for a WLAN system, to investigate the circuit nonidealities effect, to optimize the system parameters and to establish the specifications for the analog cells. The main nonidealities considered here are finite and nonlinear dc gain, slew rate and gain-bandwidth limitations, amplifier saturation voltage, capacitor mismatch, opamp input referred noise, kT/C noise, clock jitter and DAC capacitor mismatch [9,10]. In the behavioral model we have considered that the OTA presents an open-loop gain whose dependency on the output voltage can be approximated by a polynomial function. In the behavioral model of the multibit DAC we assumed that the mismatch error of the unit- elements has Gaussian distribution with standard deviation σ. For slew-rate (SR) and gain-bandwidth (GBW) limitations we have used the modeling approach interpreting these effects as a nonlinear gain. Using the behavioral simulations we have estimated the OTA requirements for a specified dynamic range. Simulation results show that the proposed modulator can tolerate an OTA dc gain of 60 dB without performance degradation and the OTA bandwidth needs to be at least 340 MHz. The 4-bit DAC in the second stage was assumed to have 17 levels and 16 unit elements with no dynamic element matching (DEM) or calibration used.

Simulations were performed using an OSR of 8 for a bandwidth of 10 MHz. Fig 4 shows the modulator output spectrum for a 0.4V/2.5MHz input signal. As shown in Fig 4, the resulting 3rd harmonic tone is -66dB below the amplitude of the input signal and the SFDR is 66 dB.

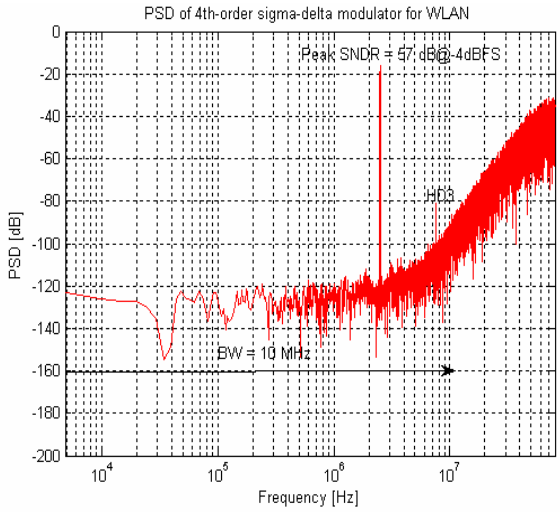


Figure 4. Modulator Output Spectrum for WLAN

Fig 5 presents the simulated SNR and SNDR versus input signal amplitude for WLAN. Simulation results show a peak SNR of 60 dB@-4dBFS and a peak SNDR of 57 dB@-6dBFS in the WLAN mode.

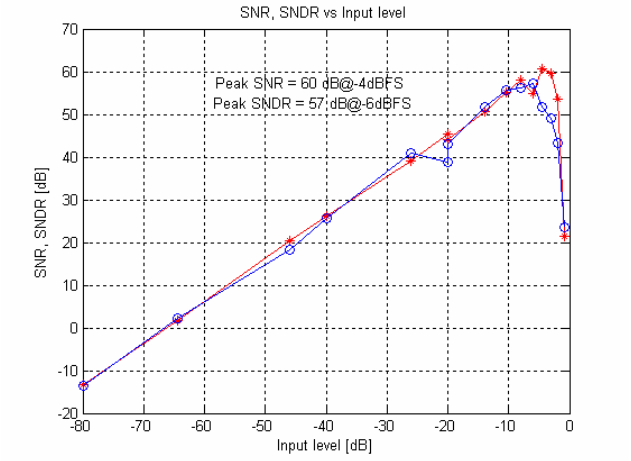


Figure 5. SNR and SNDR versus input amplitude

IV. CIRCUIT-LEVEL DESIGN

The configurable sigma-delta modulator has been designed in TSMC 0.18um CMOS technology, operating from 1.8V supply voltage. The circuit-level implementation of the 2nd order ∑Δ modulator with feedforward signal path used in the first stage is shown in Fig 6. The proposed sigma-delta modulator for WLAN receiver was implemented as a fully-differential switched-capacitor (SC) circuit, which has been simulated using Cadence/Spectre. The design of the individual circuit blocks like OTAs, switches, capacitors and comparators has been done based on the behavioral simulation results. The forward signal path was implemented by connecting a passive SC network to the input of the quantizer. The integrators were implemented in a fully differential configuration and employ the bottom-plate sampling technique to minimize signal-dependent charge-injection and clock feedthrough. The optimum values of the switches size, which yields a minimum time constant, have been used. The sizes of the sampling and integrating capacitors were governed by the noise requirements and matching requirements. The values of sampling and integration capacitors are successively 2pF, 1pF, 0.5pF, 0.2pF and 4pF, 2pF, 1pF, 0.4pF. The goal in selecting OTA was to choose a topology, which can meet the integrator requirements at minimum power dissipation. Reduced integrator output swings allowed us to choose the fully differential folded-cascode OTA for all integrators.

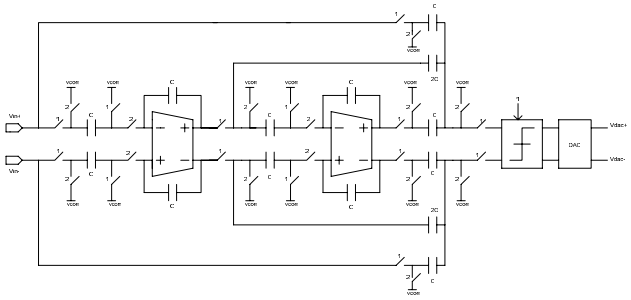
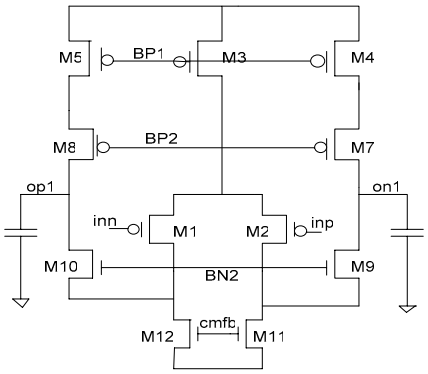


Figure 6. The first stage 2nd order single-bit ∑Δ modulator



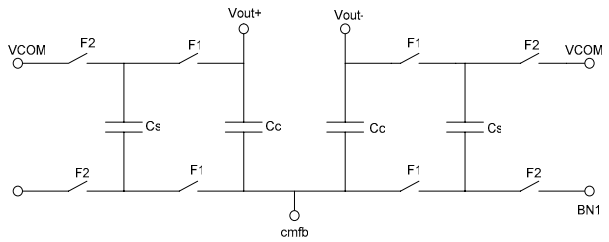


Figure 7. Fully-Differential Folded-Cascode OTA and CMFB circuit

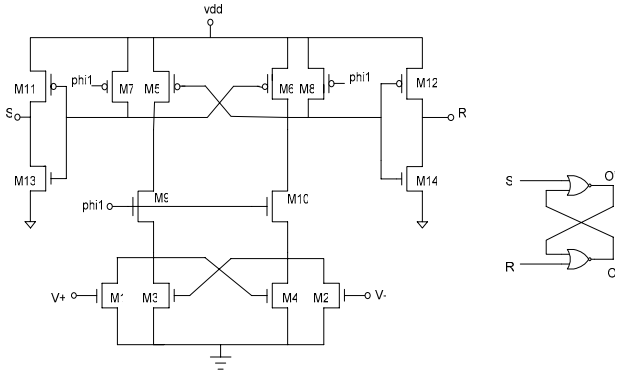


Figure 8. Regenerative Comparator

TABLE II SUMMARY OF THE FRONT-END OTA

OTA Specification	Value
DC Gain	68 dB
GBW (C_L = 2pF)	340 MHz
SR (C_L = 2pF)	160 V/us
Phase Margin	64 degree
Output Swing	2V (differential)
Maximum Current	2.1 mA
Power dissipation	3.78 mW
Technology	0.18 um CMOS

Fig 7 shows the schematic of the fully differential folded-cascode OTA and the SC common-mode feedback (CMFB) circuit. The performance summary of the front-end OTA is presented in Table II. The load capacitances and the OTAs have been scaled down to minimize the power. The single-bit quantizer is implemented with a regenerative latch followed by an SR latch as in Fig 8. The comparator hysteresis is 7.9mV and the comparator offset is 3.8mV, which is less than 0.5LSB. The single-bit DAC is a simple switch network connected to reference voltages. The 4-bit quantizer from the second stage is implemented with a 4-bit flash A/D converter and the 4-bit D/A converter is implemented in a fully differential SC configuration as

shown in Fig 9. The sampling capacitances are combined with sixteen small unit capacitance to realize the 4-bit DAC. No DEM circuit is used because the behavioral simulations suggested that there are no distortions associated with the 4-bit DAC nonlinearity.

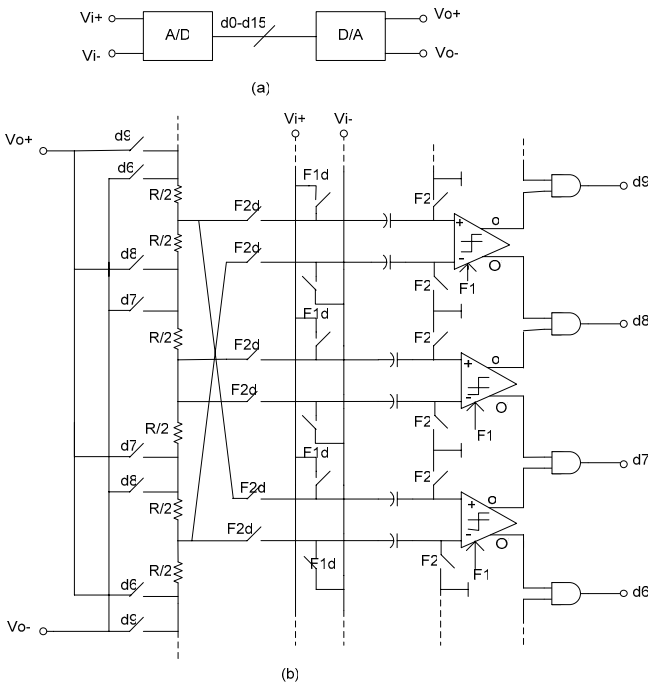


Figure 9. (a) Block diagram of A/D/A system (b) Partial view of its SC implementation

The performance summary of the modulator is shown in Table III. The overall performance demonstrates the efficiency of the proposed architecture for WLAN operation.

TABLE III. PERFORMANCE SUMMARY OF THE MODULATOR

Process Supply voltage	TSMC 0.18um CMOS (@1.8V)
Architecture	(2-2) modified cascaded ∑Δ modulator
Sampling frequency	160 MHz
Signal Bandwidth	10 MHz
OSR	8
DR	64 dB
Peak SNR	60 dB@-4dBFS
Peak SNDR	57dB@-6dBFS
Peak SFDR	66dB@-4dBFS
Estimated Power	42 mW

V. CONCLUSIONS

A highly linear sigma-delta ADC is proposed for WLAN applications. It employs a 2-2 modified cascaded architecture with a single bit in the first stage and 4 bit in the second stage to achieve a peak SNDR of 57dB over 10MHz signal bandwidth. The low-distortion topology has reduced sensitivity to OTAs nonlinearity effects and simplifies the implementation of cascaded architecture. The ∑-Δ modulator achieves a SFDR of 66 dB with 42mW power dissipation. The circuit-level simulation was carried out using TSMC 0.18um CMOS technology and operates at 1.8V supply voltage.

REFERENCES

[1] Horn R. and Demian P., "Cellular and WLAN Convergence", Wireless Broadband Forum, Cambridge, UK, 2002

[2] Xiaopeng Li and Mohammed Ismail, "Multi-standard CMOS Wireless Receivers: Analysis and Design", Kluwer Academic Publisher, 2002.

[3] Ana Rusu, Babita R. Jose, Mohammed Ismail and Hannu Tenhunen, "A Dual-Band Sigma-Delta Modulator for GSM/WCDMA Receivers" Proceedings of the International XIX Conference DCIS 2004, Bordeaux, France, Nov 2004, pp. 673-676.

[4] "Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications: Higher-Speed Physical Layer Extension in the 2.4GHz Band", IEEE Std 802.11b, Part 11, September 1999.

[5] A. Rusu, D. R. Gonzalez, M. Ismail and H. Tenhunen, "The Design of a Low-Distortion Sigma-Delta ADC for WLAN Standards", Proc. IEEE International Symposium on Signals,Circuits and Systems, pp. 511-514, July 2005.

[6] S. R. Norsworthy, R. Schreier and G. C. Temes, "Delta-Sigma Converters-Theory, Design and Simulation", IEEE Press, 1997.

[7] Jen-Shiun Chiang; Pao-Chu Chou; "Dual mode Sigma-Delta Modulator for Wideband Receiver Applications", Teng-Hung Chang; Circuits and Systems, ISCAS '03. Proceedings of the 2003 International Symposium on , Vol. 1 , 25-28 May 2003 Pages:I-997 - I-1000.

[8] J. Silva, U. Moon, J. Steensgaard, and G. C. Temes, "Wideband low-distortion delta-sigma ADC topology," *Electronics Letters,* vol. 37, no. 12, pp. 737-738, June 2001.

[9] Brigati, S., Francesconi, F., Malcovati, P., Tonietto, D., Baschirotto, A., and Maloberti, F., "Modeling sigma-delta modulator non-idealities in SIMULINK(R)", *Proc. IEEE International Symposium on Circuits and Systems 1999 (ISCAS99),* pp. 384-387, vol. 2

[10] P. Malcovati, et al, "Behavioral modeling of switched-capacitor sigma-delta modulators", IEEE Trans. Circuits Syst. II, vol.50, no. 3, 2003, pp. 352-364.