# Dual-Mode RNS based Programmable Decimation Filter for WCDMA and WLANa

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***Abstract*—The recent trends envisage multi-standard architectures as a promising solution for the future wireless transceivers. The computationally intensive decimation filter plays an important role in channel selection for multi-mode systems. An efficient reconfigurable implementation is a key to achieve low power consumption. To this end, this paper presents a dual-mode Residue Number System (RNS) based decimation filter which can be programmed for WCDMA and 802.11a standards. Decimation is done using multistage, multirate finite impulse response (FIR) filters. These FIR filters implemented in RNS domain offers high speed because of its carry free operation on smaller residues in parallel channels. Also, the FIR filters exhibit programmability to a selected standard by reconfiguring the hardware architecture. The total area is increased only by 33% to include WLANa compared to a single mode WCDMA transceiver. In each mode, the unused parts of the overall architecture is powered down and bypassed to attain power saving. The performance of the proposed decimation filter in terms of critical path delay and area are tabulated.**

## I. INTRODUCTION

The demand for new telecommunication services requiring higher capacities, data rates and different operating modes have motivated the development of new generation multi-standard wireless transceivers. The adaptability to different communication standards is achieved by performing channel select filtering on chip at baseband [1]. The baseband channel select filtering is performed in digital domain. This allows programmability to adapt to the channel bandwidths, sampling rates, carrier to noise (C/N) ratio, and blocking and interference profiles needed for multiple communication standards [2]. The analog to digital conversion is performed by sigma-delta analog to digital converter (SD-ADC) because of its wide dynamic range and high in-band signal to noise ratio (SNR). The SD-ADC consists of a sigma-delta modulator followed by a decimation filter. Sigma-delta modulator is based on over-sampling technique, and it shifts the noise into high frequency band while keeping the signal to noise ratio (SNR) high in the signal band. The digital decimation filter removes the out-of-band quantization noise produced by the modulator. Also, it reduces the sampling rate from over-sampled frequency of the modulator to the Nyquist rate of the channel [3]. A programmable decimation filter is required in multi-mode transceiver as the channel bandwidth, sampling rates and interference profile are different for each standard.

Several papers are available in literature that deals decimation filters for multi-mode wireless communication transceivers. A fifth order non-recursive comb decimation filter with programmable decimation ratios and sampling rates for GSM and DECT standards is presented in [4]. The design and implementation of digital filter processors that can be used as down-samplers in wireless transceivers is detailed in [5]. Decimation filter design for GSM, WCDMA, 802.11a, 802.11b, 802.11g and WiMAX standards are given in [6]. A decimation filter structure based on cascaded integrator comb (CIC) filters and polynomial interpolation filters to perform fractional sample rate conversion is presented in [7]. A digital IF down-converter with quadrature sampling based on polyphase filter, high rate CIC filter and interpolation filters, and compatible with WCDMA and EDGE is demonstrated in [8]. Multi-rate digital filters and fractional frequency conversion techniques are adopted to implement the front end of a dual-mode receiver for WCDMA/cdma2000 in [9]. A fast RNS field programmable logic (FPL) based communication receiver design and implementation is presented in [10].

The principle contribution of this paper is the design and implementation of a programmable RNS based decimation filter for dual-mode WCDMA and WLANa receiver. This technique fundamentally differs from the implementation proposed by [10] in two critical issues. Firstly, this technique addresses the problem of multi-standard decimation filtering. Secondly, and more importantly, since the implementation is multi-rate, the subsequent filters operate at lower sampling rates. Thus it reduces power consumption compared to the single stage implementation given in [10]. Furthermore, in the proposed architecture as the front end is a sigma-delta ADC, the forward converter which takes around 10% area of traditional RNS filter, is eliminated by suitably selecting the moduli set. The rest of the paper is organized as follows: Section II deals with the RNS basics and general RNS FIR filter architecture. Section III describes the receiver architecture and sigma-delta modulator suitable for multi-

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standard operation. Section IV presents the RNS based programmable multistage decimation filter structure with design specification for WCDMA/WLANa standards. Section V demonstrates the simulation results obtained for dual-mode decimation filter. The area requirement and critical path delay are tabulated, and is compared with the traditional FIR filter implementation. Finally, Section VI gives the conclusion.

## II. Background on RNS FIR Filters

RNS is a non-weighted number system defined by a set of 'r' relatively prime integers ($m_1$, $m_2 \ldots m_r$) called the moduli. Any integer 'X' in the interval of [0, M) can be represented as a set of 'r' residues ($x_1$, $x_2 \ldots x_r$), where $x_i = X \bmod m_i$ and $M = \prod_{i=1}^{r} m_i$. 'M' is defined as the dynamic range of the number system. In RNS, arithmetic operations are computed by the formula:

$$(x_1, x_2, ..., x_r) \Theta (y_1, y_2, ..., y_r) = (z_1, z_2, ..., z_r) \quad (1)$$

where $z_i = |x_i \Theta y_i|_{m_i}$ and $\Theta$ denotes one of the operations of addition, subtraction or multiplication. Thus arithmetic operations on residues can be performed in parallel without any carry propagation among the residue digits [11]. The process of translating a binary integer X to residue representation with respect to relatively prime moduli set is called forward conversion, and the reverse process is called reverse conversion. The reverse conversion can be done using Chinese Remainder Theorem (CRT) based on the formula:

$$X = \left| \sum_{i=1}^{r} a_i x_i \hat{M}_i \right|_M, \text{ where } \hat{M}_i = \frac{M}{m_i} \text{ and } a_i = \left| \frac{1}{\hat{M}_i} \right|_{m_i} \quad (2)$$

In RNS a large integer is broken into smaller residues which are independent of each other, and each digit is processed in parallel channels without carry propagation from one to another. This leads to significant speed up of multiply and accumulate (MAC) operations which in turn results in high data rate for RNS based FIR filters [12]. Fig. 1 shows the general block diagram of RNS based FIR filter. For the moduli set ($m_1$, $m_2 \ldots m_r$), there will be 'r' parallel filter channels, which process the signals from the forward converter. The forward converter is shown in dotted lines as it is not used in the proposed design. Finally, reverse converter combines the signals from all channels and puts the output signal back in binary form.

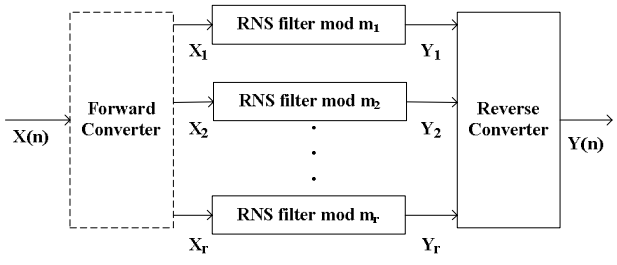


Figure 1. RNS based FIR filter

## III. Receiver Architecture for Multi-standard Operation

The direct conversion homodyne receiver architecture shown in Fig. 2 is suitable for high integration and multi-standard operation [2]. This is multi-standard capable because channel select filtering is done at baseband. The noise and DC offset created at the output of the mixer are to be reduced to achieve adequate dynamic range. A wideband high dynamic range sigma-delta ($\sum\Delta$) modulator is used to digitize both the desired signal and potentially stronger adjacent channel interferers. A highly linear $\sum\Delta$ modulator for multi-standard operation that can achieve high resolution over a wide variety of bandwidth requirements remains challenging. A reconfigurable ADC [13, 14] is a promising solution to keep the power dissipation as low as possible.

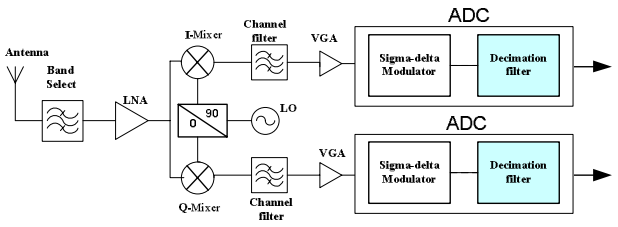


Figure 2. Direct conversion homodyne receiver architecture

MASH (multistage noise shaping) structures can be adopted for $\sum\Delta$ modulator considering the stability and reconfigurability. The theoretical dynamic range has been used in conjunction with the implementation attributes to choose the optimal topology for different RF standards. The dynamic range, DR of a $\sum\Delta$ modulator is given by

$$DR = \frac{3}{2} \frac{2L+1}{\pi^{2L}} M^{2L+1} (2^B - 1)^2 \quad (3)$$

where $L$ is the order of the modulator, $M$ is the over-sampling ratio (OSR), and $B$ is the number of bits of the quantizer. For WCDMA and WLANa the dynamic range requirements are chosen as 79dB and 69dB respectively. In order to meet the DR requirements demanded by WCDMA, a fourth order cascaded MASH topology is sufficient with a single-bit quantizer and an OSR of 16. A fifth order topology is a good compromise to achieve the required DR for WLANa, with a 4-bit quantizer and an OSR of 8. Sigma-delta modulator is followed by a programmable decimation filter operating in the digital domain. The proposed work focuses on the design of programmable multistage decimation filter for WCDMA/WLANa standards, which is highlighted in Fig. 2.

## IV. Programmable RNS Decimation Filter Design

The specifications for WCDMA and WLANa standards and the corresponding decimation filter design parameters are given in Table 1. In order to set the parameters for decimation filter, the receiver specifications and the blocking and interference profiles are defined first. The interference signals are to be limited within a certain range for proper reception of the desired signals. The decimation filter is generally designed to minimize the undesired signals in the desired band of operation. The output carrier to noise (C/N) ratio is calculated

from the bit error rate (BER) of each standard and the modulation scheme used. The passband frequency edge is taken as 80% of the bandwidth. The passband ripples are chosen to minimize signal distortions in the signal band. The stopband attenuations are selected according to the interference profile and C/N ratio for each standard.

TABLE I. STANDARD SPECIFICATIONS AND DECIMATION FILTER DESIGN PARAMETERS

| Specification | WCDMA | WLANa |
|---|---|---|
| Frequency range(GHz) | DL:2.11-2.17<br>UL:1.92-1.98 | 5.15-5.35 |
| Channel Spacing | 5 MHz | 20 MHz |
| Data rate | 3.84 Mchips/s | 12 Msymbols/s |
| OSR | 16 | 8 |
| Input sampling frequency, $F_s$ | 61.44 MHz | 96 MHz |
| Passband edge | 2 MHz | 8 MHz |
| Stopband edge | 2.5 MHz | 10 MHz |
| Offset frequency (MHz) :<br>Interference<br>magnitude(dBm) | 5 : -63<br>10 : -56<br>12.5:-44 | 20 : -63<br>40 : -47 |
| C/N ratio | 7.2 dB | 28 dB |
| Passband ripple | 0.5 dB | 0.5 dB |
| Stopband attenuation | 55 dB | 44 dB |

The decimation filter consists of a lowpass filter and a down-sampler. Implementing decimation filter in several stages reduces hardware complexity and computational effort. To prevent aliasing in the overall decimation process, the individual filter of each stage is to be designed within the frequency band of interest. The cutoff frequency for the first stage can be less constraining whereas the final stage filter operating at lower sampling rate is responsible for attaining the overall filter specifications. For stage '*i*', passband is from $0 \le F \le F_{pc}$, where $F_{pc}$ is the passband edge. If $F_{i-1}$ and $F_i$ are the input and output sampling frequencies for stage '*i*', and $F_{sc}$ is the stopband edge, transition band for stage '*i*' is from $F_{pc} \le F \le F_i - F_{sc}$ and stopband is from $(F_i - F_{sc}) \le F \le (F_{i-1}/2)$.

The OSR is 16 for WCDMA and 8 for WLANa. Decimation is done in 3 stages with decimation factors of 4, 2 and 2 for WCDMA, and in 2 stages with decimation factors of 4 and 2 for WLANa. Remez Parks-McClellan optimal equiripple FIR filter is chosen for implementation. The filter orders obtained for WCDMA are 14, 11 and 37 for first, second and third stages respectively. For WLANa filter orders are 33 and 25 respectively. The block diagram for the programmable decimation filter is shown in Fig. 3, where N1, N2 and N3 denote the order of filters in each mode. The third filter will be operating only in WCDMA mode and will be bypassed in WLAN mode using switch S. The switch can be a transmission gate. The first 14 multiply and accumulate (MAC) units of first stage filter and first 11 MAC units of the second stage are shared for both modes. The unused hardware in each mode are bypassed to get power saving.

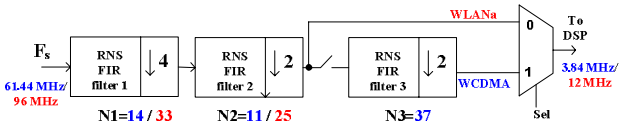


Figure 3. Programmable decimation filter for WCDMA/WiMAX

The moduli set selected for implementation of all the three filters is (25, 29, 31, 37, 43, 47, 59, 64), which provides 43 bit dynamic range. The filter coefficients are taken with 14 bit accuracy. As input to the filter has maximum of 4-bits and the moduli set consists of 5-bit and 6-bit numbers, no forward converter is required in the proposed filter. The reverse converter at the last stage converts filtered outputs from parallel channels to binary form. A filter channel corresponding to modulus '$m_i$' of the first stage is shown in Fig. 4, where $\otimes$ and $\oplus$ represent modulo multiplication and addition respectively. Modulo multiplication is implemented with look up table (LUT). The LUT contents can be easily reprogrammed as the mode changes, by implementing the LUTs in FPGA RAM blocks.

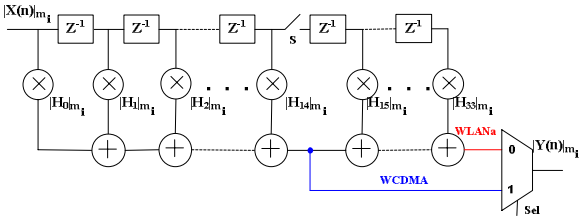


Figure 4. $i^{th}$ filter channel of stage 1

## V. SIMULATION RESULTS AND PERFORMANCE ANALYSIS

The input sampling frequency is 61.44 MHz for WCDMA and is down-sampled to the data rate of 3.84 Mchips/s in three stages. The cascaded two stage filter structure down-samples input sampling frequency of 96 MHz for WLANa to the data rate of 12 Msymbols/s. The overall decimation filter responses obtained for WCDMA and WLANa, satisfying the standard specifications, are shown in Fig. 5 and Fig. 6 respectively.

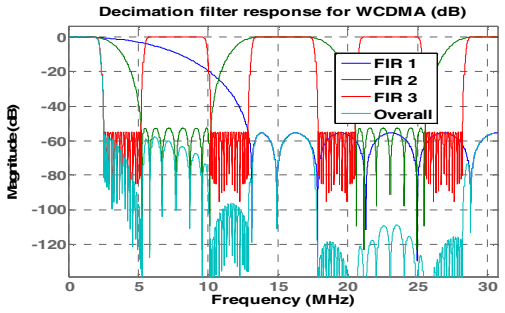


Figure 5. Decimation filter response for WCDMA

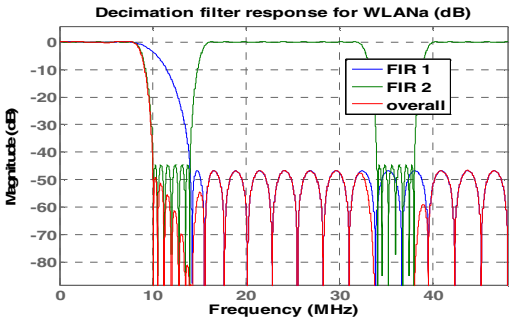


Figure 6. Decimation filter response for WLANa

The hardware synthesis is done with *Leonardo Spectrum* logic synthesis tool from Mentor Graphics. In order to operate first stage filter at 96 MHz, pipelining is done after every three modulo adders to meet the critical path delay. Two stage pipelining is done to meet the critical path delay for second filter which operates at maximum frequency of 24 MHz. The third stage is used only for WCDMA mode at a frequency of 7.68 MHz and no pipelining is required. The total area requirement and critical path delay of each block of the decimation filter is shown in Table II. The critical path delay and area for each block of the filter is normalized with respect to a full adder critical path delay of 0.45 ns and area of 38$\mu m^2$. The area requirement of the decimation filter in single mode WCDMA receiver and the additional area required for making it adaptable for dual-mode operation are given in Table III. It is observed that programmability is achieved at the expense of 33% of additional area compared to single mode WCDMA receiver. Table IV reports the characteristics of decimation filter implemented in traditional number system performing signed multiplication and addition. RNS filter implementation offers about 60% saving in area. Pipelining done as in the RNS filter will not meet the critical path delay for traditional case. Here pipelining is to be done in the multipliers as well as in the adder chain.

TABLE II. AREA AND CRITICAL PATH DELAY FOR RNS DECIMATION FILTER

| Block | Area | Percentage area of each block (%) | Critical path delay |
|---|---|---|---|
| Filter 1 | 5240.13 | 32.9 | 21.88 |
| Filter 2 | 3981.09 | 24.96 | 87.33 |
| Filter 3 | 5840.18 | 36.63 | 244.29 |
| Multiplexers | 29.47 | 0.002 | 0.69 |
| Reverse converter | 852.82 | 5.4 | 79.12 |
| Total area | 15943.69 | 100 | |

TABLE III. AREA REQUIREMENT FOR PROGRAMMABILITY

| Type of transceiver | | Area | Percentage area (%) |
|---|---|---|---|
| Single mode WCDMA | Filter 1 | 2220.44 | 66.9 |
| | Filter 2 | 1748.3 | |
| | Filter 3 | 5840.18 | |
| | Reverse converter | 852.82 | |
| | Total | 10661.74 | |
| Dual-mode Transceiver | | 15943.69 | 100 |
| Additional area for programmability | | 5281.95 | 33.1 |

TABLE IV. AREA REQUIREMENT: TRADITIONAL VS RNS

| Block | | Area |
|---|---|---|
| Traditional | Filter 1 | 3940.89 |
| | Filter 2 | 11074.45 |
| | Filter 3 | 25762.62 |
| | Total | 40777.96 |
| RNS | | 15943.69 |

## VI. CONCLUSION

A dual-mode RNS based decimation filter that meets the performance requirements of WCDMA and WLANa standards, is presented in this paper. The forward converter is eliminated in the proposed filter by suitably selecting the moduli set. Multistage implementation for sampling rate conversion results in reduced hardware complexity and power consumption. Powering down or bypassing of the unused hardware in each mode of operation leads to further power saving. As all the filter stages are implemented in RNS and are operating with the same moduli set, a reverse converter is needed only at the last stage output. The performance comparison shows that 60% of area saving is achieved with the proposed RNS implementation compared to a traditional FIR filter implementation. The programmability for dual-mode architecture which could handle both WCDMA and WLANa, is achieved with an increase in total area only by 33%, compared to that for single mode WCDMA transceiver.

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