Fault Tolerant Error Coding and Detection using Reversible Gates

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Abstract - **In recent years, reversible logic has emerged as one of the most important approaches for power optimization with its application in low power CMOS, quantum computing and nanotechnology. Low power circuits implemented using reversible logic that provides single error correction – double error detection (SEC-DED) is proposed in this paper. The design is done using a new 4 x 4 reversible gate called 'HCG' for implementing hamming error coding and detection circuits. A parity preserving HCG (PPHCG) that preserves the input parity at the output bits is used for achieving fault tolerance for the hamming error coding and detection circuits.**

Keywords: fault tolerance, reversible logic, hamming code, low power designs

I. INTRODUCTION

Error correcting codes are traditionally used to battle the corruption of transmitted data by channel noise. The encoded data, or code words, are sent through the channel and decoded at the receiving end. During decoding the errors are detected and corrected if the amount of error is within the allowed, correctable, range. This range depends on the extra information, parity bits, added during encoding. Single-error-correcting and double-error-detecting (SEC-DED) codes are generally used for this purpose. There are many ways to construct SEC-DED codes, and one of the most commonly used code is the Hamming Code.

As power has become a first-order design consideration, researchers have begun looking at techniques to reduce power consumption in error coding and detection circuitry. Energy loss during computation is an important consideration in low power digital design. Landauer's principle states that a heat equivalent to kT*ln2 is generated for every bit of information lost, where 'k' is the Boltzmann's constant and 'T' is the temperature [1]. At room temperature T, though the amount of heat generated may be less it cannot be neglected for low power designs. The amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Bennett showed that energy dissipation would not occur if the computations were carried out using reversible circuits [2] since these circuits do not lose information. Neither feedback nor fan-out is allowed in reversible circuits. Classical logic gates such as AND, OR and XOR are not reversible. Hence, these gates dissipate heat and may reduce the life of the circuit. So, reversible logic is in demand in power aware circuits. In recent years, reversible logic has emerged as one of the most important approaches for power optimization with its application in low power CMOS, nanotechnology and quantum computing.

One of the main constraints in reversible logic is to minimize the number of reversible gates used and number of unutilized outputs called "garbage" produced. Garbage output refers to the output that is not used for further computations. In other words, it is not used as a primary output or as an input to another gate. As the number of inputs and outputs are made equal there may be a number of garbage outputs produced in certain reversible implementations. In literature, there are a number of existing reversible gates such as Fredkin gate [3], Toffoli Gate [4], Feynman Gate [5], Feynman Double Gate [6] etc. In this paper, a new reversible 4 x 4 HC gate (HCG) is proposed for implementing hamming error coding and detection circuits.

Parity checking is one of the oldest, as well as one of the most widely used methods for error detection in digital systems. Detection of faults generated in a circuit can be done by using parity-preserving reversible logic gates. The feasibility of the parity-preserving approach in the design of reversible logic circuits was demonstrated by B. Parhami [6] with examples of adder circuits. In this research, a modified HCG in which the parity of the outputs matches with that of the inputs is proposed. This can be used along with other parity preserving reversible logic gates to generate the parity preserved / fault tolerant hamming code. Parity preserving characteristic of such gates allows the detection of single fault generated in the circuit at the circuit's primary outputs in reversible logic design.

The organization of this paper is as follows: The necessary background on reversible logic gates used for the current implementation is discussed initially. Then 'HC gate' (HCG) is proposed, and (7, 4) Hamming code generator is implemented using this gate without any garbage outputs. The design is chosen in such a way to reduce the number of gates, number of levels (delay) and number of garbage outputs to a minimum. A fault detection method for hamming code generator circuit based on parity-preserving reversible logic gates is introduced. The fault tolerant reversible hamming code generator implemented using such gates allow detection of single fault caused in the circuit. The design is then extended for the implementation of Hamming code error detector. Finally, a comparison in terms of number of reversible gates, garbage outputs and number of levels (delay) is done for all types of implementations.

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II. REVERSIBLE LOGIC GATES

This section gives the necessary background on reversible logic gates used for the current implementation.

A. Feynman Gate

Figure 1 shows a Feynman Gate (FG) [5]. Feynman Gate can be used as a copying gate. Since a fan-out greater than one is not allowed, this gate is useful for duplication of the required outputs. If B='0', then P=A and Q=A. But FG is not a parity preserving gate.

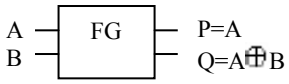

Figure1. 2 x 2 Feynman Gate (FG)

B. Feynman Double Gate

Figure 2 shows a Feynman Double Gate [6]. Feynman Double Gate (F2G) can also be used as a copying gate. If B='0' and C='0' then P=A, Q=A and R=A. Since A⊕B⊕C = P⊕Q⊕R, F2G is a parity preserving gate, and is suitable for fault tolerant implementations.

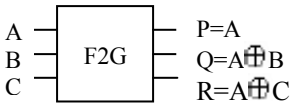

Figure 2. 3 x 3 Feynman Double Gate (F2G)

III. PROPOSED REVERSIBLE GATES

A. 4 x 4 Reversible HC Gate

In this paper, a 4 x 4 reversible gate called HC gate (HCG) is proposed, and is shown in Figure 3. Table I shows the corresponding truth table.

TABLE 1. TRUTH TABLE OF THE 4 x 4 HCG

Inputs				Outputs			
A	**B**	**C**	**D**	**P**	**Q**	**R**	**S**
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	1
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	1	1	1	0
0	1	0	1	1	1	0	1
0	1	1	0	1	0	1	1
0	1	1	1	1	0	0	0
1	0	0	0	0	1	1	1
1	0	0	1	0	1	0	0
1	0	1	0	0	0	1	0
1	0	1	1	0	0	0	1
1	1	0	0	1	0	0	1
1	1	0	1	1	0	1	0
1	1	1	0	1	1	0	0
1	1	1	1	1	1	1	1

It is obvious from the truth table that the input pattern corresponding to a particular output pattern can be uniquely determined.

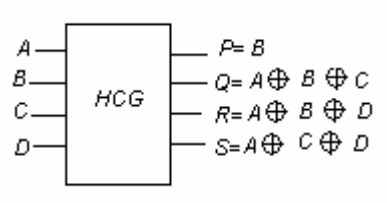

Figure 3. Reversible 4 x 4 HCG

B. 4 x 4 Reversible PPHC Gate

The proposed reversible Parity Preserving HC gate (PPHCG) is shown in Figure 4. Table 2 shows the corresponding truth table. It can be verified from the truth table that the outputs preserve the input parity.

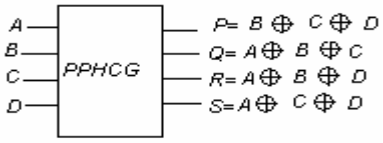

Figure 4. Reversible 4 x 4 PPHC

TABLE 2. TRUTH TABLE OF THE PROPOSED PPHC GATE

Inputs				Outputs			
A	**B**	**C**	**D**	**P**	**Q**	**R**	**S**
0	0	0	0	0	0	0	0
0	0	0	1	1	0	1	1
0	0	1	0	1	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	1	1	1	0
0	1	0	1	0	1	0	1
0	1	1	0	0	0	1	1
0	1	1	1	1	0	0	0
1	0	0	0	0	1	1	1
1	0	0	1	1	1	0	0
1	0	1	0	1	0	1	0
1	0	1	1	0	0	0	1
1	1	0	0	1	0	0	1
1	1	0	1	0	0	1	0
1	1	1	0	0	1	0	0
1	1	1	1	1	1	1	1

IV. REVERSIBLE HAMMING CODE GENERATOR

One of the most commonly used code to perform Single Error Correction - Double Error Detection (SEC-DED) is the Hamming Code. The key to the Hamming Code is the use of extra bits to allow the identification of a single error or detection of double errors. The use of simple parity allows detection of single bit errors in a received message. Correction of such errors requires more information, since the position of the bad bit must be identified if it is to be corrected. Consider a message having four data bits (D_{3-0}) which is to be transmitted as a 7-bit codeword by adding

three error check bits. This would be called a (7, 4) code. The three bits to be added are three even parity bits (P), where the parity bit is computed on different subsets of the message bits using equations (1-3).

$$P_1 = D_0 \oplus D_1 \oplus D_3 \quad (1)$$
$$P_2 = D_0 \oplus D_2 \oplus D_3 \quad (2)$$
$$P_3 = D_1 \oplus D_2 \oplus D_3 \quad (3)$$

To illustrate the application of proposed HCG a (7, 4) bit hamming code generator is designed. Figure 5 shows (7, 4) hamming code generator designed using 4 x 4 HCG and three FGs. It is seen that the circuit requires 4 gates at 2 levels and generates the 7-bit hamming code (H_7 to H_1) without any garbage outputs.

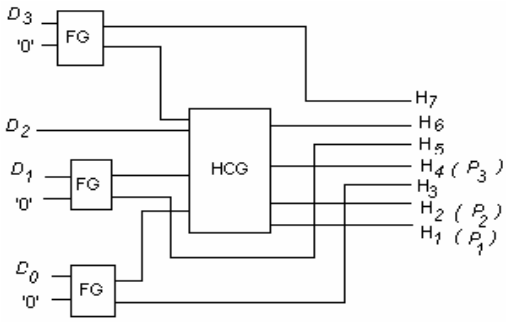

Figure 5. Reversible (7, 4) Hamming code generator using HCG

The reversible hamming code generator designed using F2G and FG gates is shown in Figure 6. On comparing the two implementations it is evident that the implementation using F2G and FG requires 6 reversible gates at 4 levels while the implementation using HCG and FG requires only 4 gates at 2 levels. However both implementations attain minimum number of garbage outputs. The types of gates used in these two implementations are not parity preserving gates except for F2G and hence are not fault tolerant implementations.

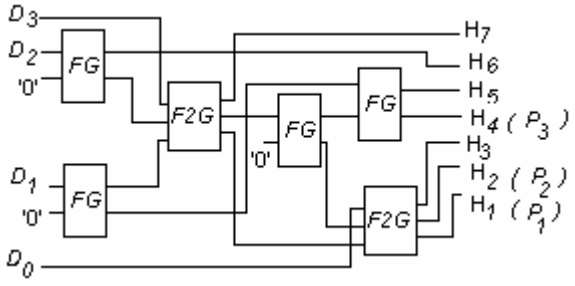

Figure 6. Reversible (7, 4) Hamming code generator using F2G

V. PARITY PRESERVING REVERSIBLE HAMMING CODE GENERATOR

Figure 7 shows the implementation of reversible hamming code generator designed using parity preserving gates. The implementation makes use of 5 gates at 2 levels and produces 5 garbage outputs. The input and output parity will be the same, since the design is done using parity preserving gates. At each level a single fault can be detected by checking the parity of the inputs and outputs.

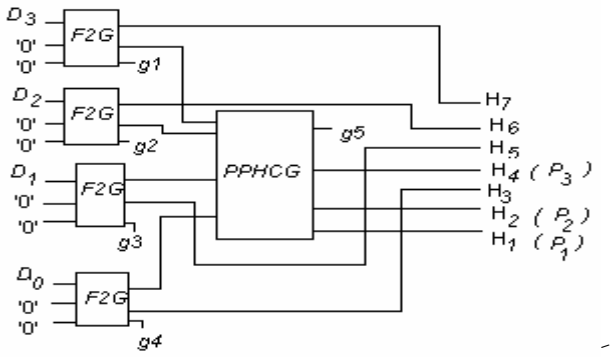

Figure 7. (7, 4) Reversible Hamming Code Generator using parity preserving gates

The design makes use of 2 types of reversible gates. VLSI implementations using only one type of modular building blocks can decrease system design and manufacturing cost. For achieving a VLSI implementation, circuits using only one type of reversible gate as the basic building block can be adopted. Figure 8 shows the implementation using six F2Gs at 4 levels with 4 garbage outputs. The implementation uses a single type of reversible gate and produces less number of garbage outputs. But this results in increased delay and makes use of more number of gates.

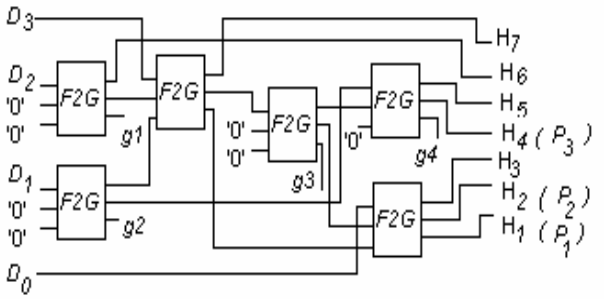

Figure 8. (7, 4) Reversible Hamming Code Generator using F2G

VI. REVERSIBLE HAMMING CODE ERROR DETECTOR

Figure 9 shows the (7, 4) hamming code error detector designed using 4 x 4 HCG and three FGs. It is seen that the circuit requires 4 gates at 2 levels and generates the check bits (C_3 to C_1) with 4 garbage outputs. Check bits are computed on different subsets of the hamming code bits using the equations (4 - 6).

$$C_1 = H_1 \oplus H_3 \oplus H_5 \oplus H_7 \quad (4)$$
$$C_2 = H_2 \oplus H_3 \oplus H_6 \oplus H_7 \quad (5)$$
$$C_3 = H_4 \oplus H_5 \oplus H_6 \oplus H_7 \quad (6)$$

If all the check bits are zeros it indicates a 'no error condition', otherwise it indicates the position of error. This implementation is not done using parity preserving gates and hence is not capable of detecting any fault in the circuit.

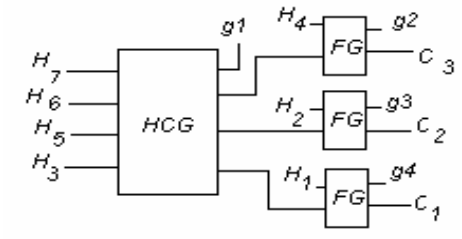

Figure 9. Reversible (7, 4) Hamming code error detector using HCG

Figure 10 shows the implementation of reversible hamming code error detector designed using parity preserving gates. The implementation makes use of 5 gates at 3 levels and produces 6 garbage outputs. The advantage of this implementation is the use of only one type of reversible gate, but it results in increased delay and makes use of more number of gates. Since the implementation uses only one type of reversible gate, the design is more suitable for VLSI circuits.

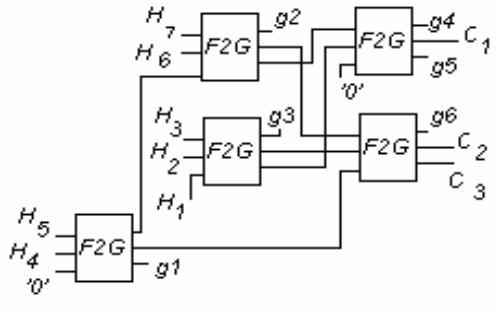

Figure 10. Reversible (7, 4) Hamming code error detector using F2G

Table 3 shows the comparisons between different implementations of hamming error coding and detection circuits in terms of number of gates, garbage outputs and levels.

VII. CONCLUSION AND FUTURE WORK

Different implementations for the reversible (7, 4) hamming error coding and detection circuits are presented. It is demonstrated that the design using 4 x 4 HCG is highly optimized in terms of number of reversible gates and/or garbage outputs. The design strategy is chosen in such a way to reduce the most important factor of the reversible circuit cost - the number of garbage outputs along with number of reversible gates and delay. This approach also provides a way of incorporating fault tolerance into reversible circuits without much extra design effort and with modest hardware overhead. It is hoped that parity preservation by itself proves useful for ensuring the robustness of reversible logic circuits in their various application domains. The fault tolerant reversible hamming code circuits implemented using parity preserving gates allow detection of single fault caused in the circuit also.

In this research, the elements of a known traditional logic implementation for an Error Correcting Code, (hamming code) coding and detection circuits were replaced with reversible equivalents. Further investigation into determining alternate implementations can be done using logic synthesis methods [7, 8, 9, 10]. Additionally, it was noted that there is a lack of simulation tools that support reversible gates, and this is most definitely an area worthy of attention. The major challenges that remain are the development of hardware and software tools for reversible logic.

TABLE 3. COMPARISON OF REVERSIBLE HAMMING ERROR CODING AND DETECTION CIRCUITS

Reversible 7-bit Hamming Code circuit	**No. of reversible gates**	**No. of Garbage outputs**	**No. of levels**
HC generator using HCG and FG	4	NIL	2
HC generator using F2G and FG	6	NIL	4
Parity preserving HC Generator using PPHC gate	5	5	2
Parity preserving HC Generator using F2G	6	4	4
HC error detector using HCG and FG	4	4	2
Parity preserving HC error detector using F2G	5	6	3

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