MULTICHANNEL REMOTE DATA ACQUISITION AND ANALYSING SYSTEMS

FOR FISHERIES / ENVIRONMENTAL INVESTIGATIONS

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By

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CERTIFICATE

This is to certify that this thesis entitled **"MULTICHANNEL REMOTE DATA ACQUISITION AND ANALYSING SYSTEMS FOR FISHERIES/ENVIRONMENTAL INVESTIGATIONS"** is a bonafide record of the project work done by Shri K.Ramakrishnan, at the Department of Electronics, Cochin University of Science and Technology and the same has been approved for the fulfilment of the award of the degree of Master of Technology in Electronics of the Cochin University of Science and Technology.

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CONTENTS

ABSTRACT

Remote Data acquisition and analysing systems developed for fisheries and related environmental studies have been reported. It consists of three units. The first one namely multichannel remote data acquisition system is installed at the remote place powered by a rechargeable battery. It acquires and stores the 16 channel environmental data on a battery backed up RAM. The second unit called the Field data analyser is used for insitue display and analysis of the data stored in the backed up RAM. The third unit namely Laboratory data analyser is an IBM compatible PC based unit for detailed analysis and interpretation of the data after bringing the RAM unit to the laboratory. The data collected using the system has been analysed and presented in the form of a graph. The system timer operated at negligibly low current, switches on the power to the entire remote operated system at prefixed time interval of 2 hours.

Data storage at remote site on low power battery backed upRAM and retrieval and analysis of data using PC are the speciality of the system. The remote operated system

takes about 7 seconds including the 5 second stabilization time to acquire and store data and is very ideal for remote operation on rechargeable battery. The system can store 16 channel data scanned at 2 hour interval for 10 days on 2K backed upRAM with memory expansion facility for 8K RAM.

chapter 1

INTRODUCTION

Remote data acquisition systems are required for collection and analysis of data in connection with various investigations related to fisheries, agriculture meteorology water resources management, natural energy resources, forestry and other environmental fields. A good number of scientists and technologists are working on various problems related to the above fields. These studies are associated with cultivation and harvesting of crops, animal-food production including fisheries, national planning and management of natural energy resources and forecasting for the future. Since such studies are field oriented, sample collection and laboratory based parameter estimation is resorted to in many cases. Electronic instruments have eased some of the problems of data collection in these areas and even modified the methodology used for data collection. Since these instruments are often field operated, the chances of failure are more. The problem is more severe in the case of imported instruments, because of lack of spare parts and adequate maintenance in time.

Indigenous instrumentation is the best solution to such problems and have been tried in some of these

fields. But the integrated systems for collection and analysis of required data is lacking in many fields.

Data acquisition methods can broadly be classified into two. (1) Remote sensing and (2) Ground based measurement.

Remote sensing has been used in geology, meteorology and oceanography and it can cover very large areas in short span of time. But this method does not contain such minute details required for many microlevel studies being carried out in most of the environmental fields. Hence ground based measurements are carried out in most of the cases. These are also used for correlating the results obtained from remote sensing methods for standardisation purposes.

PC based data acquisition systems have been extensively used in the process industry for measurement, analysis and control of various parameters in the production plants. Such systems cannot directly be employed in most of the environmental studies because the sites of measurement are too remote for installation and maintenance

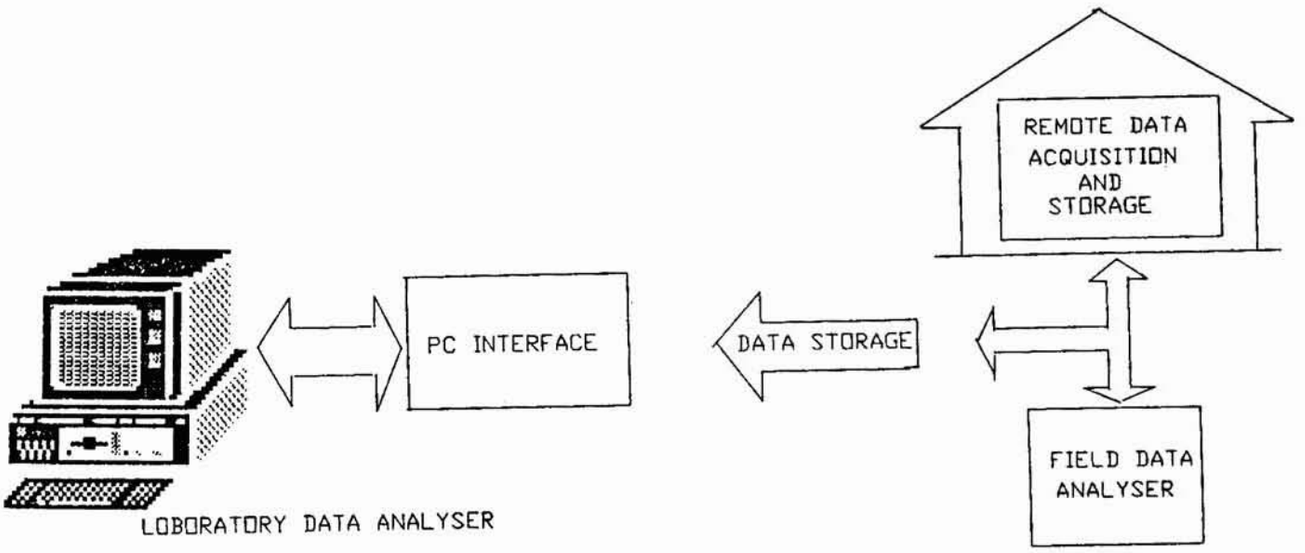


FIG. 1.1 BLOCK SCHEMATIC OF THE SYSTEMS

of such systems. But the intelligentsia and programmability associated with microprocessors can be judiciously combined for development of microprocessor based data acquisition systems required for many of these cases. One such attempt is made in this project.

This project report presents the hardware design and implementation of multichannel remote data acquisition and analysing systems for fisheries/environmental investigations. Fig.1.1 shows the block schematic of the systems.

The systems consist of three component units namely:

1. Remote data acquisition and storage.

2. Field data analyser.

3. Laboratory data analyser based on IBM compatible PC.

The remote data acquisition system and storage acquires an 8 bit data related to 16 environmental parameters and stores them on a battery backed up RAM, at a time interval of 2 hours. Field data analyser is used for on site analysis of the data stored in the remote storage

unit. The laboratory data analyser is designed for detailed analysis of the data acquired using an IBM compatible PC by bringing the storage unit to the laboratory after storing data for 10 days.

Chapters 2, 3 and 4 of this report gives detailed description of the above component systems developed.

Chapter 2 briefly describes the environmental parameters being measured, the sensors used for such measurements, the analogue to digital converter and the data storage used. The acquisition system as well as the software developed and the details of the development system used are also described here.

Chapter 3 deals with the hardware and software details of the field data analyser.

Chapter 4 explains the interfaces developed for data retrieval from the remote storage unit and the software developed for analysis of data in the laboratory using PC.

chapter 2

REMOTE DATA ACQUISITION AND STORAGE

This subsystem is operated at the remote place powered by a rechargeable battery. This can be housed in a shelter with proper arrangements. Transducers, associated signal conditioners and instrumentation amplifiers feed the analogue voltage to this unit. These transducers are installed at different locations and connected to the processing unit. Channel multiplexing, digitizing and storage on battery backed up RAM are done here. The system timer switches on the power to the entire system at prefixed time interval. At power on the system waits for about 5 seconds for the analogue voltages to get stabilized and then acquires data from different channels. It terminates storage operation on reaching the programed maximum limit of data storage memory. Different parts of this system are given below.

2.1 Transducers

Different types of transducers are commercially available for measurement of environmental parameters. The generally measured environmental parameters with respect to fisheries investigations are given below. The required measurement range of these parameters and the principle of operation of the sensors used are also given.

1. Water temperature

   Range :15°C to 40°C with an accuracy of ± 0.1°C.

   Sensor:P N junction semiconductor or thermistor properly encased.

2. Air temperature

   Range : 20°C to 45°C with an accuracy of ± 0.1°C.

   Sensor: P N junction semiconductor or thermistor properly encased.

3. Water salinity

   Range : 15 PPT to 40 PPT with an accuracy of ±0.1 PPT.

   Sensor: Platinum conductivity cell.

4. Under water solar radiation

   Range : 0 to 500 watts/m^2 with an accuracy of ±5 watts/m^2.

   Sensor: Photosensor using photodiode with suitable encasing.

5. Atmospheric solar radiation

   Range : 0 to 1400 watts/m^2 with an accuracy of ±5 watts/m^2.

   Sensor: Photosensor using photodiode with proper encasing.

6. Water level

Range : 0.5 M to 3 M with an accuracy of ±0.1 M.

Sensor: Hydrostatic pressure acting on an inductive pressure sensor.

7. Turbidity

Range : 0 to 1000 JTU with an accuracy of ± 1%.

Sensor: Opto— electric pick up.

8. Sedimentation

Range : 0 to 500 gms with an accuracy of ± 5 gms.

Sensor: Inductive weight sensor for sediments settled.

9. pH

Range : 5 pH to 9 pH with an accuracy of ± 0.1 pH.

Sensor: Potential developed between electrodes immersed in the liquid due to the presence of hydrogen ions.

10. Dissolved oxygen

Range : 2 to 8 mg/litre with an accuracy of ± 0.1 mg.

Sensor: Potential developed between working electrode and reference electrode due to the presence of oxygen.

11. Water current

Range : 0 to 400 cm/sec with an accuracy of ± 5 cm/sec.

Sensor: Rotor, based on inductive or opto-electric pick up.

12. Water current direction

Range : 0° to 360° with an accuracy of ± 1°.

Sensor: Potentiometric measurement with reference to magnetic north.

13. Relative humidity

Range : 40% to 100% with an accuracy of ± 2%.

Sensor: Hair element with inductive pick up.

14. Wind velocity

Range : 0 to 200 KM/hr with an accuracy of ± 5 KM/hr.

Sensor: Rotating cup, inductive or opto-electric pick up.

15. Wind direction

Range : 0 to 360° with an accuracy of ± 1°.

Sensor: Potentiometric measurement with reference to magnetic north.

16. Rainfall

Range : 0 to 30 cm with an accuracy of ± 0.5 cm.

Sensor: Floatation principle, with inductive pick up.

Unlike laboratory operated instruments, transducers of these field operated instruments are quite often installed away from the acquisition unit. Since these sensors are exposed to the adverse atmospheric conditions, these are designed with the following essential features.

1. Rugged and sturdy to withstand the shock and vibrations.
2. Well compensated for atmospheric changes in temperature, relative humidity etc.

2.2 Signal conditioners

Most of the sensors described above are passive and need to be energised during operation. DC or AC voltages are used for such excitation purposes. The output of the sensors need one or more of the following processing.

1. Separation of differential signal from unwanted common mode noises.
2. Magnitude amplification of the signals.

3. Linearisation.

4. Current to voltage conversion.

5. Frequency to voltage conversion.

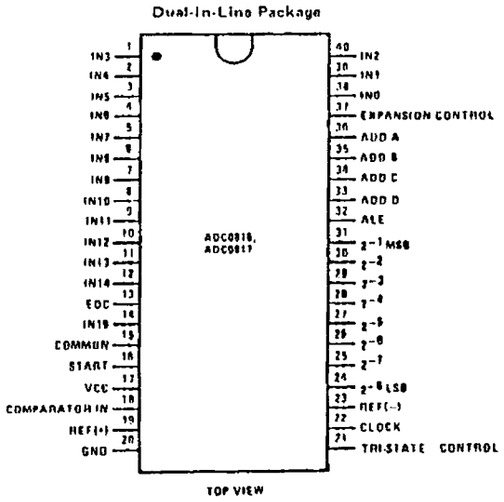
6. Buffering of signals.

The above functions are done by signal conditioners which vary depending on the type of transducers used. The output of the signal conditioners are clipped at 5 V using zener diodes in order to protect the ADC from input voltage higher than 5 V.

2.3 Analogue to digital converter

The single chip data acquisition system ADC 0816 is used as channel multiplexer and analogue to digital converter.

ADC 0816, offers high speed, high accuracy, minimal temperature dependence, excellent long term accuracy and repeatability and consumes minimal power. These features make this device ideally suited for



PIN CONFIGURATION OF ADC 0816

applications such as process control, industrial control machine control etc. Its conversion time is 100 u sec at a clock frequency of 640 KHz.

Functional description

ADC 0816, is a monolithic CMOS device with a 16 channel multiplexer, an 8 bit analogue to digital converter using successive approximation and microprocessor compatible control logic. Fig.2.1 shows the block diagram of the device.

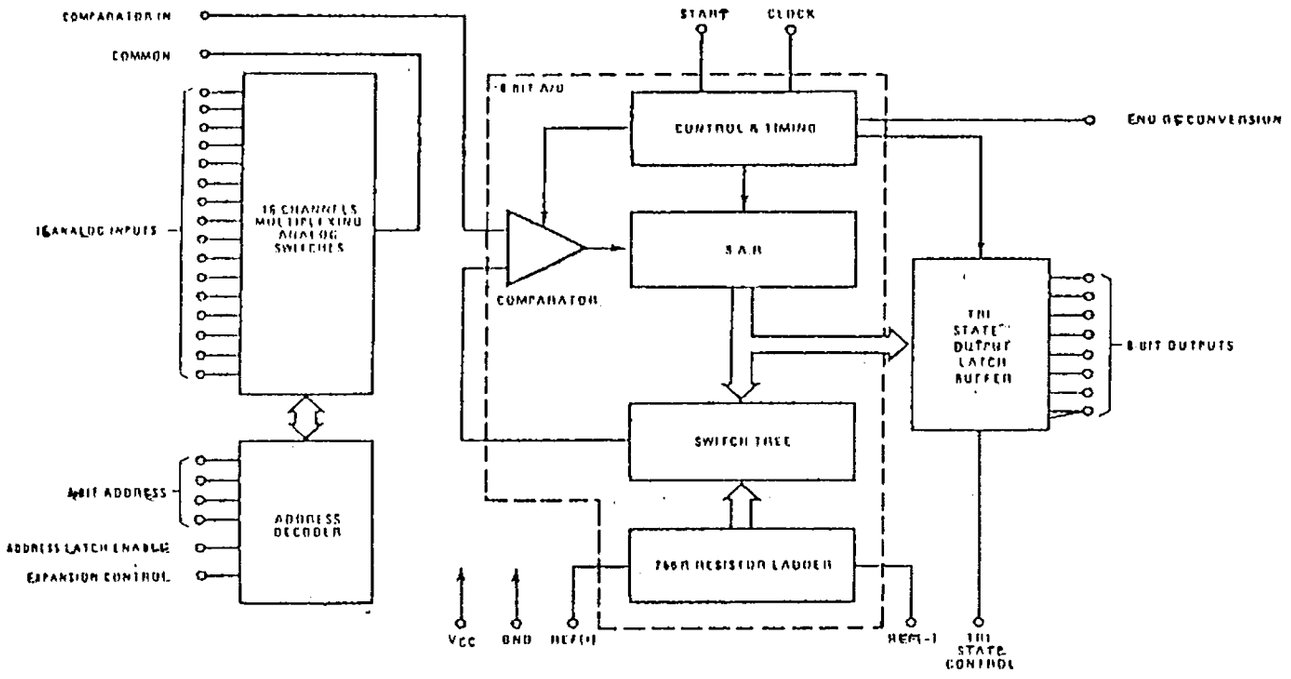


FIG. 2. 1. Block diagram of ADC 0816

Multiplexer

The device contains a 16 channel single ended analogue multiplexer. The multiplexer can directly access any one of 16 single ended analogue signals and provides the logic for additional channel expansion. The address is latched into the decoder on the low to high transition of the address latch enable signal. Additional single ended analogue signals can be multiplexed to the ADC by disabling all the multiplexer inputs and connecting the signal between the comparater input and the device ground. Additional signal conditioning such as sample and hold, instrumentation amplification etc., can also be added between analogue input signal and comparator input.

Converter

The heart of this single chip data acquisition system is its 8 bit analogue to digital converter. The 8 bit successive approximation A/D converter is designed to give fast, accurate and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 sections. The 256 R ladder network, successive approximation register and the comparator. The comparator's digital outputs are positive true.

The input voltage to the ADC 0816 is expressed by the equation,

$$V_{in}/(V_{fs}-V_z) = D_x/(D_{max}- D_{min})$$

where,

V_{in} - input voltage into the ADC

V_{fs} - full scale voltage

V_z - zero voltage

D_x - data point being measured

D_{max} - maximum data limit

D_{min} - minimum data limit.

The output code 'N' for an arbitrary input are the integers within the range.

$$N = \frac{V_{in}}{V_{ref}} \times 256 \pm \text{absolute accuracy}$$

where,

V_{in} - voltage at comparator input

$V_{ref}(+)$ - voltage at ref (+)

$V_{ref}(-)$ - ground.

The device eliminates the need for external zero and full scale adjustments features on absolute accuracy of ± 1 LSB including quantizing error. Easy interfacing to microprocessor is provided by the latched and decoded inputs and latched TTL tri-state outputs.

The input signals to the system are slowly varying dc voltage and hence no need for sample and hold circuit.

2.4 Data storage

Data is stored in a CMOS RAM with battery back up. 2K byte RAM 6116 is used in this case with provision being made for using 8K RAM, 6264 in the same socket on jumper connection. These are CMOS static RAMS designed for use in memory systems where high speed, low power and simplicity in use are desirable. They work on single power supply of 4.5 V to 5.5 V. A chip enable input and an output enable input are provided for memory expansion and output buffer control. The chip enable signal $\overline{CE}$ gates the address and output buffers and powers down the chip to the low power standby mode. The output enable signal $\overline{OE}$ controls the output buffers to eliminate bus contention.

Following table shows the selection of different modes of operation of the chip.

Truth Table of the Memory Device

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Address lines	Mode	I/O_1 to I/O_8	Device current
H	X	X	X	Not selected	HIGH Z	Standby
L	L	H	Stable	Read	Data out	Active
L	H	L	Stable	Write	Data in	Active
L	L	L	Stable	Write	Data in	Active

L = Low ; H = High ; X = H or L

The maximum access time of these RAMS range from 150 ns to 250 ns. Maximum standby current is 30 uA to 100 uA and minimum data retention voltage 2V.

The RAM with its back up supply has been made into a separate unit suitable for easy insertion and removal from the RAM socket for data analysing purposes.

2.5 The acquisition system

The remote data acquisition system is based on microprocessor 8085 with a clock frequency of 3.072 MHz. Fig.2.2 shows the circuit diagram of the entire data acquisition and storage system.

The power on reset facility is provided at the $\overline{\text{RESETIN}}$ pin of the 8055 which helps to start the program execution from OOOOH location of the PROM when power is switched on.

The non-maskable interrupt, TRAP is used to load the first data storage address at the reserved locations of the back up RAM. When power is switched on for the first time, the TRAP is initialized through a press switch SW_3 to execute the subroutine.

An 8 bit transparent latch 8282 is used to latch the low order byte address lines of the multiplexed processor bus. ALE control line of microprocessor is connected to the strobe input of the latch and address is latched during the high to low transition of the ALE signal. Output of the 8282 is connected to the low order

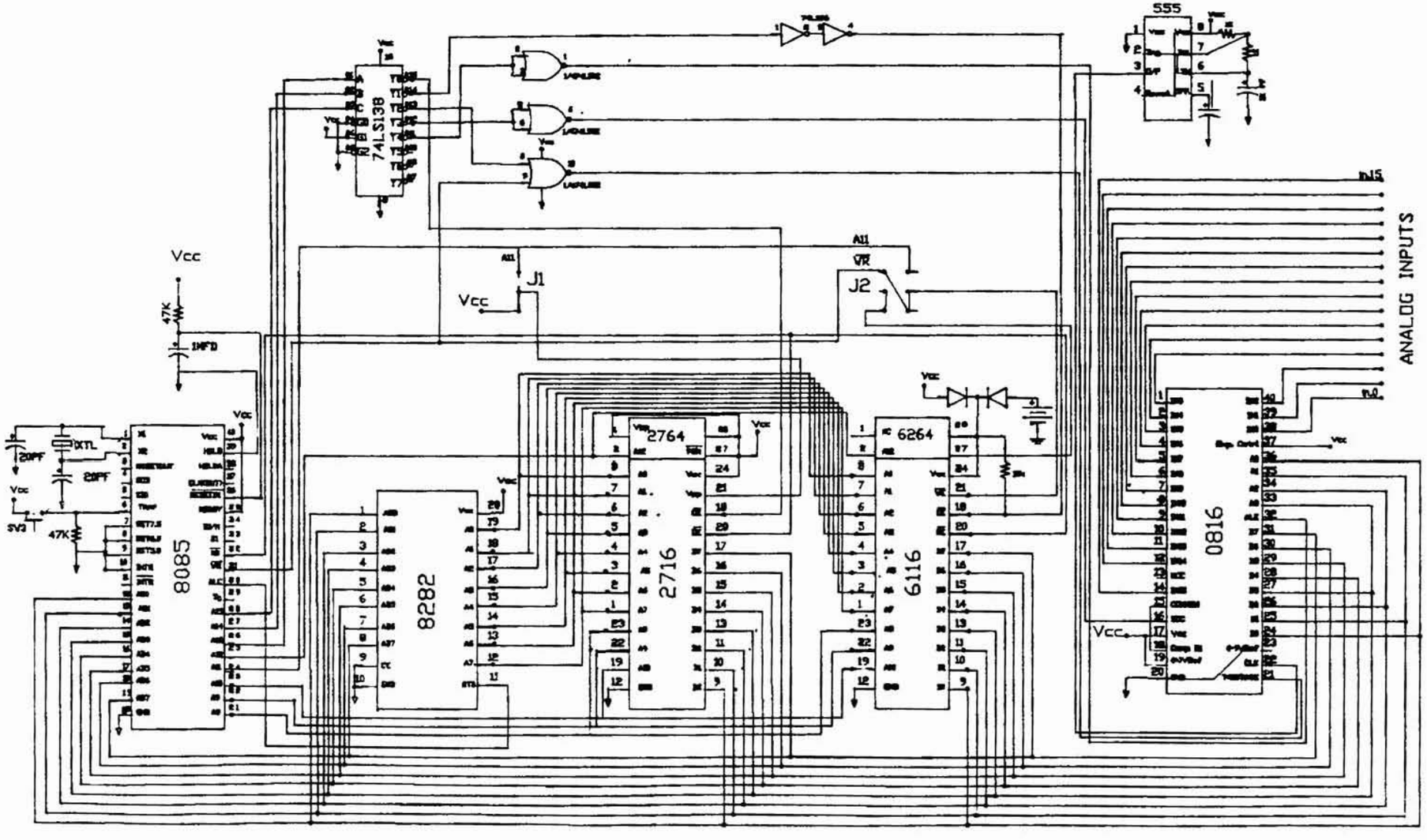


FIG. 2.2 REMOTE DATA ACQUISITION AND STORAGE SYSTEM

byte address pins of the RAM and PROM devices. The data bus of the microprocessor is connected directly to the data bus of the memory devices and the ADC. Address lines A_8, A_9 and A_{10} of the microprocessor is also directly connected to the memory devices.

Pin connections of the sockets for 2K and 8K memory devices are shown in the diagram. The jumper connection J_1 selects between 2716 and 2764 EPROM devices. When J_1 is shorted in the lower position as shown in the figure, +5V is connected to pin 21 and hence correspond to V_{PP} control signal of 2716. In this position 2716 is inserted in the lower 24 pins of the socket. When J_1 is shorted in the upper portion, A_{11} is connected to Pin 23 of the 2764. In this condition V_{PP} and $\overline{PGM}$ pins of 2764 are connected to V_{CC}.

Similarly the jumper connection J_2 selects between 6116 and 6264 RAM devices. When the lower portion of J_2 are shorted, 6116 is selected and in the other case 6264 is selected. A pull up resister is connected to the $\overline{CE}$ pin of the RAM device to keep the chip in low power standby mode when the chip is not selected. Two protection

diodes are connected to the V_{CC} pin of the RAM for giving the system power supply and the battery back up supply simultaneously. $\overline{RD}$ signal of the microprocessor is connected to both memory devices and $\overline{WR}$ is connected to the RAM alone.

Chip select signals for the memory devices and the ALE, SOC and TRISTATE signals for the ADC are produced using the 3 to 8 decoder 74 LS 138. Address lines A_{13}, A_{14} and A_{15} of the microprocessor are used for the purpose. The outputs of the decoder are active low. The Y_o output is having address OOOOH to IFFFH and forms the $\overline{CS}$ signal of the EPROM. Y_1 output having address 2OOOH to 3FFFH is buffered using two open collector inverter gates of 74LS06 and connected to $\overline{CE}$ pin of the RAM device, which is pulled up using a 10K resistor. In this condition the chip goes low power standby mode when not selected and data retained.

Channel address lines ADD A to ADD D are connected to the lower four bit data lines. Memory maped I/O mode is used in interfacing the ADC in the circuit. Y_2 output of the decoder having address 4OOOH to 5FFFH is NORed with $\overline{WR}$ signal of the processor using 74LS02 and

forms ALE control signal of the ADC. Similarly Y_3 output of address range 6000H to 7FFFH is inverted and used as the SOC signal. Y_4 output having address 8000H to 9FFFH is inverted and connected to the TRISTATE input. Considering the decoder input lines and assuming logic zero for the don't care address lines, the ALE, SOC and TRISTATE signal line address can be taken as 4000H, 6000H and 8000H respectively. These control signals are applied using the memory mapped instructions. The convertion time of 195 micro sec. corresponding to 65 clock cycles is given between SOC and TRISTATE signals.

The ADC clock is generated from an IC555 timer wired as an astable multi-vibrator having a frequency of 350 KHz.

The system timer switches on the power supply to the remote DAS at every 2 hour time intervel. The entire system except the timer which is operated at a very low current of less than 1 mA, is switched off during the non-acquisition period.

2.6 System timer

The system timer controls the timing intervel between two consecutive scanning of the data acquisition. It switches on the relay through which battery supply is given to the remote data acquisition and storage system. The circuit diagram of the timer is given in Fig.2.3. A crystal oscillator of frequency 2 Hz, made of IC 1444 operated at very low current is the basic timing unit. The scan time intervel is produced by dividing the oscillator output using a 14 bit binary ripple counter CD 4020 and a 4 input NAND gate CD 4012. The Q_{14}, Q_{13}, Q_{12} and Q_7 outputs of the 14 stage counter are fed to the NAND gate to get a time intervel of 2 hours. This two hour interval pulse drives a monostable oscillator made of CD 4047 with a period of 7 seconds which in turn switches on the relay driver transistor SL 100.

2.7 Development system used

The Intel Personal Development System (IPDS) was used for the design development and testing of hardware and software required for the remote data acquisition system. The IPDS supports the design and development of products

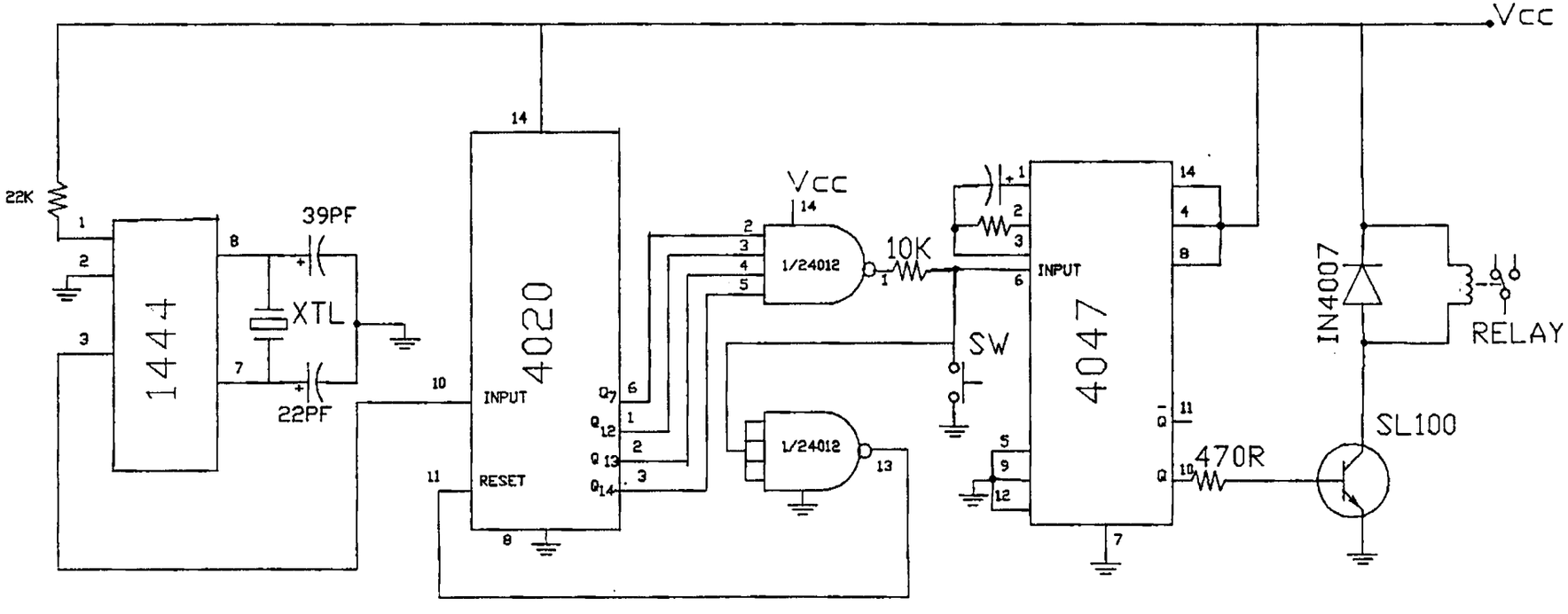


FIG. .2.3 SYSTEM TIMER

that incorporate Intel Microprocessors or Microcontrollers. It supports integrated hardware and software development by assembling or compiling source programs for execution and by emulating the target microprocessor (8085). The system includes a PROM programer for programing EPROMs and to store software in the target processor's memory. It typically allowes the designer to write software using assembly language mnemonics. The IPDS also allows the designer to write the software in high level languages such as Fortran and Basic.

The basic unit consists of the following:

(a) Base processor board containing 8085-2 CPU operating at 5 MHz, 64K byte RAM, 2K byte ROM, CRT and keyboard controller, flexible disk controller with ports for three additional drives, emulator and PROM programer port etc.

(b) 640K byte formated 5¼" flexible disk drive for mass storage.

(c) Switching type power supply.

Assembling Source Program

The source program is developed in mnemonics using AEDIT-80 text editor utility program. The source program is assembled using the ISIS-11 8080/8085 Macro Assembler (ASM-80).

In addition to creating the object file the assembler performs the error checking and memory allocations. The assembler creates the object file which contains the machine language instructions and data that can be loaded into memory for execution and interpretation. In addition, it contains control information governing the loading process. The assembler can produce object files in relocatable object code format. The object modules can be linked to form a larger program for execution. After execution the assembler issues a sign off message and error summary.

The assembler also creates a formated list file designed to be output to a line printer or terminal. It includes a listing of assembled object codes, the source program, a table of symbols and their values and a summary of assembly errors.

The summary of assembled errors can be used for further editing and perfecting the source program.

Emulation

Emulator is the imitation of another system, mainly by hardware, so that the imitating system accept the same data, executes the same programs and achieves the same results of the imitated system. The EV-85 emulation vehicle provides an artificial hardware environment for the 8085 microprocessors. The system consist of an emulator pod, EV-85 emulation vehicle and the IPDS.

The EV-85 supports 16K of overlay memory, real time execution to 6 MHz clock frequency, command driven user interface, symbolic debugging with user defined address or object code labels.

The system contains a trace display of all 16 address bits, all 8 bit data bits disassembled instructions and 15 status lines. It contains an eventpoint system with four specific event triggers, two address range event triggers, one pass counter and sixteen state sequencer to specify sequences of break and trace conditions.

The object file created is loaded into the R/W memory of the IPDS and the execution of the program done either on real time or on single stepping with or without trace option for display of CPU status. The software can be resident either with host or on the target system. The memory locations of the target system can be read or written by the host system.

PROM Programming

A plug-in module adapter board is used along with the IPDS for PROM programming. The IDPS software used for the purpose is a utility that runs under the ISIS-PDS operating system. The software supports the following features.

* Reading and writing data to and from disk files.
* Modifying the data in the memory buffer.
* Programming the contents of a particular PROM device.
* Reading back the contents of the PROM device.
* Verifying the contents of the PROM device by comparing it to the contents of the memory buffer.

2.8 The software

The flow chart of the software developed for the remote data acquisition and storage system is shown in Fig.2.4.

At power on the microprocessor enters a delay routine of 5 seconds for the analogue voltages to get stabilized. The address of data storage is read from the reserved RAM locations and compared with the limit address of data storage. In case it correspond to the limit address, the program stops otherwise it proceeds. Then the first channel address is latched into the ADC address decoder and the start of conversion signal is given. A conversion delay time of 195 micro sec. was given for the analogue to digital conversion process to complete. The data is read from the ADC output buffer and stored in the prescribed location of the battery backed up RAM. Then the next channel is selected and the corresponding data stored at the next location of the RAM. The process is continued untill 16 channels are scanned, at the end of which the programe stops, after storing the next data storage address in the reserved space. The process of data storage continues at every two hour intervel until the limit

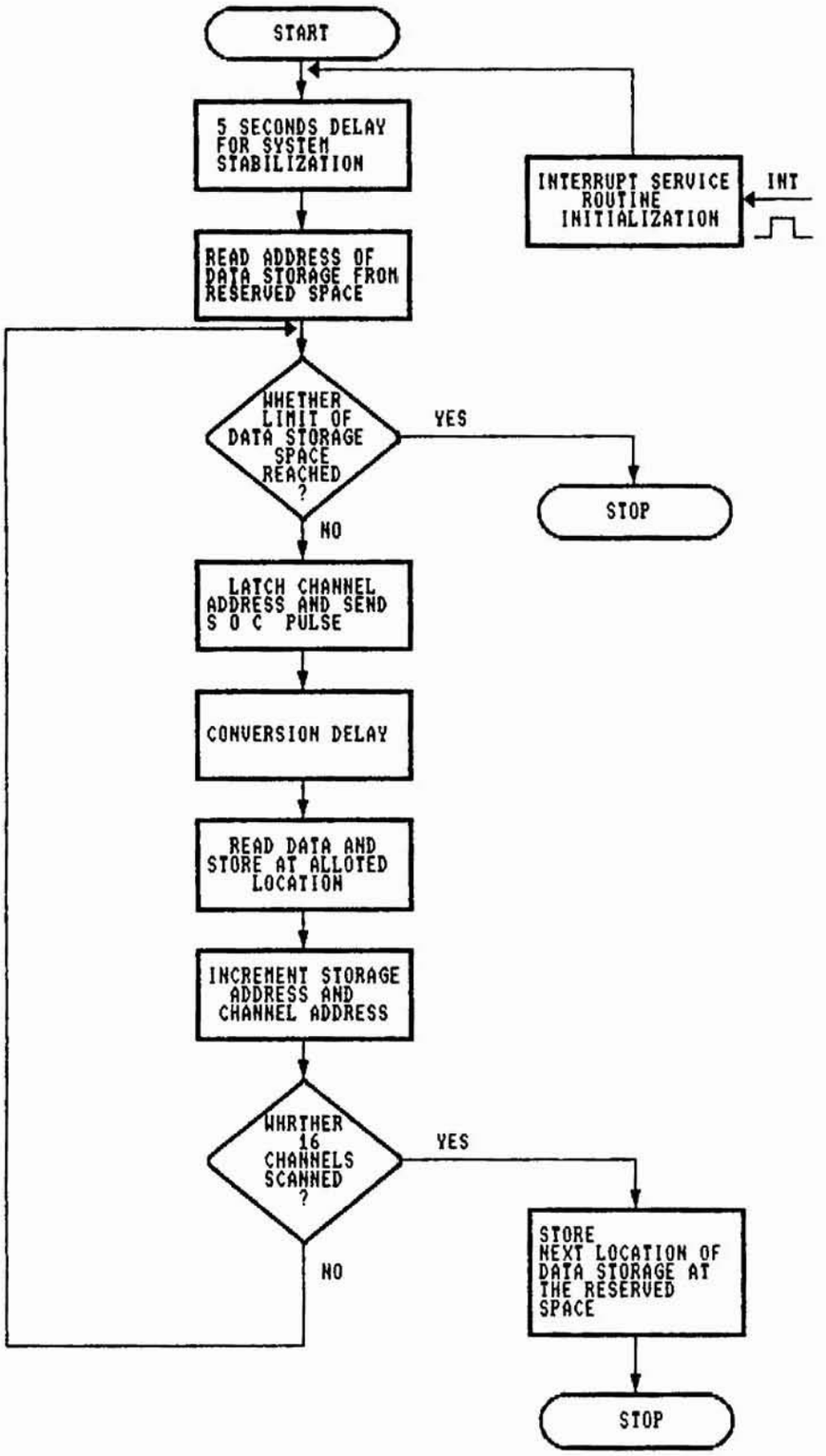


FIG.2.4 FLOW CHART OF THE REMOTE DATA ACQUISITION AND STORAGE SYSTEM

address of data storage is reached, when it stops further storage operation. When the power is switched on after the next two hours, the processor halts execution after the 5 sec. delay time since the limit address of data storage is reached. TRAP interrupt subroutin stores the first data storage address in the reserved RAM location. This routin is initialized immediately after the power is switched on for the first time when a fresh RAM is used for data storage. The software developed and tested using the IPDS was programmed into the EPROM 2716.

2.9 PCB design

A double sided PCB of size 100x150 mm^2 was designed for the remote data acquisition system with SMART WORK program and fabricated. Fig.2.5(a) and 2.5(b) shows the layouts of the PCB developed. Assembled and tested the PCB in the laboratory and found working satisfactorily.

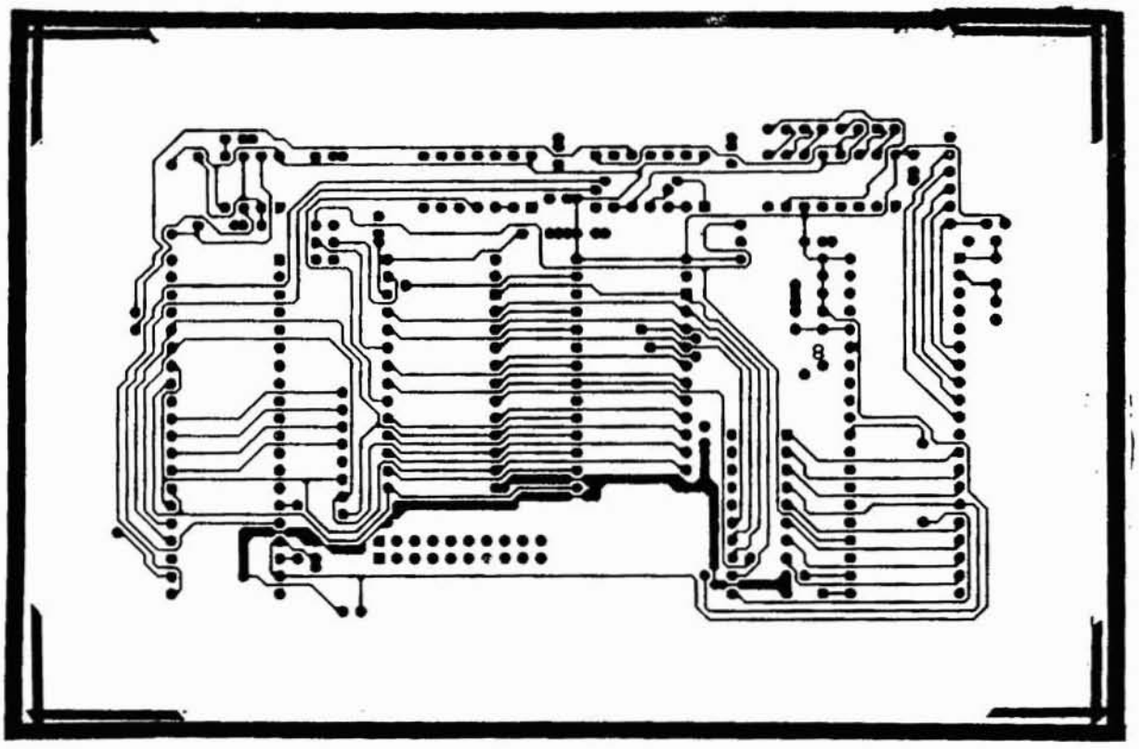


FIG. 2.5(a) Layout of PCB for Remote data acquisition and storage system
(Solder side)

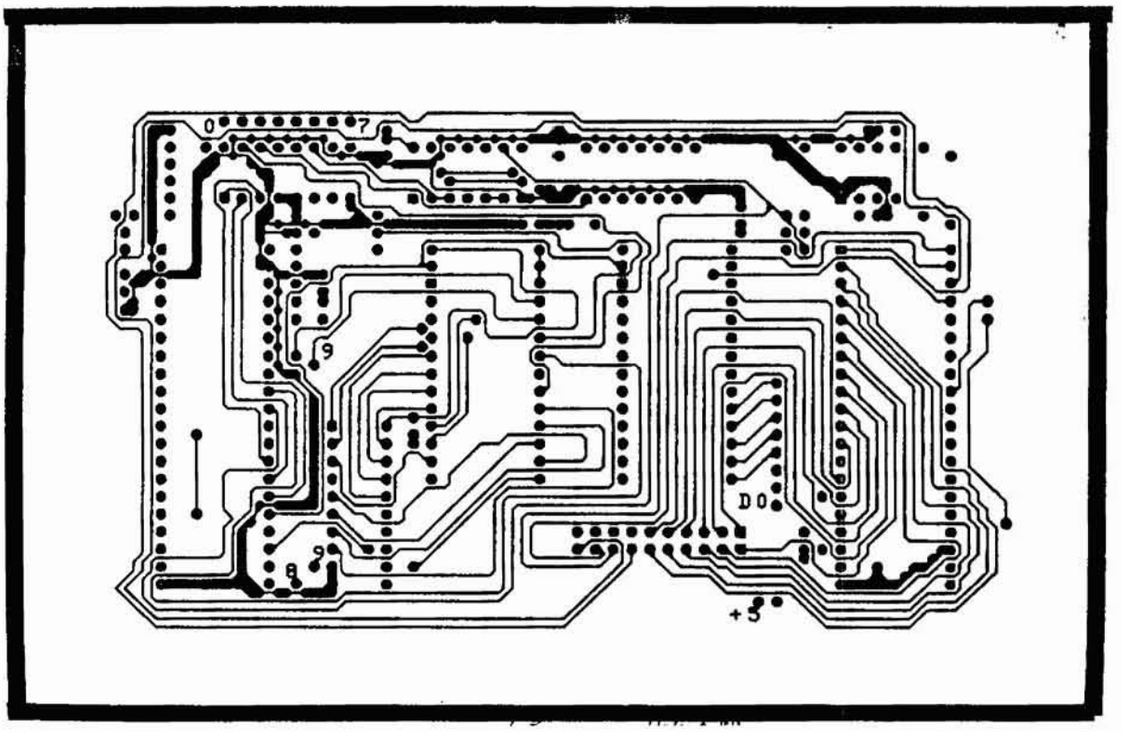


FIG. 2.5(b) Layout of PCB for Remote data acquisition and storage system
(Component side)

chapter 3

FIELD DATA ANALYSER

The remote data acquisition system has not been provided with provision for display of data in order to reduce the power consumption. Instead, a field data analyser has been developed for display and analysis of the data at the measuring site. The field analyser also helps to occasionally confirm the proper working of the DAS at the remote site.

3.1 Organization of the analyser unit

The organization of this unit is based on microprocessor 8085 with 2K byte RAM (6116) and 2K byte EPROM (2716) as memory devices. Provision has been made for use of 8K byte RAM and EPROM devices in the same respective sockets on jumper connection. Programmable keyboard/display interface chip 8279 is used for keyboard scanning and display of address and data. A programmable interface device 8255 has also been provided which can be used as three 8 bit I/O ports.

Memory maped I/O mode is used in interfacing the pheripheral devices. IC 74LS138 is used for decoding of address lines A_{13}, A_{14} and A_{15}. The outputs of this IC is used as different chip select signals.

Please refer to circuit diagram of the field data analyses shown in Fig.3.1. The Y_0 output having address OOOOH-IFFFH forms the chip select signal for the EPROM. Y_1 output having address 2OOOH-3FFFH is buffered through an open collector buffer 74LS07 and forms chip select signal for the RAM. The pull up resistor provided at the $\overline{CS}$ pin of the RAM helps to keep the memory device in low power standby mode when the chip is not selected. In addition it also helps to retain data using battery backed up RAM, when the system power is switched off. Y_2 output having address 4OOOH-5FFFH corresponds to the port address of 8279. Similarly Y_3 output having address 6OOOH-7FFFH forms the port address of 8255.

The jumper connections J_1 and J_2 shown in the figure correspond to memory devices, 6116 RAM and 2716 EPROM. If the upper portions of J_1 and J_2 are shorted, then 8K RAM 6264 and 8K EPROM 2764 can be used.

3.2 Key board/display interface

General purpose programmable keyboard and display I/O interface device, the Intel 8279 is used here which is designed for use with Intel microprocessors. Its keyboard

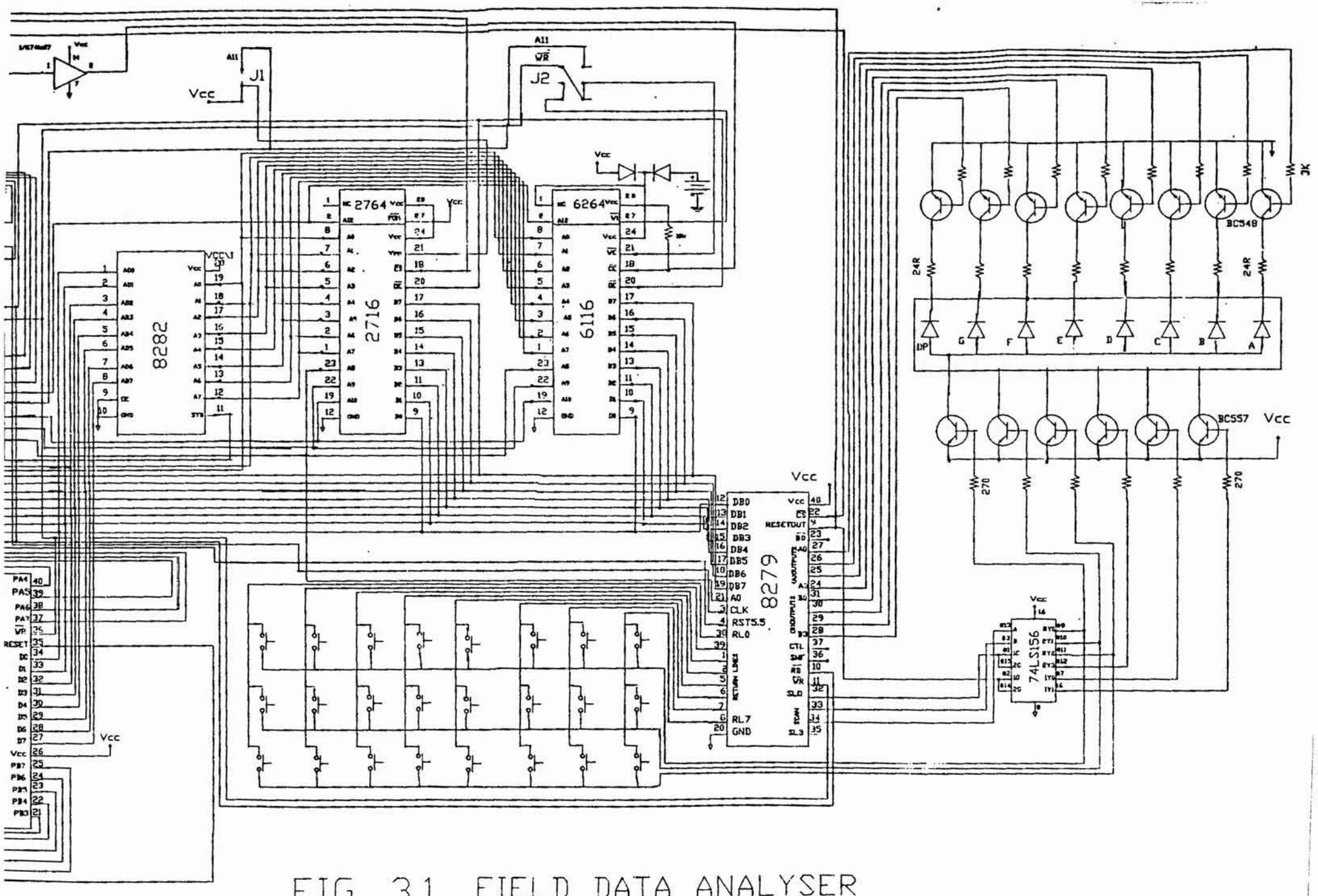


FIG. 3.1 FIELD DATA ANALYSER

portion can provide a scanned interface to a 64 contact key matrix. Keyboard entries are debounced and stored in an 8 character FIFO. Entry of more than 8 character sets the overrun status. Key entries set the interrupt output line to the CPU. The display portion provides a scanned display interface for LED, and other popular display technologies. 8279 has 16x8 display RAM which can be organised into dual 16x4. Both read and write of the display RAM can be done with auto-increment of the display RAM address.

The I/O control uses the $\overline{CS}$, AO, $\overline{RD}$ and $\overline{WR}$ lines to control data flow to and from the various internal registers and buffers.

3.3 Circuit description

Interfacing of 8279 with matrix keyboard of 24 keys and six seven-segment LEDs with transistor current drivers are shown in Fig.3.1.

Return lines RL_0-RL_7 are connected to the columns of the matrix keyboard and output lines A_0-A_3 and B_0-B_3 are connected to drive the LED segments through the transistors. The three scan lines are connected to the decoder 74LS156,

to generate eight decoded signals. In this circuit, six output lines of the decoder are connected as digit drivers to turn on the six seven segment LEDs. Two output lines are not used. In addition, the first three output lines are also used to scan the rows of the keyboard. Data lines of 8279 are connected to the data lines of the 8085 and the IRQ(interrupt request) line is connected to the RST 5.5 of the system.

The port address of the 8279 registers are determined by the two signals $\overline{CS}$ and A_0. The $\overline{CS}$ Pin of 8279 is connected to decoded output of the 74LS138 having address 4000H-5FFFH. A_0 Pin is connected to A_8 address line of the processor. For commands and status A_0 should be high. For data transfer A_0 should be low. By examining the decoder input lines and assuming logic 0 for the don't care address lines the port address becomes.

COMMAND/STATUS PORT : 4100H

DATA PORT : 4000H

Four signals $\overline{RD}$, $\overline{WR}$, CLK and RESETOUT are connected directly from the 8085. The system has a

3.072 MHz clock frequency, and when 8279 is reset, the clock prescaler is set to 31. This divides the clock frequency by 31 to provide the scan frequency of approximately 100 KHz. The reset signal also sets the 8279 in the mode of sixteen character display with two key lock out keyboard.

After the initialization of the 8279 the respective codes are sent to the display RAM to display any characters. The 8279 takes over the task of displaying the characters by outputing the codes and digit stroks. To read the keyboard, the 8279 scans the columns, if a key closure is detected, it debounces the key. If a key closure is valid, it loads the key code into the FIFO and the IRQ line goes high to interrupt the system.

3.4 Data analysis

Onsite data analysis is carried out using the field data analyser. The data storage unit is removed from the remote data acquisition system and inserted in the RAM socket of the data analyser. Contents of the battery backed up RAM is examined by displaying the address locations and the crresponding data stored, by pressing the particular

command key and incrementing the memory locations. This can be done without affecting the normal operation of the acquisition system by performing the data analysis during the non-acquisition period when power is switched off by the system timer. Suitable software can be developed and the following data analysis can be carried out.

1. Display the parameters and data in corresponding engineering units.

2. Display the maximum and minimum value of the parameters for the required time interval.

3. Display average value of the parameters.

4. Display the parameters and data in the required sequential order.

5. Get the parameters and data printed using a Centronics printer interface.

3.5 System software

The monitor software developed using IPDS was programmed into EPROM 2716. Simplified flow chart of the working of data analyser is given in Fig.3.2.

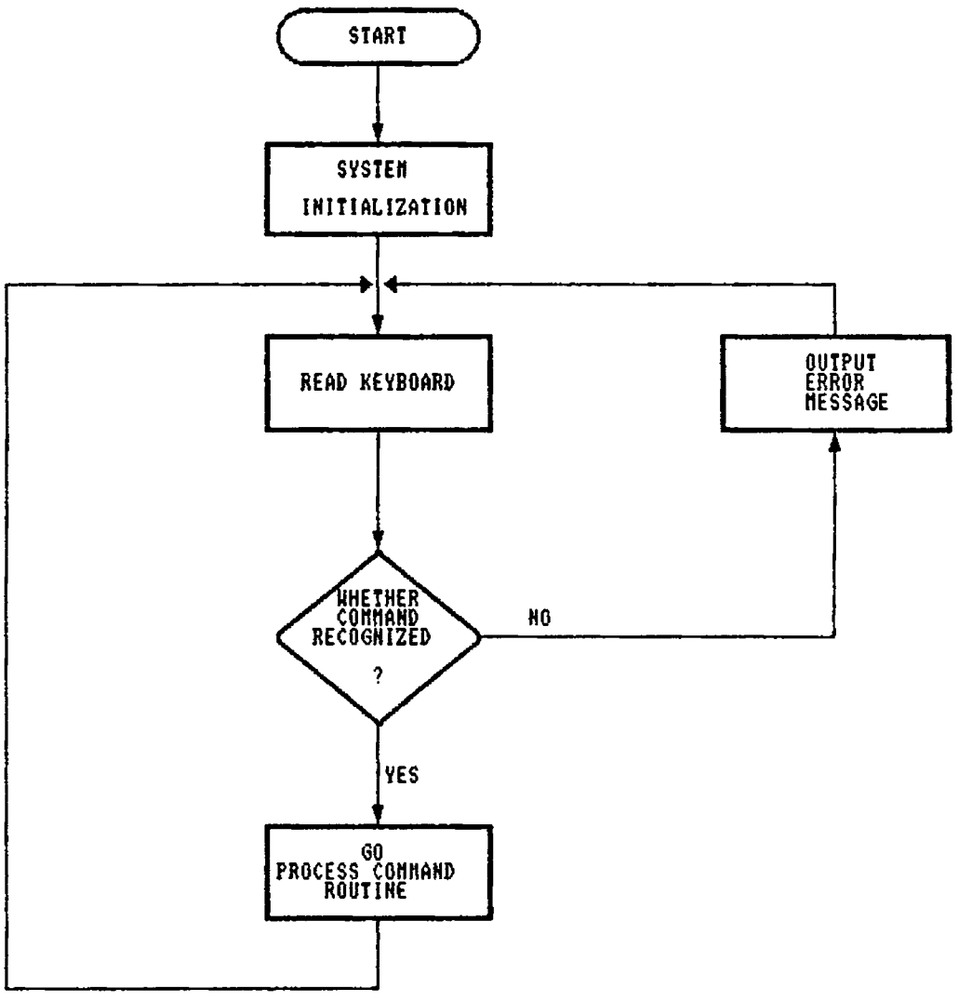


FIG. 3.2 FLOWCHART OF FIELD DATA ANALIZER

At power on the processor is rest and starts execution from OOOOH location. First the keyboard/display interface and the microprocessor registers are initialized and the sign on message 'CUSAT 85' is displayed. Then the key depression is checked. When a key is pressed the monitor checks whether it is a valid command key. If it is not a valid command key an error message 'Err' is displayed and further key depression is checked. When a valid command key is pressed , the command is recognised and the program jumps to execute the command routine. After execution of the command, the key depression is checked again and the process is repeated.

3.6 PCB development

A double sides PCB of size 125x250 mm^2 was designed for the field data analyzer using SMARTWORK program and fabricated. Fig.3.3(a) and 3.3(b) shows the layout of the PCB developed. The PCB was soldered and tested in the laboratory and the monitor software developed. The Intel Personal Development System was used for the design development and testing of the hardware and software.

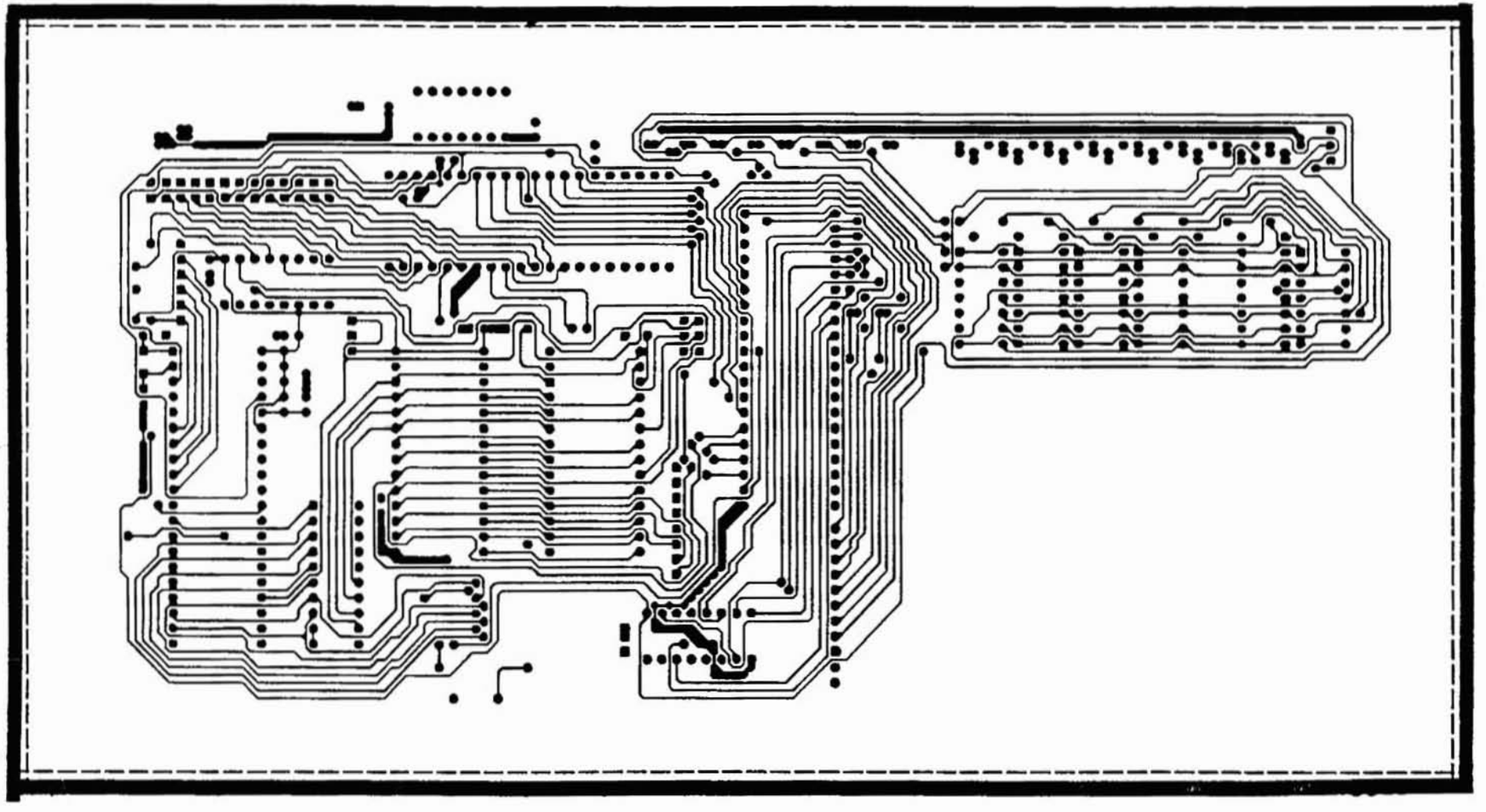


FIG.3.3(a) Layout of PCB for Field data analyser
(Solder side)

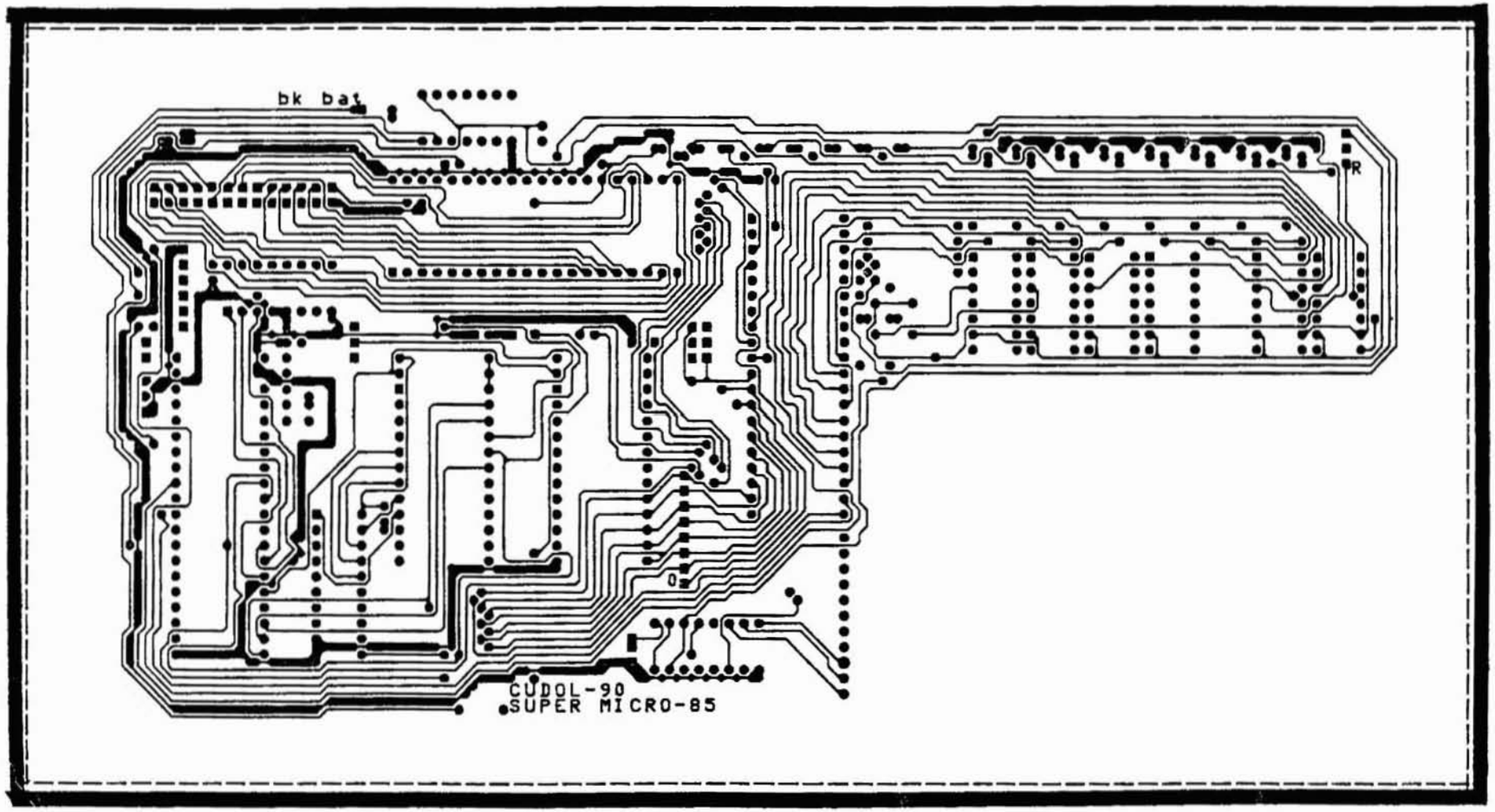


FIG.3.3(b) Layout of PCB for Field data analyser
(Component side)

chapter 4

LABORATORY DATA ANALYSING SYSTEM

This is an IBM compatible PC based unit consisting of an IBM PC/XT, PC interface module and a memory interface card. These two interfaces are interconnected through a flat cable with connectors at both ends. The battery backed up RAM unit of the remote data acquisition system is brought to the laboratory and data analysed using the PC based analysing system. Different components of the data analysing system are given below.

4.1 IBM PC/XT

The heart of the laboratory data analyser is the IBM PC/XT. This is a multiboard system with Intel 8088 microprocessor as CPU.

Specifications

CPU	:	Intel 8088
Coprocessor	:	Intel 8087
Main memory (DRAM)	:	640 KB
Secondary memory		
Hard disk	:	20 MB
Flopy drives	:	360 KB (2 nos.)
System clock	:	4.77 MHz
Graphics card	:	CGA
Colour monitor		
Operating system	:	MS DOS 3.2.

Fig.4.1 shows a view of the component side of the main microprocessor board, often called the motherboard for IBM PC. Along with the RAM, ROM and microprocessor on this board there are eight system expansion slots in the upper left corner. These slots allow the addition of specific function boards that are required in our system, in addition to the basic CPU board.

Fig.4.2 shows a block diagram of the motherboard of IBM PC. Starting from the left side of the diagram and looking across it, we see first the 8088 CPU and then the 8259 interrupt controller below it. The next vertical line of the devices to the right consists of the address bus buffers, the data bus buffers and the 8288 bus controller chip. The bus controller chip is required because the 8088 is operated in maximum mode. The buses from these devices go across the drawing and connect to the 62 pin peripheral board connectors. The CPU then can use these buses to communicate directly with the board in the peripheral expansion slots. Now we find the ROM in the lower right, the keyboard logic etc., in the middle side and the dynamic RAM in the upper right. Finally we see at the column of devices, the 8258 DMA controller 8253 programmable timer and 8255 programmable port device.

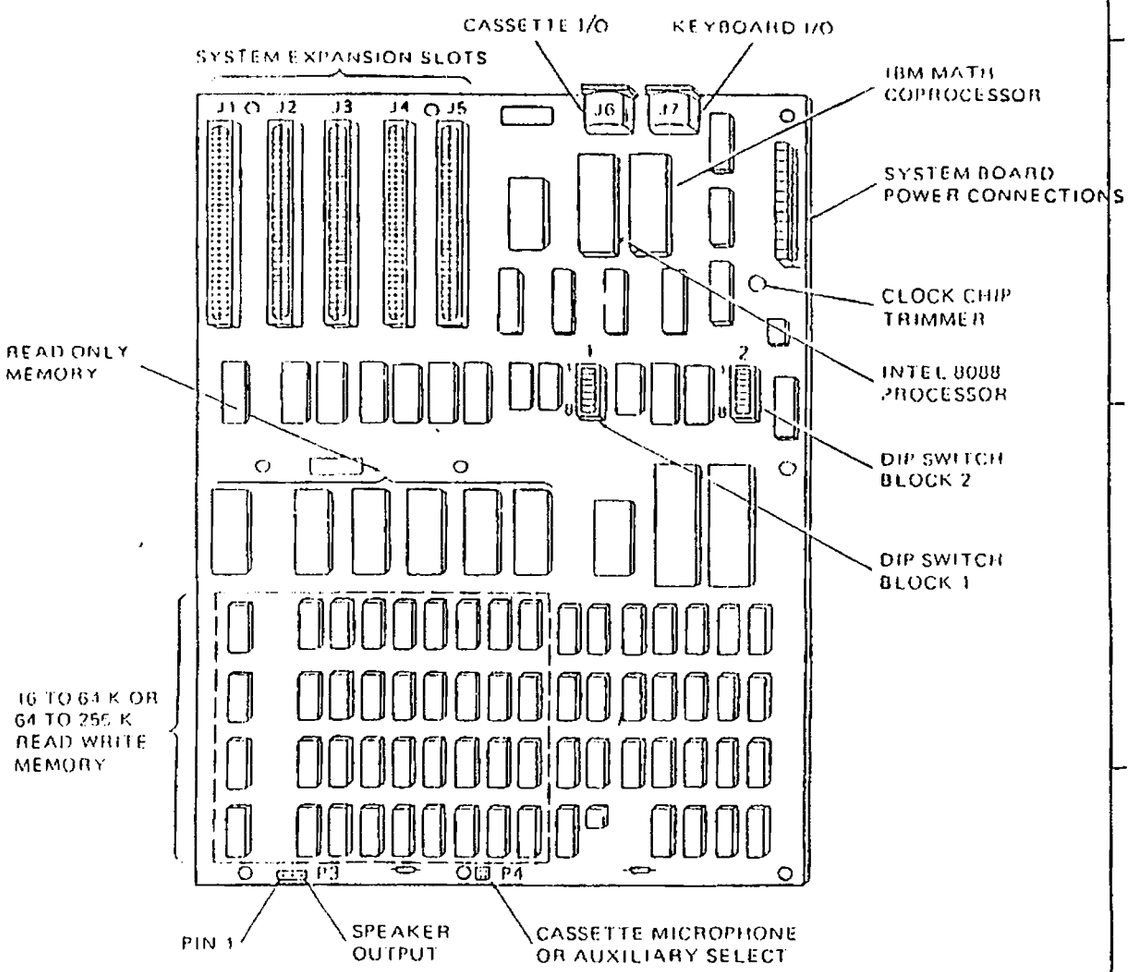


FIG.4.1 Component layout diagram of IBM PC Mother board

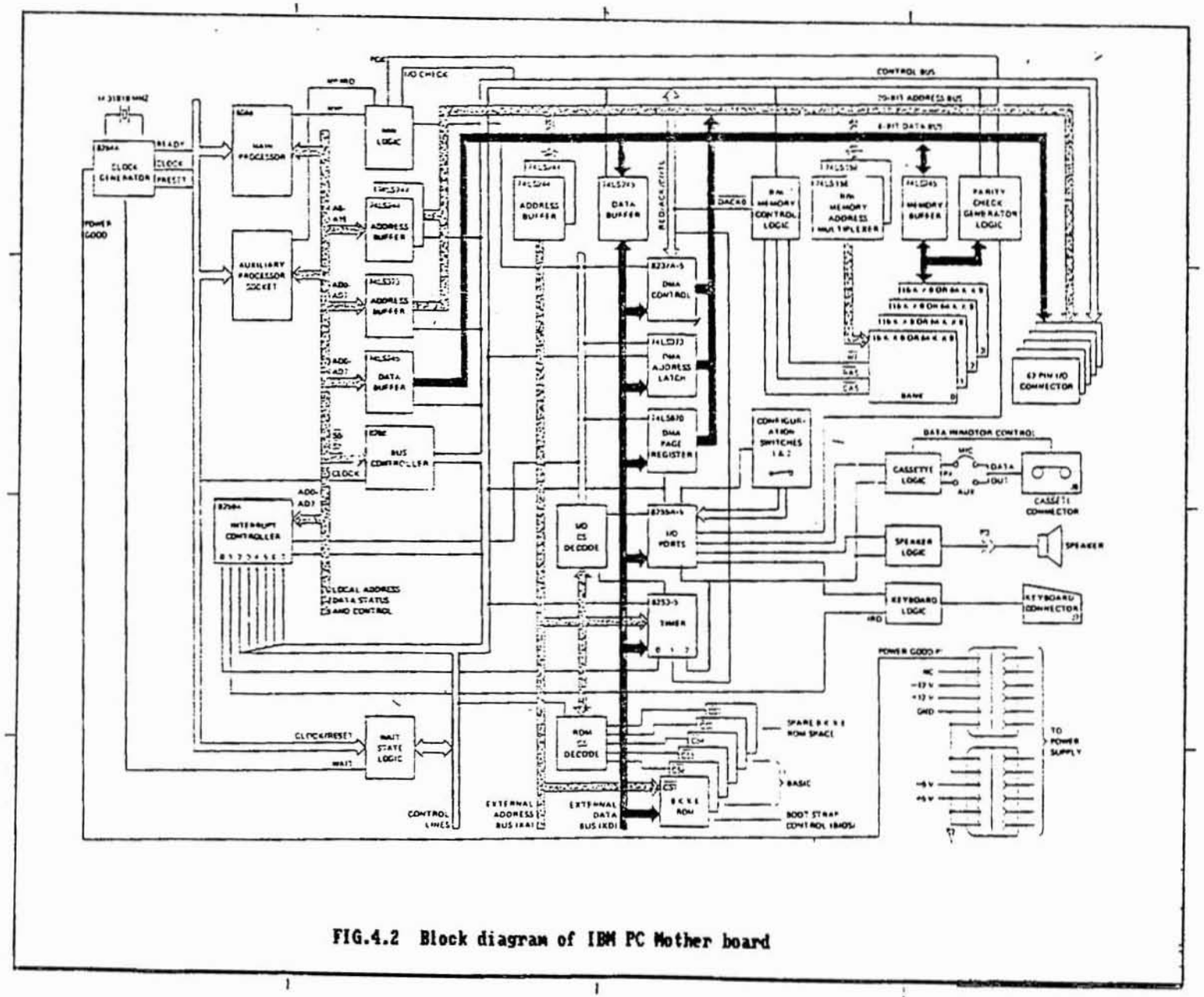


FIG.4.2 Block diagram of IBM PC Mother board

Fig.4.3 shows the pin names and numbers of the peripheral slots. '+' sign, infront of a signal indicates that the signal is active high and a '-' sign indicates that the signal is active low. A_0-A_{19} on the connectors are the 20 demultiplexed address lines, and D_0-D_7 the eight data lines. IRQ_2-IRQ_7 are interrupt request lines which go to 8259 interrupt controller; so that the peripheral boards can interrupt the 8088 if necessary. Some other signals on the connectors are the power supply voltage, ALE, MEMWR, MEMRD, IOW, IOR, control bus signals and some clock signals. The DMA request pins DRQ_1-DRQ_3 allow peripheral boards to request the use of the buses.

4.2 PC interface module

Circuit diagram of the PC interface module is shown in Fig.4.4. This module consist of address decoders, a data lines transceiver and an address line buffer. The first decision that has to be made when designing a PC card is just where in the input/output map it should be placed. Although the I/O channel address range of IBM PC/XT seems to be rather crowded there are actually a few gaps that can be exploited. Moreover, the address range 300H - 31FH is exclusively allotted for prototype cards which can be made

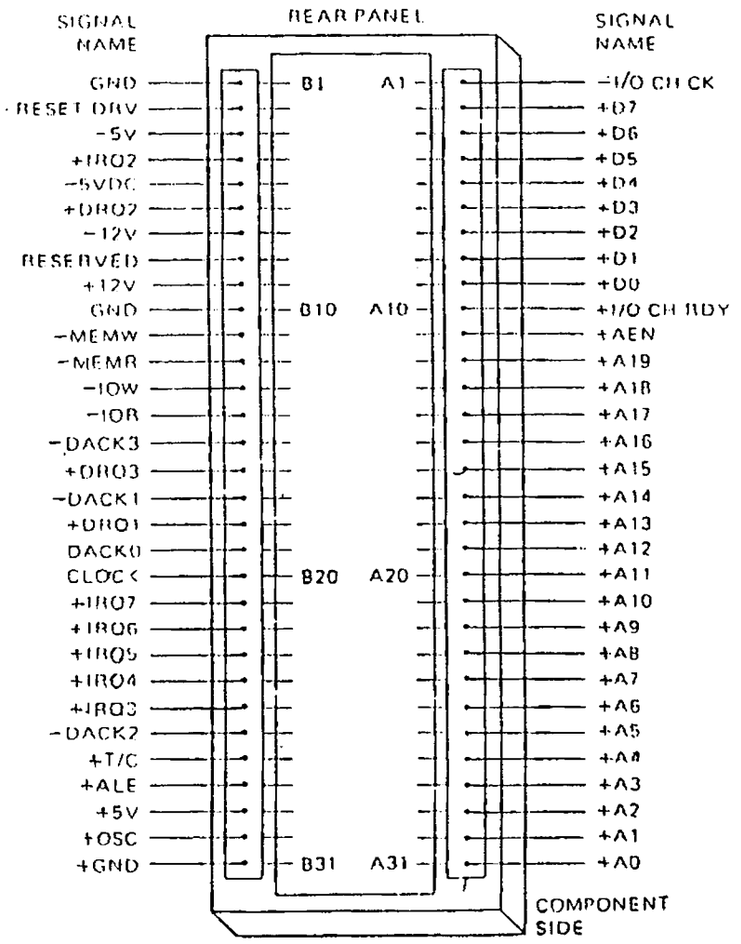


FIG.4.3 Numbering system used for the PC expansion connector with pin names

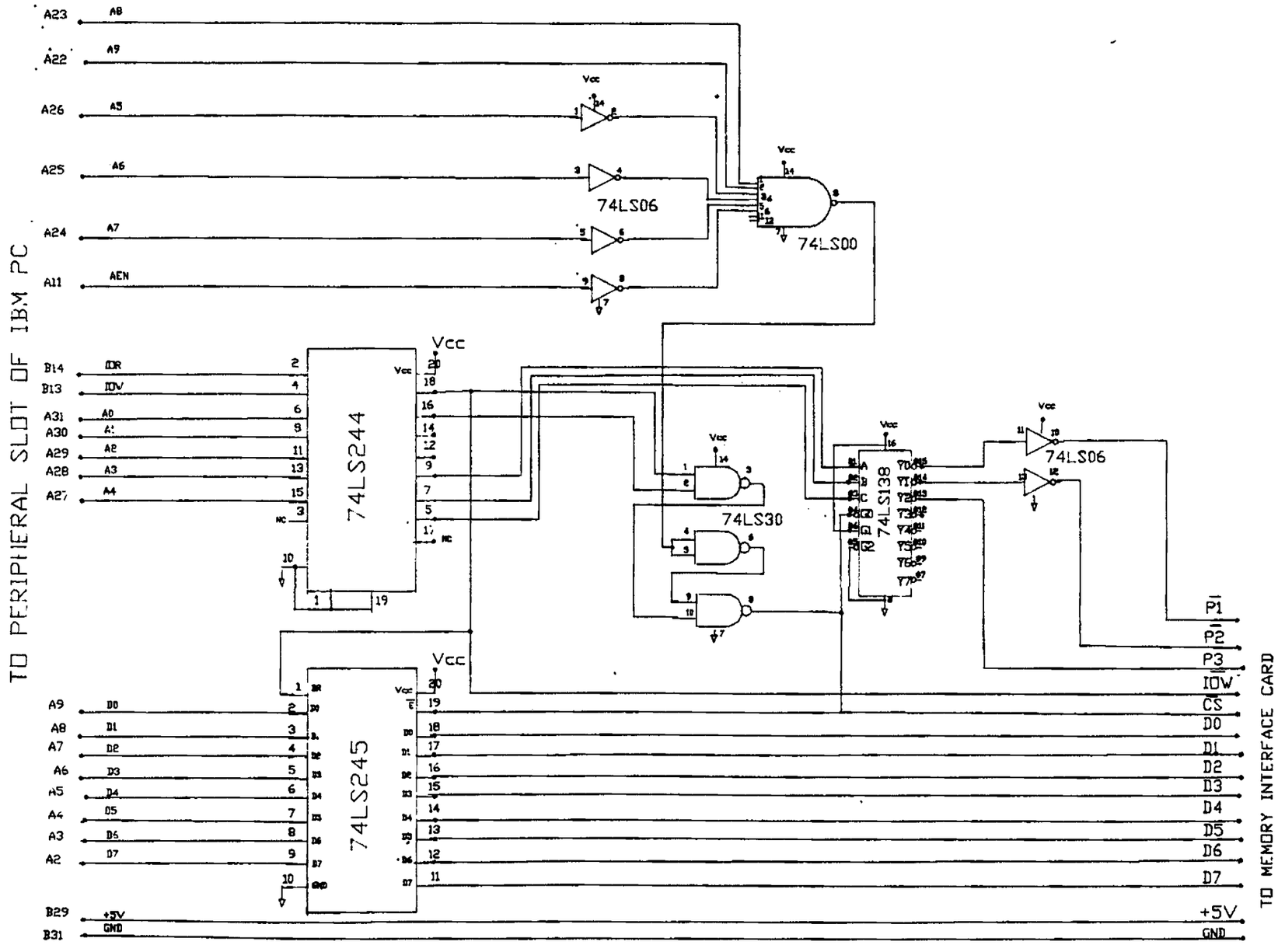


FIG. 4.4 PC INTERFACE MODULE

use of for user add ons. In the present case address 300H - 308H are made use of for I/O port addresses.

Apart from the $\overline{IOR}$ and $\overline{IOW}$, the control line AEN is also included for decoding purposes. AEN (address enable) goes high during DMA cycles and becomes low during processor cycle times.

Please refer the circuit diagram of the PC interface card shown in Fig.4.4. The $\overline{CS}$ signal for the memory chip in the storage system is produced by decoding address lines A_5, A_6, A_7, A_8 and A_9 and control signals AEN, $\overline{IOR}$ and $\overline{IOW}$. This has a port address 300H - 31FH. The same $\overline{CS}$ line is connected to the chip enable $\overline{E}$ pin of data bus transceiver 74LS245, so that whenever the memory chip is enabled its data bus is directly connected to the data lines of the PC. Direction control pin DR of the bus transceiver is connected to the $\overline{IOR}$ control line, to control the direction of flow of data through the bus. 74LS244 is an octal line driver used to buffer the decoding address lines A_2, A_3, A_4 and control lines $\overline{IOR}$ and $\overline{IOW}$.

Address lines A_2, A_3 and A_4 are decoded using 74LS138 to produce active low signals P_1, P_2 and P_3 of address 300H - 303H 304H - 307H and 308H - 30BH

respectively. P_1, P_2 and P_3 are used as strobe signals and output enable signal for the eight bit latches used in the storage system interface.

The data lines, control signals of $\overline{IOR}$, $\overline{CS}$, $\overline{P}_1$, $\overline{P}_2$, P_3 and V_{CC} supply and ground are brought out to one end of the PCB and connected to a socket for linking to the storage system interface through flat cable.

4.3 Data storage interface

This is a small card used along with the PC interface module for connecting the data storage unit of the remote data acquisition system for data retrieval and analysis. It has got a 28 pin RAM socket on which a zero insertion force socket is mounted. The remote data storage RAM is inserted in the ZIF socket. Though 2K byte RAM is used in this case, 8K RAM can also be inserted in the same socket without any alteration. Circuit diagram of the data storage interface is shown in Fig.4.5.

Three eight bit transparent latches 8282 are provided for addressing and data transfer from the storage RAM. The least sifnificant 8 address lines of the RAM is

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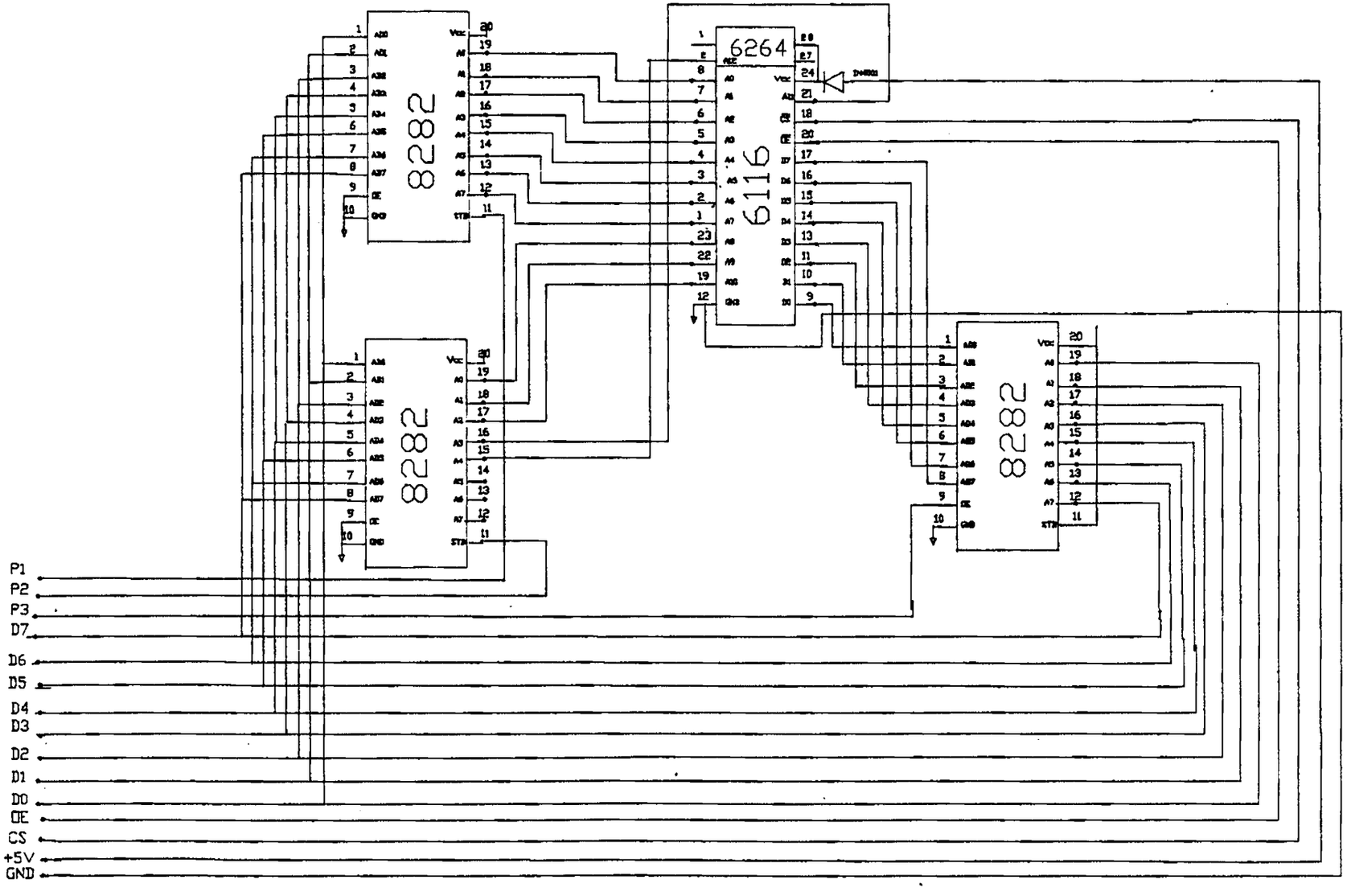

FIG. 4.5 DATA STORAGE INTERFACE

selected through the first 8282 having a port address 300H. The active high $\overline{P}_1$ line from the PC interface module is used as strobe signal for this latch. The high order address lines are selected through the second 8282 of port address 304H. Similar to the previous case $\overline{P}_2$ line strobes the second latch. The $\overline{OE}$ pins of these latches are grounded. Data transfer is done through the third latch. The data lines of the storage RAM are connected as input to this latch having a port address 308H. The active low P_3 line is connected to the $\overline{CE}$ pin of this latch. Its strobe pin is permanently connected to the V_{CC}. The address of the memory locations are selected by inputting the address bits to the first two latches by the 'OUT' instruction in Basic. Similarly data is outputted to the PC lines from the memory by the 'INP' instruction. The $\overline{CS}$ signal line for the memory chip has got an address 300H - 31FH so that this chip is enabled whatever address bits are latched or data is outputted to PC bus through the latches.

4.4 Analysing capabilities

The software of this unit is written in basic and consists of two parts.

1. For retrieval of data from the battery backed up RAM and storing on a disk file.

2. For analysing data from the disk file.

Programs have been developed for carrying out the following data analysis.

* Listing of data parameterwise in corresponding engineering units along with the time of measurement.

* Listing of average value of parameters for different days.

* Plotting the variation of parameters along with time.

Figs.4.6(a), 4.6(b) and 4.6(c) shows the variation of atmospheric temperature, relative humidity and solar radiation respectively, plotted at 5 minutes interval during a day in June this year. The data was collected around Cochin using the multichannel data acquisition system.

4.5 Development of PCBs

Double sided PCBs of size 110x160 mm^2 and 45x110 mm^2 were designed using SMARTWORK programme for

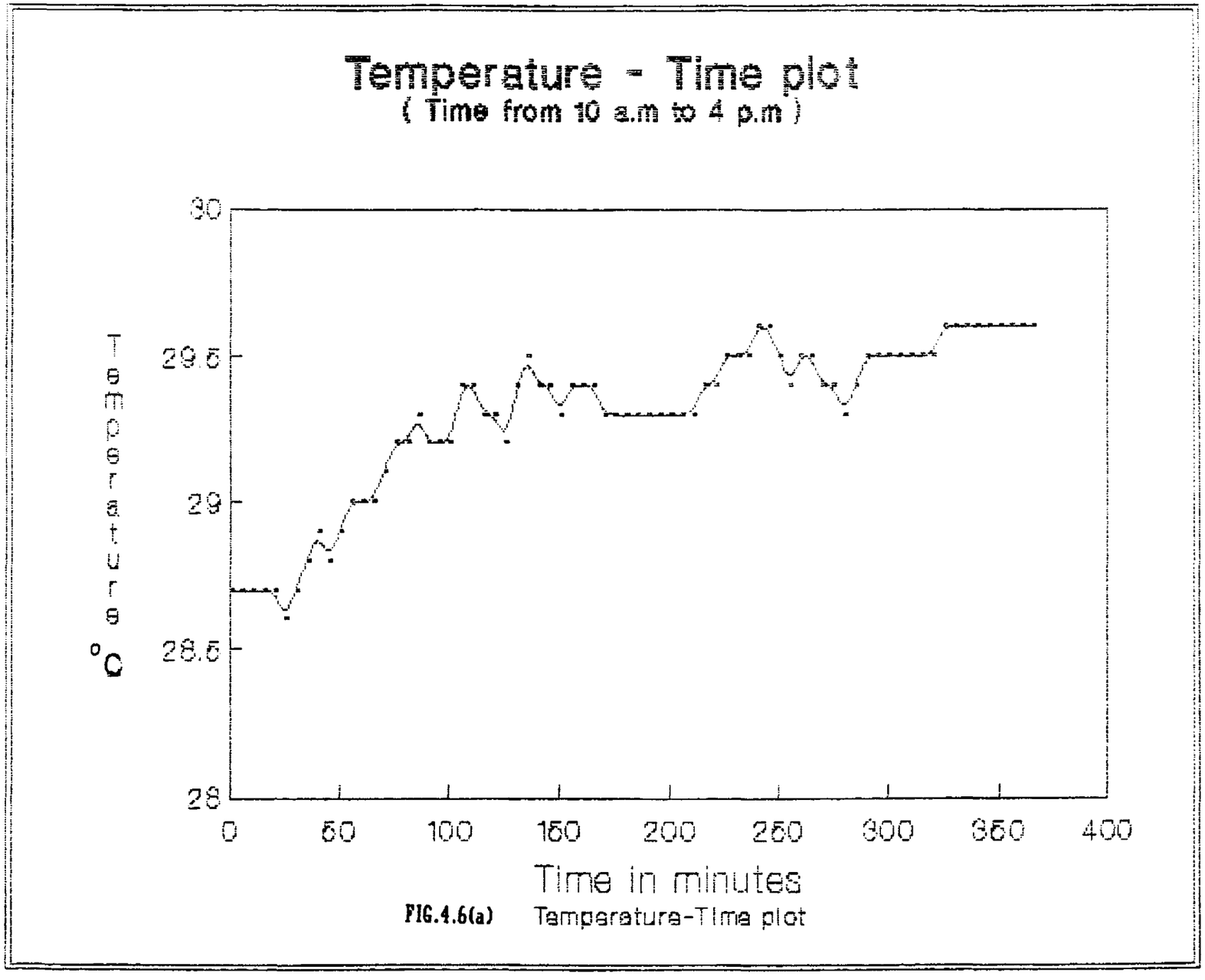

FIG.4.6(a) Temperature-Time plot

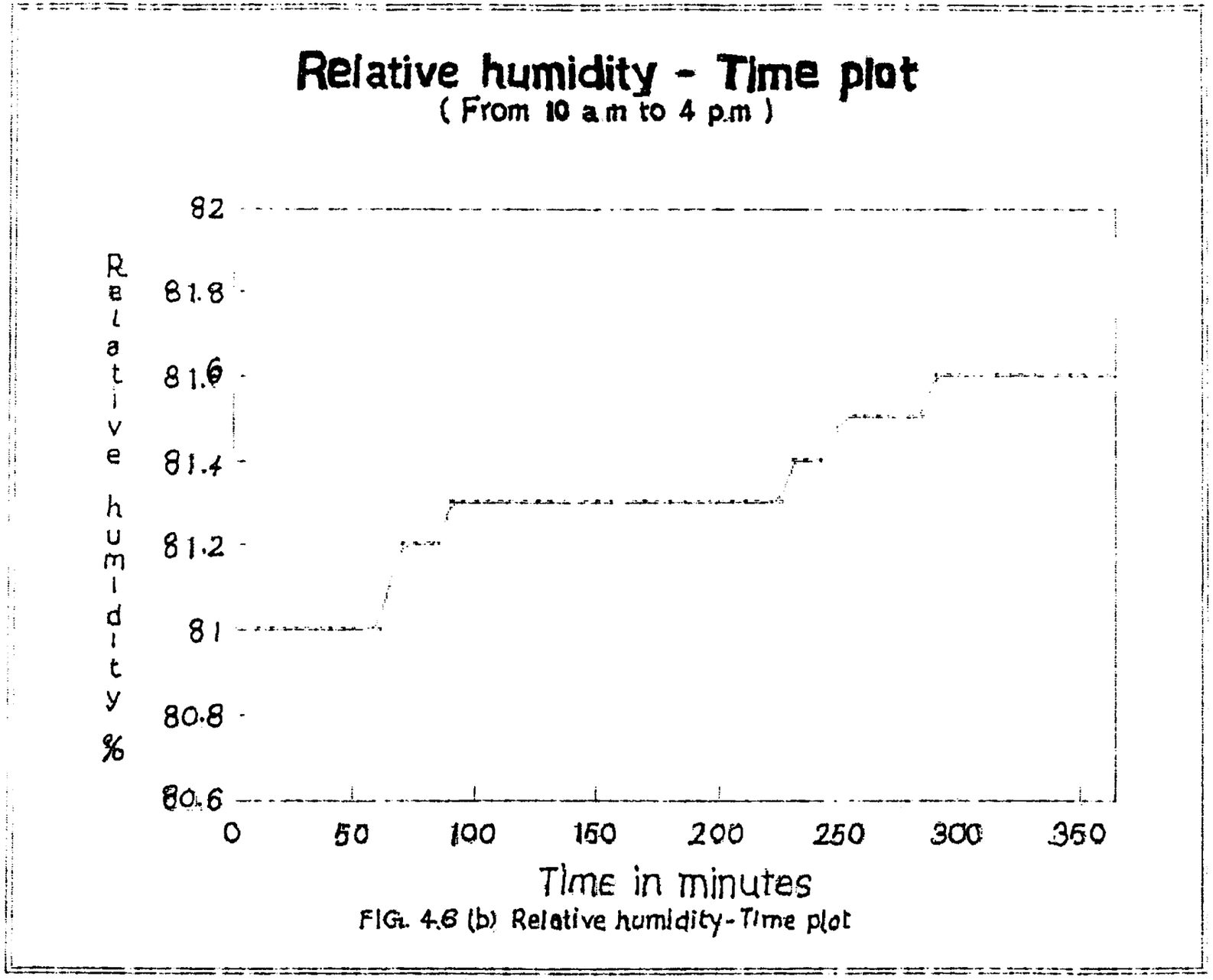

FIG. 4.6 (b) Relative humidity-Time plot

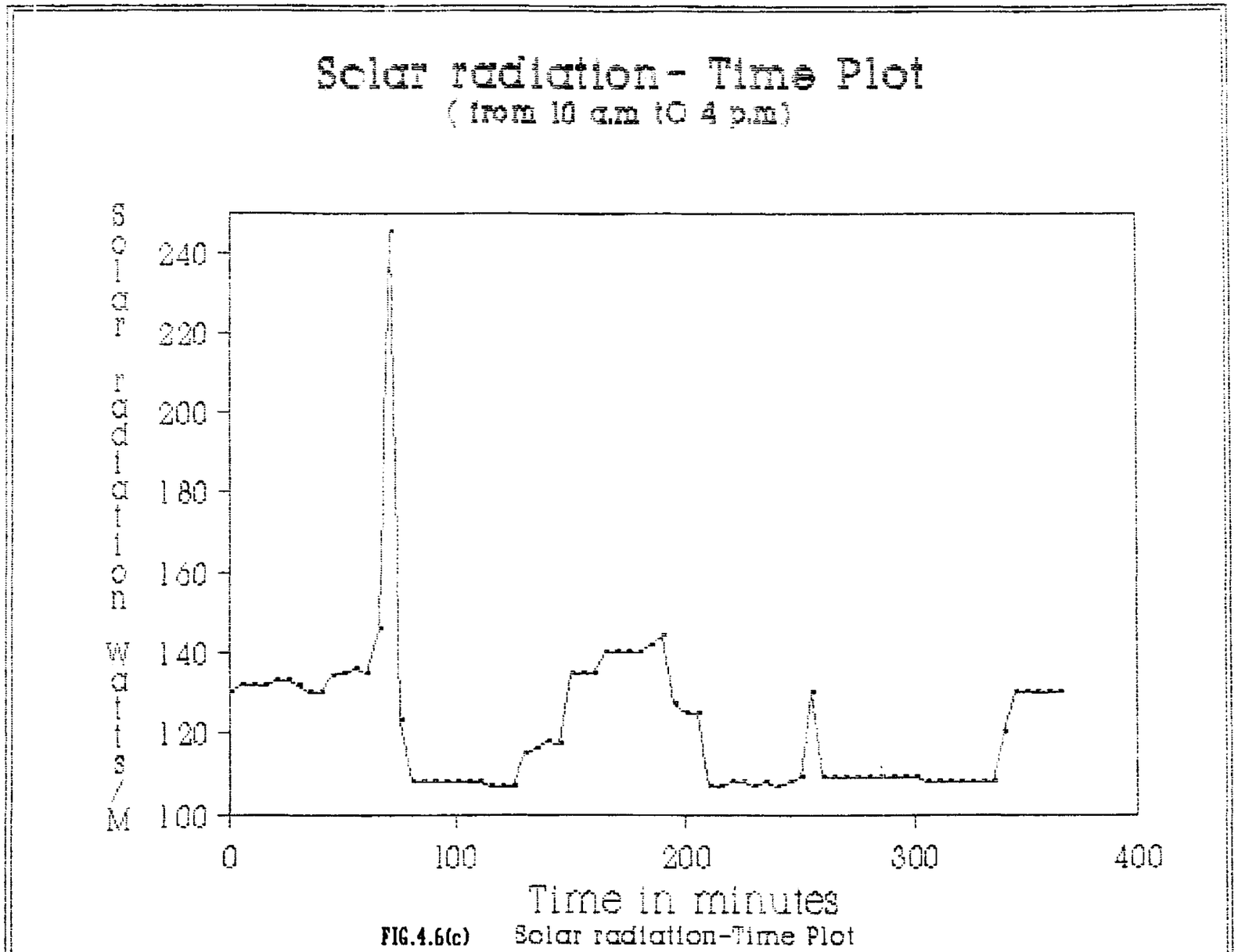

FIG.4.6(c) Solar radiation-Time Plot

the PC interface module and storage interface card respectively. The PCBs were fabricated assembled and tested in the laboratory. Figs.4.7(a) to 4.7(d) shows the layouts of the PCBs developed.

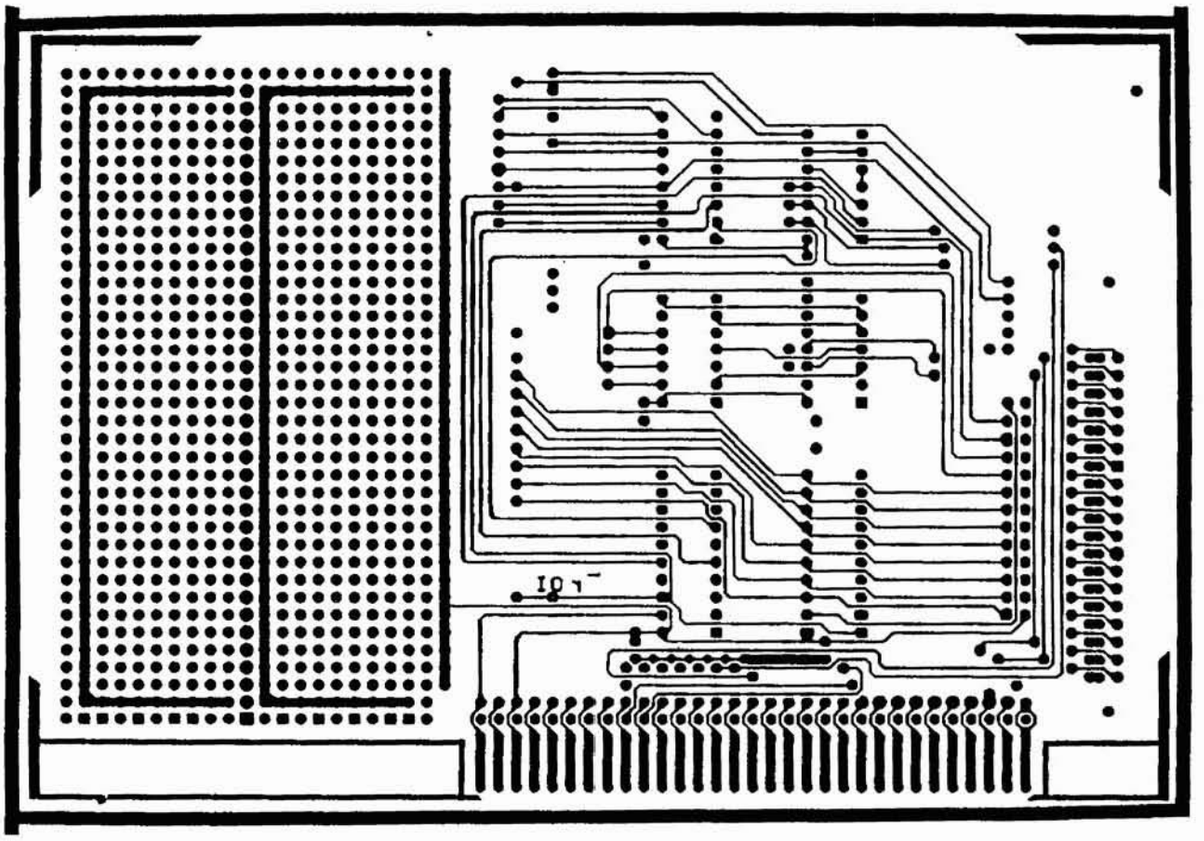

FIG.4.7(a) Layout of PCB for PC interface module
(Solder side)

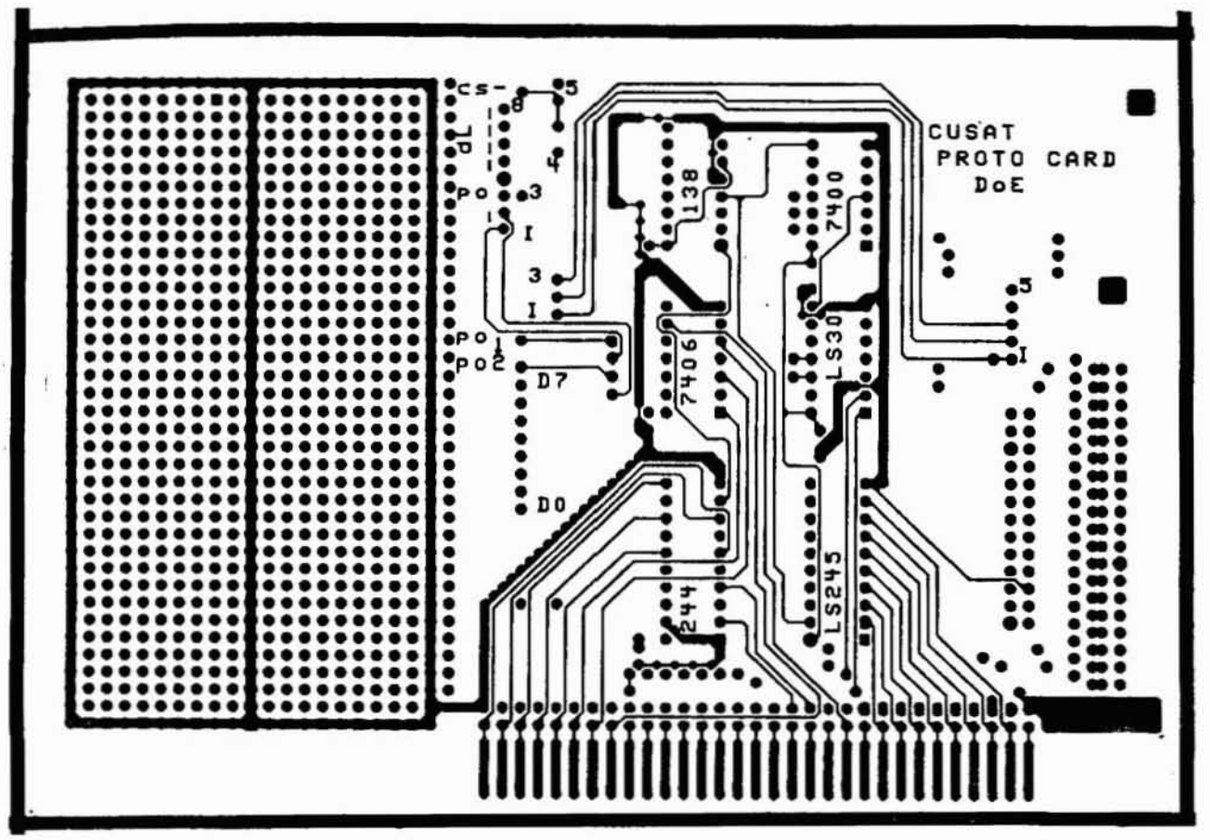

FIG.4.7(b) Layout of PCB for PC interface module
(Component side)

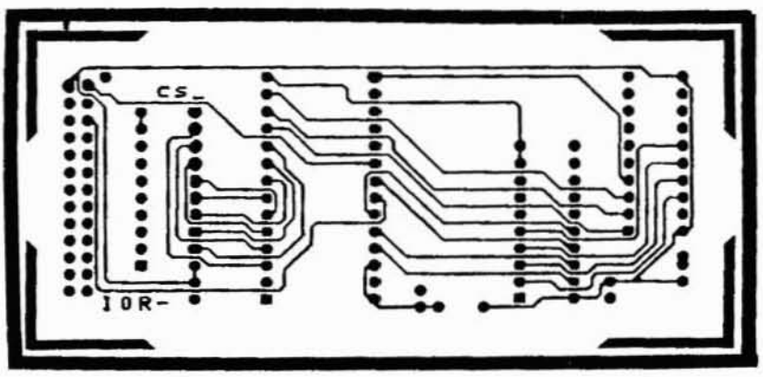

FIG.4.7(c) Layout of PCB for data storage interface (solder side)

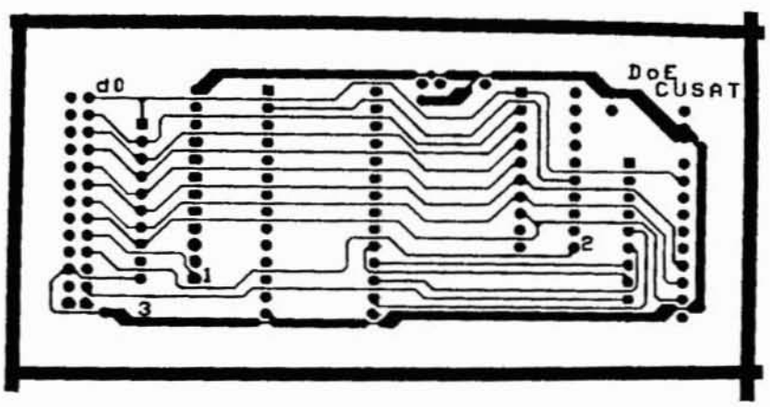

FIG.4.7(d) Layout of PCB for data storage interface (component side)

CONCLUSION

The multichannel remote data acquisition and analysing systems developed have been found to be ideal and very much useful for data collection and analysis from remote areas where power supply is a major constraint, as encountered in many of the environmental studies. The remote data acquisition and storage unit developed consumes very low power so that it is very much suitable for operation from rechargeable batteries. The 8 bit data resolution is found to be sufficient for the data related to different environmental parameters measured using the system. Use of single chip data acquisition system ADC 0816 has reduced the chip count and contributed to less power consumption.

Future Expansion

The remote data acquisition and storage system can easily be incorporated with audio, visual alarms to indicate any malfunctioning of the system.

In cases where it is required, provision for automatic control of the parameters can be incorporated.

The system can further be expanded incorporating automatic remote data acquisition facility with PC based control from the laboratory through wire or wireless link. The processing of data can be on real-time or after storing on mass storage devices.

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