DESIGN TECHNIQUES FOR SIGMA-DELTA BASED ADC FOR WIRELESS APPLICATIONS

A thesis submitted by

BABITA ROSLIND JOSE

for the award of the degree of

DOCTOR OF PHILOSOPHY
(Faculty of Engineering)

DIVISION OF ELECTRONICS

SCHOOL OF ENGINEERING

COCHIN UNIVERSITY OF SCIENCE AND TECHNOLOGY

KOCHI – 682 022

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DECLARATION

*I hereby declare that the work presented in this thesis entitled "**DESIGN TECHNIQUES FOR SIGMA-DELTA BASED ADC FOR WIRELESS APPLICATIONS"** is based on the original research work carried out by me under the supervision and guidance of **Dr. P. Mythili**, Reader, Division of Electronics, School of Engineering, Cochin University of Science and Technology, Kochi-22. This work did not form part of any dissertation submitted for the award of any degree, diploma or other similar title or recognition from this or any other institution.*

Kochi – 682 022 **BABITA ROSLIND JOSE**

30th December 2009

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I would like to express my gratitude to Dr. P. Mythili, Reader, Cochin University of Science and Technology, for the professional and personal guidance and the constant support at all stages of this research.

Also, I would like to thank Dr. Gopikakumari, Head of the department, for her constructive comments in Ph.D reviews

It is difficult to identify many friends who contributed so much unmentioned support. However, I am indebted to Shahana T. K, and Rekha K James for the wholehearted and enthusiastic help at all stages of this research. I take this opportunity to thank all the people in the department for their support.

Finally, I would like to thank our principal and office staff for all other logistical support.

Babita Roslind Jose

Abstract

Analog-to-digital Converters (ADC) have an important impact on the overall performance of signal processing systems. This research is to explore efficient techniques for the design of sigma-delta ADC, specifically for multi-standard wireless transceivers. In particular, the aim is to develop novel models and algorithms to address this problem and to implement software tools which are able to assist the designer's decisions in the system-level exploration phase. To this end, this thesis presents a framework of techniques to design sigma-delta analog-to-digital converters. We present different re-configurable sigma-delta modulator architectures, techniques for coefficient optimization and a tool box.

First, after introducing the basic concepts, a dual mode sigma-delta converter is presented. A modified cascaded 2-2 sigma-delta modulator topology is chosen to meet both Global System for Mobile communications (GSM) and Wideband Code Division Multiple Access (WCDMA) specifications. To reduce sensitivity to operational amplifier non-linearities, both stages are implemented using the sigma-delta modulator with feed forward signal path. Also presented is a cascaded 2-2-2 reconfigurable sigma-delta modulator that can handle GSM, WCDMA and WLAN standards. The modulator makes use of a low-distortion swing-suppression topology which is highly suitable for wide band applications. In GSM mode, only the first stage (2nd order sigma-delta ADC) is used to achieve a peak SNDR of 88dB with an over-sampling ratio of 160 for a bandwidth of 200KHz and for WCDMA mode, a 2-2 cascaded structure (4th order) is turned on with a 1-bit quantizer in the first stage and a 2-bit quantizer in the second stage to achieve 73 dB peak SNDR with an over-sampling ratio of 16 for a bandwidth of 2MHz. Moreover, a 2-2-2 cascaded MASH (Multi-stage noise shaped) architecture with 4-bit in the last stage is proposed to achieve a peak SNDR of 58dB for WLAN for a bandwidth of 20MHz. The novelty lies in the fact that unused blocks of second and third stages can be made inactive to achieve low power consumption. The configurable sigma-delta modulator has been designed in 0.18um CMOS technology, operating from 1.8V supply voltage. The proposed sigma-delta modulator for GSM/WCDMA/WLAN receiver was implemented as a fully-differential switched-capacitor (SC) circuit which has been simulated using SPICE. The design of the individual circuit blocks like operational transconduc-

tance amplifier (OTAs), switches, capacitors and comparators has been done based on behavioral simulation results. The modulator achieves a peak SNDR of 82/68/54 dB for GSM/WCDMA/WLAN standards respectively from the circuit-level implementation.

Secondly, to expedite the handling of complicated design calculations, a Graphical User Interface (GUI) based design tool is also proposed. In particular, multi-standard sigma-delta modulator design for three wireless communication standards consisting of GSM, WCDMA and WLAN is considered. A 2-2-2 reconfigurable sigma-delta modulator is chosen to meet the design specifications of the three standards. The toolbox incorporates most of the important sigma-delta non-idealities. The main non-idealities considered here are finite and nonlinear dc gain, slew rate and gain-bandwidth limitations, amplifier saturation voltage, capacitor mismatch, opamp input referred noise, kT/C noise, clock jitter and DAC capacitor mismatch. The sigma-delta modulator design tool is developed using the Graphical User Interface Development Environment (GUIDE) in Matlab^{TM}.

Finally, in sigma-delta modulator design, the scaling coefficients determine the peak signal-to-noise ratio. Therefore, selecting the optimum value of the coefficient is very important. Towards this, the design of a fourth-order multi-bit sigma-delta modulator suitable for Wireless Local Area Networks (WLAN) receivers with feed forward path is selected as an example. Further, a Genetic Algorithm (GA)-based search method is introduced. In particular, the proposed converter makes use of low-distortion swing suppression SDM (Sigma Delta Modulator) architecture which is highly suitable for low oversampling ratios to attain high linearity over a wide bandwidth. A second-order traditional topology has been chosen as the second design example to validate our proposed method. The basic aim is the identification of the best coefficients suitable for the proposed topology in order to achieve the desired signal-to-noise ratio. GA-based search engine is a stochastic search method which can find the optimum solution within a given set of constraints.

Glossary

ASIC — Application Specific Integrated Circuit;
ADC — Analog-to-digital converter;
BW — Bandwidth;
CMOS —Complementary metal oxide semiconductor;
DAC — Digital to analog converter;
FPGA — Field Programmable Gate Array;
INL —integral non-linearity;
IFFT — Inverse Fast Fourier Transform;
GA — Genetic Algorithm;
GSM — Global System for Mobile communications;
GUI — Graphical User Interface;
GUIDE — Graphical User Interface Development Environment;
MASH — Multi-stage noise Shaped;
Opamp — operational amplifier;
OTA — Operational Transconductance Amplifier;
$\Sigma\triangle$— Sigma-delta;
SOC — System on Chip;
SC — Switched-capacitor;
SR — Slew rate;
SNDR — Signal to Noise-plus-Distortion Ratio;
SDM — Sigma Delta Modulator;
TSMC — Taiwan Semiconductor Manufacturing Company;
WLAN — Wireless Local Area Network;
WCDMA — Wideband Code Division Multiple Access;
WPAN — Wireless Personal Area Network;
UWB — Ultra Wide Band;
SDC — Sigma Delta Converter;

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Chapter 1

Introduction

1.1 Motivation

Rapid evolution of digital integrated circuit technologies has led to sophisticated signal processing systems. Future mobile systems will be able to communicate with various heterogeneous systems which are different by means of the algorithms used to implement baseband processing. This may pose many challenges in designing flexible, energy efficient and adaptable architectures. Moreover, demand for new telecommunication services requiring higher capacities, data rates and different operating modes have motivated the development of new generation multi-standard wireless transceivers. Transceivers for multi-mode and multi-standard telephony are often implemented by replicating the receiver circuits for each operating band or standard (89),(1). By using conventional receiver architectures, simultaneous operation at different frequencies can only be achieved by building multiple independent signal paths which may eventually increase the cost and power dissipation. Therefore, multi-standard receivers often re-use circuit blocks, or multiple RF front-ends (i.e., one for each standard if necessary). To achieve higher data rates in emerging wireless generations , (for example WCDMA, IEEE 802.11b), the analog front-end must be able to handle wider bandwidths at lower noise and power levels. Efficient integration can be obtained by using receiver architectures and circuit techniques that eliminate the need for external components. Utilizing a receiver architecture that performs channel select filtering on

chip at baseband allows for the programmability necessary to adapt to multiple communication standards.

The most important component for the success of multi-mode systems has been the analog-to-digital converter (ADC) that converts continuous time signals to a discrete time, binary coded form for later digital signal processing. Different signal types to be digitized has led to a diverse selection of data converters in terms of architectures, resolution and sampling rates. In the wireless communications arena transmitters and receivers and ADC in particular, have to cope with the requirements imposed by many different standards operating in the same geographical zone, making it necessary for mobile communications equipment to manage multiple standards. A direct conversion of a radio frequency signal to the digital domain directly at the receiver antenna or after some amplification stages will give efficient multi-standard architectures implementation. In digital domain, all other operations to detect and recover the desired signal are performed in a fully digital fashion, by means of programmable hardware. This would allow the upgrading of a mobile terminal completely by software following the evolution of the communications standards, as well as its adaptability to different operating environments. To meet the above requirements analog-to-digital converter requirements on sampling linearity, conversion rate, resolution, and power consumption are becoming stringent. In general, in order to achieve a wide bandwidth and a high resolution, the sampling frequency, the noise-shaping order and the quantizer resolution should be increased (89), (93).

The sigma-delta (64), (46), (5) analog-to-digital converters (ADCs) are widely used in wireless systems because of their superior linearity, robustness to circuit imperfections, inherent resolution-bandwidth trade off and increased programmability in digital domain. Sigma-delta modulator is the most promising candidate to achieve high resolution over a wide variety of bandwidth requirements in multi-mode receivers. Many of the desired integration aspects can be satisfied with sigma-delta converter front-ends. The advantage of sigma-delta ADCs in providing high resolution with low precision components lies on the use of over-sampling and noise shaping. As bandwidth requirement increases, the over-sampling ratio decreases which results in a decrease in the resolution. Designing sigma-delta

modulators that can achieve high resolution and wide bandwidth remains challenging. These solutions based on switched-capacitor (SC) based implementation cover a wide variety of wireless standards like GSM, WCDMA, WLAN etc.

In modern deep-submicron CMOS processes, the ultimate goal is to reduce cost using a single chip solution (system on a chip (SoC)). This brings the additional design challenges in the data converter design, such as decreasing supply voltage, short channel effects (65) in MOS devices, and matching of devices. Therefore, the requirements of sampling linearity, process matching, high DC gain and high gain-bandwidth product opamps in the traditional data converter architectures are becoming more and more difficult to be realized. The performance requirements of analog circuits should be significantly relaxed, so that sigma-delta ADC architectures are suitable for realizing high resolution broadband ADCs with new technologies (24), (45), (8), (86). In this scenario, a novel low-distortion multi-bit sigma-delta modulator with improved performance is indeed essential. This motivates the development of various design techniques considering various non-idealities.

1.1.1 Research Focus

This work focused on the analysis, design techniques and optimization of oversampled sigma-delta ADCs aimed for multimode wireless receivers. Even though the properties of oversampling ADC converters are well known, the increasing bandwidth of the signals to be converted in the communications systems, as well as the required resolution imposed by the standards, require high oversampling ratios. ADCs with higher sampling frequencies and low power consumption is a design challenge, which is an essential constraint of portable systems.

1.2 Author's Contributions

The primary technical contributions of this thesis are in the area of developing design techniques for sigma-delta ADC for multi-standard wireless transceivers. An investigative study was conducted to develop a tool box for the modeling and

analysis. Additionally, a methodology is also developed for coefficient optimization using genetic algorithms. The main contributions and the papers on which they are based are listed below.

J1. Babita Roslind Jose, J. Mathew, P. Mythili, "A Multi-mode Sigma-delta ADC for GSM/WCDMA/WLAN Applications," in *Journal of Signal Processing Systems (Springer),*$DOI 10.1007/s11265-008-0326-z$, ISSN:1939-8018, January 2009.

C1. Babita Roslind Jose, J. Mathew, P. Mythili, "A Triple-mode Feed-forward Sigma-delta Modulator Design For GSM / WCDMA / WLAN Applications", *20th IEEE International System On Chip Conference (IEEE SOCC 2007)*, September 2007.

Author's Contribution: A new low-distortion triple-mode architecture for multi-standard receivers is proposed. This topology is less sensitive to circuit imperfections compared with the traditional one, suitable for wideband applications where low oversampling ratios are used. The author came up with the concept, theoretical formulations and simulations, and wrote the manuscript. The concise version is presented in the conference and extended version is published in the journal.

J2. Babita Roslind Jose, J. Mathew, P. Mythili, "Dual-Band Sigma-delta ADC for WCDMA/WLAN Receivers", in *International Journal of Applied Engineering and Research, vol 3, pp.257-273* , 2008.

C2. Babita Roslind Jose, J. Mathew, P. Mythili, "A Low Power Programmable Sigma-Delta Modulator for Dual-Band Multi-Mode Receivers", *International Conference on Embedded Systems and Applications (ESA'07)* , 2007.

Author's Contribution: A programmable sigma-delta modulator for dual-band multi-mode receivers is proposed, which is less sensitive to circuit imperfections compared with the conventional architectures. The author came up with the concept, theoretical formulations and simulations, and wrote the manuscript. The concise version is presented in the conference and extended version is published in the journal.

J3. Babita Roslind Jose, J. Mathew, P. Mythili, " Wideband Low-Distortion Sigma-Delta ADC For WLAN With RNS Based Decimation Filter", in *IETECH*

Journal of Information Systems, International Engineering & Technology Publications, vol.2, No.2, pp.68-75 , 2008.

C3. Babita Roslind Jose, Shahana T K, P. Mythili, " Wideband Low-Distortion Sigma-Delta ADC For WLAN With RNS Based Decimation Filter ", *IET International Conference on Information and Communication Technology in Electrical Sciences (ICTES 2007)*, Chennai, December, 2007.

Author's Contribution: A highly linear sigma-delta ADC with a high speed computationally efficient RNS (Residue Number System) based decimation filter is proposed for WLAN applications. The low-distortion topology has reduced sensitivity to OTAs (Operational Transconductance Amplifier) nonlinearity effects and simplifies the implementation of cascaded architecture. The author came up with the concept, theoretical formulations and simulations, and wrote the manuscript. Co-author developed decimation filter. The concise version is presented in the conference and extended version is published in the journal.

J4. Babita Roslind Jose, J. Mathew, P. Mythili, "GA-based Optimization of Sigma-delta Modulators for Wireless Transceivers" in *Engineering letters, vol 16, no.4, pp.473-479*, 2008.

C4. Babita Roslind Jose, J. Mathew, P. Mythili, "GA-based Optimization of a Fourth-order Sigma-delta Modulator for WLAN". *IEEE International Conference on Systems, Man & Cybernetics*, 12-15 October 2008, Singapore, 2007.

Author's Contribution: A new optimization technique using Genetic Algorithm is proposed. This approach gives better and fast optimization of modulator coefficients. The author came up with the concept, theoretical formulations and simulations, and wrote the manuscript. The concise version is presented in the conference and extended version is published in the journal.

C5. Babita Roslind Jose, Shahana T.K., P. Mythili, "GUI-based Sigma-delta Modulator Design Tool for Multi-standard Wireless Transceivers", *National Conference On Communication Engineering, Signal Processing and VLSI Design*, 16-18 December 2009, Cochin, India.

Author's Contribution: A new tool box is developed to aid design and analysis of multi-standard sigma-delta modulator design. This toolbox will help

the user to do a quick design and analysis. The author came up with the concept and developed the tool box. The concise version is presented in the conference and a journal version is under preparation.

1.2.1 Other Contributions not Included in this Thesis

J1. Shahana T. K, **Babita R. Jose**, Rekha K. James, K. Poulose Jacob, Sreela Sasi, "RNS based Programmable Decimation Filter for Multi-Standard Wireless Transceivers," in *ECTI Transaction on Electrical Engineering, Electronics and Communications, ECTI-Transaction Journal, Vol. 6, No. 2, pp. 57-66, 2008.*

J2. Shahana T. K, **Babita R. Jose**, Rekha K. James, K. Poulose Jacob, Sreela Sasi, "A Novel Sigma-Delta based Parallel Analog-to-Residue Converter," in *International Journal of Electronics, Taylor and Francis, 2009.*

J3. Shahana T. K, **Babita R. Jose**, K. Poulose Jacob, Sreela Sasi, "RRNS-Convolutional Concatenated Code for OFDM based Wireless Communication with Direct Analog-to-Residue Converter, " in *International Journal of Electrical, Computer and Systems Engineering, World Academy of Science, Engineering and Technology, Vol. 2, No. 2, Spring 2008, pp.86-93, 2009.*

J4. Shahana T. K, **Babita R. Jose**, Poulose Jacob, Sreela Sasi, "Decimation Filter Design Toolbox for Multistandard Wireless Transceivers using Matlab," in *International Journal of Signal Processing, Volume 5, Number 2, 2009* .

C1. Shahana T. K, **Babita R. Jose**, Rekha K. James, K. Poulose Jacob, Sreela Sasi, "Dual-Mode RNS based Programmable Decimation Filter for WCDMA and WLANa," in *IEEE International Symposium on Circuits and Systems (ISCAS 2008).*

C2. Shahana T. K, **Babita R. Jose**, Rekha K. James, K. Poulose Jacob, Sreela Sasi, "RNS based Programmable Multi-mode Decimation Filter for WCDMA and WiMAX," in *IEEE 67th Vehicular Technology Conference: VTC 2008-Spring,11-14 May, Singapore.*

C3. Shahana T. K, **Babita R. Jose**, Rekha K. J., K. Poulose Jacob, Sreela Sasi, "RRNS-Convolutional encoded Concatenated Code for OFDM based

Wireless Communication," in *16th IEEE International Conference on Networks (ICON 2008)*, New Delhi, India, 12-14 December 2008 .

C4. Shahana T. K, Rekha K. J., **Babita R. Jose**, K. Poulose Jacob, Sreela Sasi, "Polyphase Implementation of Non-recursive Comb Decimators for Sigma-Delta A/D Converters," in *IEEE International Conference on Electron Devices and Solid-State Circuits*, Taiwan, December 20-22, 2007.

1.3 Thesis Outline

Chapter 2 provides the background material relevant to this thesis. Since, majority of the techniques described in this thesis is for Ato D converters, in particular sigma-delta ADC, the basics of sigma-delta analog-to-digital converters is reviewed.

Chapter 3 describes system level design of a re-configurable sigma delta analog-to-digital converter for three wireless communication standards namely GSM, WCDMA and WLAN, which reduces the overall system complexity in software defined radios. A low-distortion swing suppression topology has been selected for our architecture which has reduced sensitivity to op-amp non-linearities, especially at low oversampling ratios. The expressions for the coefficients are derived from the fundamentals. The triple mode design, when compared with existing techniques, gives better performance. This chapter also describes a dual mode design for GSM and WCDMA. Chapter 4 deals with configurable sigma-delta modulator implementation. The proposed sigma-delta modulator for GSM/WCDMA/WLAN receiver was implemented as a fully-differential switched-capacitor (SC) circuit which has been simulated using SPICE. The design of the individual circuit blocks like operational transconductance amplifier (OTAs), switches, capacitors and comparators are described.

Chapter 5 introduces a design tool box for sigma delta converters. A Matlab^{TM} based toolbox help the designers to choose appropriate architecture based on the requirement. To mitigate the design time, various architectures have been designed using Simulink. Various non-linearity models are also incorporated into the tool.

Chapter 6 describes genetic algorithm which is used for the identification of the best coefficients suitable for the proposed sigma-delta topology in order to achieve the desired signal-to-noise ratio. GA-based search engine is a stochastic search method which can find the optimum solution within the given constraints.

The last chapter summarises the work presented in this thesis and provides an outlook of future work.

Chapter 2

Background

Mobile communication has seen a tremendous explosive growth since 1983. The recent advances in technologies for wireless access, digital signal processing, integrated circuits, and increased battery life have continued the exponential growth in mobile and personal communication services. The need for multi-mode cellular handsets that support a wide range of communication standards, each with a different RF frequency, signal bandwidth, modulation scheme, etc. is currently driving worldwide research towards the implementation of fully integrated multi-standard transceivers. In order to allow the user to switch seamlessly among different standards, the so-called "global roaming" for both voice and data applications, all these standards have to be supported by an integrated transceiver.

Software defined radios (SDRs) have become a promising solution to support multiple competing and incompatible air interface standards in future wireless communications. The ideal architecture for multi-standard transceiver is the software radio as shown in Figure 2.1 (54). The transceiver incorporates most of the functionality in software as possible, along with the flexibility of maximum hardware sharing of the transceiver building blocks which will help us to reduce cost as well as power consumption. Thus re-configurability is a major concern in multi-standard receiver design while meeting the design specification of the various standards. This in turn generates several design challenges for the analog and digital building blocks.

Sigma-delta analog-to-digital converters (SD-ADCs) are widely used in multi-standard transceivers to adapt to the requirements of different standards. Sigma-

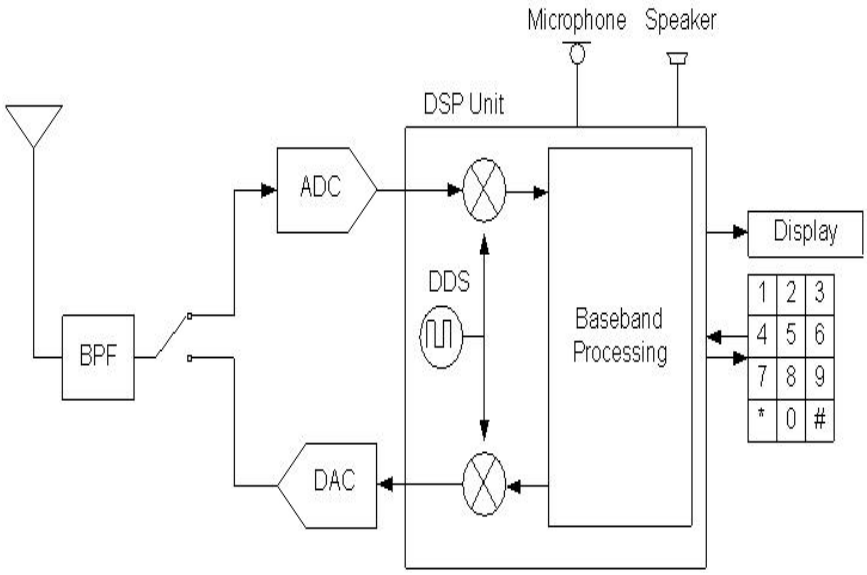

Figure 2.1: Ideal software radio transceiver

delta ADC is one of the promising candidate to achieve high resolution over a wide variety of bandwidth requirements in multi-mode receivers. Based on the multi-standard approach, some important specifications of GSM, WCDMA and WLAN (IEEE 802.11b) are collected and listed in Table 2.1 (54).

Taking into account the above considerations, different receiver architectures are discussed focusing on the feasibility of fully integrated implementation for multi-standard solution (42).

Table 2.1: Specifications of GSM, WCDMA and WLAN standards

	Frequency range	Channel Spacing	Modulation Scheme	Duplex	Channel bandwidth
GSM 900	Tx- 890 - 915 MHz	200 KHz	GMSK	FDD	190 KHz
WCDMA (UMTS)	Rx- 935 960 MHz Tx- 1920-1980 MHz Rx-2110 - 2170 MHz	5 MHz	QPSK	TDD FDD	3.84 MHz
WLAN (IEEE 802.11b)	Tx, Rx 2.4, 2.4835 GHz	25 MHz	1Mbps: DBPSK 2Mbps: DQPSK 5.5Mbps: CCK 11Mbps: CCK	TDD	22 MHz

2.1 Radio Receiver Architectures

In this section, we discuss the receiver at the architectural level. Complexity, cost, power dissipation and integration level have been the primary criteria in selecting transceiver architecture. Furthermore, multi-standard capability is another important factor (54), (6), (27)

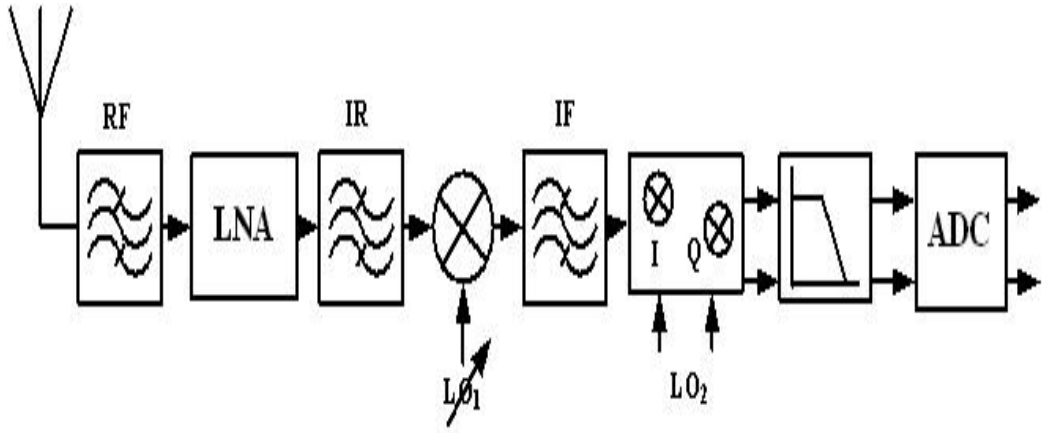

Figure 2.2: Superheterodyne receiver

2.1.1 Superheterodyne Receiver

A conventional architecture choice is the superheterodyne receiver shown in Figure 2.2. Here the incoming RF signal received by the antenna is sent through an RF filter and a low noise amplifier (LNA) which amplifies the received signal. An image reject (IR) filter removes any image frequencies present which is then given to a mixer. Then mixing with a tunable LO signal at RF down converts the selected channel to IF. An off-chip, high-Q band pass filter performs partial channel filtering at a relatively high intermediate frequency. A second down conversion mixing step translates the signal down to baseband and further reduces the requirements for the final, integrated channel selection filter. Therefore, the use of a RF (Radio Frequency), IR (Image Rejection) and IF (Intermediate Frequency) filters turns this architecture unsuitable for integration and consequently for multi-standard purposes that would require even more off-chip filters.

2.1.2 Direct Conversion Homodyne Receiver

The homodyne architecture shown in Figure 2.3 uses a single frequency translation step to convert the RF channel directly to baseband without operations at intermediate frequencies. It is therefore also called zero-IF or direct conversion architecture. Channel selection is done by tuning the RF frequency of the LO to the centre of the desired channel, making the image equal to the desired channel. Hence, the problem of images is not present, and the off-chip IR filter can be omitted. A subsequent channel selection low-pass filter (LPF) then removes nearby channels or interferers prior to A/D conversion. Thus channel filtering is now possible entirely on-chip due to direct conversion to DC. Therefore, the direct conversion receiver is more suitable for higher integration and multi-standard operation. On the other hand, DC offset and flicker noise are the problems associated with this type of architectures.

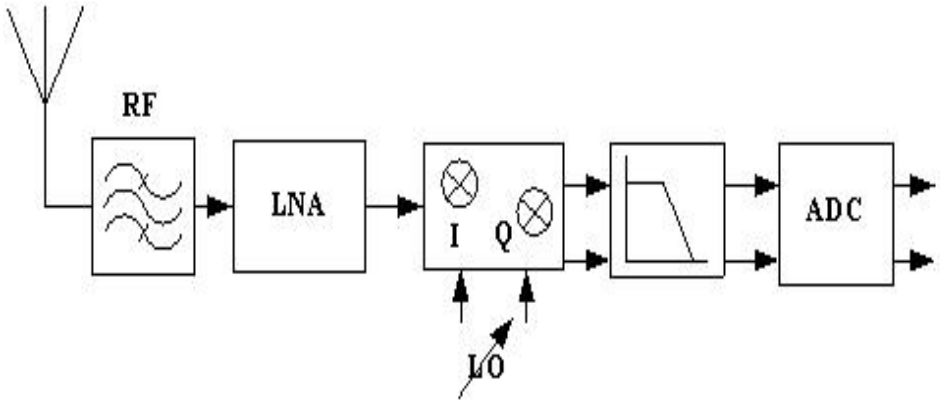

Figure 2.3: Direct conversion homodyne receiver

2.1.3 Low-IF Receiver

The low IF receiver shown in Figure 2.4 converts the received RF signal to a low intermediate frequency, eliminating the problems of DC offset and 1/f noise associated with the direct conversion. A low IF on-chip bandpass filter is used to perform baseband channel selection. Besides maintaining the same level of integration as the Zero-IF, multi-standard ability is affected, since the more severe

constraints are posed on bandpass filter and ADC for wide channel bandwidth, leading to an increase in power consumption.

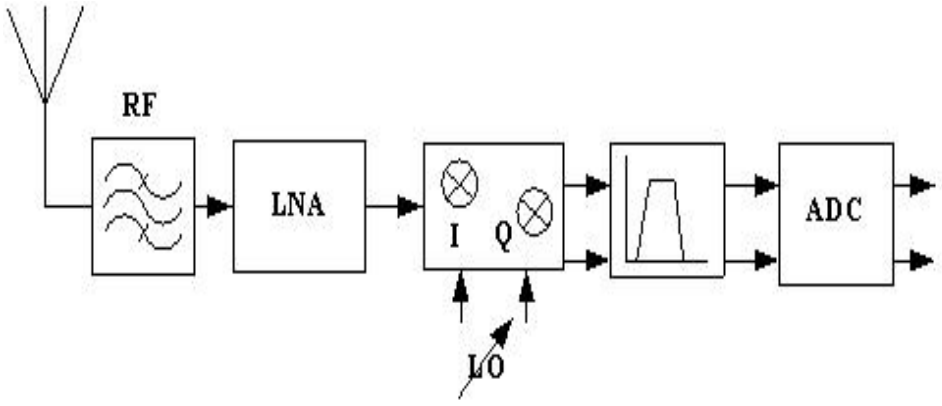

Figure 2.4: Low-IF receiver

2.1.4 Wideband IF Double-conversion Receiver

An alternative architecture well suited for integration of the entire receiver is wideband IF with double conversion shown in Figure 2.5. This receiver employs a two-step conversion from RF to IF and from IF to DC. Though the first mixer with fixed LO frequency, the RF frequency signal goes down to the IF and then straight to baseband with another programmable mixer. This architecture combines the strengths of heterodyne and homodyne receivers and, it has a high degree of integration and programmability suitable for multi-standard operation. This architecture also suffers from DC offsets as in homodyne receivers.

Analog-to-Digital Converters (ADC) is one of the fundamental building block in any transceiver architecture. As a bridge between the analog-to-digital world, the ADC functions as a translator from an analog quantity to a digital code.There are many types of ADCs and each of them has its own advantages and shortages. Among them the sigma-delta $\Sigma\triangle$ ADC features high resolution without requirement of high-precision devices, making it a popular choice of high resolution ADCs in cheap CMOS technologies.

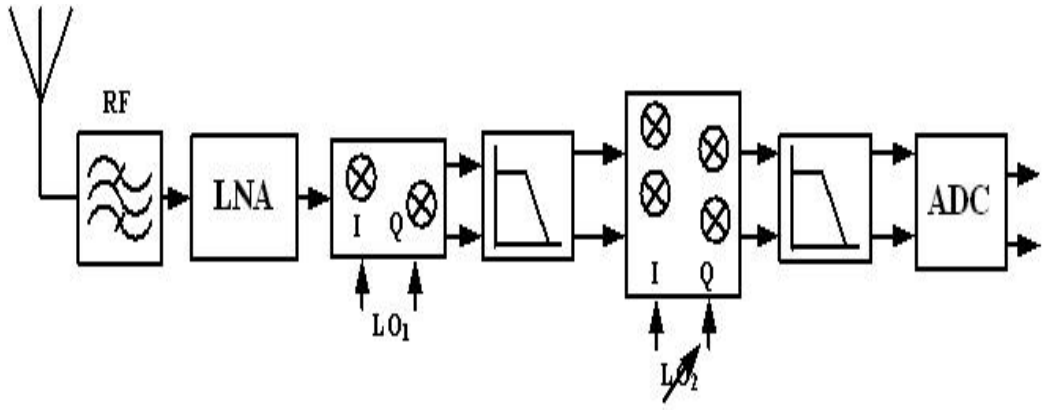

Figure 2.5: Wideband IF double conversion receiver

2.2 Analog-to-digital Converters

For an ADC, the most important parameters are input signal bandwidth and the resolution. Illustrated in Figure 2.6, there are many applications that need different input signal bandwidth and resolution parameters. Different types of ADCs are developed according to different requirements. The Figure 2.6 also shows different types of ADC that can be used for different applications. The $\Sigma\triangle$ ADC is suitable for high resolution low-speed applications such as industrial measurement, voiceband, audio where the conversion speed is normally less than a few hundred Hz (92), (78). For conversion speeds of 100KHz to 1MHz, successive approximation ADC find its best position. For higher conversion speeds, the pipelined ADC is suitable and the resolution is normally around 10-12 bit. For conversion speed of 1GHz and above, it is the area of the Flash ADC. So there is a speed and resolution trade-off in ADC performance, which can be seen from Figure 2.6 (43).

2.3 Classification of ADC

The ADCs are generally classified as Nyquist rate ADCs and Oversampling ADCs based on the rate at which the signal is sampled relative to the signal bandwidth.

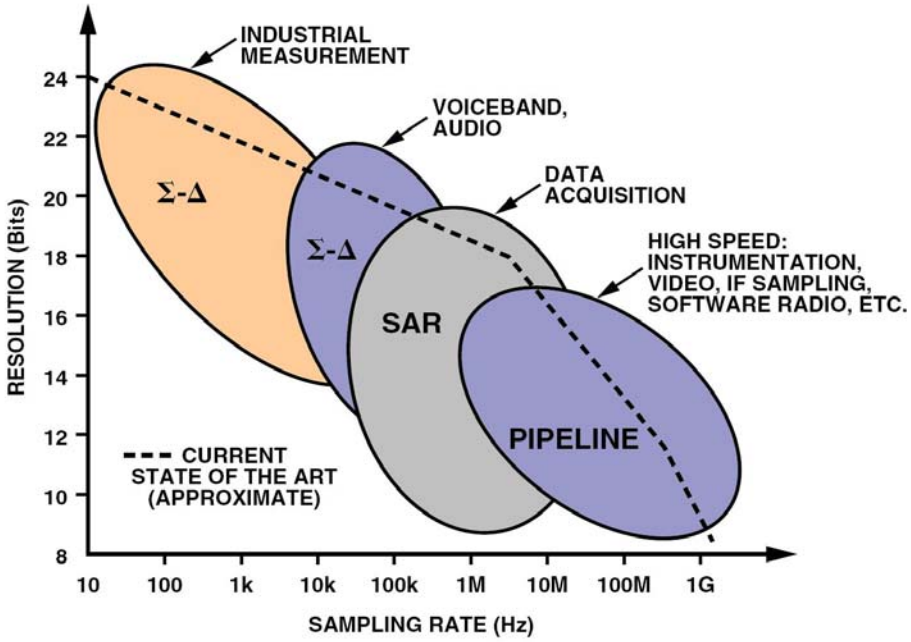

Figure 2.6: Different ADC architectures, applications, resolution and sampling rates

2.3.1 Nyquist rate ADCs

Nyquist rate ADCs sample the signal at approximately twice the signal bandwidth, which is the minimum rate required for the reconstruction of the signal according to sampling theorem. Nyquist rate ADCs are fast, but their resolution is limited to 10-12 bit range due to stringent component matching and circuit non-idealities. Also, the antialiasing filter requires a very sharp cut off to avoid aliasing. Examples of Nyquist rate ADCs are flash ADC, successive approximation ADC, pipelined ADC etc, whose conversion rates are constrained by the bandwidth limitations imposed by the implementation technology (35).

2.3.2 Oversampling ADCs

Oversampling ADCs sample the analog input signal at a rate much higher than the Nyquist rate. The ratio of the sampling rate and the Nyquist rate is called the oversampling ratio (OSR). ADCs exchange resolution in time for resolution

in amplitude (4) in order to ease the demands on the precision with which the signal must be quantized. This class of ADCs do not require stringent component matching requirements and hence are more suitable for high resolution applications (upto 20-bits or more). In Nyquist-rate converters, each digital word is obtained from an accurately quantized input samples, whereas in oversampled converters, each output is obtained from a sequence of coarsely quantized input samples. Oversampling converters take advantage of todays VLSI technology providing high-speed/high-density digital circuits rather than accurate analog circuits by performing most of the conversion process in the digital domain. The analog part of these converters is relatively simple and occupies a small area, unlike their Nyquist rate counterparts. Most implementations use switched capacitor techniques. In the state-of-the art oversampling ADCs, oversampling ratio is typically between 8 and 256 . Another advantage is very relaxed requirement on the analog antialiasing filter because of the high sampling rate. Sigma-delta ADC is an oversampling ADC in which oversampling and noise shaping are the two key techniques used to achieve high accuracy.

2.4 Basic Analog-to-Digital Conversion

Signals that are progressing continuously in time and amplitude are classified as analog signals. An analog-to-digital converter (ADC) produces a digital representation of the analog input signal by sampling the input signal at discrete time moments and quantizing the amplitude of the input signal in discrete amplitude levels (4). Thus the A/D conversion includes two procedures: 1) sampling, to make the signal discrete in time and 2) quantizing, to make the signal discrete in amplitude (66). Accordingly there are two important specifications for an ADC: speed and resolution. The speed represents how fast the discretization in time can be done. The resolution represents how accurate the discretization in amplitude can be done. ENOB (Effective Number of Bit) is often used to characterize the conversion resolution. Figure 2.7 shows the block diagram of an ADC.

The antialiasing filter is used to limit the bandwidth of the analog input to less than half of the sampling frequency. This ensures that the sampling operation will not alias noise or out-of-band signals back into the baseband of the ADC.

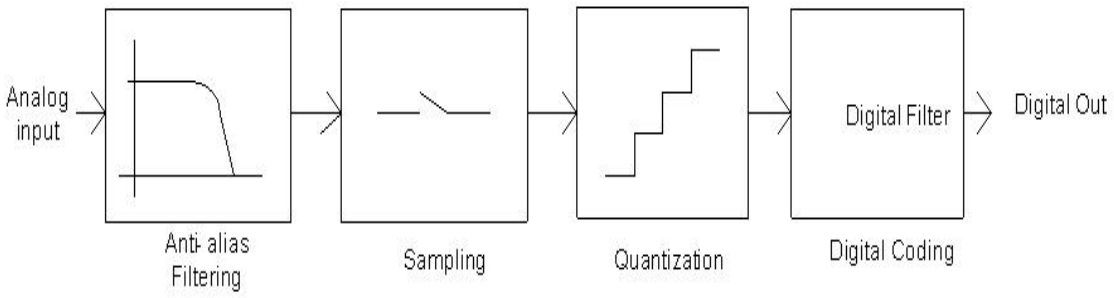

Figure 2.7: Block diagram of analog-to-digital conversion

The width of the antialias filters transition band increases with the sampling rate relative to input signal bandwidth (BW). The quantized signal is digitally encoded based on the resolution which in turn dictates the quantization error.

2.4.1 Sampling

Figure 2.8 shows the sampling operation. Ideal uniform sampling of a continuous-time, band-limited signal, x(t) corresponds to a multiplication of that signal by an ideal impulse train which results in a sampled signal $x_s(t)$ with uniformly spaced samples obtained at nT, where T is the inverse of the sampling frequency, f_s. The sampled signal $x_s(t)$ can be described as a continuous time signal by

$$x_s(t) \;=\; \sum_{n=-\infty}^{n=\infty} x(t)\partial(t-nT), \quad where \;\; \partial(t-nT) = \left\{ \begin{array}{l} 1, t = nT \\ 0, t \neq nT \end{array} \right\} \qquad (2.1)$$

In the frequency domain this is equivalent to convolving the input spectrum with a train of impulses and results in images of the input spectrum centered at integer multiples of the sampling frequency as shown in Figure 2.8.

2.4.2 Quantization

Quantization is the discretization in amplitude as shown by the characteristic curve of Figure 2.9(a). For an ADC, there is always an error e_q defined by equation 2.2 associated with the ADC. This error is called quantization error. The higher resolution the ADC is, the smaller quantization error it has. Since

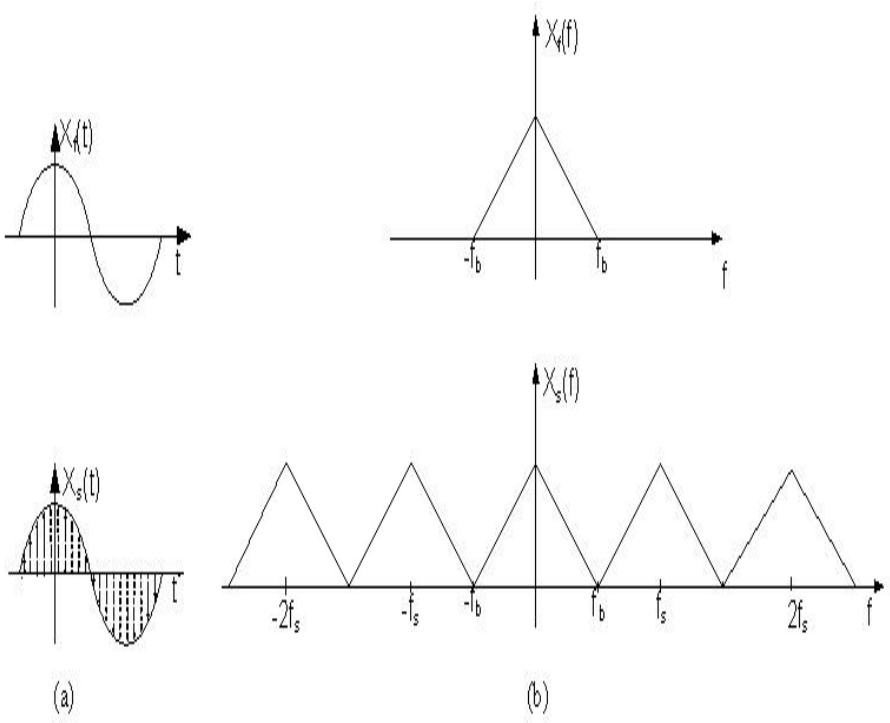

Figure 2.8: Sampling operation (a) in time domain (b) in frequency domain

the process of quantization is a classification process in amplitude, there is always a quantization error in an ADC, as shown in Figure 2.9(b). The quantization error e_q is smaller than the quantization step Δ of the ADC.

$$e_q \;=\; y \;-\; x \tag{2.2}$$

$$-\frac{\Delta}{2} \leq e_q \leq \frac{\Delta}{2} \tag{2.3}$$

The quantization step Δ , with a value of $V_{ref}/2^N$ is called the least significant bit (LSB) of an ADC. Assuming the quantization error is uniformly distributed between ±LSB/2, the quantization error power is related to the quantization step:

$$e_q^2 = \frac{1}{LSB}\int_{-LSB/2}^{LSB/2} e_q^2 de_q = \frac{\Delta^2}{12} \tag{2.4}$$

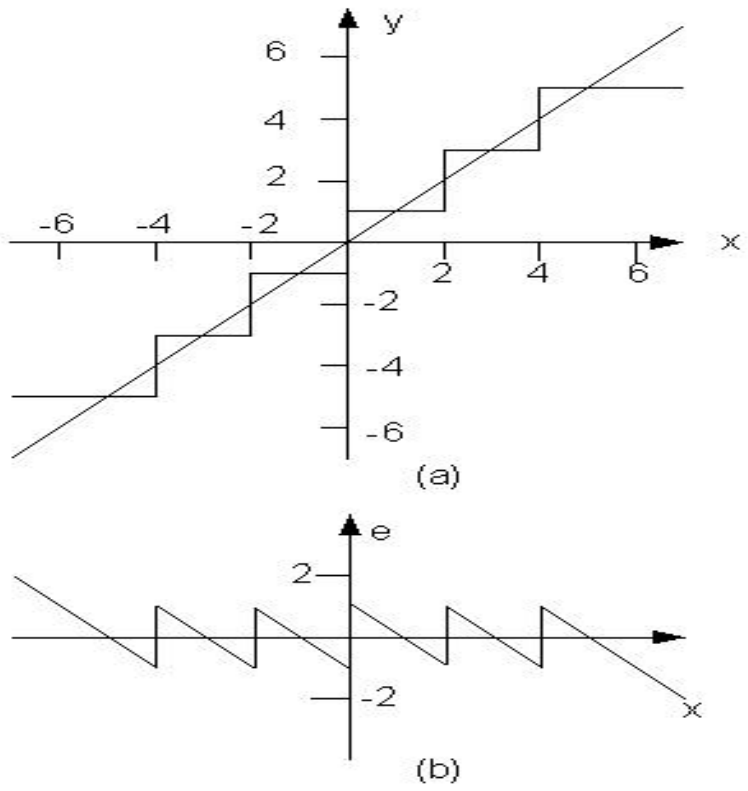

Figure 2.9: (a)Characteristic transfer curve for multi-level quantization (b) Resulting error

The quantization error is dependent on the resolution of the ADC and it is often referred to as the quantization noise of an ADC. The quantizer can be modeled as a quantization noise source, shown in Figure 2.10. From the equation 2.4, the peak SNR of an ideal N bit ADC for a sinusoidal input signal can be calculated as shown in equation 2.5

$$SNR_p = 10\log(\frac{e_s^2}{e_q^2}) \quad = 6.02N + 1.76dB \tag{2.5}$$

where e_s^2 is the maximum input signal power. Here equation 2.5 gives the best possible SNR for a N-bit ADC.

2.4.3 Quantization Noise

The noise resulting from the quantization process is called the quantization noise and it is independent of the input signal. Moreover, the quantization noise power spectral density $S_e(f)$ is white and uniformly distributed in the sampling frequency band $\pm f_s/2$, where f_s is the sampling frequency. The total quantization power is $\Delta^2/12$, so the amplitude of the power spectral density is:

$$h_e = \left[\frac{\Delta^2}{12}\right] \frac{1}{f_s} \tag{2.6}$$

as shown in Figure 2.11. The total power of the quantization noise is evenly distributed within $\pm f_s/2$. As the sampling frequency increases, the amplitude of the spectral density decreases, but the total quantization noise power remains the same.

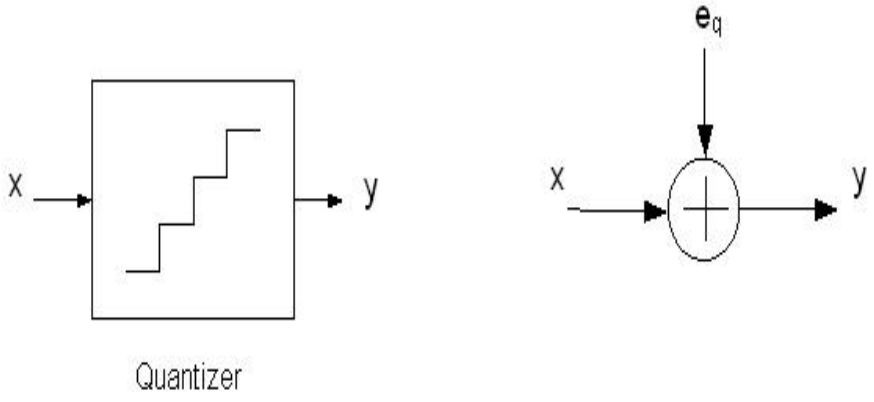

Figure 2.10: Linear model of a quantizer

2.5 Oversampling ΣΔ ADCs : Fundamentals

In contrast to Nyquist-rate ADCs, oversampling ΣΔ converters make use of two key techniques to decrease the quantization error power within the signal band and increase the accuracy of the A-to-D conversion. These techniques are oversampling and noise shaping (76).

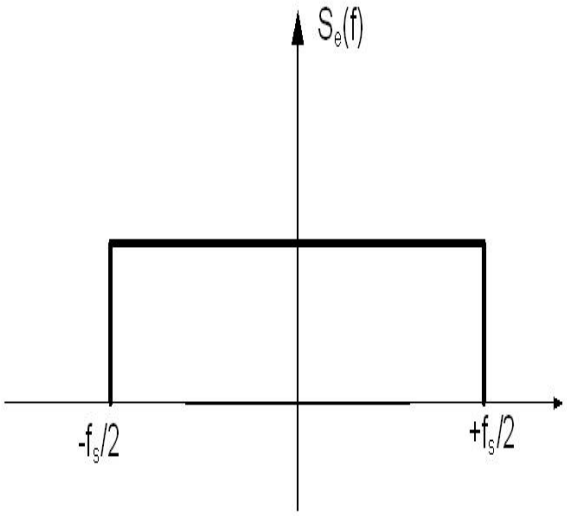

Figure 2.11: Power spectral density of quantization noise

2.5.1 Oversampling

Oversampling consists of sampling a signal faster than Nyquist rate- the minimum sampling frequency required to avoid aliasing. How much faster than required the signal is sampled is expressed through the oversampling ratio, defined as the ratio between the sampling frequency and the Nyquist frequency.

$$OSR = \frac{f_s}{f_n} = \frac{f_s}{2f_B} \tag{2.7}$$

In an oversampled converter, the power of the quantization error is uniformly distributed across the sampling frequency -f_s/2 to +f_s/2, but only a part of the total error falls within the signal band, as long as $f_s > 2f_B$ as shown in Figure 2.12. A low-pass decimation filter can be used to eliminate the quantization noise that falls outside the signal band f_B. Thus the quantization noise power is reduced to equation 2.8.

$$P_e = \int_{-f_s/2}^{f_s/2} S_e(f) \left|H(f)\right|^2 df = \left(\frac{\Delta^2}{12}\right) \frac{1}{OSR} \tag{2.8}$$

Therefore, by using an oversampling technique, the quantization noise power of an ADC can be reduced by a factor of OSR. It is an effective way to increase

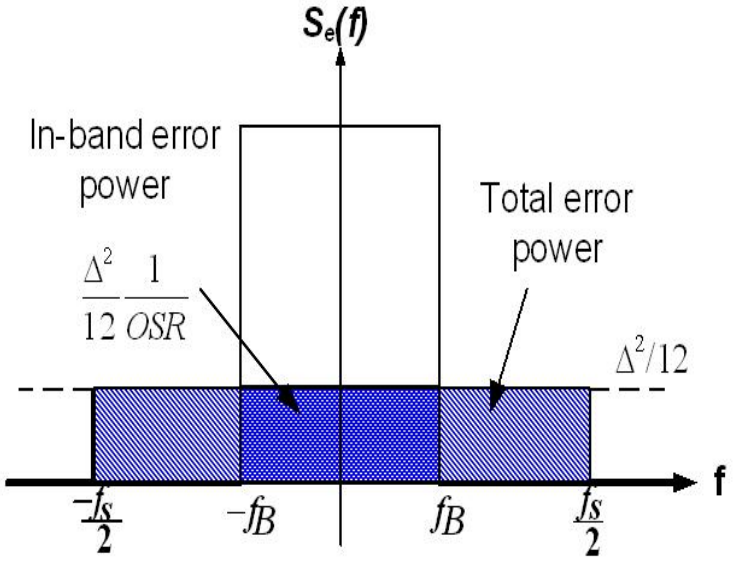

Figure 2.12: PSD of the quantization error in an oversampled converter. Total power of the quantization error and power within the signal band are highlighted

the SNR, and hence the resolution, of an ADC system. Therefore, the peak SNR now is given by equation 2.9

$$SNR_p = 10\log(\frac{e_s^2}{P_e}) = 6.02N + 1.76 + 10log(OSR)dB \tag{2.9}$$

This formula clearly shows the benefit of oversampling. For example, the peak SNR of an ADC can be increased by 3 dB by doubling the sampling frequency, i.e. the resolution of the ADC increases by 0.5 bit/octave. Therefore, an increase in OSR augments the effective resolution of the converter, but reduces the maximum signal frequency that can be processed. So, in an oversampling converter, signal bandwidth and accuracy are exchanged.

2.5.2 Noise-shaping

An approach to further increase the accuracy of the A-to-D conversion is through noise shaping. Noise-shaping implies filtering of the quantization errors, in order to shape their frequency response. As a result, the quantization error power is reduced in the frequency band of interest, while it is increased outside that

band as shown in Figure 2.13. In this way, high resolution can be obtained in a relatively small bandwidth (75).

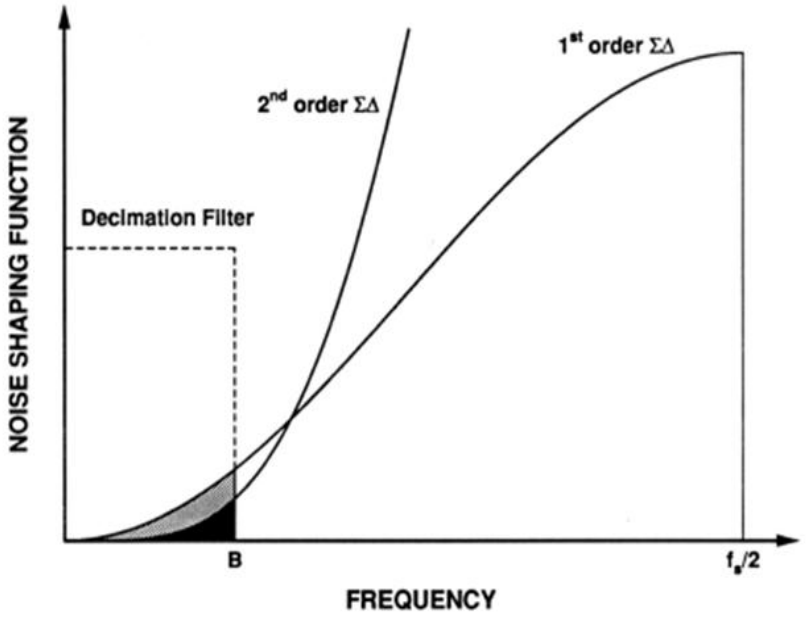

Figure 2.13: Noise shaping characteristics of ΣΔ ADC

By applying a loop filter H(f) before the quantizer and introducing the feedback, shown in Figure 2.14, a ΣΔ modulator can be constructed and different signal and quantization noise transfer functions is realized. After the decimation, the in-band quantization noise power is greatly suppressed. While combining with oversampling and noise shaping, a significant SNR improvement can be achieved for a ΣΔ ADC compared to the ADC with oversampling only.

The basic ΣΔ modulator is shown in Figure 2.15 and its linear model is shown in Figure 2.16. The basic ΣΔ modulator consists of a loop filter, a quantizer and a feedback loop. Since the output of the quantizer is a digital signal, a digital to analog converter (DAC) is placed in the feedback path. The linear model of a ΣΔ modulator models the quantizer with a quantization gain k and a noise source. It is assumed that the DAC inside the feedback loop is an ideal one. In this system, there are two input signals, x(n) and e(n), and one output signal

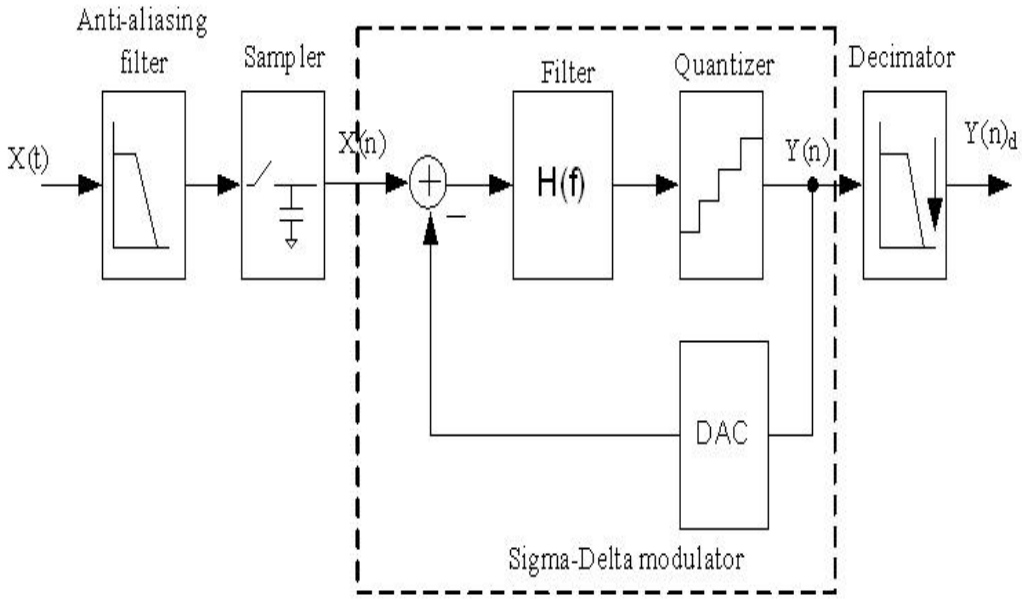

Figure 2.14: Block diagram of a noise shaping ADC system

y(n). The output of the ΣΔ modulator can be expressed as in equation 2.10:

$$Y(z) = H_x(z)X(z) + H_e(z)E(z) \tag{2.10}$$

where $H_x(z)$ represents the signal transfer function and $H_e(z)$ represents the quantization noise transfer function in the domain. The signal and noise transfer function can be calculated as in equations (2.11-2.12):

$$H_x(z) = \frac{H(z)}{1 + H(z)} \tag{2.11}$$

$$H_e(z) = \frac{1}{1 + H(z)} \tag{2.12}$$

By properly choosing the loop filter transfer function H(z), the desired signal and noise transfer function can be obtained. For example, if an integrator is chosen to be the loop filter, its transfer function is given in equation 2.13:

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{2.13}$$

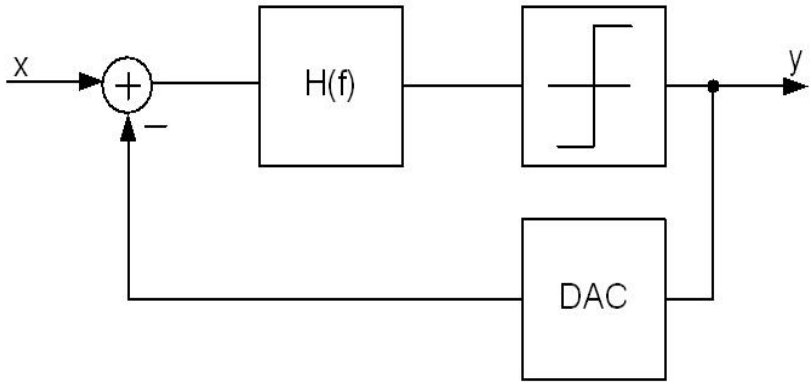

Figure 2.15: Block diagram of a ΣΔ modulator

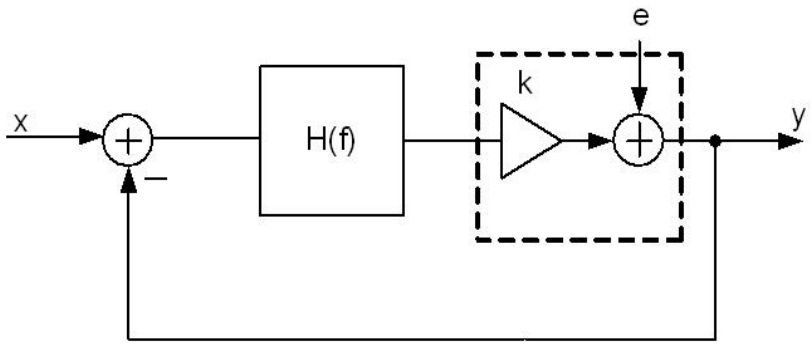

Figure 2.16: Linear model of a ΣΔ modulator

Then the signal and noise transfer functions of the ΣΔ modulator can be calculated as in equation 2.14-2.15:

$$H_x(z) = z^{-1} \tag{2.14}$$

$$H_e(z) = 1 - z^{-1} \tag{2.15}$$

Substituting equations 2.14 and 2.15 in equation 2.10, the general expression for a first-order low-pass ΣΔ modulator is obtained as in equation 2.16:

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z) \tag{2.16}$$

The equation 2.16 indicates that the signal can pass the ΣΔ modulator directly with a unit delay z^{-1} and the quantization noise has a high-pass characteristics 1-z^{-1}, allowing noise suppression at low frequencies (74).

2.6 ΣΔ Modulator

The ΣΔ modulator is a feedback system. In the time domain, the integrator integrates the difference between the input signal and the feedback output signal of the ΣΔ modulator. The result of the integrator is then fed to the quantizer (79). The negative feedback tries to minimize the difference between the input signal and the output signal of the ΣΔ modulator. As a result, the average of the output signal of the ΣΔ modulator is tracking the input signal. This behavior is illustrated in Figure 2.17.

It can be seen that the output of the ΣΔ modulator tracks the input signal. In Figure 2.17a, a single-bit quantizer is used in the ΣΔ modulator. The benefit of using a single-bit quantizer is that the linearity of a single-bit quantizer is assured. Since there are only two output states in the single-bit quantizer and two points define a straight line, so the single-bit quantizer is inherently linear. Therefore the single bit quantizer is widely used in oversampled ADCs. The multi-bit quantizer generates less quantization noise power compared to the single-bit quantizer, as shown in Figure 2.17b. As a result the average value of the output tracks the input signal much closer than the single-bit one.

So far we have discussed low-pass ΣΔ modulators. Depending on the frequency band of interest, there is another type of ΣΔ modulator, band-pass ΣΔ modulator, widely used in wireless transceivers. By applying different loop filters inside the ΣΔ modulator, a high attenuation of quantization noise in a certain frequency band can be realized. For example, when the loop filter is of second-order given by equation 2.17:

$$H(z) = \frac{-z^2}{1 + z^{-2}} \tag{2.17}$$

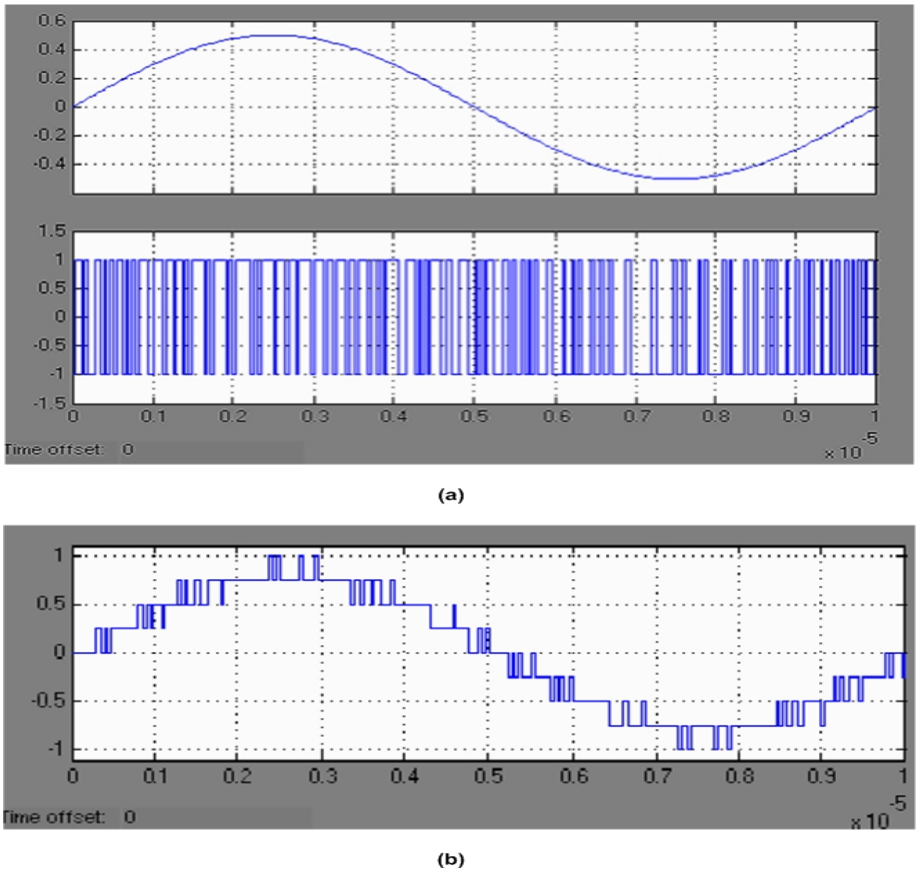

Figure 2.17: (a)Input and output waveforms of a first-order ΣΔ modulator with single-bit quantizer (b) Output waveform of a first-order ΣΔ modulator with multi-bit quantizer

Then the signal and noise transfer functions of the ΣΔ modulator is given by equations 2.18 and 2.19

$$H_x(z) = -z^2 \tag{2.18}$$

$$H_e(z) = 1 + z^{-2} \tag{2.19}$$

The output spectrum of a bandpass ΣΔ modulator is shown in Figure 2.18. The quantization noise is suppressed in the frequency band around $f_s/4$. This type of modulator is useful in digitizing signals within a certain frequency range and find its applications in wireless transceivers.

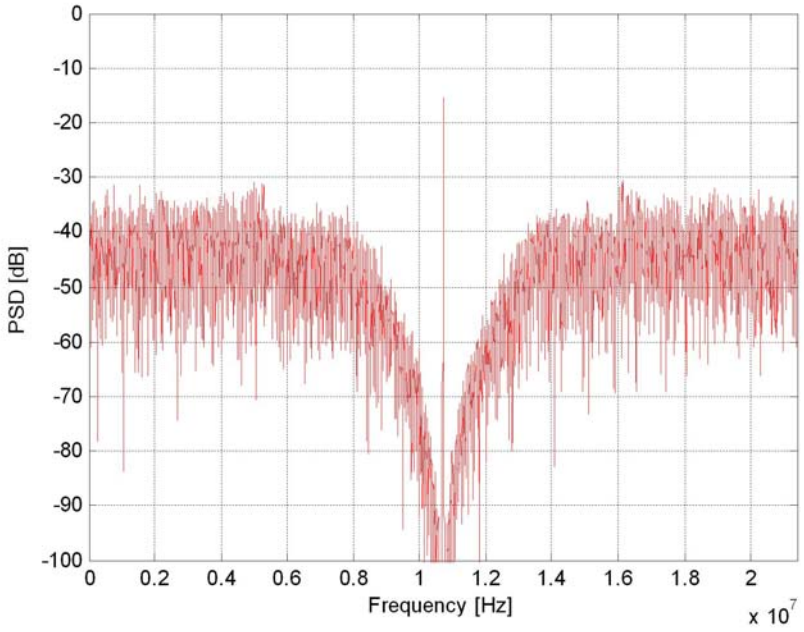

Figure 2.18: Output spectrum of a bandpass ΣΔ modulator

2.7 Performance Metrics for the ΣΔ ADC

For oversampled ADCs, since the operation principles are different from the Nyquist ADCs, different performance metrics are used to evaluate the performance of oversampled ADCs. Some important specifications are discussed here.

Signal to Noise Ratio (SNR) The SNR of a converter is the ratio of the input signal power to the noise power measured at the output of the converter. The maximum SNR of a converter can achieve is called peak signal-to-noise-ratio (SNRp). The noise here include the quantization noise and circuit noise.

Signal to Noise and Distortion Ratio (SNDR) The SNDR of a converter is the ratio of the input signal power to the power of the distortion components and noise measured at the output of the converter. The maximum SNDR of a converter can achieve is called peak signal-to-noise-and-distortion-ratio (SNDRp).

Dynamic Range (DR)

The DR is the ratio between the maximum input signal power can be applied to the input of the converter without significant performance degradation, and the minimum detectable input signal power. A significant performance degradation of a converter is considered as the SNR drops more than 3 dB below the peak SNR value. The minimum detectable input signal is the input power that the converter has for a SNR of 0 dB.

Overload Level The OL is the relative input amplitude where the SNR decreases by 3 dB below the peak SNR.

Spurious Free Dynamic Range (SFDR) The SFDR is defined as the ratio of the power of the signal to the power of the highest harmonic or spurious noise component. SFDR gives an indication of how far below the signal it is possible to go without hitting any noise or distortion.

Total Harmonic Distortion (THD) The total harmonic distortion (THD) is defined as the ratio of the total harmonic distortion power and the power of the fundamental frequency of the signal. THD is normally calculated for a certain number of harmonics.

The figure 2.19 shows the SNR and SNDR of the ΣΔ modulator versus the amplitude of the signal applied to the input of the converter. Naturally, the SNR increases linearly with the increase of the input amplitude for an ideal converter. When the input signal amplitude is small, the distortion component is immersed in the noise floor of the converter. Therefore, the SNR and SNDR curves are merged together. With the increase of the input amplitude, the distortion power becomes larger than the noise power and the SNDR starts to decrease. The SNDRp reflects the linear performance of the converter. Due to the distortion power, the SNDRp is smaller than the SNRp for the same converter. After the converter reaches its SNRp, the performance of the converter degrades drastically due to the overload of the modulator, where instability occurs. The overload is the special characteristics of the ΣΔ modulator. The overload level of a ΣΔ modulator defines the dynamic range of a converter. When the input amplitude

is larger than a certain value, the ΣΔ modulator loop becomes unstable and the noise shaping disappears. Large quantization power in the signal band results into a drastic decrease of the SNR. In the normal operation of the ΣΔ modulator, overload should be avoided.

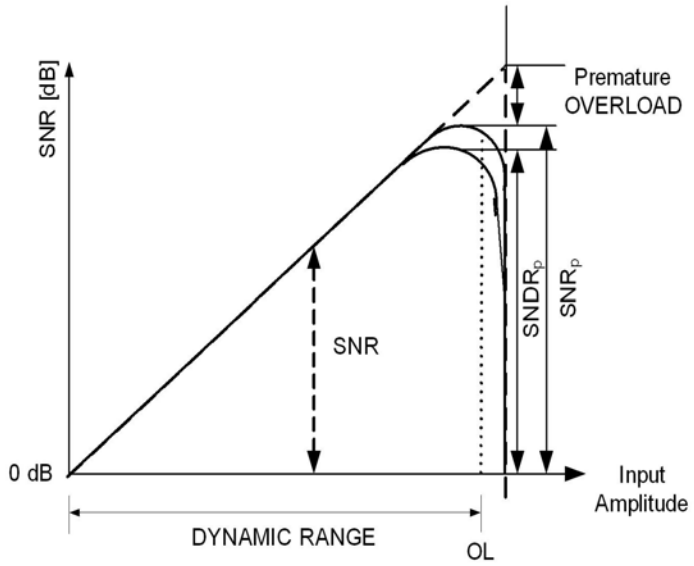

Figure 2.19: Definitions of the performance metrics used to characterize a ΣΔ ADC

2.8 Traditional ΣΔ ADC Topology

The ΣΔ ADC trades speed with resolution by means of oversampling and noise shaping. In this section, the single-loop ΣΔ modulator is introduced along with the relationship between the performance and the topology parameters. Then the cascaded ΣΔ modulator is presented. To make a difference from the feed-forward topology introduced in Chapter 3, the ΣΔ modulator topology without feedforward is called traditional topology.

2.8.1 Single-Loop Single-Bit ΣΔ modulators

The single-loop ΣΔ converter is defined as there being only one single ΣΔ loop in the whole converter. The ability of noise shaping can be improved by increasing

the order of the loop filter. Shown in Figure 2.20 is the block diagram of a first-order single-loop ΣΔ modulator. By inserting another integrator inside the loop a second-order ΣΔ modulator can be obtained as shown in Figure 2.21.

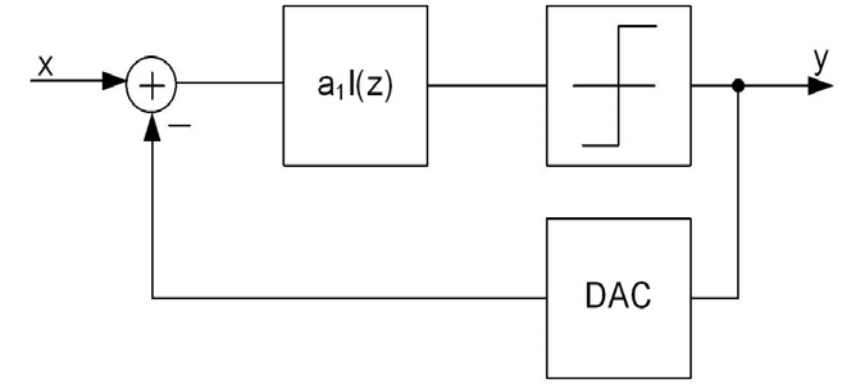

Figure 2.20: The first-order single-loop ΣΔ modulator

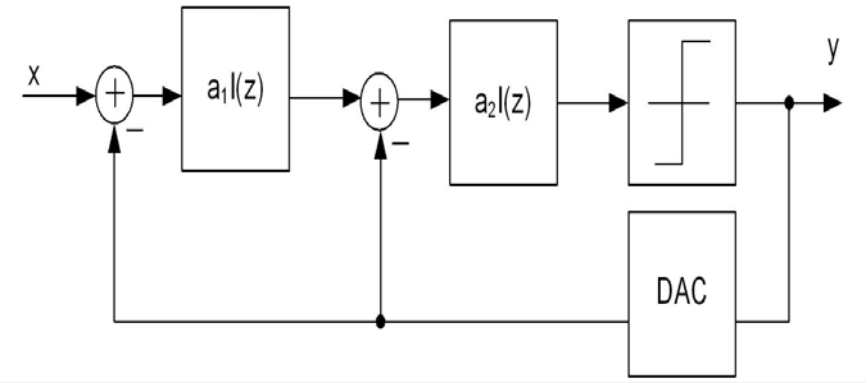

Figure 2.21: The second-order single-loop ΣΔ modulator

Similarly, by inserting more integrator stages inside the loop, a higher-order ΣΔ modulator can be realized. In Figure 2.22, a general block diagram of a n-th order single-loop ΣΔ modulator is shown. Consequently, the noise transfer functions become steeper in the signal band for higher-order ΣΔ modulators.

The signal transfer function of an ideal n-th order ΣΔ modulator can be expressed as shown in equations 2.20-2.21

$$H_x(z) = z^{-n} \tag{2.20}$$

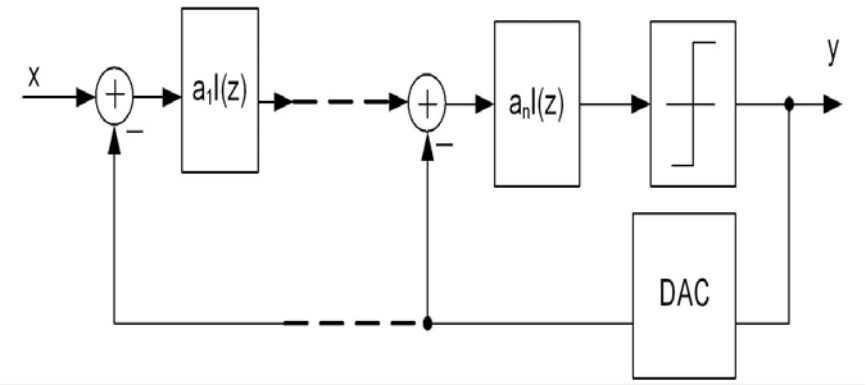

Figure 2.22: General block diagram of the n-th order single-loop ΣΔ modulator

$$H_e(z) = \left(1 - z^{-1}\right)^n \tag{2.21}$$

The signal transfer function is only a n-th order delay and the noise transfer function is a n-th order high-pass filter. The total quantization noise power inside the signal band is:

$$P_e = \int_{-f_s/2}^{f_s/2} S_e(f) \left|H(f)\right|^2 df = \left(\frac{\Delta^2}{2}\right) \frac{1}{3\pi(2n+1)} \left(\frac{\pi}{OSR}\right)^{2n+1} \tag{2.22}$$

Then the SNRp of the n-th order ΣΔ modulator can be calculated as shown in equation 2.23

$$SNR_p = \frac{3\pi}{2}(2^B - 1)^2(2n+1)\left(\frac{OSR}{\pi}\right)^{2n+1} \tag{2.23}$$

where B is the number of bits in the quantizer. This is the theoretical performance of an ideal n-th order single-loop ΣΔ modulator. Compared to the first-order ΣΔ modulator, the noise shaping ability of the n-th order ΣΔ modulator is greatly improved. However, the ΣΔ modulator loop can be unstable when the order is greater than two (64). The reason is that the higher loop-gain of the high-order loop filter causes the overload of the quantizer. Loop coefficients, $a_1 \ \ldots a_i$, are introduced to ensure the stability of a high order ΣΔ modulator. The constant a_i in front of the integrator is called the loop coefficient of this

stage. Then the transfer function of the quantization noise is:

$$H_e(z) = \frac{1}{1 + k\sum_{i=1}^{n}\prod_{j-i}^{n} a_j \left(\frac{z^{-1}}{1-z^{-1}}\right)^{n-i+1}} \tag{2.24}$$

The amplitude of the noise transfer function can be approximated as in equation 2.25.

$$|H_e(z)| \approx \frac{|1 - z^{-1}|^n}{k\sum_{i=1}^{n} a_i} \tag{2.25}$$

Then the SNR of the ΣΔ modulator can be calculated as:

$$SNR_p = SNR_{p(ideal)} \left(k\prod_{i=1}^{n} a_i\right)^2 \tag{2.26}$$

The quantization gain k is not determined in a single-bit quantizer, since it only responds to the polarity of the input signal. As a result, the gain of the last integrator is irrelevant to the operation of the ΣΔ modulator. In other words, the last loop coefficient can be chosen to have any value without affecting the performance of the ΣΔ modulator. For a single-bit ΣΔ modulator, the quantization gain k can be combined with the last integrator gain.

According to equation 2.23 and 2.26, the noise shaping ability of a ΣΔ modulator is determined by the following factors: oversampling ratio, order of the noise shaping, number of bits of the quantizer and loop coefficients.

Oversampling ratio The SNR of the ΣΔ ADC can be increased by (2n+1) 3 dB, or n+0.5 bits by doubling the oversampling ratio, where n denotes the order of the loop filter. It is tempting to raise the oversampling ratio to increase the SNR of the ΣΔ modulator. However, it is restricted by the speed limit of the circuit and the power consumption. In practice, for the same performance, it is preferred to lower the oversampling ratio. Another driving force is the ever-increasing bandwidth requirement, which also needs to lower the oversampling ratio. For high bandwidth converters, the oversampling ratio should be kept as low as possible. A lot of efforts

have been made at the system level to lower the oversampling ratio and maintain the same performance.

Order of the loop filter The SNR of the converter can be increased by increasing the order of the loop filter 'n' ideally. However, while increasing the order of the loop filter, the stability problem is the prior concern. Smaller loop coefficients are then introduced to maintain the stability of the converter. Consequently, the noise shaping ability is compromised. Moreover, more circuits are also required to expand the order of the loop filter.

Number of bits of the quantizer For the intrinsic linearity of the single-bit quantizer and the single-bit DAC in the feedback loop, many ΣΔ ADCs employ the single-bit quantizer. However, increasing the number of bits in the quantizer increases the SNR of the converter significantly. For each additional bit in the quantizer, the SNR of the converter increased by 6 dB. Moreover, by employing a multi-bit quantizer, the loop stability can also be improved and loop coefficients can be enlarged. Thus more powerful noise shaping ability is obtained. The linearity of the multi-bit DAC in the feedback loop directly affects the linearity of the converter. Since the feedback loop is connected directly to the input of the ΣΔ modulator, any non-linearity in the DAC cannot be distinguished from the input signal and will appear at the output. Therefore, the accuracy of the DAC should be at least as good as the ΣΔ modulator in order not to degrade the performance of the ΣΔ converter. Dynamic matching techniques are the main solution to tackle this problem (59),(60), (26).

Loop coefficients Loop coefficients are introduced to stabilize the ΣΔ modulator. However, they degrade the SNR of the ΣΔ modulator. The larger coefficients are, the better noise shaping ability can be achieved, and the higher the risk is to get instability for the ΣΔ modulator. Balance between the stability and the SNR is necessary. Optimized loop coefficients are developed for high performance ΣΔ modulators in (48).

Figure 2.23 shows the output spectrum of single-loop single-bit ΣΔ modulator of the first-order to the fourth-order. The loop coefficients are taken

from Table 2.2(47). In Table 2.2, the loop coefficients and the performances are presented. It is worth to mention that in the first-order ΣΔ modulator, large idle tones are found in the spectrum of the output. Such modulators are thus better avoided.

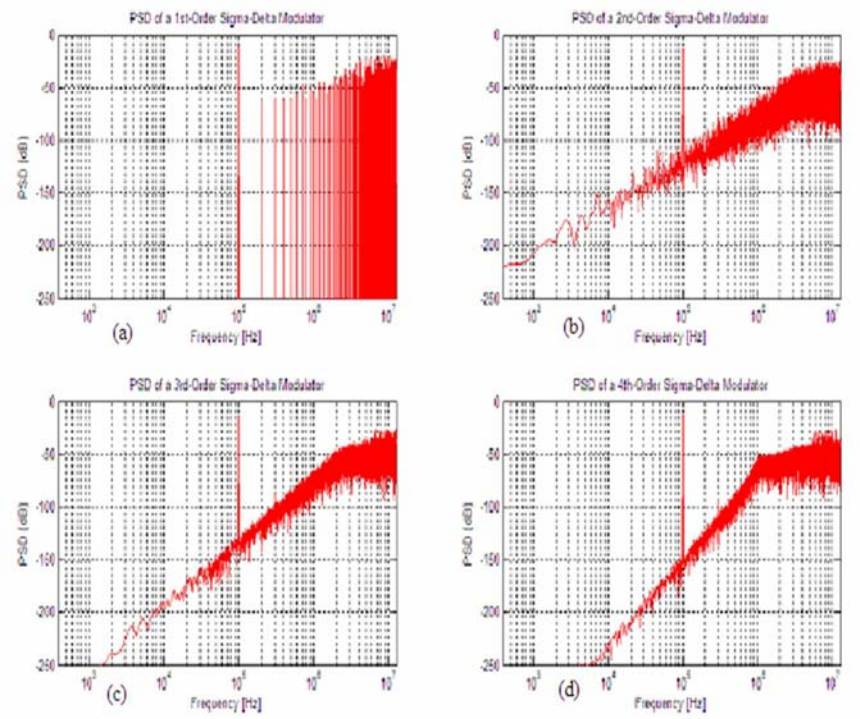

Figure 2.23: Figure (a) to (d): Output spectrum of first-order to fourth-order single-loop single-bit ΣΔ modulators.

2.8.2 Single-loop Multi-bit ΣΔ Modulators

The above discussed ΣΔ modulators are limited to the single-bit topology, whose quantizer is a single-bit one. The most appealing characteristic of the single-bit quantizer is the intrinsic linearity of the single-bit quantizer and the single-bit DAC in the feedback loop. The precision of the DAC in the feedback loop defines the precision of the whole ΣΔ modulator since the DAC error cannot be processed by the ΣΔ modulator loop. Therefore, for the single bit ΣΔ modulator, there

Table 2.2: Topology parameters and modulator performance for second to fourth-order single-loop single-bit ΣΔ modulators.

Loop Coeff.	(a_1, a_2) (0.5, 0.5)		(a_1, a_2, a_3) (0.2, 0.5, 0.5)		(a_1, a_2, a_3, a_4) (0.2, 0.2, 0.5, 0.5)	
Loop order	2		3		4	
OSR	SNRp (dB)	OL	SNRp (dB)	OL	SNRp (dB)	OL
16	42	0.7	43	0.6	40	0.6
32	57	0.7	65	0.55	71	0.6
64	74	0.7	86	0.55	100	0.55
128	88	0.65	108	0.55	128	0.55

is no linearity problem encountered and the linearity of the ΣΔ modulator is guaranteed.

However, based on the quantization noise equation, the quantization noise power is related to the number of bits of the quantizer itself. It is a very effective way to reduce the quantization noise power by increasing the number of bits in the quantizer. Another benefit gained from the multi-bit quantizer is that the loop coefficients can be scaled-up due to the improvement of the loop stability. For example, for a fourth-order single-bit ΣΔ modulator, the loop coefficients are (a_1, a_2, a_3, a_4) = (0.2,0.2,0.5,0.5), and the SNRp is 71 dB when OSR is 32. For the same fourth-order four-bit ΣΔ modulator, the loop coefficients are (a_1, a_2, a_3, a_4) = (0.25,0.5,0.75,2.25), and the SNRp is 117 dB under the same condition. The use of a four-bit quantizer improves the SNRp with 24 dB, while the scaling-up of loop coefficients contributes extra 14 dB for the SNRp of the converter (24). Compared to the single-bit version, this is a great improvement on the performance. Especially for wide-band ΣΔ modulators, it is advantageous to choose a multi-bit ΣΔ modulator topology to lower the OSR. Table 2.3 summarizes the loop coefficients and the performance of the second to fourth-order single-loop 4-bit ΣΔ modulators.

There are many ways to increase the linearity of the DAC in the feedback loop, such as digital correction (14), (82) and dynamic element matching(DEM) (59), (60), (13), (24), (26). Without additional trimming or calibration, the dynamic element matching technique is an effective way to increase the linearity of the DAC and it is widely used in the multibit ΣΔ converters.

Table 2.3: Topology parameters and modulator performance for second to fourth-order single-loop 4-bit ΣΔ modulators.

Loop Coeff.	(a_1, a_2) (0.5, 0.5)		(a_1, a_2, a_3) (0.2, 0.5, 0.5)		(a_1, a_2, a_3, a_4) (0.2, 0.2, 0.5, 0.5)	
Loop order	2		3		4	
OSR	SNRp	OL	SNRp	OL	SNRp	OL
16	78	0.9	86	0.85	89	0.8
32	94	0.9	107	0.85	117	0.85
64	106	0.9	128	0.85	144	0.85
128	123	0.9	145	0.85	168	0.85

2.9 Cascaded ΣΔ Modulators

Smaller loop-coefficients are used in the single-loop high-order ΣΔ modulator due to the stability problem. Consequently, for the single-bit high-order ΣΔ modulator, the SNR significantly degrades compared to the ideal one. This effect significantly restricts the benefit of increasing the order of the loop filter. The cascaded ΣΔ modulator is an effective way to solve this problem.

The noise canceling of a n-th order ΣΔ modulator is shown in Figure 2.24. The quantization noise of the n-th order ΣΔ modulator is extracted by a subtractor and then fed to an ideal ADC. The digital output of the ΣΔ modulator and the ideal ADC are then processed in the digital domain.

If the transfer function of the block H_1 and H_2 is defined by:

$$H_1(z) = 1 + (b-1)(1-z^{-1})^n \tag{2.27}$$

$$H_2(z) = (1-z^{-1})^n \tag{2.28}$$

Then the output of the whole system is:

$$Y(z) = z^{-1}X(z) \tag{2.29}$$

It can be seen from the above equation that the quantization noise of the n-th order ΣΔ modulator is cancelled completely (70), (98). In practice, the matching

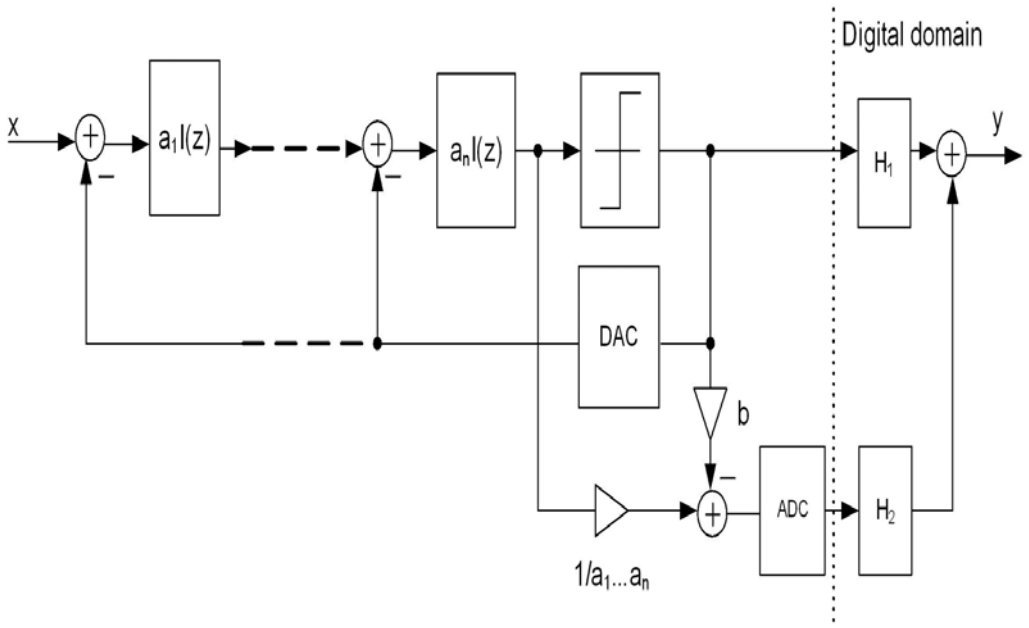

Figure 2.24: Block diagram of the noise cancelling concept

between the two loops can introduce some errors and perfect cancellation may not be achieved. On the other hand, the quantization errors of the last ADC still can be seen in the output. Therefore, the exact noise cancellation depends on the matching of the two loops and the precision of the ADC in the cancellation loop.

By exploiting such a noise cancellation technique, a cascaded ΣΔ modulator can be built. Normally, the ADC in the noise canceling loop is implemented by another ΣΔ modulator. The quantization noise of the last ΣΔ modulator is present in the output of the cascaded ΣΔ modulator. The cascaded topology is the combination of several intrinsically stable first or second-order ΣΔ modulators. By employing a cascaded topology, higher noise shaping can be obtained without the stability problem. Figure 2.25 shows the block diagram of a third-order cascaded 2-1 ΣΔ modulator topology composed by a second-order ΣΔ modulator and a first-order ΣΔ modulator. The cascaded ΣΔ modulator consists of several stages of low-order ΣΔ modulators. The quantization noise of the previous ΣΔ modulator is fed to the next ΣΔ modulator. Then the outputs of all ΣΔ modulators are processed in the digital domain to cancel the quantiza-

tion noise of the ΣΔ modulators except the last stage ΣΔ modulator. It is seen that there is no feedback branch across different ΣΔ modulators. Therefore, the cascaded ΣΔ modulator is stable as long as each stage of ΣΔ modulator is stable (49), (70).

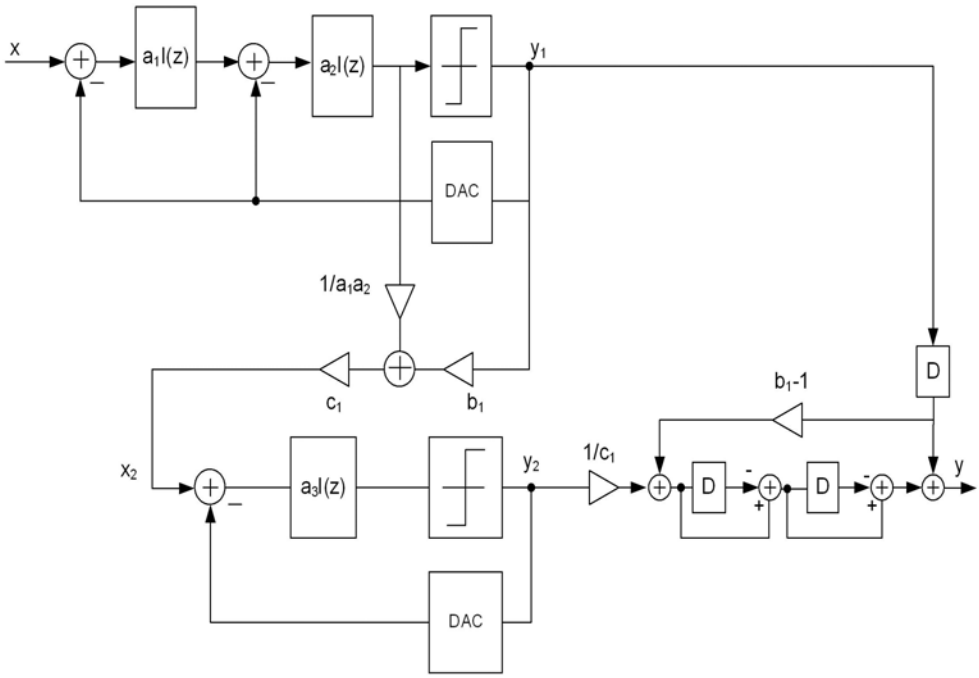

Figure 2.25: Block diagram of a third-order cascaded 2-1 ΣΔ modulator topology

Taking the cascaded 2-1 topology as an example, the output of the first ΣΔ modulator can be expressed as:

$$Y_1(z) = \frac{a_1 a_2 k_1 z^{-2} X(z) + (1 - z^{-1})^2 E_1(z)}{D(z)} \tag{2.30}$$

where $D(z) = 1 + (a_2 k_1 - 2)z^{-1} + (a_1 a_2 k_1 - a_2 k_1 + 1)z^{-2}$and k_1 is the quantization gain of the first ΣΔ modulator. The output of the second ΣΔ modulator is:

$$Y_2(z) = \frac{a_3 k_2 z^{-1} X_2(z) + (1 - z^{-1}) E_2(z)}{1 - (1 - a_3 k_2) z^{-1}} \tag{2.31}$$

The input of the second ΣΔ modulator is:

$$X_2(z) = \frac{Y_1(z) - E_1(z)}{a_1 a_2 k_1} - b_1 Y_1(z) \tag{2.32}$$

Then the output of the cascaded ΣΔ modulator is:

$$Y(z) = Y_1(z)H_1(z) + Y_2(z)H_2(z) \tag{2.33}$$

The digital processing block transfer functions are:

$$H_1(z) = z^{-1}(1 + (b_1 - 1)(1 - z^{-1})^2) \tag{2.34}$$

$$H_2(z) = \frac{(1 - z^{-1})^2}{c_1} \tag{2.35}$$

Assuming,

$$a_1 a_2 k_1 = 1 \tag{2.36}$$

$$a_2 k_1 = 2 \tag{2.37}$$

$$a_3 k_2 = 1 \tag{2.38}$$

Then finally the output of the cascaded 2-1 topology is the combination of equation 2.33 and equations 2.34- 2.38:

$$Y(z) = z^{-3}X(z) + \frac{(1 - z^{-1})^3}{c_1} E_2(z) \tag{2.39}$$

It is seen that the quantization noise of the first ΣΔ modulator is completely cancelled. Only the quantization noise of the second ΣΔ modulator, $E_2(z)$ is seen in the output. The quantization noise is noise-shaped by a third-order noise shaping function and reduced by a factor c_1.

In addition to the above mentioned cascaded 2-1 topology, there are other ways to cascade several ΣΔ modulators. The performance achieved is different. For example, a fourth-order cascaded ΣΔ modulator can be composed by a 2-2 topology or a 2-1-1 topology, shown in Figures 2.26 and 2.27 respectively. The cascaded 2-2 topology is constructed by two second-order ΣΔ modulators and

the cascaded 2-1-1 topology is constructed by a second-order ΣΔ modulator and two first-order ΣΔ modulators. Tables 2.4, 2.5 and 2.6 summarize loop coefficients and the performance of the cascaded 2-1, 2-2 and 2-1-1 ΣΔ modulators respectively (48), (47), (25) , (24).

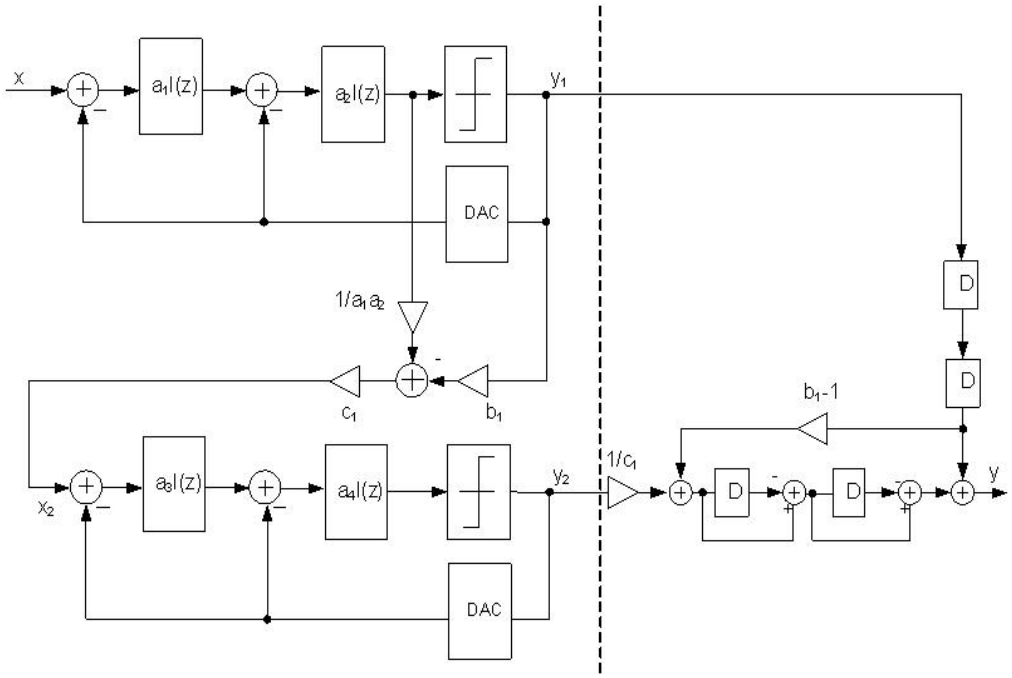

Figure 2.26: Block diagram of a fourth-order cascaded 2-2 ΣΔ modulator topology

In principle any ΣΔ modulator can be used in the cascaded ΣΔ modulator. For stability consideration, only first and second-order ΣΔ modulators are used in cascaded ΣΔ modulators. Therefore, the cascaded ΣΔ modulator maintains intrinsic stability and achieves high-order noise shaping. It should be avoided to use the first-order ΣΔ modulator as the first stage of the cascaded ΣΔ modulator, since large idle tones from the first stage can directly leak to the output. Normally the second-order ΣΔ modulator is put in the first stage to avoid the idle tone problem.

Generally by applying linear analysis, the quantization noise transfer function

Table 2.4: Topology parameters and modulator performance for the Cascaded 2-1 ΣΔ modulator

Loop Coeff.	(a_1, a_2, a_3, b_1, c_1) (0.5, 0.5, 0.5, 2, 0.5)	
Topology	2-1	
OSR	SNRp	OL
16	56	0.75
32	77	0.7
64	96	0.7
128	119	0.65

Table 2.5: Topology parameters and modulator performance for the Cascaded 2-2 ΣΔ modulator

Loop Coeff.	(a_1, a_2, a_3, a_4, b_1, c_1) (0.5, 0.5, 0.5, 0.5, 2, 0.5)	
Topology	2-2	
OSR	SNRp	OL
16	64	0.7
32	92	0.7
64	119	0.65
128	144	0.6

Table 2.6: Topology parameters and modulator performance for the Cascaded 2-1-1 ΣΔ modulator

Loop Coeff.	(a_1, a_2, a_3, a_4, b_1, c_1, b_2, c_2) (0.5, 0.5, 0.5, 0.5, 2, 0.5, 1, 1)	
Topology	2-1-1	
OSR	SNRp	OL
16	72	0.7
32	99	0.7
64	125	0.65
128	152	0.65

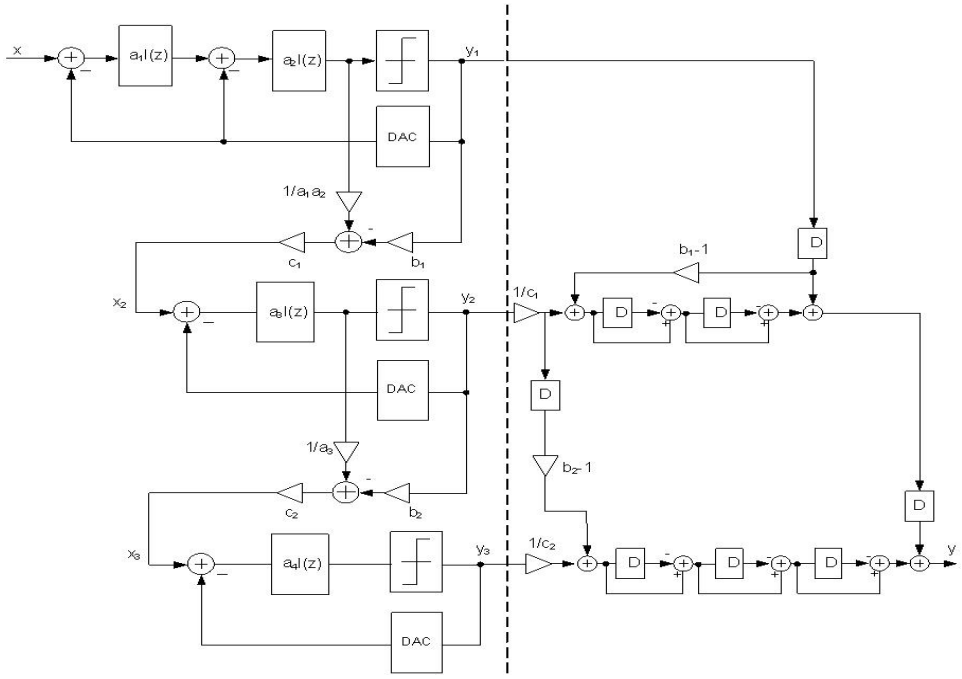

Figure 2.27: Block diagram of a fourth-order cascaded 2-1-1 ΣΔ modulator topology

of a cascaded ΣΔ converter is given by (47):

$$H_e(z) \approx \frac{(1-z^{-1})^n}{\prod_{i=1}^{m} c_i} \tag{2.40}$$

where m is the number of cascaded stages and c_i is the coupling coefficient between different stages. Compared to the ideal n-th order ΣΔ modulator, the performance degradation depends on the coupling coefficients. For best noise shaping, it is preferred to increase the coupling coefficient. However, the coupling coefficient defines the input amplitude of the next stage and is restricted by circuits characteristics. The best strategy for a cascaded ΣΔ modulator design is to maximize the coupling coefficients without overloading the next stage to achieve a higher SNR.

The main drawback of the cascaded ΣΔ modulator is the severe requirement of the building blocks. The noise cancellation relies on the matching of the

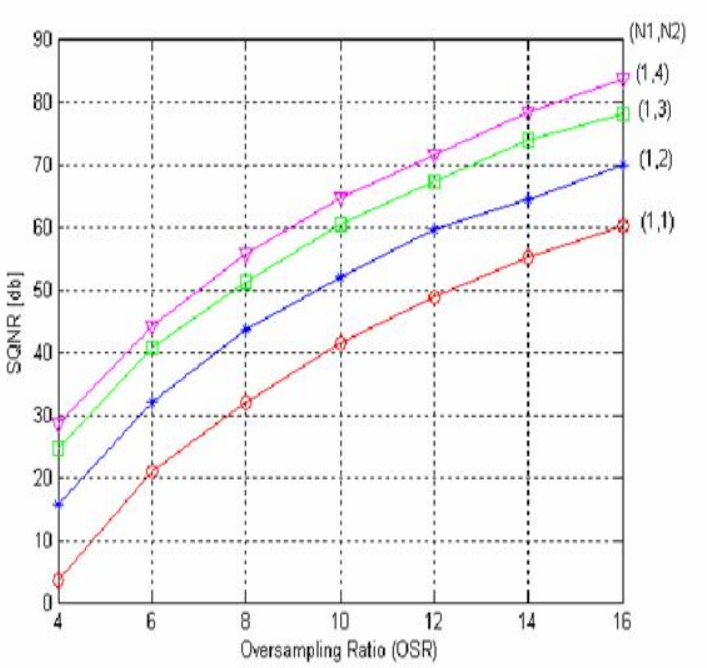

Figure 2.28: SQNR vs oversampling ratio for a 2-1 third-order cascaded ΣΔ topology.

cascaded converters. If the matching is not well controlled, then the noise cancellation is not perfect. There is a quantization noise component from the previous converter appearing in the output of the whole converter. This is called noise leakage (70), (99). In a real circuit implementation, the mismatch of the loop coefficient, the finite OTA DC gain and the settling error of the integrator are the main sources of the noise leakage of a cascaded ΣΔ converter. In nanometer CMOS technologies, the non-idealities is getting more severe. The high sensitivity to the non-idealities of the building blocks makes the implementation even more difficult in nanometer CMOS technologies.

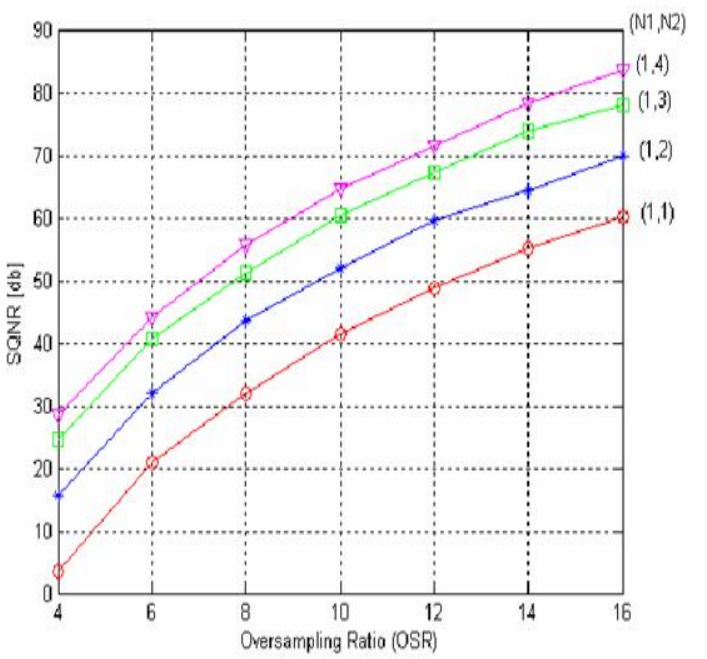

Figure 2.29: SQNR vs oversampling ratio for 2-2 (fourth-order) cascaded ΣΔ topology.

2.10 Performance Comparison of Traditional ΣΔ Topologies

Figure 2.28 and 2.29 shows the simulated peak signal-to-quantization noise ratio (SQNR) versus the oversampling ratio for 2-1 (third-order) and 2-2 (fourth-order) cascaded ΣΔ modulator respectively. Here N1 and N2 represents the number of quantizer bits in the first and second stages respectively. The cascaded modulator offers good performance, but it requires high-performance building blocks. The multi-bit modulator offers the best performance, but suffers from the non-linearity problem of the feedback DAC. Hence a single-bit quantizer has been chosen in the first stage because of its inherent linearity. However, the single-loop single-bit modulator is the worst one in terms of performance, but it is not sensitive to the non-idealities of the building blocks.

2.11 Chapter Summary

This chapter gives an overview of different receiver architectures. Among the different architectures, zero-IF is the most promising candidate for multi-standard operation. Further, we discussed all the fundamentals of data converters in general and the important definitions associated with it. It also gives an insight into where the sigma-delta stands and their concepts. By introducing oversampling and noise-shaping concepts, the basic operation principle of the $\Sigma\triangle$ ADC is presented. A systematic study on the traditional single-loop, cascaded and multibit $\Sigma\triangle$ modulator topologies has been presented in this chapter. The advantages, disadvantages and optimized parameters are also given for each topology.

Chapter 3

System Level Design and Analysis

This chapter introduces a low-distortion swing-suppression (feed forward) topology which has reduced sensitivity to integrator non-idealities. It also investigates the high level design of $\Sigma\triangle$ architecture for wide bandwidth receiver, which contains dual-bandwidth for WCDMA and GSM system applications. First a dual mode architecture is considered. Later the blocks are re-used for triple mode operation.

3.1 Introduction

Sigma-delta modulator is the most promising candidate to achieve high resolution over a wide variety of bandwidth requirements in multi-mode receivers. The advantage of $\Sigma\triangle$ ADCs in providing high resolution with low precision components lies on the use of over-sampling and noise shaping. As bandwidth requirement increases, the over-sampling ratio decreases which results in a decrease in the resolution. Designing $\Sigma\triangle$ modulators that can achieve high resolution and wide bandwidth remains challenging. Sigma-delta A/D converters suitable for dual-mode and triple-mode receivers have already been published in the literature (11), (29), (53), (20), (95), (103), (33). These solutions of switched-capacitor (SC) $\Sigma\triangle$ modulators that cover mainly GSM, WCDMA and WLAN standards are presented in Table 3.1.

Table 3.1: Summary of the published multi-standard ΣΔ ADCs .

Parameter	Dual-mode ΣΔ ADC				Triple Mode		
	(11)	(29)	(53)	(20)	(95)	(103)	(33)
Order	3	2	2	2/(2-1)	2-1-1	2-1-1-1	2-2
No. of bits	1	2.5	6	1/2.3	1/1/1	1/1.5/3	2.5/2.5
Fs (MHz)	104/184.32	26/46	23/46	39/38.4	138/245/320	51.2/100/100	23/46
BW (MHz)	0.2/3.84	0.2/2	0.2/1.92	0.1/1.92	0.271/3.84/20	0.2/5/20	0.2/1.5/1.92
DR (dB)	86/54	79/50	81/70	82/70	103/82/66	94/88/56	70/51/50
CMOS Process	0.25 um)	0.13um	0.18 um	0.13 um	0.35 um	0.18 um	0.18 um
Power (mW)	11.5/13.5	2.4/2.9	30/50	2.4/4.3	58/82/128	—	5.8/5/11

A triple-mode cascaded ΣΔ architecture for GSM/UMTS/WLAN has been reported in (95) whose wide range of programmability of input frequency and dynamic range descends from modulator order programmability. Another reconfigurable ΣΔ modulator for a triple standard receiver has been introduced in (103) where a feedback path from the last stage to the third stage is done in order to further suppress the quantization noise power. A low-power multi-standard ΣΔ ADC which uses a 2-2 cascaded structure with five level quantizer in each stage has been published in (33). Yet another triple-mode ΣΔ ADC has been explored in (72) which uses low-distortion architecture and Pseudo-Data-Weighted-Averaging technique to attain high linearity over a wide bandwidth. Traditional topology is increasingly sensitive to circuit imperfections, especially at very low over-sampling ratios.

In this chapter, first we present a low-distortion swing suppression (feed-forward) topology which has reduced sensitivity to integrator non-idealities. A programmable dual-mode ΣΔ modulator which uses the low-distortion topology is then proposed for GSM/WCDMA applications. Then it has been extended to a triple mode architecture which uses multi-bit quantizer in the last stages in order to eliminate the necessity of DEM techniques to improve the linearity of multi-bit DAC, for use in wideband applications like WLAN (81), (56), (73).

3.2 Low-distortion Swing-suppression SDM

A second-order ΣΔ topology with low sensitivity to integrator non-linearities, which can be used for wide-band applications with very low oversampling ratios

of 8 or 16, is described. At very low over-sampling ratios in such applications, ADCs are increasingly sensitive to circuit imperfections, and require high-quality analog components. This feed-forward technique is applicable to any modulation order and for any over-sampling ratio. Here the integrators are processing only the quantization noise, which will relax the requirements for the opamp design.

Single-stage ΣΔ architecture for GSM is presented in Figure 3.1 which meets the requirements of GSM specifications and has reduced sensitivity to opamp non-linearities and exhibits lower distortion than traditional single stage topologies (101), (63). The proposed low-distortion topology solves the non-linearity distortion problem by cancelling the transfer function from X(z) to $I_1(z)$ and $I_2(z)$. This is achieved by making STF(z) =1. The proposed architecture is shown in Figure 3.1 and the STF and NTF can be expressed as shown in equation 3.1.

$$STF(z) = 1; \quad NTF(z) = (1 - z^{-1})^2 \tag{3.1}$$

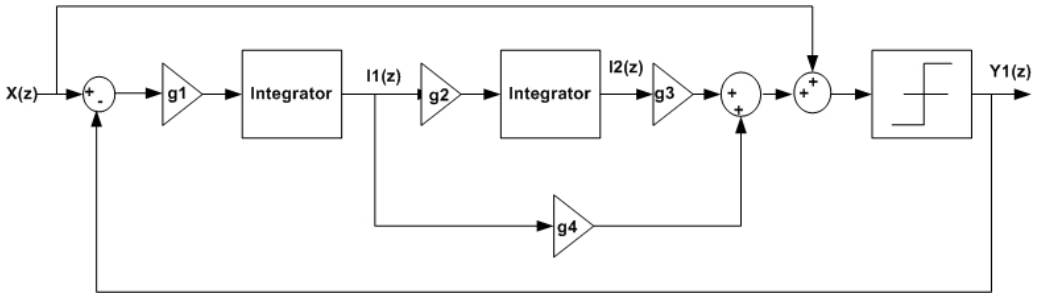

Figure 3.1: Low-distortion swing-suppression SDM

By feed-forwarding the input signal, the noise transfer function is unaffected, but the integrators will process the quantization noise only. Therefore, their performance requirements are significantly relaxed. Another advantage is that only one DAC is required in the feedback loop. For multi-bit quantization, this reduces the circuit complexity and chip area significantly (77).

3.3 A Dual-mode ΣΔ Modulator Design

By implementing feed-forwarding in both stages of the cascaded structure, a topology which is suited to wide-band applications like WCDMA can be obtained

as shown in Figure 3.2. In traditional cascaded structure, the input to the second stage is the actual quantization noise of the first stage, that is, the output of the first stage quantizer minus its input. But here, the input to the second stage can be directly taken from the output of the second integrator since the integrators are only processing the quantization noise. The non-linearity problem is solved by cancelling the transfer functions from X to I_1 and I_2. This is achieved by making the STF(z) = 1.

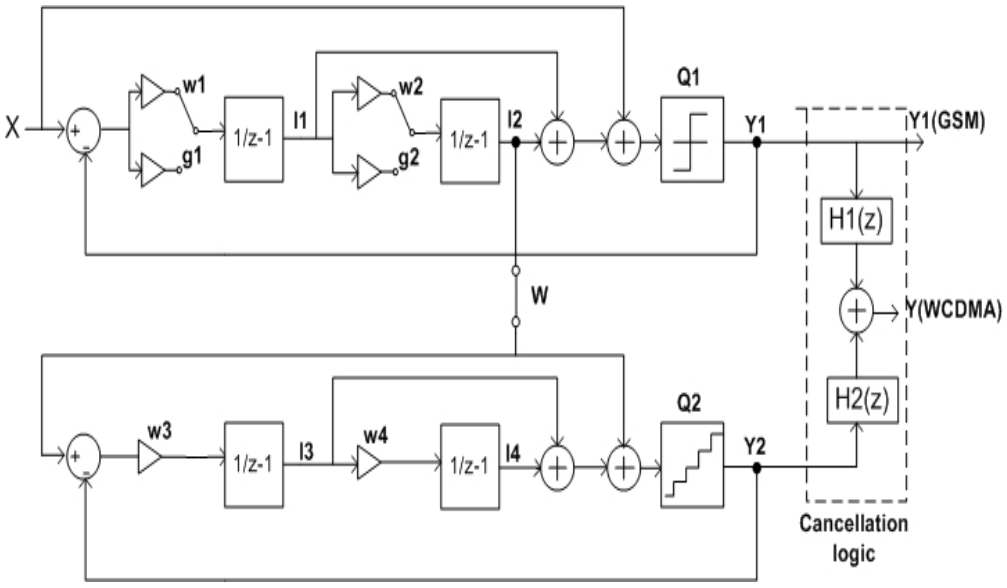

Figure 3.2: Dual-mode sigma-delta modulator

In this architecture, the 2nd order modulator in the first stage is used to meet the requirements for GSM by closing the switches labelled G1 and G2. In this mode, the unused blocks in the second stage can be switched off, thus minimizing the power consumption. In the WCDMA mode, the whole modulator (2-2 cascaded) is switched to operation by closing the switches labelled W, W1, W2, thus making it programmable.

3.3.1 Estimation of Gain Coefficients

$$Y_1(z) = (X(z) - Y_1(z)) \left(g_1 \frac{z^{-1}}{(1-z^{-1})} \right) \left[\left(g_2 g_3 \frac{z^{-1}}{(1-z^{-1})} \right) + g_4 \right] + X(z) + Q_1(z) \tag{3.2}$$

$$Y_1(z)\left[1+g_1g_2g_3\left(\frac{z^{-2}}{(1-z^{-1})^2}\right)+g_1g_4\left(\frac{z^{-1}}{(1-z^{-1})}\right)\right]=X(z)P(z)+Q_1(z) \quad (3.3)$$

$$where \;\; P(z) \;=\; \left[1+g_1g_2g_3\left(\frac{z^{-2}}{(1-z^{-1})^2}\right)+g_1g_4\left(\frac{z^{-1}}{(1-z^{-1})}\right)\right] \quad (3.4)$$

Equation 3.3 in the form shown in equation 3.5

$$Y(z)=STF(z)X(z)+NTF(z)Q_1(z) \quad (3.5)$$

where

$$STF(z)=1 \quad (3.6)$$

and

$$NTF(z)=\frac{(1-z^{-1})^2}{(1+(g_1g_4-2)z^{-1}+(1+g_1g_2g_3-g_1g_4)z^{-2}} \quad (3.7)$$

For

$$NTF(z)=(1-z^{-1})^2 \Longrightarrow g_1g_4-2=0 \Longrightarrow g_1g_4=2 \quad (3.8)$$

and

$$1+g_1g_2g_3-g_1g_4=0; \quad g_1g_2g_3=1; \quad (3.9)$$

Let g_1=0.5, then g_4=2/0.5=4. Also g_2g_3=1/0.5=2. And the output of the second integrator is given by equation 3.10.

$$I_2(z)=(X(z)-Y_1(z))\left(g_1\frac{z^{-1}}{(1-z^{-1})}g_2\frac{z^{-1}}{(1-z^{-1})}\right) \quad (3.10)$$

$$I_2(z)=-g_1g_2z^{-2}Q_1(z) \quad (3.11)$$

If g_2=0.5, then g_3=4. Therefore the gain factors at the integrators are g_1=0.5, g_2=0.5, g_3=4, g_4=4.

As long as equations 3.8 and 3.9 hold, there are infinite combinations of g_1 and g_2 which satisfies these equations. Numerical simulation is then needed to find out the optimized value. In simulation, the two parameters g_1 and g_2 are sweeped respectively in a reasonable region and for each combination of coefficients the

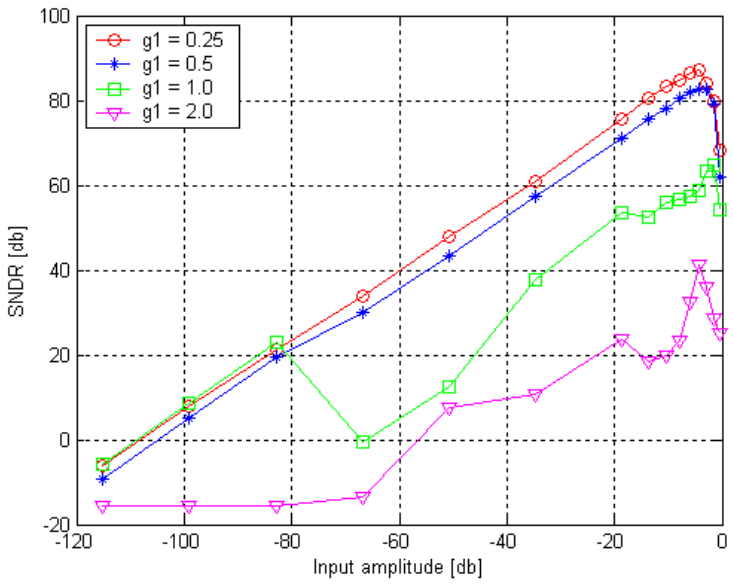

Figure 3.3: Sweep of g_1 keeping $g_2 = 0.5$

whole input dynamic range should be simulated. This is a time-consuming procedure. Figure 3.3 and 3.4 shows the result of sweeping g_1, keeping g_2 fixed, and vice-versa.

Finally some optimal combinations are found, $g_1 = 0.25$ or 0.5 with $g_2 = 0.25$, 0.5 or 1.0.

3.3.2 Error cancellation

Output of the first stage

$$Y_1(z) = X(z) + (1 - z^{-1})^2 Q_1(z) \tag{3.12}$$

Output of the second stage

$$Y_2(z) = I_2(z) + (1 - z^{-1})^2 Q_2(z) \tag{3.13}$$

$$Y_2(z) = -g_1 g_2 z^{-2} Q_1(z) + (1 - z^{-1})^2 Q_2(z) \tag{3.14}$$

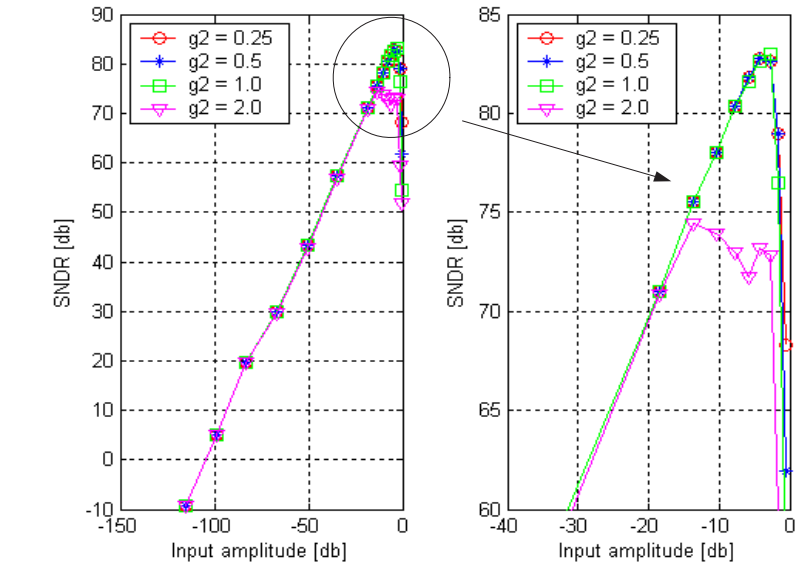

Figure 3.4: Sweep of g_2 keeping $g_1 = 0.5$

Multiplying equation 3.12 with $z^{-2} \Longrightarrow H_1(z)$ and equation 3.14 with $\frac{1}{g_1 g_2}(1-z^{-1})^2 \Longrightarrow H_2(z)$ we get,

$$z^{-2}Y_1(z) = z^{-2}X(z) + z^{-2}(1-z^{-1})^2 Q_1(z) \tag{3.15}$$

$$\frac{1}{g_1 g_2}(1-z^{-1})^2 Y_2(z) = -z^{-2}(1-z^{-1})^2 Q_1(z) + \frac{1}{g_1 g_2}(1-z^{-1})^4 Q_2(z) \tag{3.16}$$

Equation 3.15+3.16 gives

$$z^{-2}Y_1(z) + \frac{1}{g_1 g_2}(1-z^{-1})^2 Y_2(z) = z^{-2}X(z) + \frac{1}{g_1 g_2}(1-z^{-1})^4 Q_2(z) \tag{3.17}$$

$$Y(z) = z^{-2}X(z) + \frac{1}{g_1 g_2}(1-z^{-1})^4 Q_2(z) \tag{3.18}$$

Since $g_1 g_2 = 0.25$,

$$Y(z) = z^{-2}X(z) + 4(1-z^{-1})^4 Q_2(z) \tag{3.19}$$

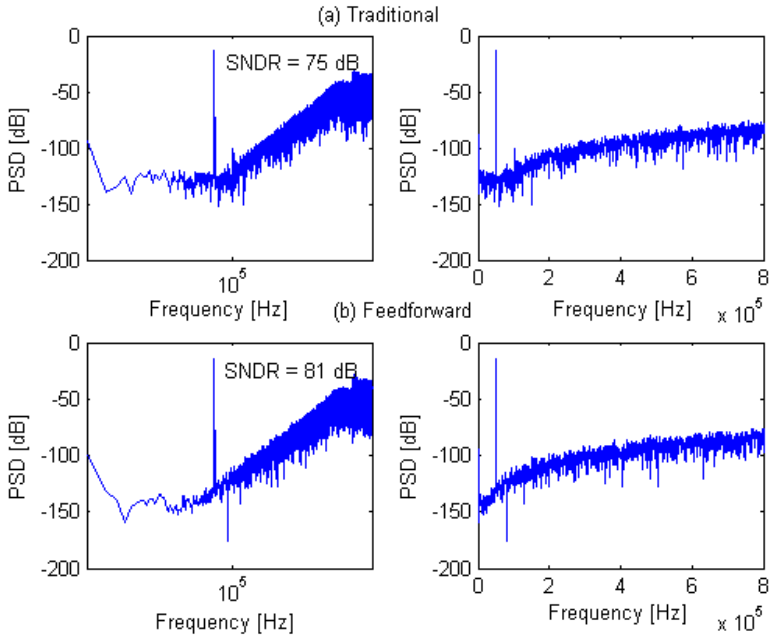

Figure 3.5: PSD of (a) Traditional second-order $\Sigma\triangle$ modulator (b) Feed forward second-order $\Sigma\triangle$ modulator

and

$$Y(z) = z^{-2}Y_1(z) + 4(1 - z^{-1})^2 Y_2(z) \tag{3.20}$$

The coefficients selected for GSM and WCDMA are given in Table 3.2.

3.4 Simulations

In the simulations, first the single stage low-distortion, swing suppression SDM is compared with the traditional one. The two architectures are modelled with real integrator blocks having the same kind of non-linearities. A single-bit quantizer is used for the first two architectures. The input signal had amplitude of 0.5 V and a frequency of 50 KHz. The sampling frequency was 32 MHz and an oversampling ratio of 160 was used for a bandwidth of 100 KHz for both the architectures.

Figure 3.5 compares the power spectral densities (PSD) at the output of the modulator, when the same kind of non-idealities like non-linear finite dc gain, integrator leakage, finite gain-banwidth (GBW) and slew rate (SR) are introduced

Table 3.2: Integrator gain coefficients

GSM		WCDMA	
Coefficients	Value	Coefficients	Value
g_1	0.5	w_1	0.5
g_2	0.5	w_2	0.5
g_3	4.0	w_3	4.0
g_4	4.0	w_4	4.0

in both of these architectures which is explained in Chapter 5. The spectra reveals how feed forward topology is less sensitive to the above mentioned circuit imperfections while the traditional one produces harmonic distortion, thus degrading the in-band noise-plus-distortion ratio giving an SNDR of only 75 dB while the other one achieves 81 dB.

3.4.1 Integrator Output Swing

The proposed architecture has the characteristic of swing suppression when compared to the traditional one. The integrator output swing should be reduced to avoid the non-linearity and overload in low power supply voltage SDM. The integrator outputs are expressed as shown in equations 3.21 and 3.22

$$I_1(z) = -g_1(1 - z^{-1})Q_1(z) \tag{3.21}$$

$$I_2(z) = -g_1 g_2 z^{-2} Q_1(z) \tag{3.22}$$

From equations 3.21 and 3.22, $I_1(z)$ and $I_2(z)$ contain only quantization noise $Q_1(z)$, without input signal X(z). Therefore, the integrator output swings of the proposed architecture are smaller than that of the conventional one. The simulated integrator output histograms of both the traditional and feed forward second-order SDMs, with a sampling frequency of 32 MHz, a 50 KHz sine wave input with -6dB amplitude are shown in Figure 3.6. According to Figure 3.6, the integrator output swings of the proposed feed forward architecture are much

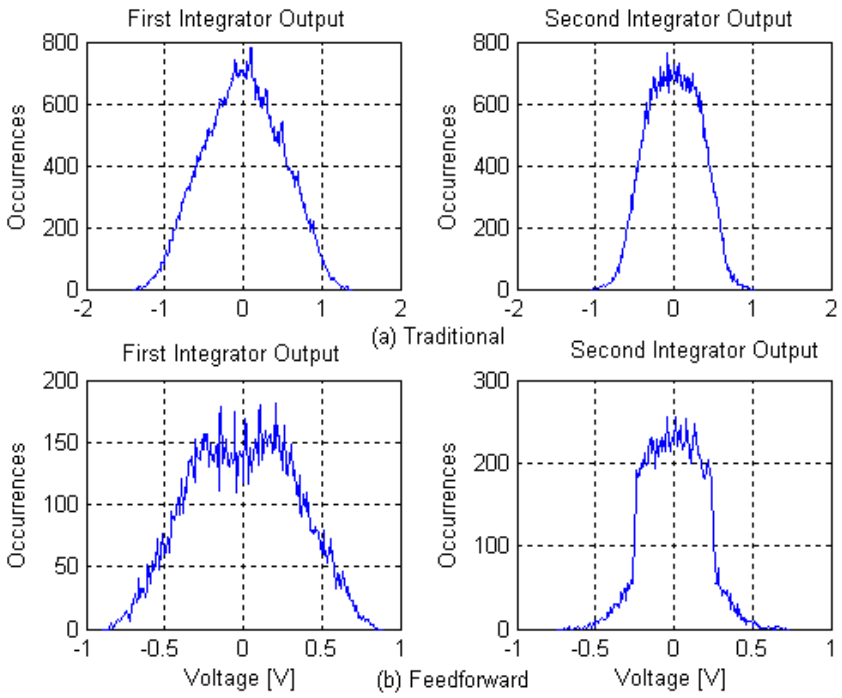

Figure 3.6: Comparison of the output swing

smaller than that of the conventional architecture especially in the second integrator.

Second part of the simulations was carried out using cascaded 2-2 MASH topologies comparing the traditional and low-distortion cascaded SDMs. The two architectures are modelled with real integrator blocks having the same kind of non-linearities. A single-bit quantizer is used in the first stage and a 4-bit quantizer in the second stage for both the architectures. The input signal had amplitude of 0.5 V and a frequency of 50 KHz. The sampling frequency was 64 MHz and an oversampling ratio of 16 was used for a bandwidth of 2 MHz.

In Figure 3.7, it is seen that the low-distortion cascaded topology achieves an improved signal-to-noise ratio of 74 dB compared to the traditional one which has only 66 dB. Also the proposed architecture has a noise floor well below the -100 dB gridline, which is not the case for the traditional. Simulations were made using Matlab^{TM}.

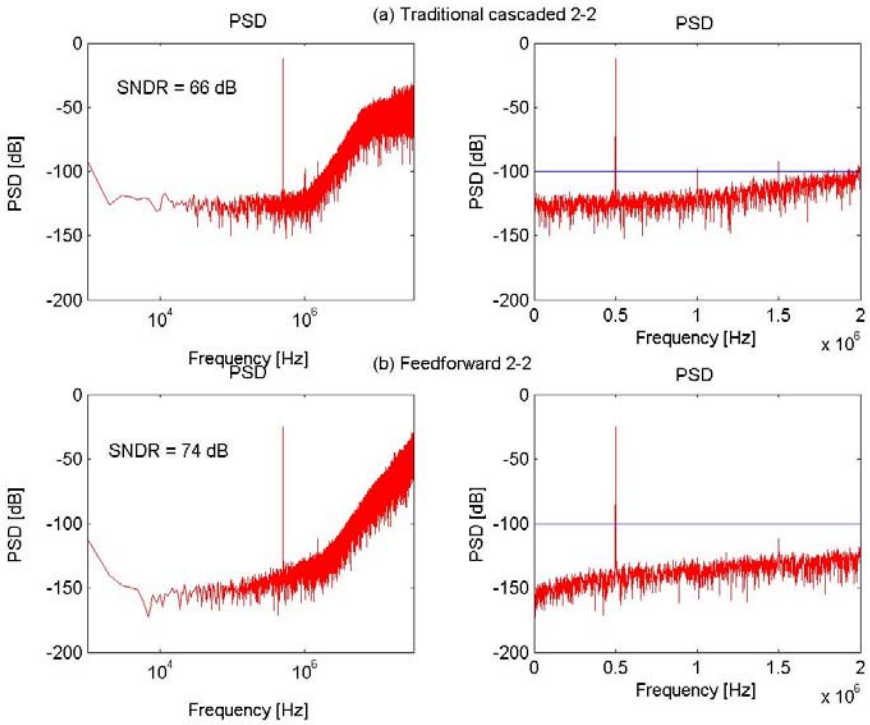

Figure 3.7: PSD of traditional cascaded 2-2 and feedforward 2-2

3.4.2 Dynamic Range

In order to find the performance of GSM and WCDMA architectures, signal-to-noise(plus distortion) ratio is plotted for the entire range of input amplitudes as shown in Figure 3.8.

Simulation results in Figure 3.8 shows an SNDR of 83 dB for GSM and 75 dB for WCDMA in the presence of circuit non-idealities. It assumes a non-linear finite dc gain of 1000 with first and second order non-linearities of 0.01 percent and 0.05 percent respectively. A slew-rate of 150V/us and a GBW of 150 MHz are the other limitations assumed in this simulation with a saturation voltage of 1.5 V. The modulator works properly upto a signal amplitude of -6 dB for WCDMA and -4 dB for GSM, and a significant degradation occurs for amplitudes larger than those values, due to the saturation of the operational amplifiers, and the modulator loop cannot follow the input signal.

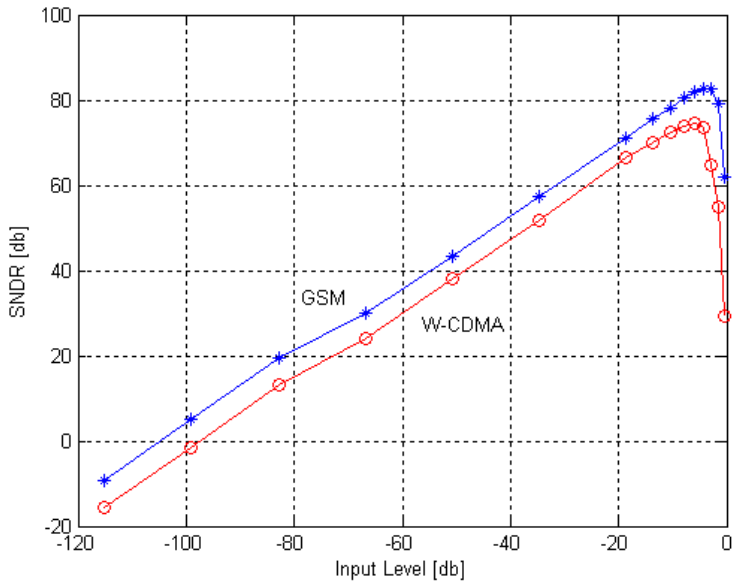

Figure 3.8: SNDR versus the input level for GSM and WCDMA architecture

3.5 A Triple-mode ΣΔ Modulator Design

In this section, we discuss a triple-mode sigma-delta architecture which is an extended version of the dual-mode design. Based on the triple-standard Zero-IF/Low-IF approach, GSM/WCDMA/WLAN triple-mode receiver architecture is proposed in Figure 3.9. In this architecture, three sets of band filters and LNAs are required for GSM/WCDMA/WLAN selection. The multi-standard ADC is shared by these three standards. Table 3.3 summarizes the channel bandwidth and dynamic range requirements of the base-band ADC for the three standards, obtained from the Simulink^{TM} model of the receiver.

3.5.1 Modulator Architecture

This section explores tradeoffs among the wide variety of ΣΔ modulator architectures that can be used to implement a ΣΔ A/D converter suitable for low power and high integration triple-standard receiver. The search for an optimal wide-band ΣΔ topology has been performed by varying the order L, the over-sampling

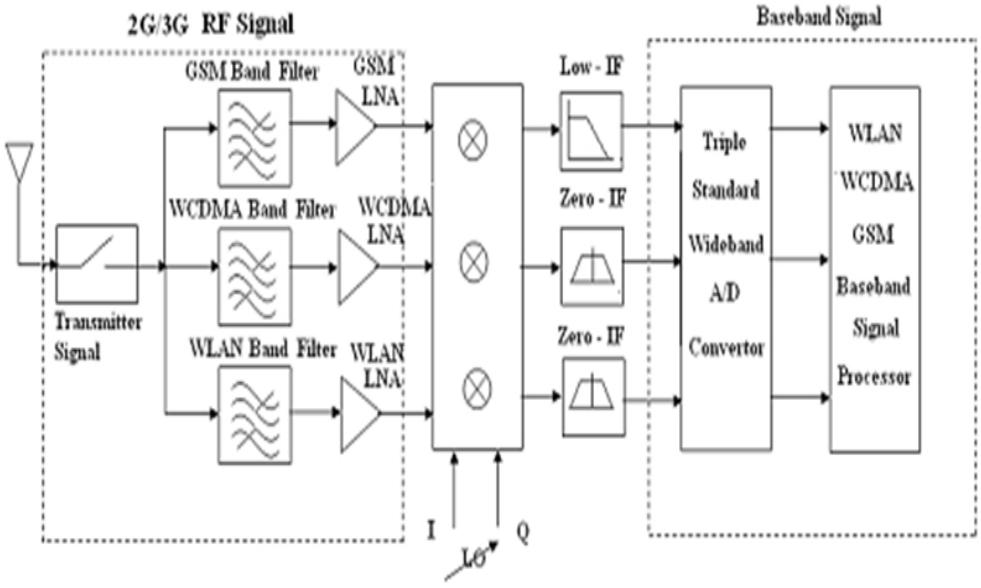

Figure 3.9: Triple standard wideband receiver architecture

ratio (OSR) M and the number of bits B in the quantizer as shown in Table 3.4.

For signals of very wide bandwidth, such as in WLAN receiver, oversampling ratio (OSR) cannot be very high (4 or 5) because the achievable clock frequency is constrained by the process technology. Therefore, the only solution is by increasing the order L and quantizer bits B in order to achieve the required solution.

Table 3.3: ADC requirements for multi-standard receiver

Wireless Standard	Frequency (MHz)	Channel Bandwidth	Dynamic Range
GSM	890-915(Tx) 935-960 (Rx)	200 KHz	> 80 dB
WCDMA	1850-1910 (Tx)1920-1980 (Rx)	2 MHz	>60 dB
WLAN	2401-2473	20 MHz	>50 dB

The dynamic range of a ΣΔ modulator is given by equation 3.23

$$DR = \left(\frac{2}{3}\right)\left(\frac{2L+1}{\pi^{2L}}\right) M^{(2L+1)} \left(2^B - 1\right)^2 \tag{3.23}$$

For low-data rate applications, such as GSM receiver, oversampling ratio (M) can be made higher, due to much smaller signal bandwidth. For higher order or multi-bit modulators the complexity becomes higher, and for higher sampling frequency the requirements of analog building blocks becomes more demanding.

Taking into account the above considerations, a cascaded 2-2-2 structure with multi-bit quantizer is proposed which is shown in Figure 3.10. A second order single bit ΣΔ modulator has been selected as the first stage in order to meet the specifications of GSM mode. Here, we choose a low-distortion swing suppression topology (84), which is highly suitable for wide band applications because of its relaxed requirements on the analog building blocks. The unused blocks in the second and third stages are switched off while working in the GSM mode, taking into account the design considerations like power consumption. In the WCDMA mode, the 4th order modulator (2-2 cascaded) is switched to operation by closing the switch labeled W thus making it programmable. In the WLAN mode, a sixth order modulator (2-2-2 cascaded) is switched to operation by closing the switch labeled S, in order to get more than 50dB SNDR. The novelty lies in the fact that the input to the second and third stages can be directly taken from the output of the second integrator of the preceding stages, since the integrators are only processing the quantization noise.

The modulator output in GSM mode is the output of the first stage. It is given by equation 3.24 and the output of the second stage is given by equation 3.25

$$Y_{GSM}(z) = X(z) + (1 - z^{-1})^2 Q_1(z) \tag{3.24}$$

$$Y_2(z) = I_2(z) + (1 - z^{-1})^2 Q_2(z) \tag{3.25}$$

where,

$$I_2(z) = -g_1 g_2 z^{-2} Q_1(z) \tag{3.26}$$

Table 3.4: Comparison of ΣΔ modulator architectures

Wireless Standard	Order	OSR	F_{clk} (MHz)	Bits (B)	SNR (dB)
GSM	2	64	25.6	1	78
	2	128	51.2	1	80
	2	160	64	1	88
	3	64	25.6	1	105
WCDMA	3	16	80	2	68
	4	16	64	2	73
	4	20	100	1	88
	5	16	80	1	94
WLAN	4	5	100	4	52
	5	4	80	4	50
	6	5	100	3	64
	6	8	160	4	65

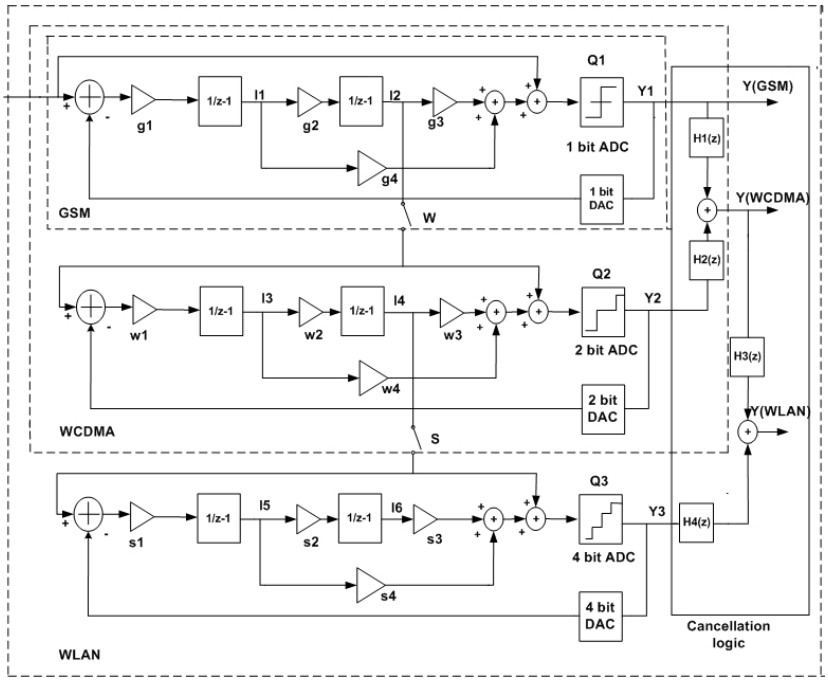

Figure 3.10: Programmable ΣΔ modulator for $GSM/\ WCDMA/WLAN$

The modulator output in WCDMA mode is given by the output of the modified 2-2 cascaded modulator as in equation 3.27

$$Y_{CDMA}(z) = z^{-2}X(z) + g_5(1 - z^{-1})^4 Q_2(z) \tag{3.27}$$

Table 3.5: Coefficients of the triple-mode sigma-delta modulator

GSM		WCDMA		WLAN	
Coeff.	Value	Coeff.	Value	Coeff.	Value
g1	0.5	w1	0.5	s1	0.5
g2	0.5	w2	0.5	s2	0.5
g3	4.0	w3	4.0	s3	4.0
g4	4.0	w4	4.0	s4	4.0

where

$$g_5 = \frac{1}{g_1 g_2} \tag{3.28}$$

is the digital coefficient and the digital transfer functions are

$$H_1(z) = z^{-2} and \;\; H_2(z) = g_5(1 - z^{-1})^2 \tag{3.29}$$

Proceeding in this manner, we have the modulator output in the WLAN mode as in equation 3.30.

$$Y_{WLAN} = z^{-4}X(z) + g_6(1 - z^{-1})^6 Q_3(z) \tag{3.30}$$

where

$$g_6 = \frac{1}{(g_1 g_2)(w_1 w_{2)}} \tag{3.31}$$

is the gain coefficient in the digital cancellation filter, and the digital transfer functions are given in equation 3.32.

$$H_3(z) = z^{-2} and \;\; H_4(z) = g_6(1 - z^{-1})^2 \tag{3.32}$$

The optimal set of coefficient for the three standards are given in Table 3.5.

3.6 Simulations

Figures 3.11, 3.12 and 3.13 show the modulator output spectrum for $GSM/WCDMA/WLAN$ modes for a 0.5V, 0.1/1/10MHz input signal at a sampling

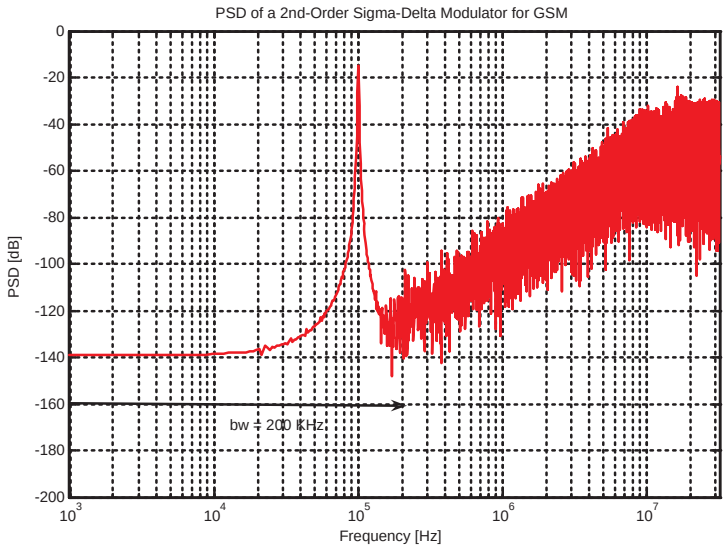

Figure 3.11: Modulator output spectrum in GSM mode.

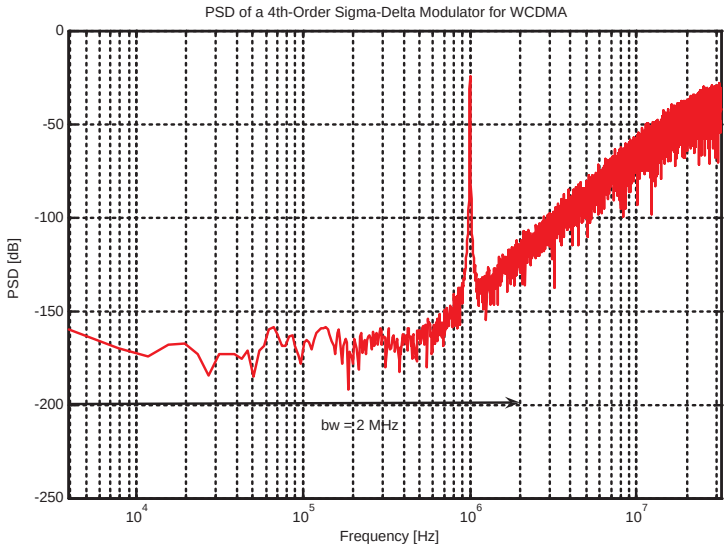

Figure 3.12: Modulator output spectrum in WCDMA mode.

frequency of 64/64/200 MHz respectively. These results show that a high linearity can be achieved due to the low-distortion $\Sigma\triangle$ modulator architecture,

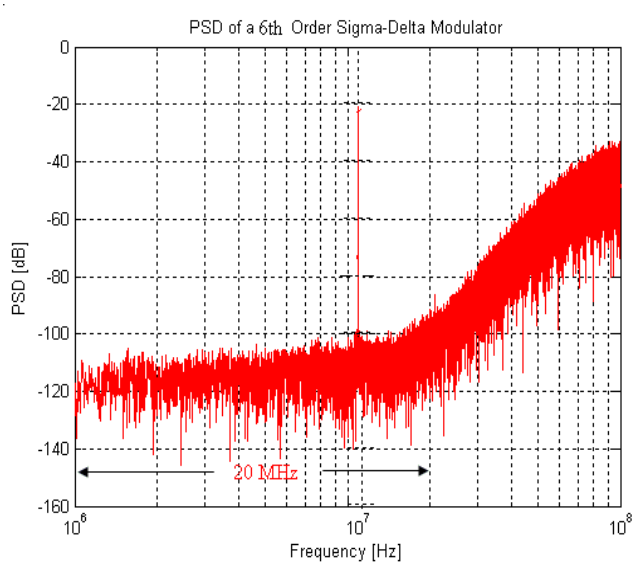

Figure 3.13: Modulator output spectrum in WLAN mode.

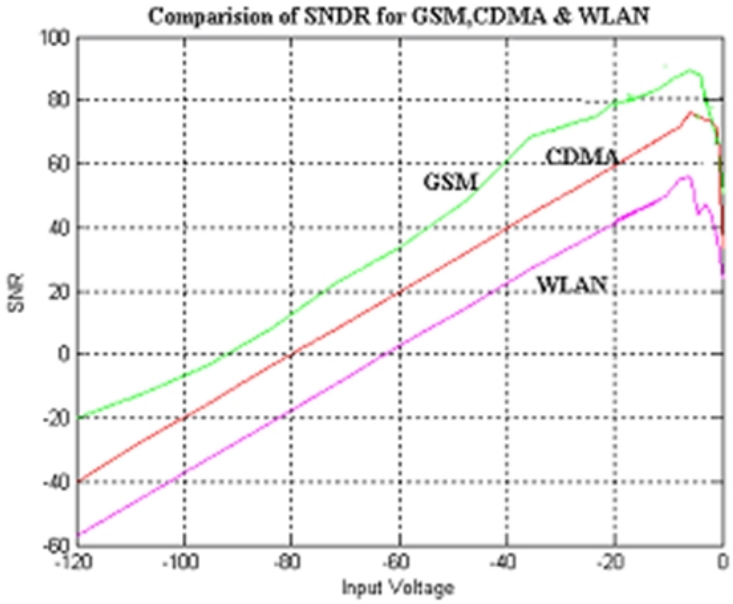

Figure 3.14: SNDR versus input level for GSM/WCDMA/WLAN mode.

multi-bit quantization and modified cascaded architecture. Figure 3.14 presents the simulated Signal-to-Noise plus Distortion Ratio (SNDR) versus input signal

Table 3.6: Performance summary of the triple-mode sigma-delta modulator

Process Supply voltage	TSMC 0.18um CMOS process 1.8V		
Mode Architecture	GSM	WCDMA	WLAN
Sampling frequency	64 MHz	64 MHz	200 MHz
Signal Bandwidth	200 KHz	2 MHz	20 MHz
OSR	160	16	5
Peak SNDR	88 dB	73 dB	58 dB

amplitude, for $GSM/\ WCDMA/WLAN$ standards. Simulation results show a peak SNDR of 88 dB@-4dBFS in GSM mode, a peak SNDR of 73 dB@-6dBFS in WCDMA mode, and a peak SNDR of 58 dB@-6dBFS in the WLAN mode. Table 3.6 summarizes simulated performance of this multi-standard $\Sigma\triangle$ modulator.

3.7 Chapter Summary

This chapter describes the low-distortion swing-suppression topology which has reduced sensitivity to opamp non-idealities compared to the traditional topology. Then a dual-mode architecture is proposed suitable for GSM and WCDMA standards. The behavioral level simulations show the advantages of using feed-forward topology compared to the classical topology with special focus on the optimal selection of scaling coefficients in order to maximize the achievable dynamic range. Further, the dual-mode design has been extended to a triple-mode architecture in which the blocks in the second and third stages can be switched off inorder to reduce the power consumption. Simulation results show that the proposed topology results in a good dynamic range achievable from a given architecture.

Chapter 4

Circuit-level Design

4.1 Introduction

This chapter focuses on the circuit level design of the basic building blocks in the sigma-delta ($\Sigma\triangle$) modulator. It explores the design considerations in selecting the key blocks like operational transconductance amplifiers (OTA), bias networks, common-mode feedback circuit, switches, capacitors, comparators and two-phase clock generation circuitry. The modulator has been designed and simulated in a TSMC 0.18um CMOS process at 1.8V supply voltage using SPICE.

4.2 Sampled-Data vs. Continuous-Time

Sigma-delta modulators can be implemented either as a sampled-data system or in the continuous-time domain. The main difference is that sampled-data sigma-delta systems employ switched-capacitor integrators while continuous-time systems use active RC integrators in the modulators as in Figure 4.1. There are a number of advantages and disadvantages associated with each option which are discussed here.

The need for on-chip resistors (51), (1) (87) with very high linearity makes continuous-time integrators less attractive when compared to switched capacitor integrators which use capacitor ratios which are well-controlled. It also helps to minimize the thermal noise associated with these resistors which occupies a large

area and makes almost impractical to realize on-chip. The frequency response of switched-capacitor integrators can be more accurately predicted because the time constant is a function of capacitor ratios (C_s/C_i) and of the sampling frequency. The time constant of continuous-time integrators, on the other hand is a product of the resistor and the capacitor, and suffers severely from process variations.

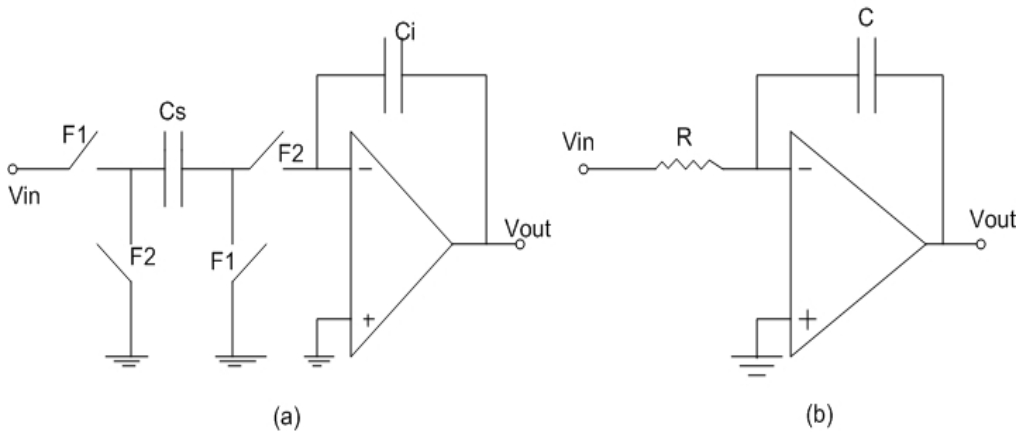

Figure 4.1: (a) Switched-capacitor integrator (b) Continuous-time integrator

Another advantage of switched capacitor $\Sigma\triangle$ systems is that they are less sensitive to clock jitter since most of the charge transfer takes place during the first half clock period rather than being spread uniformly over the entire clock period as in continuous-time integrators. As long as the op-amp settles to the required accuracy, it does not matter whether the op-amp slews or linearly settles. Continuous-time integrators must be linear at all times.

Continuous-time integrators also have their advantages. Since the amplifier settling requirements are generally more relaxed than in switched-capacitor circuits, a very high oversampling ratio is achievable. The oversampling ratio in switched-capacitor integrators is limited by the achievable bandwidth of the op-amps. This makes continuous-time $\Sigma\triangle$ modulators very appealing for high-speed applications. Because of the above mentioned implementation difficulties, the continuous-time approach were not adopted in this work.

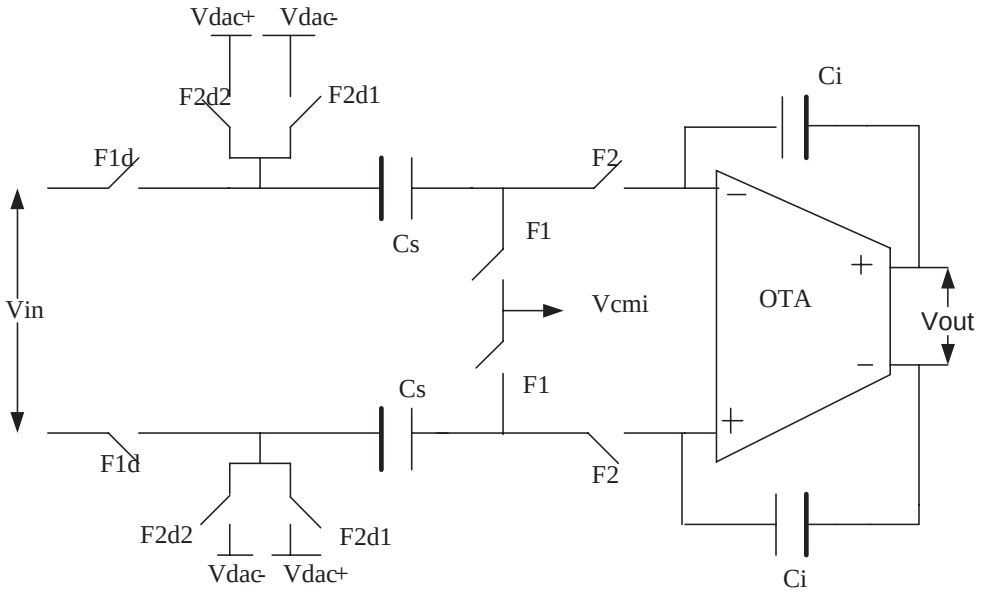

Figure 4.2: Fully-differential switched-capacitor integrator

4.3 Switched-Capacitor Integrator

The integrator is implemented in a fully differential configuration as shown in Figure 4.2 and employs a two-phase non-overlapping clock as shown in Figure 4.3. The input is sampled during phase 1 (F_1 and F_{1d}). During phase 2, the charge is transferred from the sampling capacitor (C_s) to the integrating capacitor (C_i). At the same time, depending on the output value, the appropriate DAC reference level is applied by closing either switches labelled F_{2d1} or F_{2d2}, thus performing the subtraction operation and the results are being accumulated in the integration capacitors.

The integrator employs the bottom-plate sampling technique to minimize signal-dependent charge-injection and clock-feed through. This is achieved through delayed clocks: F_{1d}, F_{2d1} and F_{2d2}. When switches labeled F_1 are first turned off, the charge injection from those switches remains, to a first order, independent of the input signal. Because one of plates is now floating, turning off switches labelled F_{1d} shortly after does not introduce charge-injection errors. Further the switches F_{1d}, F_{2d1} and F_{2d2} are implemented as CMOS transmission gates in or-

Table 4.1: Switches and capacitors in the integrator

Switch/ capacitor	Size
F_1	N: 10/0.18 um P: 10/0.18 um
F_2	N: 10/0.18 um P: 10/0.18 um
F_{1d}	N: 10/0.18 um P: 40/0.18 um
F_{2d1},	N: 10/0.18 um P: 40/0.18 um
C_s	2 pF
C_i	4 pF

der to ensure a small variation in on-resistance across the full input signal range. This also serves to reduce signal-dependent charge injection from the switches to C_s and C_i to a negligible level. Table 4.1 shows the switches and capacitors sizes used in the integrators.

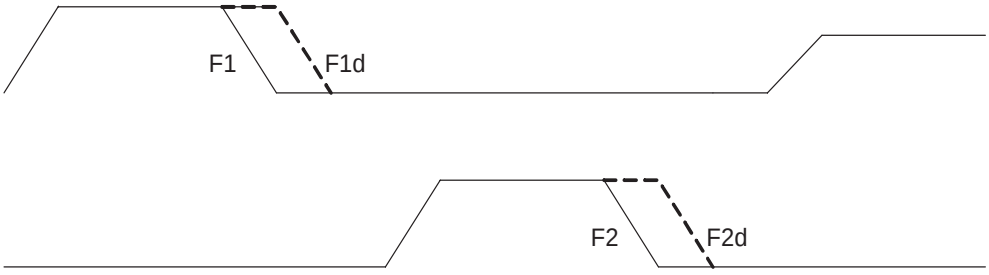

Figure 4.3: Two-phase non-overlap clock

4.3.1 Operational Trans-conductance Amplifier (OTA)

The basic building block in a switched-capacitor integrator is OTA. Figure 4.4 shows the schematic of a fully differential folded-cascode OTA used in the integrators. One of the major driving forces behind the use of fully differential opamps is to help reject noise from the substrate as well as from pass-transistor

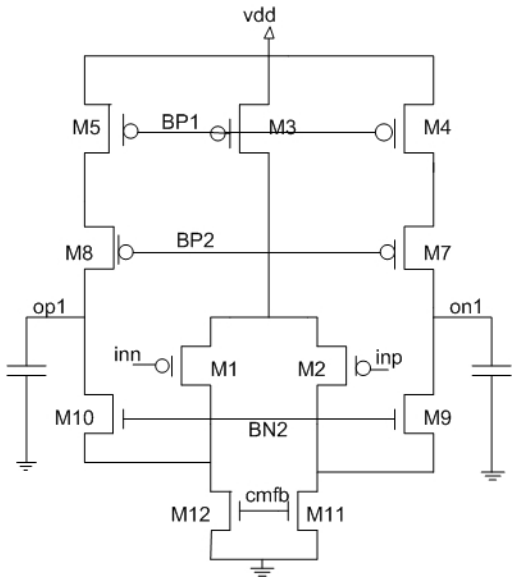

Figure 4.4: Fully-differential folded-cascode OTA

switches turning off in switched-capacitor applications. Since the DC gain requirement is not so demanding, this is a good selection because of its high operation speed/power consumption ratio. The output common-mode voltage was also stabilized using a dynamic switched-capacitor common-mode feedback (CMFB) circuit (64) whose linearity is good enough for this application and does not require extra power consumption. The schematic also includes the biasing stage formed by transistors M_1 to M_4.

Transistors M_1 and M_2 forms the p-type input differential pair taking into account the noise constraints, M_3 acts as a current source, M_{11} and M_{12} act as active load for the input stage, and their gate voltages are controlled by the common-mode feedback circuit; M_9 and M_{10} are cascode transistors which have opposite type as the input transistors. M_4, M_5, M_7, M_8 are current mirrors acting as active load. The main advantages of using folded-cascode are high dc gain even with a single-stage OTA, ease of biasing with a supply voltage as low as 1.8V when compared with normal telescope-cascoded OTAs, simple structure where frequency compensation is realized by the load capacitance. Also the common-mode control is easier and more accurate, since there is only one stage. Table 4.2 shows the transistor sizes of folded-cascode OTA.

Table 4.2: Transistor sizes of folded-cascode OTA

Transistor	Size (um)
M1, M2	720/0.48
M3	432/0.48
M4, M5, M7, M8	216/0.48
M9, M10	144/0.48
M11, M12	72/0.48

4.3.2 Common-mode Feedback

Common-mode feedback is required in fully-differential amplifiers to define the voltages at the high-impedance output nodes. The amplifier employs dynamic or switched-capacitor common-mode feedback as shown in Figure 4.5. Capacitors labelled C_c generate the average of the output voltages, which is used to create control voltages for the opamp current sources. The dc voltage across C_c is determined by capacitors C_s, which are switched between bias voltages and desired common-mode voltage. The bias voltages are designed to be equal to the difference between the desired common-mode voltage and the desired control voltage used for the opamp current sources.

The capacitors being switched, C_s, might be between one-quarter and one-tenth the sizes of the non-switched capacitors, C_c. Using larger capacitance values overloads the opamp more than is necessary during the phase ϕ_2, and their size is not critical to circuit performance. Reducing the capacitors too much causes common-mode offset voltages due to charge injection of the switches. Normally, all of the switches would be realized by minimum-size n-channel transistors (0.22um/0.18um) only, except for the switches connected to the outputs, which might be realized by transmission gates to accommodate a wider signal swing. In applications where the opamp is being used to realize switched-capacitor circuits, switched-capacitor CMFB circuits are generally preferred over their continuous-time counterparts since they allow a larger output signal swing. Table 4.3 shows the capacitor sizes used in the switched-capacitor common-mode feedback

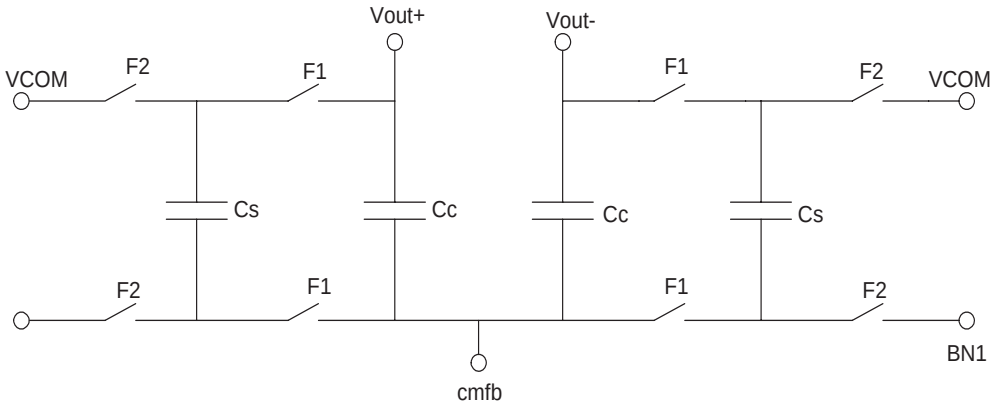

Figure 4.5: A switched-capacitor common-mode feedback

Table 4.3: Capacitor sizes in the switched-capacitor CMFB

Capacitor	Size
C_s	20f
C_c	100f

4.3.3 Bias

Figure 4.6 shows the biasing scheme for the OTA which incorporates a wide-swing cascode current mirror without restricting the signal swings much. The n-channel wide-swing cascode current mirror consists of transistors Q_1-Q_4, along with the diode-connected biasing transistor Q_5. The pair Q_3, Q_4 acts similarly to a diode-connected transistor at the input side of the mirror. The output current comes from Q_1. The gate voltages of cascode transistors Q_1 and Q_4 are derived by the diode-connected transistor Q_5. The current for this biasing transistor is actually derived from the bias loop via Q_{10} and Q_{11}.

Similarly, the p-channel wide-swing cascade current mirror is realized by Q_6-Q_9. Transistors Q_8 and Q_9 operate as a diode-connected transistor at the input side of the mirror. The current-mirror output current is the drain current of Q_6. The cascade transistors Q_6 and Q_9 have gate voltages derived from diode-connected Q_{14}, which has a bias current derived from the bias loop via Q_{12} and

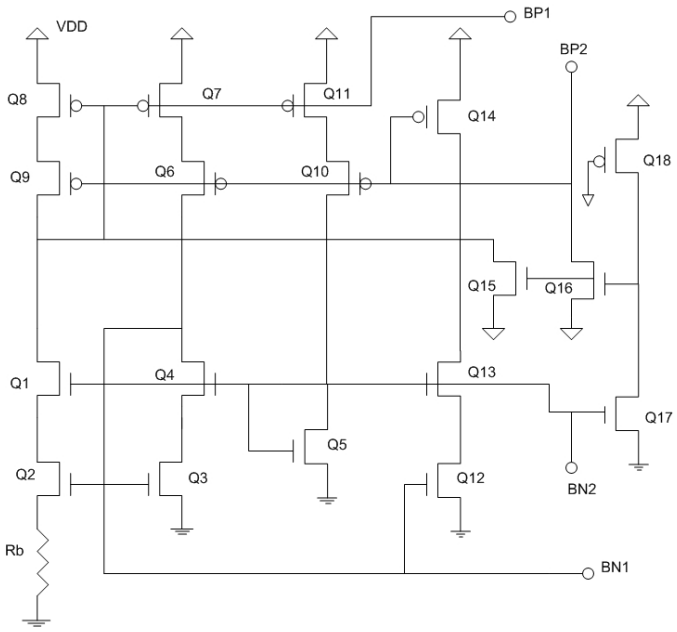

Figure 4.6: Wide swing constant transconductance bias circuit

Table 4.4: Transistor sizes in the bias circuitry

Transistor	Size (um)	Transistor	Size (um)	Trasistor	Size (um)
Q1, Q2	10/0.48, 30/0.36	Q8, Q9	30/0.36, 30/0.48	Q15	10/0.36
Q3, Q4	10/0.36, 10/0.48	Q6, Q7	30/0.48, 30/0.36	Q16	10/0.36
Q5	1.5/0.48	Q14	5/0.48	Q17	10/0.36
Q12, Q13	10/0.36, 10/0.48	Q10, Q11	30/0.48, 30/0.36	Q18	20/2

Q_{13}. Table 4.4 shows the transistor sizes used in the bias circuitry.

The bias loop does have the problem that at start-up it is possible for the current to be zero in all transistors, and the circuit will remain in this stable state forever. To ensure this condition does not happen, it is necessary to include start-up circuitry that affects only the bias-loop in the case that all currents in the loop are zero. Here the start-up circuitry consists of transistors Q_{15}, Q_{16}, Q_{17} and Q_{18}. In the event that all currents in the bias loop are zero, Q_{17} will be off. Since Q_{18} operates as a high-impedance load that is always on, the gates of Q_{15} and Q_{16} will be pulled high. These transistors then will inject currents into the

bias loop which will start up the circuit. Once the loop starts up, Q_{17} will come on, sinking all of the current from Q_{18}, pulling the gates of Q_{15} and Q_{16} low, and thereby turning them off so they no longer affect the bias loop.

4.3.4 Simulation Results of OTA

Table 4.5 gives the performance summary of OTA. Figure 4.7 shows the frequency response of OTA. Simulation results show that OTA has more than 60 dB gain, unity gain-bandwidth (UGB) of 442 MHz and a phase margin of 62 degree. Figure 4.9 show the transient response which shows that the maximum output swing of OTA is 2V (differential). Figure 4.10 shows the Slew Rate (SR) of OTA whose value is 300V/us at load capacitance C_L=2pF. OTA draws a maximum current of 2.1 mA dissipating 3.78 mW in 0.18 um CMOS technology. A second configuration is also considered which is shown in Figure 4.8 (Cascode OTA circuit with high output resistance). This OTA design is more stable with increased load capacitance.

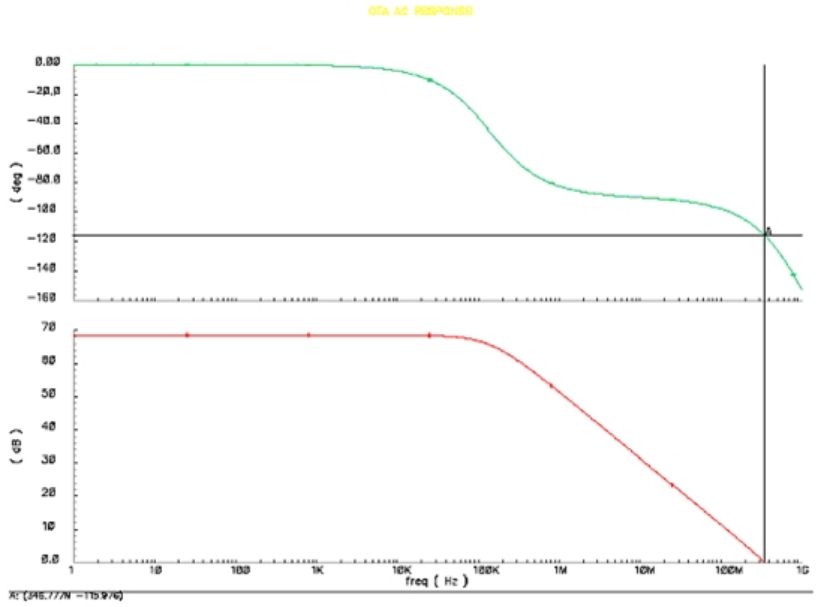

Figure 4.7: Frequency response of OTA.

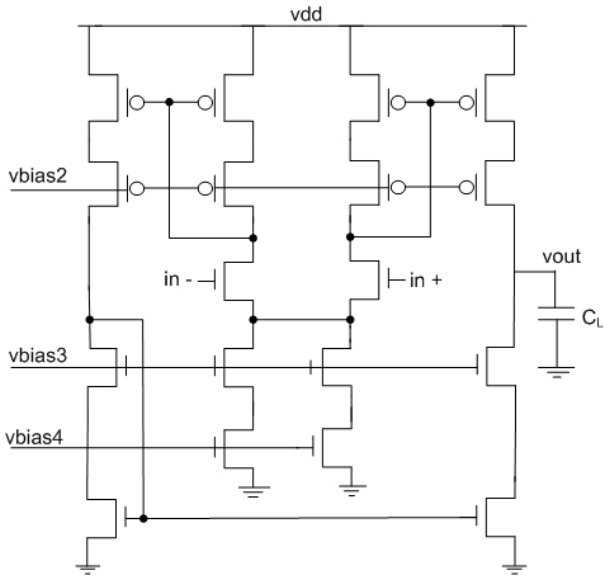

Figure 4.8: Cascode OTA circuit with high output resistance.

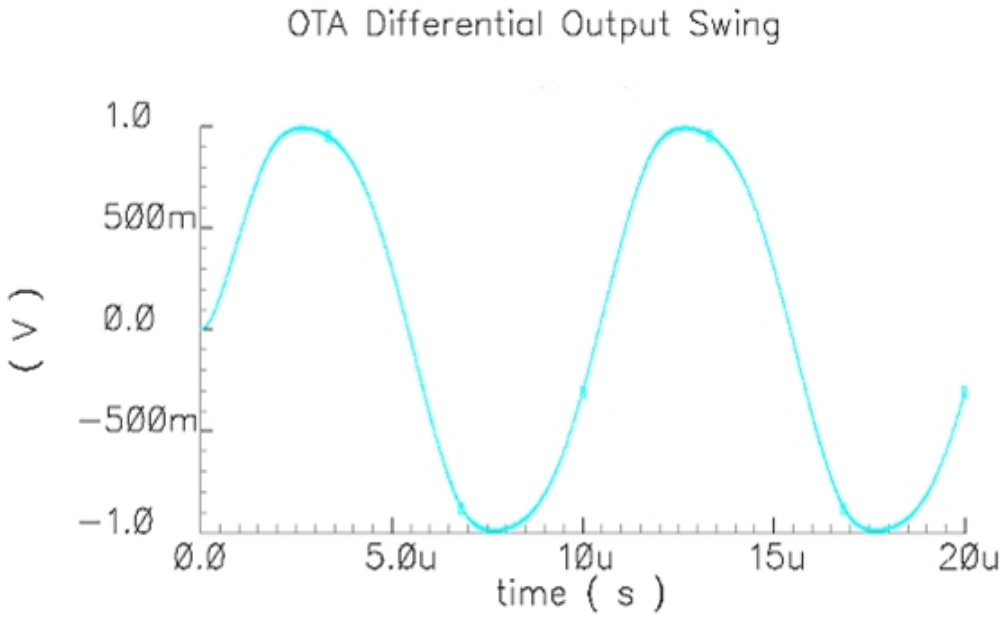

Figure 4.9: Transient response of OTA.

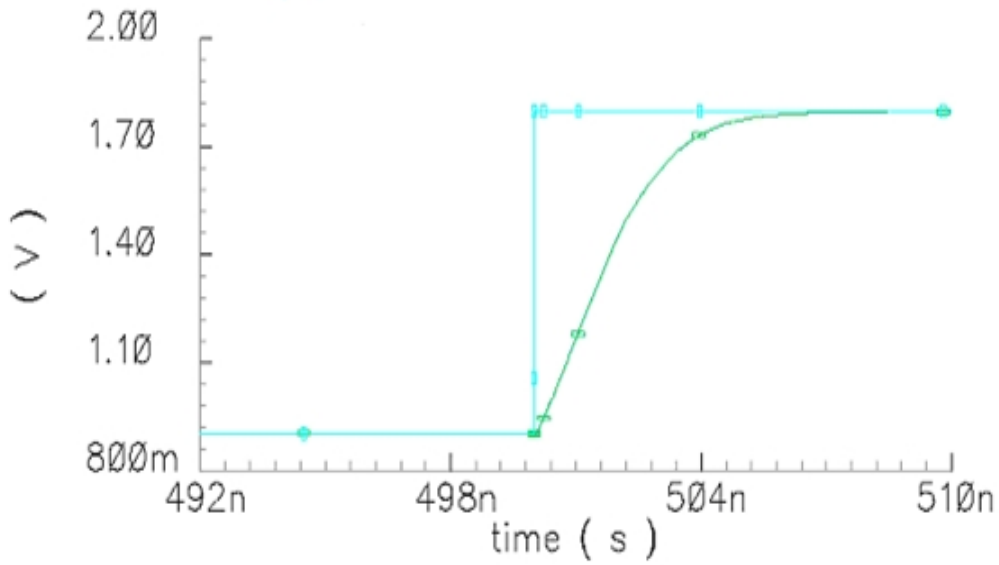

Figure 4.10: Slew rate of OTA.

4.3.5 Process Variation Analysis

Severe uncertainty is involved in nano-scale CMOS fabrication which causes variation in device parameters (7), (36), (58), (55). This leads to variation in different process parameters such as channel length, gate-oxide thickness, threshold voltage, metal wire thickness etc. These variation are categorized into inter-die variation and intra-die (systematic or random). Moreover, the increasing statistical variation in the process parameters has emerged as a problem in deep sub-micron circuit design and can cause significant difference in performance of the fabricated chip compared to designed. Hence, variability analysis and modeling of the factors contributing to the total performance, considering the effects of random variation in the process parameters, is important for designing analog CMOS circuits as well. Since opamp is the key building block in this design, in this section, opamp variability is discussed. First, gain variation corresponding to different loading effect is considered. Figure 4.11 shows parametric analysis of the gain and phase variation corresponding to load capacitance 1fF to 10fF. As the load capacitance is increased the gain slightly decreased, due to various second order effects.

Table 4.5: Performance summary of the folded-cascode OTA

Opamp Specification	OTA
DC Gain	63.7 dB
GBW (CL = 2pF)	442 MHz
SR (CL = 2pF)	300 V/us
Phase Margin	62 degree
Output Swing	2V (differential)
Maximum Current	2.1 mA
Power Dissipation	3.78 mW
Technology	0.18 um CMOS

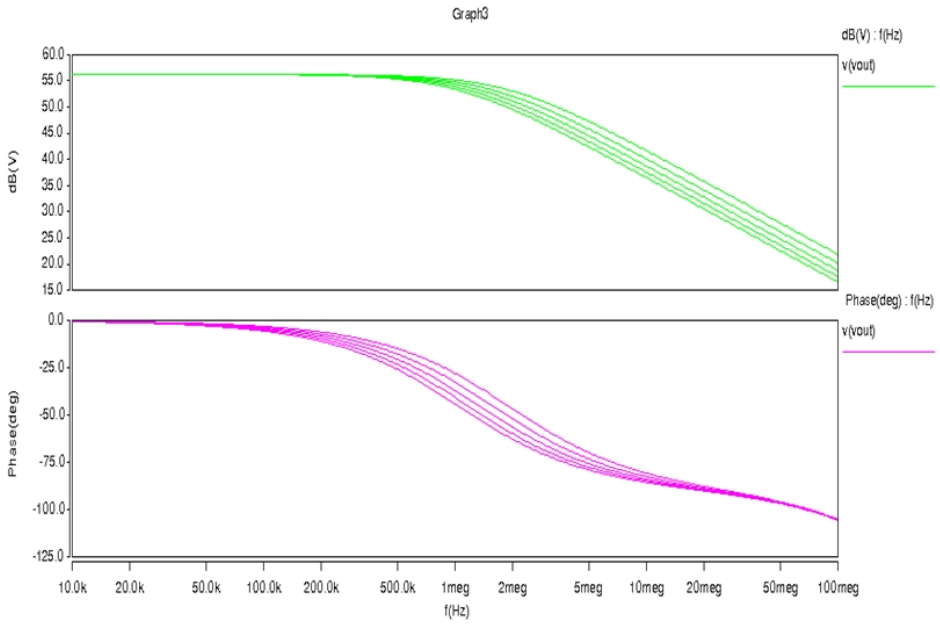

Figure 4.11: Frequency response of OTA corresponding to load capacitance 1fF to 10fF.

Figure 4.12 shows gain and phase variation corresponding to threshold voltage variation. The primary goal of this analysis is to assess the gain and phase variation as a result of threshold voltage (V_{th}) variation. These characterizations were carried out for opamp design with the help of Monte Carlo Simulations (10), (94). The distribution ($\pm$ 3σ) of these parameters is assumed to be Gaussian with the

variance of 10%.

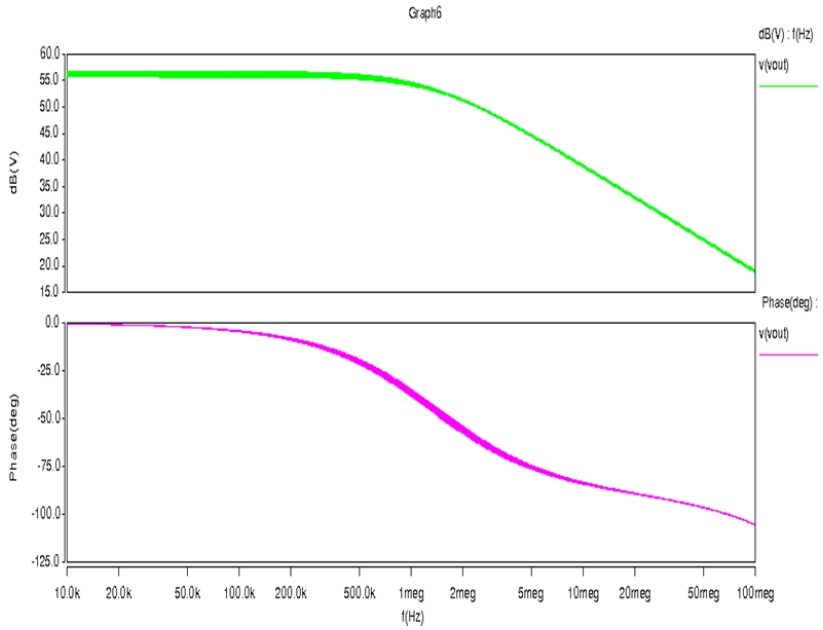

Figure 4.12: Monte carlo simulation of frequency response of OTA with 10 % variation in threshold voltage.

4.4 Switches

The switches used in the integrator are implemented with complementary MOS devices because the DC voltages are biased at mid-supply (67). In CMOS switches, the sizing of the NMOS and PMOS devices is critical. Figure 4.13 shows the on-resistance of the CMOS switch for varying widths of NMOS and PMOS transistors. For linearity reasons, the input switches, labeled F_{1d}, F_{2d1}, and F_{2d2} in Figure 4.2 should be designed for equal impedances. This means the PMOS should be made larger than the NMOS by a factor equal to the ratio μ_N/μ_P as shown in equation 4.1.

$$\frac{(\frac{W}{L})_P}{(\frac{W}{L})_N} = \frac{\mu_N}{\mu_P} \tag{4.1}$$

A switch size of 10/0.18 μm for NMOS and 40/0.18 μm for PMOS is chosen for F_{1d}, F_{2d1}, and F_{2d2} as shown in the Table 4.1. The bottom-plate switches, labelled F_1 and F_2 should be designed for a first-order cancellation of charge-injection errors. The error is given in equation 4.3.

$$\Delta V_{OUT} = -\frac{1}{2}.\frac{(Q_{chan})_N}{C_S} + \frac{1}{2}.\frac{(Q_{chan})_P}{C_S} \tag{4.2}$$

$$= -\frac{1}{2}.\frac{C_{ox}}{C_S}\{(W_N L_N(V_{DD} - V_{IN} - V_{THN}) - W_P L_P(V_{IN} - V_{THP})\} \tag{4.3}$$

For a partial cancellation of charge-injection error, the NMOS and PMOS devices should be designed to have equal sizes as shown in equation 4.4.

$$W_N L_N = W_P L_P \tag{4.4}$$

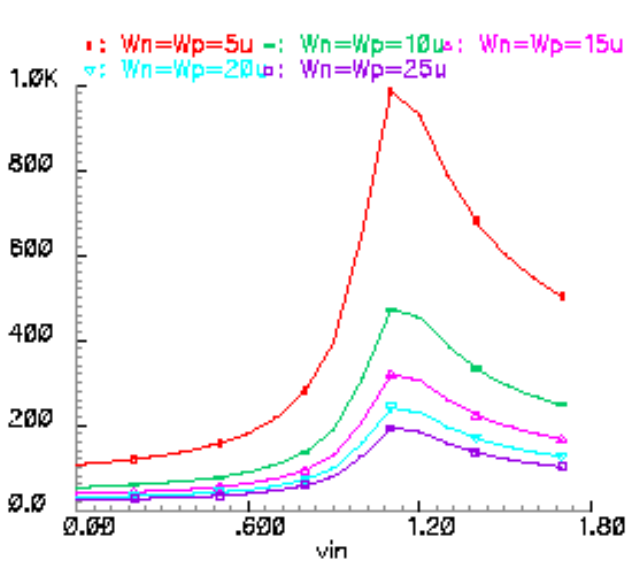

Figure 4.13: On-resistance of the sampling switch.

A switch size of 10/0.18 μm is selected for F_1 and F_2 as from the Table 4.1 which has an on-resistance of 500 ohm. The fully-differential configuration of the integrator further mitigates the effects of signal-dependent charge injection. The

values of sampling and integration capacitors are 2pF, 1pF, 0.5pF, 0.2pF and 4pF, 2pF, 1pF, 0.4pF respectively.

In addition to sizing the switches for linearity and charge-injection reasons, the sampling network also needs to be designed for sufficient bandwidth. Increasing the switch sizes decreases the resistance but increases the parasitic capacitance of the network. An optimum value of the switch size which yields a minimum R-C time constant can be determined.

4.5 Circuit Noise

There exist mainly two sources of circuit noise (50), (37) which degrades the performance of well-designed high-resolution $\Sigma\triangle$ modulator. They are thermal noise (kT/C) and flicker (1/f) noise in the transistors comprising the modulator. Thermal noise is the result of the random motion of electrons in a conductor. It is proportional to absolute temperature, it has a Gaussian amplitude distribution, and its power spectral density is white.

The source of flicker noise is believed to be due to imperfections in the crystal lattice at the interface between the oxide and the silicon layers. The power spectral density of flicker noise is approximately inversely proportional to frequency and is independent of the device biasing conditions. Its amplitude distribution tends to vary from device to device and may not be Gaussian. The flicker noise of a MOS transistor is inversely proportional to its gate area. So the 1/f noise in an amplifier can be reduced to a great extent simply by increasing the size of transistors that contribute significantly to the input-referred flicker noise. Therefore the total power spectral density of the equivalent input-referred noise can be found by adding the two independent noise sources and is given by equation 4.5 where k is Boltzmanns constant, T is the absolute temperature, γ is a bias and technology dependent factor, g_m is the transconductance of the device, K_f is an experimentally determined constant that is bias independent but highly technology dependent, and long-channel transistor behaviour is assumed.

$$\frac{\overline{v_{in}^2}}{\Delta f} = 4kT\gamma\frac{1}{g_m} + \frac{K_f}{WLC_{ox}f} \tag{4.5}$$

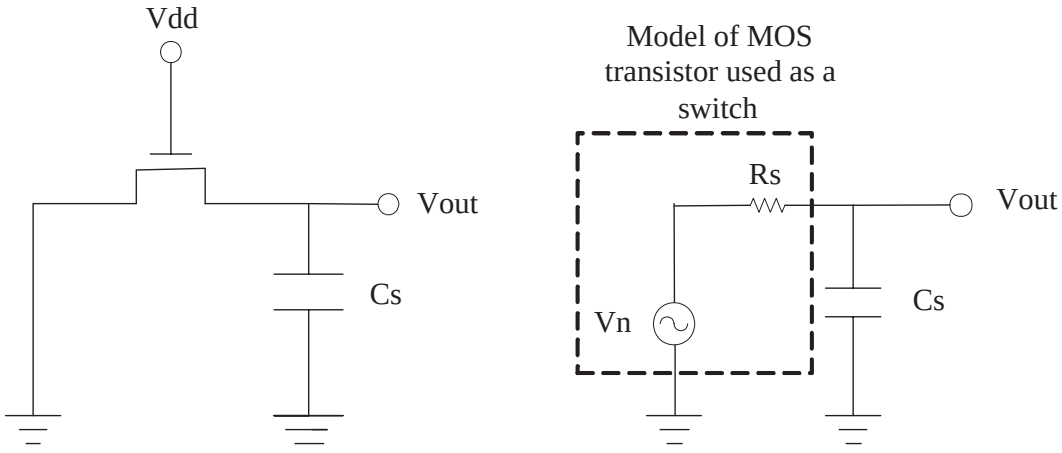

Fig (a) A switched-capacitor sampling network

(b) Circuit model for sampling noise

Figure 4.14: A switched-capacitor sampling network

4.6 Sampling and Integrating Capacitors

The sizes of the sampling and integrating capacitors are governed by the noise requirements. The ideal input-referred thermal noise of the integrator is given by equation 4.6

$$P_{Ni} = 4\frac{kT}{C_s} \tag{4.6}$$

Figure 4.14a represents the switched-capacitor sampling network in the integrator of Figure 4.2 when F_1 is high. The power of the sampled noise can be estimated using the circuit in Figure 4.14b, where the MOS switch is modelled as a resistor in series with a noise voltage source. When the sampling switch in Figure 4.2 is opened, the noise voltage is stored on C_s. If the sampling period is much longer than the time constant formed by R_s and C_s, the high frequency components of the noise are aliased into the frequency band from 0 to f_s. As a result, the full power of the sampling noise appears in this band with an approximately white spectral density. kT/C_s is thus the total power of the input-referred

sampling noise introduced during F_1 in the integrator. Since the sampling noise is distributed uniformly across the Nyquist band, if the signal is oversampled by a factor M the thermal noise power appearing in the base band is given by equation 4.7

$$\overline{v_M^2} = \frac{kT}{MC_s} \tag{4.7}$$

When the charge that was sampled during F_1 is transferred from C_s to C_i during F_2, additional thermal noise is introduced by the switches. The thermal noise introduced by the switches in the circuit during F_2 is band limited by the response of the operational amplifier as well as the time constant formed by the on-resistance of the switches and the sampling capacitor.

4.7 Incomplete Linear Settling and Slew Rate Limitation

The finite bandwidth of operational amplifiers translates into incomplete linear settling in the time domain when the amplifiers are used in switched-capacitor integrators. This causes an integrator gain error as given in equation 4.8.

$$\frac{V_{OUT}(z)}{V_{IN}(z)} = \frac{C_s}{C_i}\frac{z^{-1}}{(1-z^{-1})}(1-\varepsilon) \tag{4.8}$$

where

$$\varepsilon_s \;=\; e^{-n_\tau} = 2^{-N}, \quad (settlingError) \tag{4.9}$$

$(1-\varepsilon)$ is the gain error.

$$n_\tau = -\ln(2^{-N}), (Number\ of\ Time\ Constants) \tag{4.10}$$

$$\frac{C_s}{C_i} \;=\; feedback\ factor. \tag{4.11}$$

From equation 4.9, it is clear that higher the required resolution (N) of the ADC, the smaller the tolerable settling error will be. This means a higher bias current is needed in amplifiers.

If we substitute the unity-gain frequency of the OTA we designed, we can compute the number of time constants using the equation 4.12.

$\omega_{uT} = \frac{1}{\tau} \geqslant 2 f_s n_\tau$

$442\text{MH}_z \geqslant 2 \times 64 MHz \times n_\tau,\ n\tau \leqslant 3.45$

which gives a resolution of around 5 bits using the equation 4.10.

This shows how important it is to improve the unity gain bandwidth and dc gain of the opamp to have small settling error as the clock frequency increases, and to get the required accuracy. There exists a relationship between the slew rate 'S' and settling time constant 'τ' such that slewing never occurs and the settling process is entirely linear and is given by equation 4.12

$$S = \left(1 + \frac{C_s + C_p}{C_i}\right) \times \frac{V_{GS} - V_T}{\tau} \tag{4.12}$$

where V_{GS} is the gate-to-source voltage, V_T is the threshold voltage of the input transistors, and V_{GS}-V_T is referred to as the transistor overdrive voltage. C_s is the sampling capacitance, C_i is the integrating capacitance and C_p is the parasitic capacitance in equation 4.12.

If we compute τ by substituting the SR (300 V/us) of our OTA, and assuming an overdrive voltage of 0.5 and parasitic capacitance of 1 pF, we get

$\tau = \left(1 + \frac{2p+1p}{4p}\right) \times \frac{0.5}{0.3} = 2.92ns$, which is the settling time constant. Hence it is clear that it is necessary to employ relatively large overdrive voltages to simultaneously achieve both a high slew rate and a large settling time constant.

4.8 Integrator Leakage and Amplifier Gain Requirements

Integrator leak, (100) which is a consequence of finite amplifier dc gain, limits the extent to which low-frequency quantization noise is shaped in a $\Sigma\triangle$ modulator, thereby increasing the base band noise. The transfer function of a leaky integrator is given by equation 4.13,

$$H(z) = \frac{z^{-1}}{1 - (1 - \epsilon)z^{-1}} \tag{4.13}$$

where ϵ is referred to as the leakage factor.

In a switched-capacitor integrator of Figure 4.2 , the integrator leakage factor is given by equation 4.14,

$$\epsilon = \frac{1}{A_0 + 1} \times \frac{C_s}{C_i} \tag{4.14}$$

where A_0 is the amplifiers open loop gain. An amplifier gain of 63 db (1.5 K) gives the integrator leakage factor as 0.02% in order to ensure sufficient linearity and parasitic insensitivity in the integrator response.

4.9 Quantizers

The quantizers (23) in the cascaded modulator comprises of a single comparator (68) and a 1-bit D/A converter in the first stage and a multi-bit A/D and D/A in the second and third stages (30). The comparator is implemented as a cascade of a regenerative latch followed by an SR latch, while the 1-bit DAC is a simple switch network connected to off-chip reference voltages. Errors introduced by the DAC in the first stage of the modulator are added to the input signal and directly degrade the performance of the modulator. Therefore, this DAC is designed to settle to the resolution of the modulator. However, errors associated with the other components of the quantizers are greatly attenuated in the base band by noise shaping. Thus the principle design objective for these circuits is low power consumption.

4.9.1 Comparators

The regenerative latch (cross-coupled inverters) in Figure 4.15 is made up of M_3, M_4, M_5, and M_6. When phi_1 is low, the p-channels, M_5 and M_6 of the latch are isolated from the n-channels, M_3 and M_4. In addition, the outputs of the decision circuit are pulled high, that is, the outputs of the comparator are low, $Q = \overline{Q} = 0$. When phi_1 signal transitions high, the regenerative action of the latch causes an imbalance in the decision circuit, forcing the outputs into a state determined by V+ and V-. Table 4.6 shows the transistor sizes in the regenerative latch. Figure 4.17 shows the time domain response of the comparator. A second

Table 4.6: Transistor sizes in the regenerative latch

Transistors	Size (μm)
M_1, M_3, M_2, M_4	0.9/0.45
M_9, M_{10}	2.25/0.45
M_5, M_6, M_7, M_8	2.25/0.45
M_{11}, M_{12}, M_{13}, M_{14}	1.2/0.18

configuration is also considered which is shown in Figure 4.16 (Clamped push-pull output comparator). The layout design of clamped push-pull output comparator is simpler compared to Figure 4.15.

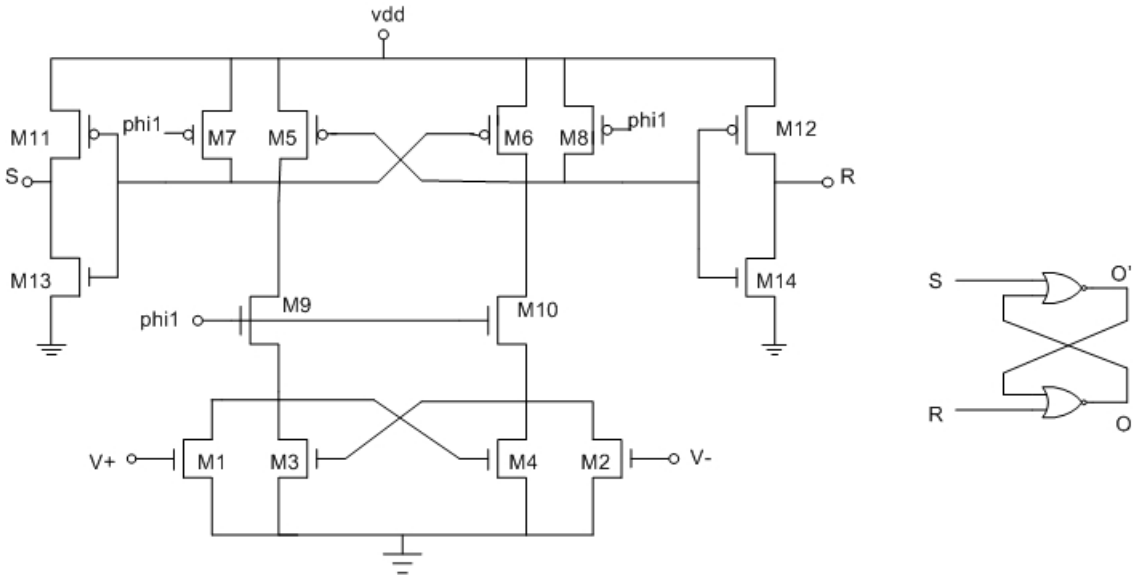

Figure 4.15: Regenerative comparator.

The need for pre-amplification stage depends on the comparator sensitivity and speed. The preamp stage amplifies the input signal to improve the comparator sensitivity and isolates the input of the comparator from switching noise coming from the positive feedback stage.

Sigma-delta modulators show little sensitivity to the errors induced during the

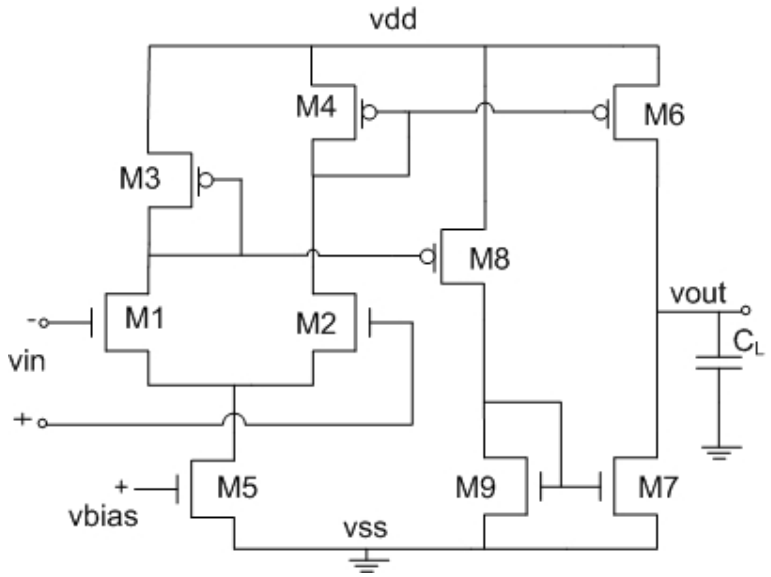

Figure 4.16: Clamped push-pull output comparator

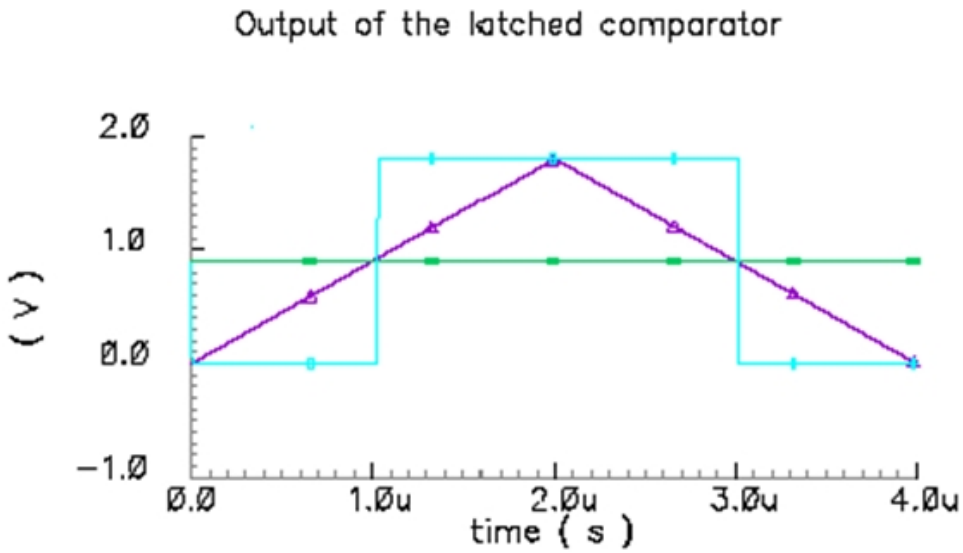

Figure 4.17: Time domain simulation of comparator

internal quantization. The position of the quantizer in the modulator loop causes these errors, the same as the quantization error, to be attenuated in the signal band. Such errors include offset, hysteresis, gain error and non-linearity. For the case of single-bit (two-level) quantization, the error possibilities are reduced to

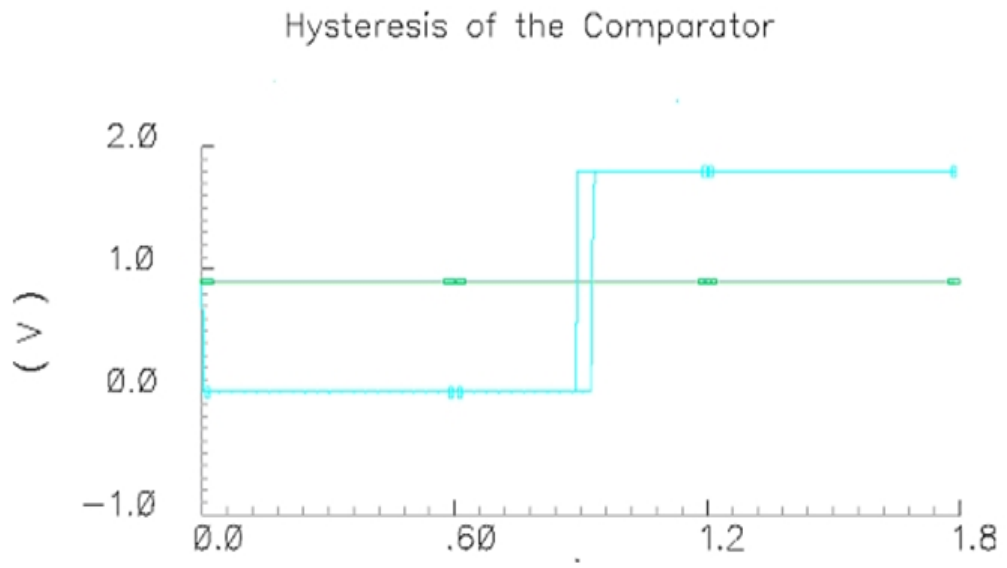

Figure 4.18: Hysteresis of the comparator

offset and hysteresis because it is not possible to define either gain or non-linearity. The effect of comparator offset voltage on the overall modulator is reduced with value equal to the one given in equation 4.15, where L stands for the order of the modulator loop and A_v is the amplifier open-loop low-frequency gain. For a second-order modulator the offset of the comparator is attenuated by A_v^2, which makes negligible the effect of offset voltage. On the other hand, the hysteresis, as the indetermination of the output state for small input values, which is another source of error, whose contribution to the total noise power is also attenuated in the signal band by the high DC-gain of the integrators. Thus, resolutions as low as 10% full scale do not degrade the modulator performance.

$$V_{off,\mathrm{mod}} = \frac{V_{off,comp}}{(A_v)^L} \tag{4.15}$$

The plot in Figure 4.18 shows the hysteresis of the comparator which is equal to 20 mV. Because the hysteresis requirement for the comparator is not very demanding in the case of single-bit quantizer, a simple regenerative latch without a pre-amplification stage is a good candidate in order to minimize power consumption. However, in the case of multi-bit quantizers, as the LSB decreases and the resolution requirements becomes more stringent, the hysteresis inherent

in the latched comparators might become a problem. In that case, more complex topologies with pre-amplification stages must be used, with a considerable increase in the power consumption.

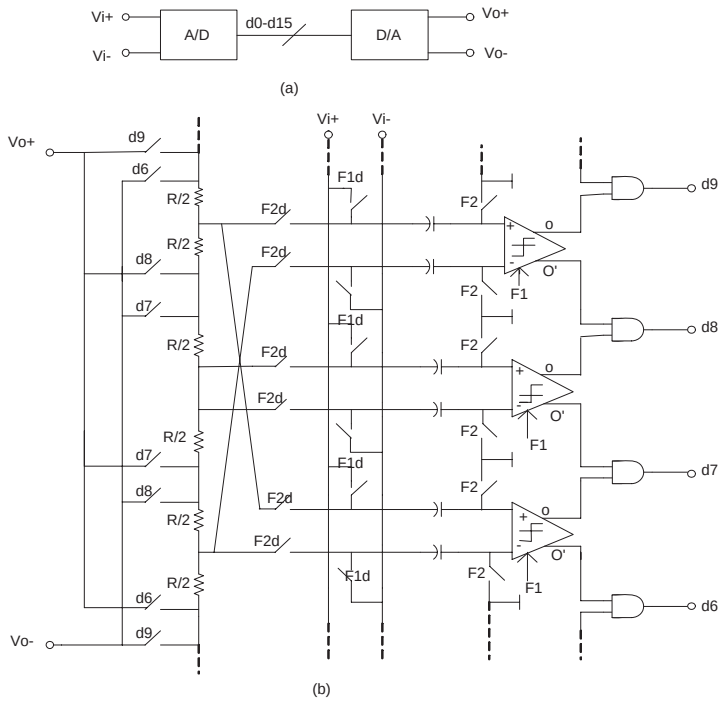

Figure 4.19: (a) Block diagram of the A/D/A system (b) Partial view of its SC implementation.

4.9.2 Multi-bit A/D/A Converters

A 4-bit A/D converter, a flash architecture is suitable, because data have to be coded into a small number of bits at the clock rate. Figure 4.19 shows three of sixteen comparison stages of the converter. The classical architecture of these stages has been slightly modified to enable the comparison of differential signal v_i, and reference v_r, voltages, using two capacitors to compute the difference (v_{i+} - v_{i-}) - (v_{r+} - v_{r-}). During phase F_2, the reference voltages are sampled onto the two capacitors which are derived from the stream of resistive network. At the end of phase F_2, the comparator is activated to evaluate the sign of the difference.

All the comparators are identical that are used in the first and second stage of the quantizers. Without a pre-amplification stage, a comparator may provide a resolution not much better than 50mV, which is enough to guarantee the INL requirements, taking into account the value of the least significant bit (LSB). However, if the LSB decreases, as would happen if the gain of the ADC had to be increased, the hysteresis inherent in the latched comparators might become a problem. In that case, more complex topologies with pre-amplification stages must be used, with a considerable increase in the power consumption. That is the reason why it is interesting to keep the ADC gain equal to unity. After the comparator array, sixteen AND gates generate a 1-of-16 code which is translated to binary by an encoding logic using an encoder. To implement the DAC, the 1-of-16 code is used to select through analog switches the voltages generated in a resistive ladder, also used to generate the reference voltages for the ADC. The resistances in the ladder are R/2 = 100 ohm; this value is low enough to ensure that the settling error of the voltages in the ADC input capacitors are not excessive. All switches are complementary with a size of 10um/0.18um for both NMOS and PMOS transistors. The value of the two sampling capacitance was chosen to be 500 fF.

4.9.3 Digital-to-Analog Converters

The 1-bit D/A converters are implemented as switch networks that are controlled by the comparator outputs. The outputs of the SR latches used in the comparators are buffered by inverters that drive two switches connected to the positive and negative reference voltages which are generated off chip.

4.10 Clocks

In switched-capacitor circuit two non-overlap clock phases are needed. In order to reduce the influence of charge injection (also called clock feed through), a delayed version is needed for each clock phase. A complement version is also needed for each clock phase when a transmission gate is used. Normally 4-8 clock phases are needed in a $\Sigma\triangle$ modulator. These clock phases are usually generated on-chip.

In a normal signal generator the delayed version clock phase has a same delay at both rising edge and falling edge. However in most modulators only the falling edge needs to be delayed in order to reduce the signal-dependent charge injection. The rising edge does not have to be delayed. The advantage of non-delayed rising edge is that the settling time can be increased, which reduces the requirement on the OTA driving capability. The rising edges of the delayed clocks should be lined up with the rising edges of the non-delayed versions to increase the amount of available settling time for the OTA, which is given by the equation 4.16.

$$T_{settleavailable} = \frac{T_s}{2} - t_{nol} - t_r - t_f \tag{4.16}$$

where T_s is sampling period, t_{nol} =Nonoverlap Time, t_r =Rise Time and t_f =Fall Time. A circuit to realize two-phase non-overlapping clocks is shown in Figure 4.20. The two basic non-overlap phases F_1 and F_2 are generated by latches. The delayed versions of these two phases are generated by inverters working as delay-line. The complement versions of these phases are also generated by inverters, but these inverters are large and cause very short extra delay. The special two-input "inverter" guarantees that the delay happens only at falling edges.

4.11 Simulation Results

The configurable $\Sigma\triangle$ modulator has been designed in TSMC 0.18um CMOS technology, operating from 1.8V supply voltage using SPICE. The circuit-level implementation of the 2nd order $\Sigma\triangle$ modulator with feed forward signal path used in the first stage is shown in Figure 4.21.

Circuit simulation of a 2nd order modulator with a single-bit quantizer (GSM) of feed-forward topology was carried out after verifying the results of each block separately. The 1-bit D/A converters are implemented as switch networks that are controlled by the comparator outputs. The input signal had amplitude of 0.5 V (p-p) and a frequency of 100 KHz. The sampling frequency was set to be 64 MHz with an oversampling ratio of 160. The modulator design employs feedback reference voltages equal to the supply voltages since lowering the feedback levels

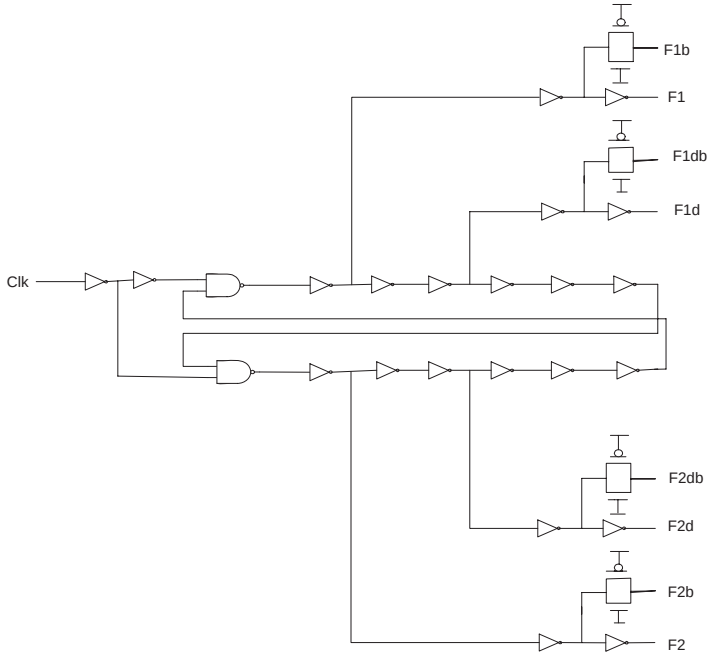

Figure 4.20: Two-phase clock generator schematic.

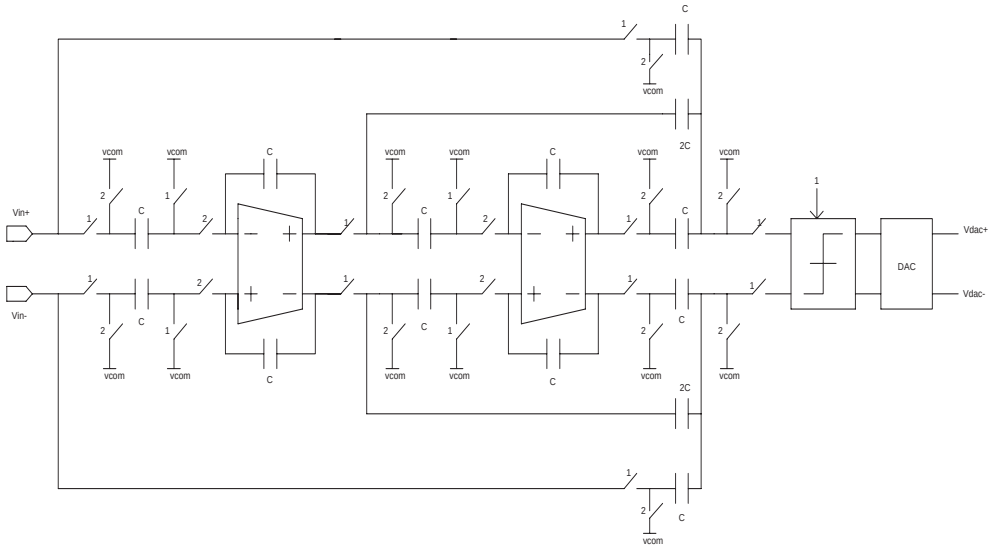

Figure 4.21: The first stage 2^{nd}-order feed-forward single-bit $\Sigma\triangle$ modulator

reduces the dynamic range of the converter. The reference voltages must be conditioned so that they do not introduce noise into the modulator. If the references

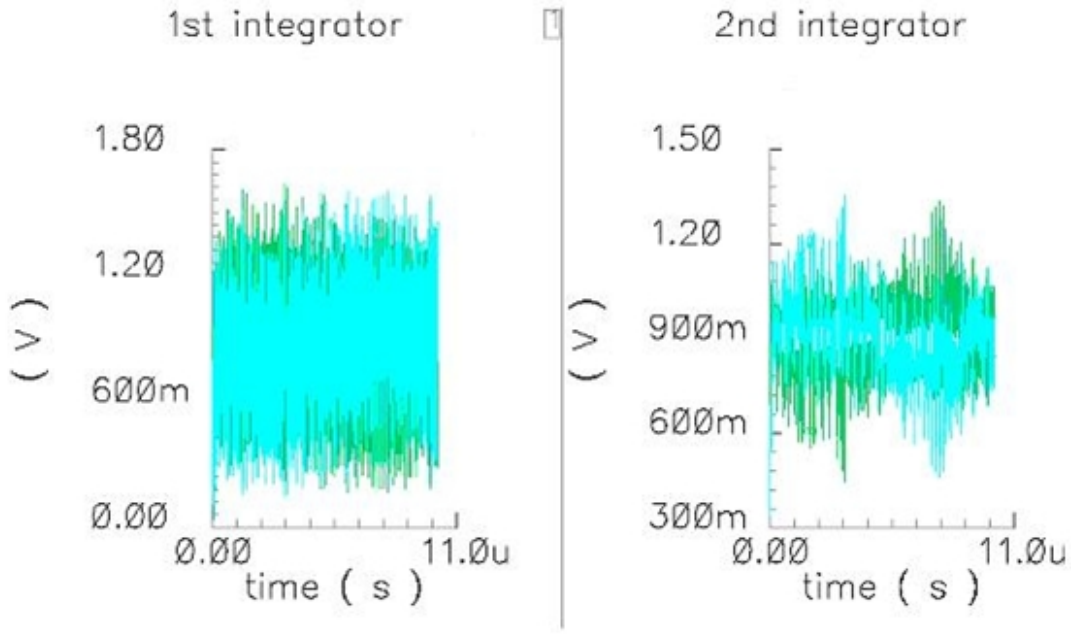

Figure 4.22: Time domain plots of 1^{st} and 2^{nd} integrator

are generated on chip, a supply-independent circuit that can provide a voltage close to Vdd should be used. Figure 4.22 shows the time domain plots of the first and second integrator carried out in SPICE using TSMC 0.18um CMOS process at 1.8V supply. Figure 4.23 shows the time domain response of a $\Sigma\triangle$ modulator output with a single-bit quantizer which gives a pulse-density modulated wave.

The integrator outputs are well within the linear range and the output swing of the second integrator is much smaller compared to the first one as expected from the matlab simulations. The performance of the modulator was evaluated after printing out the bit streams at the quantizer output to a file. Then it was transferred to a workstation and processed using Matlab^{TM}. Figure 4.24 shows the modulator output spectrum obtained by processing 16,384 consecutive output samples at 64 MHz clock rate for a sinusoidal input of amplitude 0.5 V (p-p) and frequency 100 kHz in the GSM mode. A good noise shaping with a signal-to-noise ratio of 82 dB can be observed in the figure maintaining a low noise floor in the base-band.

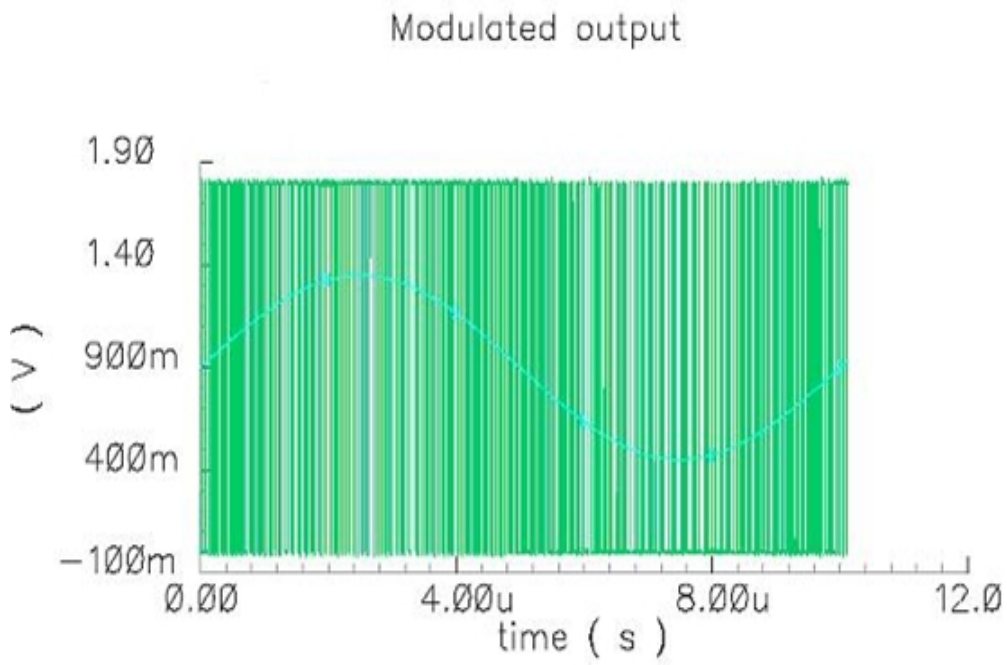

Figure 4.23: Modulator response with the modulator input and quantizer output

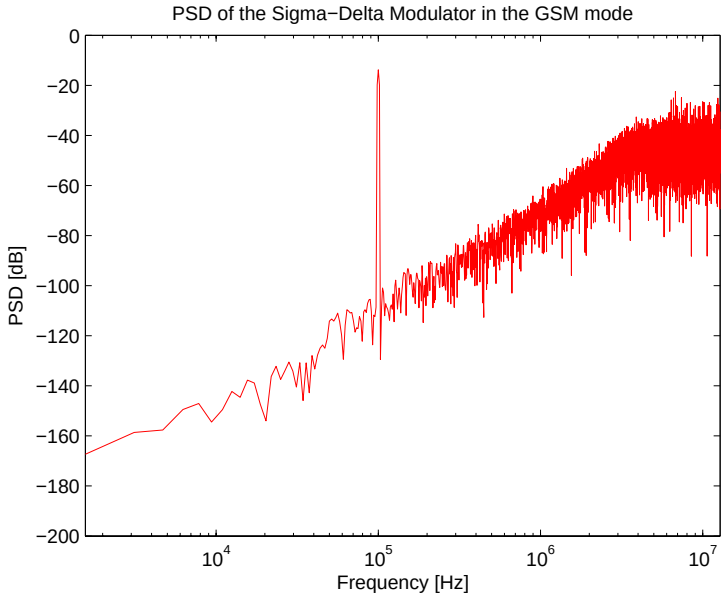

Figure 4.24: Output spectrum in GSM mode

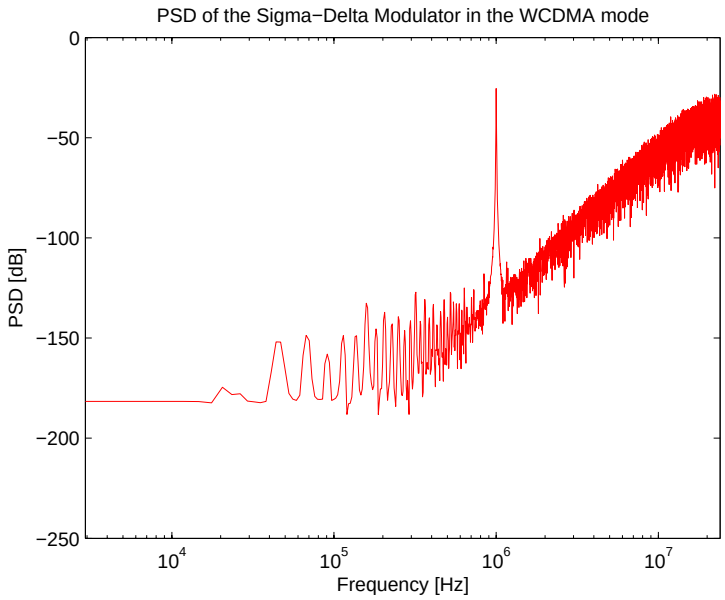

Figure 4.25: Output spectrum in WCDMA mode

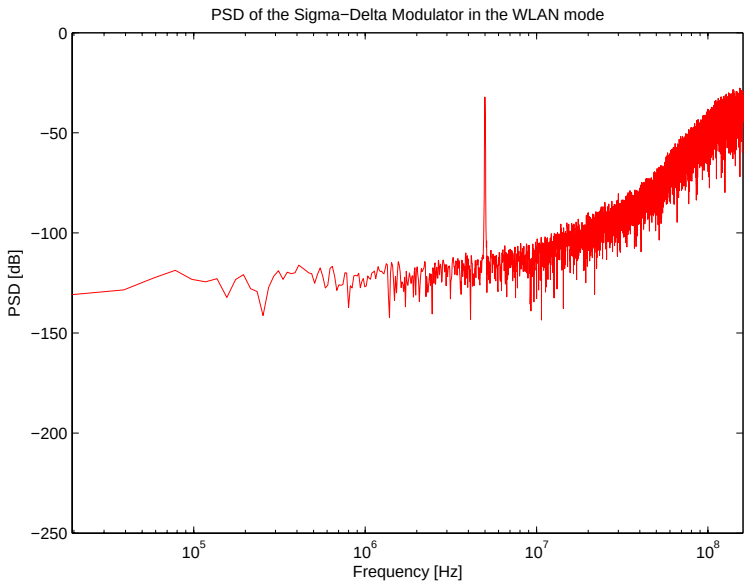

Figure 4.26: Output spectrum in WLAN mode

In order to implement the second and third stages for the WCDMA/WLAN mode, a 2-2 cascaded(fourth-order) and a 2-2-2 cascaded (sixth-order) modulator

with 2-bit and 4-bit quantizers has been simulated respectively . The 4-bit ADC employs a flash architecture with sampling network in front of the 16 comparators for the comparison of the fully differential input and the reference voltages. The output of the comparators are given to an AND gate which generates the thermometer code which is further converted into a binary code using an encoder. The 4-bit feedback DAC circuits are implemented using capacitors. The sampling capacitances are combined with sixteen small unit capacitances to realize the 4-bit DAC.

Figures 4.24, 4.25 and 4.26 shows the modulator output spectrum obtained from circuit-level simulation for GSM/WCDMA/WLAN modes for a 0.5V, 0.1/1/5 MHz input signal at a sampling frequency of 64/64/200 MHz respectively.The simulation results indicates that the proposed architecture dissipates 11mW / 20mW / 35mW at 1.8V supply and achieves a peak SNDR of 82/68/54 dB in GSM/ WCDMA/ WLAN modes respectively.

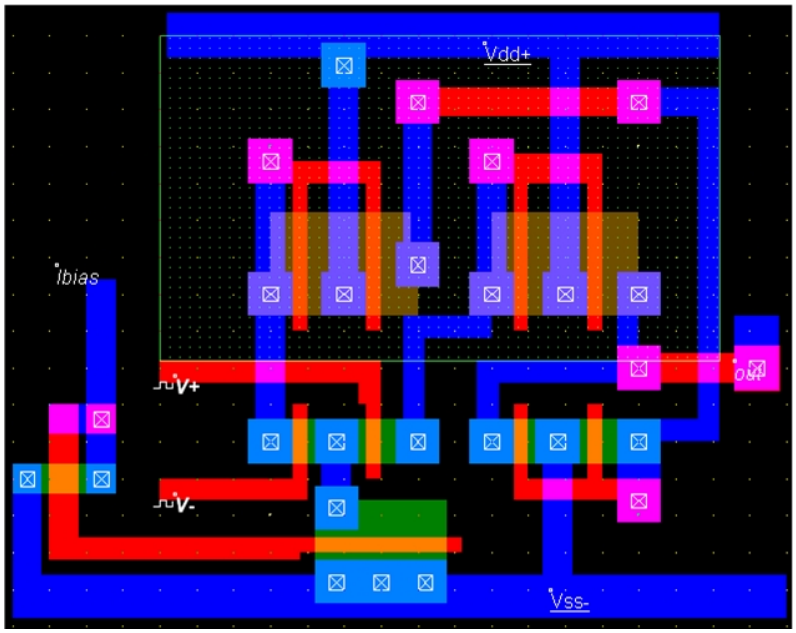

Figure 4.27: Opamp layout

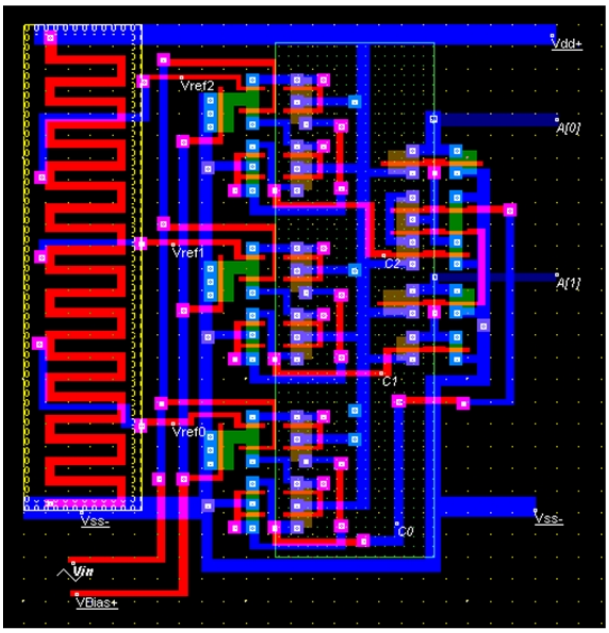

Figure 4.28: Two bit flash converter layout

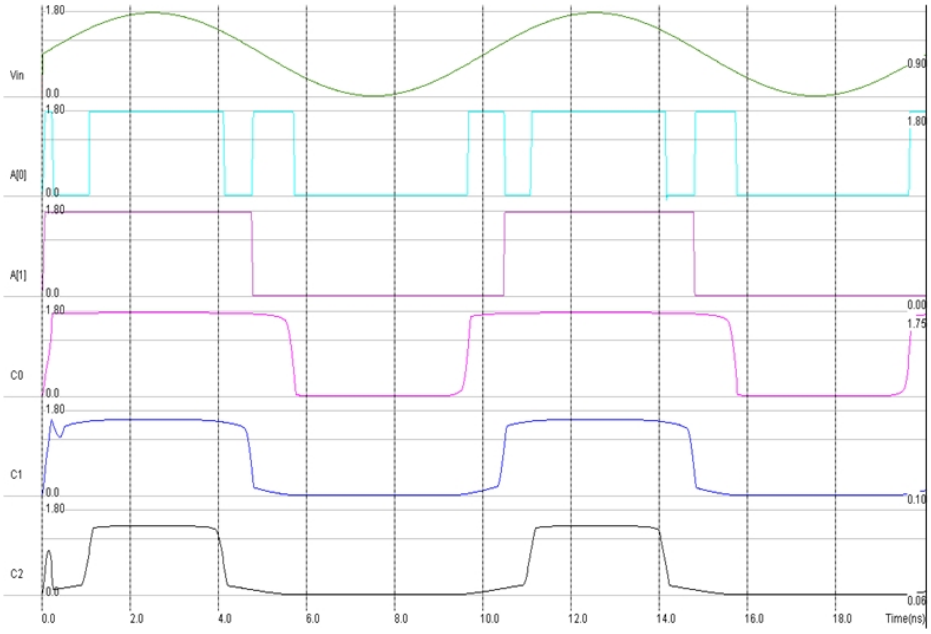

Figure 4.29: Two bit flash converter layout simulation output

Table 4.7: Performance comparison with other multi-standard ΣΔ ADCs

Parameters	Dual-mode sigma-delta ADC				Triple Mode			
	(11)	(29)	(53)	(20)	(95)	(103)	(33)	Proposed
Order	3	2	2	2/(2-1)	2-1-1	2-1-1-1	2-2	2-2-2
No. of bits	1	2.5	6	1/2.3	1/1/1	1/1.5/3	2.5/2.5	1-2-4
Fs (MHz)	104/184.32	26/46	23/46	39/38.4	138/245/320	51.2/100/100	23/46	64/64/200
BW (MHz)	0.2/3.84	0.2/2	0.2/1.92	0.1/1.92	0.271/3.84/20	0.2/5/20	0.2/1.5/1.92	0.2/2/20
DR (dB)	86/54	79/50	81/70	82/70	103/82/66	94/88/56	70/51/50	82/68/54
CMOS Process	0.25 um)	0.13um	0.18 um	0.13 um	0.35 um	0.18 um	0.18 um	0.18 um
Power (mW)	11.5/13.5	2.4/2.9	30/50	2.4/4.3	58/82/128	—	5.8/5/11	11/20/35

4.12 Layout Design

A number of layout strategies have to be adopted while doing analog and mixed signal layout. A digital layout is made by interconnecting simple blocks with less regard to individual transistors. In contrast, the layout of analog circuits mainly involves optimizing transistor layouts with much less concern for interconnections. Important design criteria influenced by the layout are accuracy and noise immunity.

When analog and digital circuitries are integrated onto the same chip, additional problems arise. The noise generated by the digital circuitry may couple into the analog circuitry and corrupt the overall analog circuit performance. Therefore, the control of the noisy interaction is vital in mixed circuits. This can be done by careful circuit design, for example, by achieving good PSRR.

Figures 4.27 and 4.28 shows the layout of OTA and flash ADC obtained using the tool called MICROWIND in 0.18um technology respectively. Simulation results indicate that the OTA layout occupies an area of 6.3um × 5.1um consuming 1mW of power under 1.8 V supply as illustrated in Figure 4.27. The simulation output of 2-bit flash converter is shown in Figure 4.29. Further, the 2-bit flash ADC dissipates 2.5 mW occupying an area of 13.8um ×15.6um.

4.13 Performance Comparison

Table 4.7 shows the already published multi-standard ΣΔ ADC in terms of both dual-mode and triple-mode architectures. The triple-mode ΣΔ which has been published in (95) uses 0.35um technology and consumes considerably large

amount of power. Though (33) uses 0.18um technology, it achieves less dynamic range compared to our performance.

4.14 Chapter Summary

This chapter describes the circuit level design of the basic building blocks in a $\Sigma\triangle$ modulator based on the results obtained from the Matlab^{TM} simulations. The design considerations involves selecting the key blocks like operational transconductance amplifiers (OTA), bias networks, common-mode feedback circuit, switches, capacitors, comparators and two-phase clock generation circuitry. The modulator has been designed and simulated in a TSMC 0.18um CMOS process at 1.8V supply voltage. Circuit simulation of a second-order $\Sigma\triangle$ modulator for GSM with feedforward topology was carried out after verifying the results of each block separately. Later it was extended to simulate a fourth-order and sixth-order modulator for WCDMA and WLAN respectively.

Chapter 5

Sigma-delta Modulator Design Tool

5.1 Motivation

A multi-standard design often involves extensive system level analysis and architectural partitioning, typically requiring extensive calculations. To expedite the handling of complicated design calculations, a Graphical User Interface (GUI) based design tool is described in this chapter. In particular, multi-standard sigma-delta modulator design for three wireless communication standards consisting of GSM, WCDMA and WLAN is focussed. A 2-2-2 reconfigurable sigma-delta modulator is proposed which can meet the design specifications of the three standards. A low-distortion swing suppression sigma-delta modulator (SDM) has been chosen which is less sensitive to circuit imperfections, especially at very low oversampling ratios. Further, the toolbox incorporates all the significant non-idealities which affect the performance of a sigma-delta modulator. The sigma-delta modulator design tool is developed using the Graphical User Interface Development Environment (GUIDE) in Matlab^{TM}.

5.2 Introduction

The rapid evolution of digital integrated circuit technologies and an ever expanding growth of wireless communications have motivated the development of highly integrated multi-standard receivers. New architectures and circuit techniques need to be explored in the design of fully integrated, multi-standard RF transceivers (3), (39). Thus reconfigurability is a major focus of recent RF transceiver IC designs which has been used to increase both the integration and adaptability to multiple RF communication standards. The main challenge here is to design low-power, high dynamic range, compact multi-mode (89) analog to digital converters which can meet the resolution and bandwidth requirements of different communication standards. Our choice is a sigma-delta ADC because of its great features for adaptability and programmability.

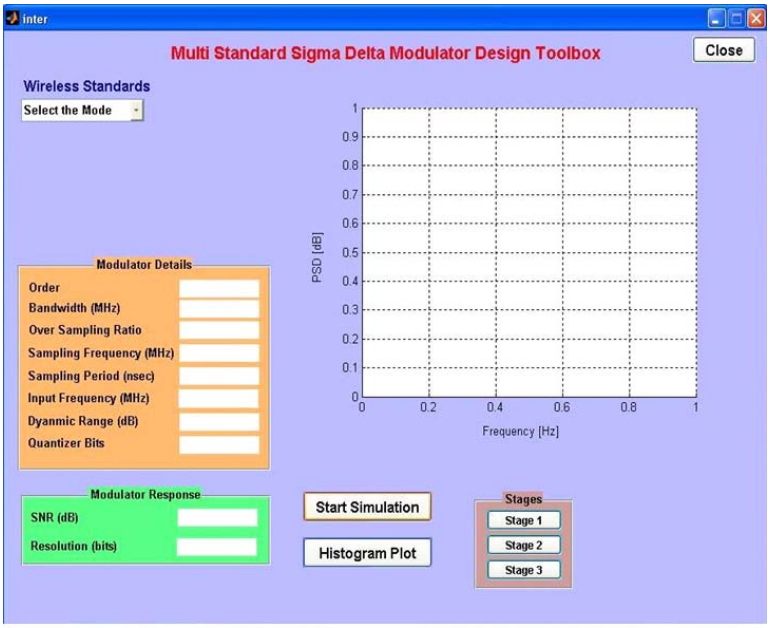

Figure 5.1: GUI for Multi-standard Sigma-Delta Modulator Design Toolbox

5.3 Sigma-delta Modulator Design Toolbox

The toolbox is developed using Matlab^{TM} Simulink models and the front-end GUI is developed using GUIDE. With this toolbox, the user can select the required wireless communication standard and obtain the corresponding multistage sigma-delta implementation. The toolbox will help the user or designer to develop the sigma-delta modulator for multiple standards without requiring a complete understanding of the underlying methods. Thus it provides a powerful tool for the design engineer to perform a quick design and analysis.

The front panel of the GUI is shown in Figure 5.1. Initially, the desired standard is selected from the pop-up menu as in Figure 5.2a and the modulator is designed by pressing the push button named *Start Simulation*. The modulator details such as the order, bandwidth for a selected standard, oversampling ratio, sampling frequency and its corresponding sampling period, input signal frequency, required dynamic range and the number of quantizer bits are displayed on the GUI as in Figure 5.4. The modulator response, signal-to-noise ratio (SNR) in dB and the number of resolution in bits are displayed using the message box shown in Figure 5.2b. *Stages* is a button group that holds a group of three buttons tagged as *Stage* 1, *Stage* 2, and *Stage* 3 shown in Figure 5.2c. The desired response, of the individual stages, cascaded responses after each stage or the multistage overall response, can be displayed in the *Axes* window by pressing each stage button. The push button named *Histogram Plot* is used to display the histogram of the integrator outputs as shown in Figure 5.3. The power spectral density (PSD) plot for the selected standard WLAN is displayed in Figure 5.4 using the *Axes* in the GUI. The *Close* is a push button which closes the GUI window, once it is pressed.

The simulations were performed by incorporating most of the significant sigma-delta non-idealities in the toolbox. The main non-idealities considered here are finite and non-linear dc gain, slew rate and gain-bandwidth limitations, amplifier saturation voltage, capacitor mismatch, opamp input referred noise, kT/C noise, clock jitter and DAC capacitor mismatch.

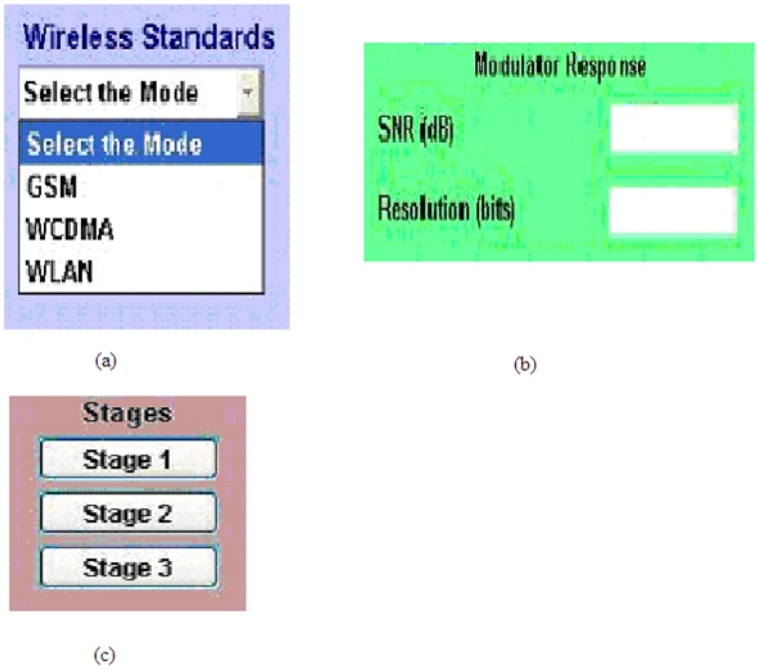

Figure 5.2: GUI:(a) Pop-up menu for standard selection; (b) Message box displaying the modulator response (c) Button group for stage selection

5.4 Sigma-delta Non-idealities

In the design of sigma-delta ADCs, we need to optimize a large set of parameters including the overall structures and the performance of the building blocks to achieve the required signal-to-noise ratio. Therefore, behavioral simulations were carried out using a set of Simulink^{TM} models (57), (80), (19), (83) in Matlab Simulink^{TM} environment in order to verify the performance of both WCDMA/GSM system, to investigate the circuit non-idealities effect, to optimize the system parameters and to establish the specifications for the analog cells. The most important building block of a sigma-delta ADCs is the switched-capacitor (SC) integrator which has been explained in Figure 4.2 (Chapter 4). The non-idealities can be grouped into three categories considering switched-capacitor implementation:

- Integrator-related

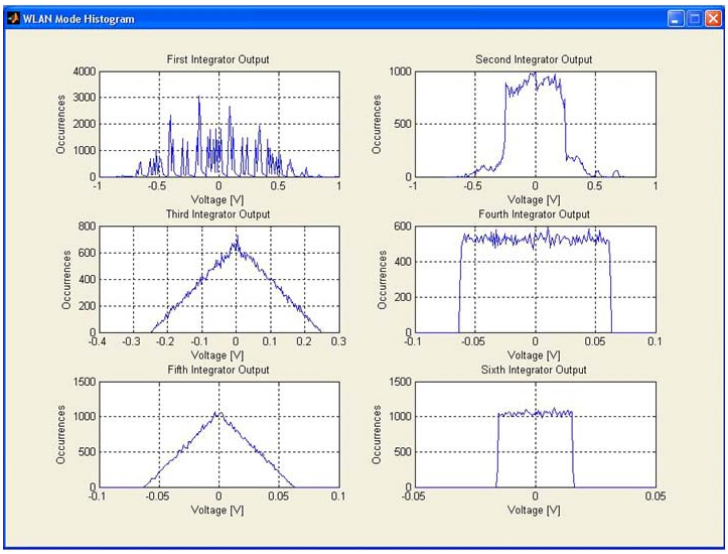

Figure 5.3: Histogram plot of the integrator outputs

- Circuit related non-idealities
- Feedback DAC-related

5.4.1 Clock Jitter

Switched capacitor sigma-delta modulator is a sampled-data system, where the variations of the clock period have no direct effect on the circuit performance, once the signal has been sampled. Thus it is independent of the structure or order of the modulator. Sampling clock jitter results in non-uniform sampling and increases the total error power in the quantizer output. The magnitude of this error is a function of both the statistical properties of the jitter and the input signal to the converter. The error introduced when a sinusoidal signal with amplitude A and frequency f_{in} is sampled at an instant which is in error by an amount δ is given by equation 5.1.

$$x(t+\delta) - x(t) \approx 2\pi f_{in}\delta A\cos(2\pi f_{in}t) = \delta\frac{d}{dt}x(t) \tag{5.1}$$

This effect can be simulated with Simulink^{TM} by using the model (80) shown in Figure 5.5, which implements equation 5.1. Here we assumed that the sam-

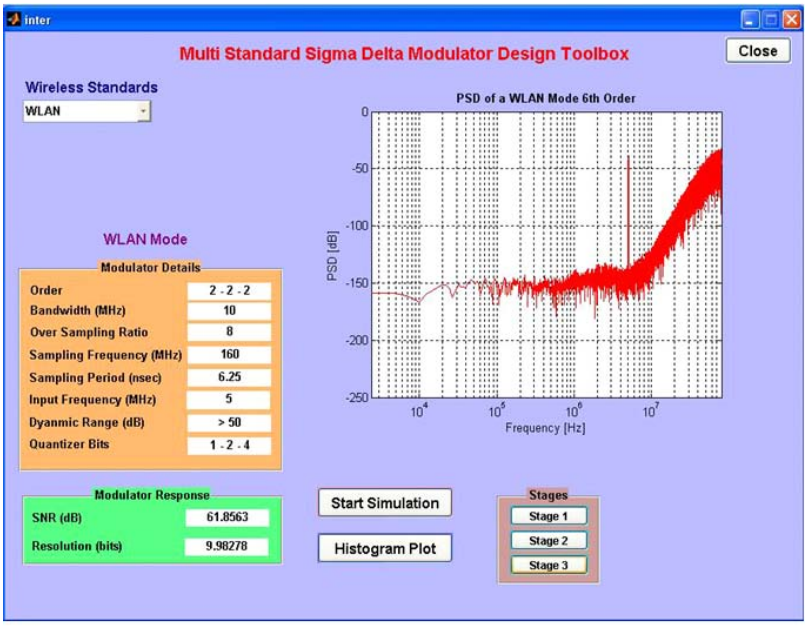

Figure 5.4: Display of the PSD plot of the selected standard WLAN

pling uncertainity δ is a Gaussian random process with standard deviation $\Delta\tau$. Whether oversampling is helpful in reducing the jitter depends on the nature of the jitter. Since we assume the jitter white, the resultant error has uniform power spectral density from 0 to $f_s/2$, with a total power of $(2\pi f_{in}\Delta\tau A)^2/2$.

5.4.2 Integrator Noise

The most important noise sources affecting the operation of an SC sigma-delta modulator are the thermal noise associated to the sampling switches and the intrinsic noise of the operational amplifier (71), (16). The total noise power of the circuit is the sum of the theoretical loop quantization noise power, the switch noise power and the opamp noise power. Because of the large low frequency gain of the first integrator, the noise performance of a sigma-delta modulator is determined mainly by the switch and opamp noise of the input stage.

These effects can be simulated with Simulink^{TM} using the model (80) of a noisy integrator shown in Figure 5.6, where the coefficient b represents the integrator gain which is equal to C_s/C_f (sampling capacitance/integration capaci-

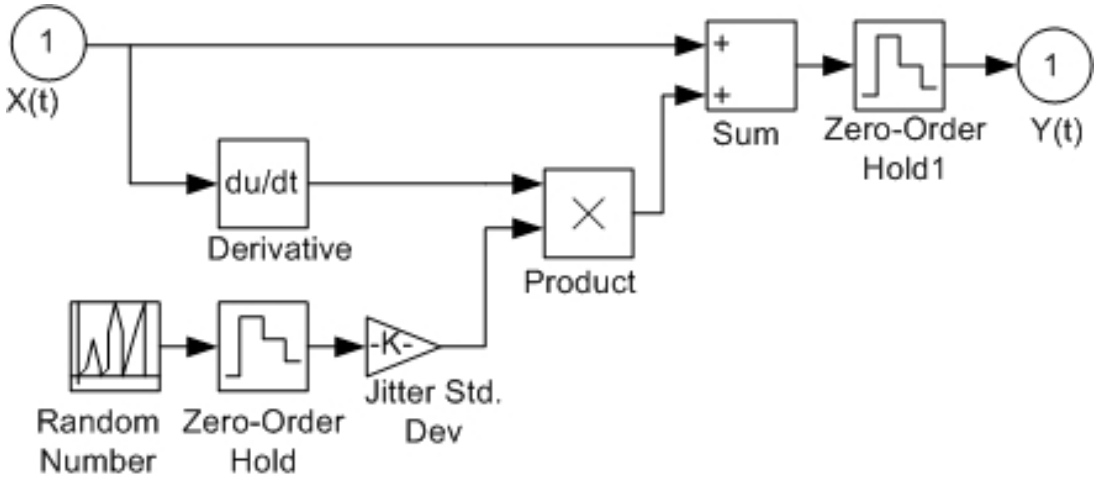

Figure 5.5: Modeling a random sampling jitter

tance).

5.4.3 Switches Thermal Noise

Thermal noise is caused by the random fluctuations of carriers due to thermal energy and is present even at equilibrium. Thermal noise has a white spectrum and wide band limited only by the time constant of the switched capacitors or the bandwidths of opamps. Therefore, it must be taken into account for both the switches and the opamps in an SC circuit. In a SC first-order sigma-delta modulator, the sampling capacitor C_s is in series with a switch, with a finite resistance R_{on}, that periodically opens, thus sampling a noise voltage onto C_s. The total noise power can be found evaluating the integral in equation 5.2,

$$e_T^2 = \int_0^\infty \frac{4kTR_{on}}{1+(2\pi f R_{on}C_s)^2}df = \frac{kT}{C_s} \tag{5.2}$$

where k is the Boltzmann's constant, T the absolute temperature, and $4kTR_{on}$ the noise PSD associated with the switch on-resistance. The switch thermal noise voltage e_T (usually called kT/C noise) is superimposed to the input voltage x(t) leading to

$$y(t) = [x(t) + e_T(t)]b = \left[x(t) + \frac{\sqrt{kT}}{\sqrt{C_s}}n(t)\right]b = \left[x(t) + \frac{\sqrt{kT}}{\sqrt{bC_f}}n(t)\right]b \tag{5.3}$$

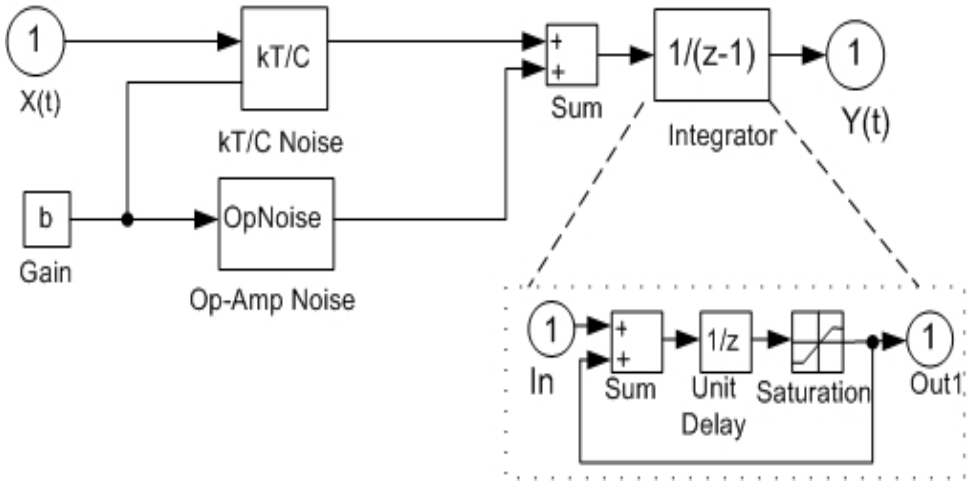

Figure 5.6: Model of a 'noisy' integrator

where n(t) denotes a Gaussian random process with unity standard deviation, while b is the integrator gain. Equation 5.3 is implemented by the model shown in Figure 5.7.

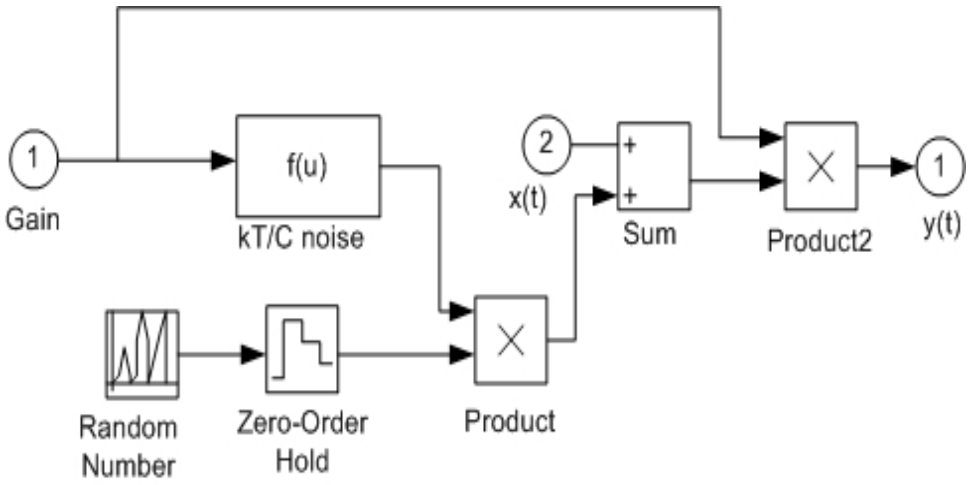

Figure 5.7: Modeling switches thermal noise (kT/C) block

Since the noise is aliased in the band from 0 to $f_s/2$, its final spectrum is white with a spectral density

$$S(f) = 2kT/f_s C_s \tag{5.4}$$

Typically the first integrator will have two switched input capacitors, one carrying the signal and the other providing the feedback from the modulator output, each of them contributing to the total noise power.

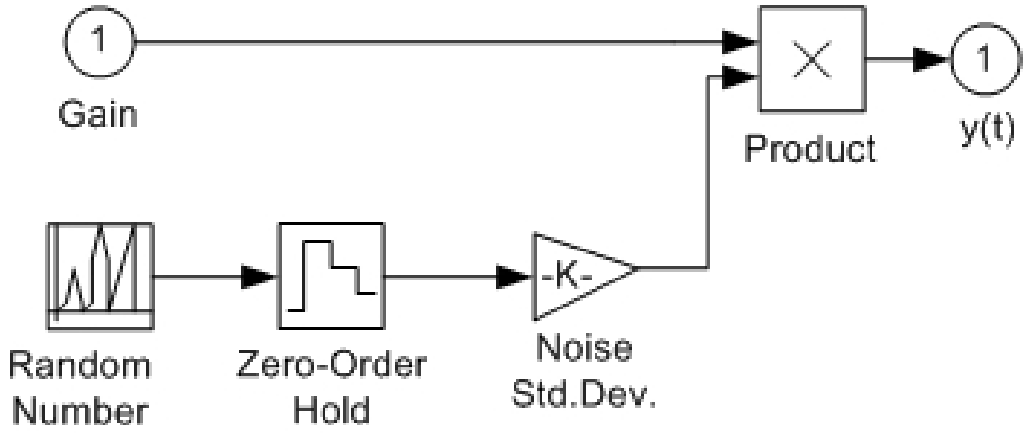

Figure 5.8: Opamp noise model

5.4.4 Opamp Noise

Figure 5.8 shows the model used to simulate the effect of the opamp noise. Here V_n represents the total rms noise voltage referred to the opamp input. Flicker (1/f) noise, wide-band thermal noise and dc offset contribute to this value. The total opamp noise power V_n^2 can be evaluated, through circuit simulation, by adding the noise contributions of all the devices referred to the opamp input and integrating the resulting value over the whole frequency spectrum.

5.5 Integrator Non-Idealities

The most important part of sigma-delta modulator is the integrator and its non-idealities. The two integrators in the forward path of a second order sigma-delta modulator serve to accumulate the large quantization errors that result from the use of a two-level quantizer and force their average to zero. The constant g_1 represents the gain preceding the input to the first integrator in the triple-mode

architecture, whose value is 0.5 for each of the integrators. The transfer function for an ideal integrator:

$$H(z) = g_1 \frac{z^{-1}}{1 - z^{-1}} \tag{5.5}$$

Analog circuit implementations of the integrators deviate from this ideal in several ways. Errors which result from the gain variations and those due to operational-amplifier non-idealities, are considered in the following sections.

5.5.1 Gain Variations

The scalar preceding the second integrator has no effect on the performance of sigma-delta modulator because it is absorbed by the two-level quantizer. However, the deviations in g_1 from its nominal value in the first integrator alter the noise shaping function of the sigma-delta modulator and consequently change the performance of the A/D converter.

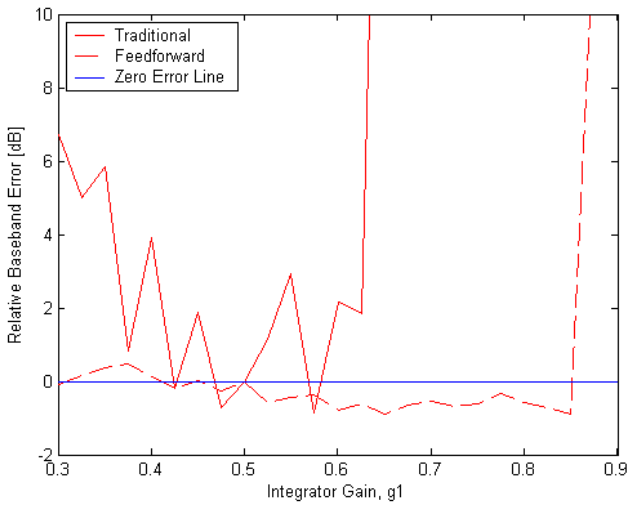

Figure 5.9: Simulated influence of variations in integrator gain on base band quantization noise

Figure 5.9 shows the change of the in-band quantization noise as a function of g_1 for an input signal level of -40 dB. The thick line shows the variations

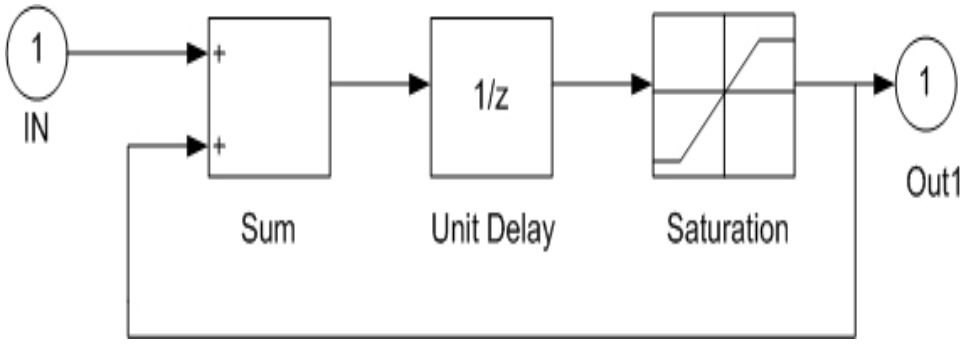

Figure 5.10: Ideal integrator

for a traditional sigma-delta modulator, whereas the dotted line stands for feed forward topology. Gain variations of as much as 20% from the nominal value (0.5) has minor impact on the performance of the traditional one, whereas the feed forward has almost no impact on the variations of g_1 showing the insensitivity of the feed forward topology to component variations as the integrators process only the quantization noise. However, gains larger than 0.6 for traditional, causes the signal amplitudes at the integrator outputs to increase rapidly and the system becomes unstable at an early stage, whereas for feed forward this comes into effect only after 0.8.

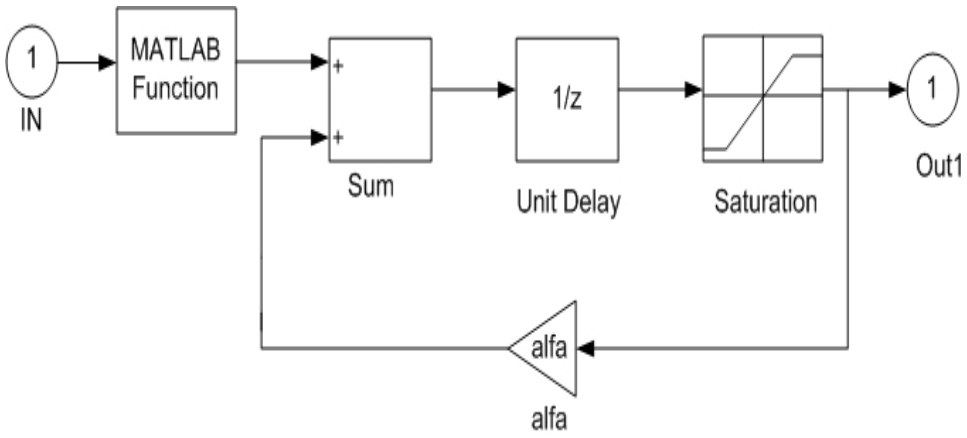

Figure 5.11: Real integrator

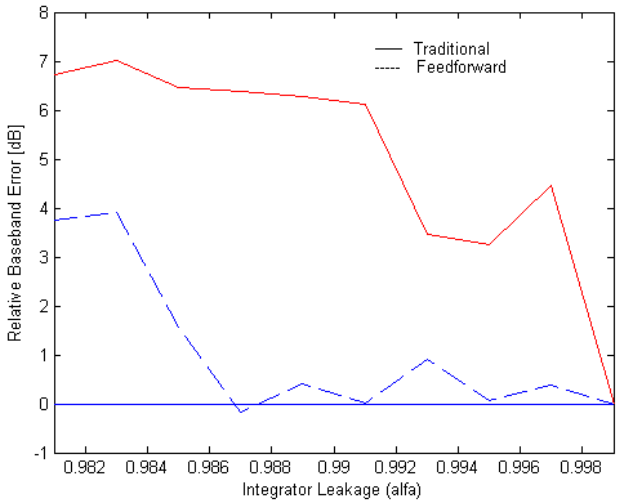

Figure 5.12: Influence of integrator leak on baseband quantization noise

5.6 Operational-Amplifier Non-Idealities

The behavioural model of an ideal integrator is given in Figure 5.10. One of the major causes of performance degradation in SC sigma-delta modulators is the incomplete transfer of charge in the SC integrators. This non-ideal effect is a consequence of the operational amplifier non-idealities, namely finite gain and bandwidth (BW), slew rate (SR) and saturation voltages. These will be considered separately in the following sections. Figure 5.11 shows the model of the real integrator including all the non-idealities.

5.6.1 Leak

The ideal transfer function of the integrator assumes that its gain is infinite, a characteristic impossible to obtain in practice. However, the actual gain is limited by circuit constraints and in particular by the operational amplifier open-loop gain A_0. The result is lossy integration or known as integrator leakage because only a part of the integrator output $'\alpha'$ of the previous period is added to the new input sample. The limited dc gain of the integrator increases the in-band noise. The

transfer function of the integrator with leakage is shown in equation 5.6

$$H(z) = \frac{z^{-1}}{1 - \alpha z^{-1}} \tag{5.6}$$

The dc gain of the integrator H_0, can be represented as in equation 5.7.

$$H_0 \;=\; H(1) = \frac{1}{(1-\alpha)} \tag{5.7}$$

The limited gain at low frequencies increases the in-band noise. Figure 5.12 shows the simulated influence of integrator leak for both traditional and feed forward topologies. The thick line depicts the variations in base band error for traditional, and the dotted line shows the changes for feed forward topology as the integrator leakage $'\alpha'$ is sweeped from a value of 0.98 to 0.999 (which is almost ideal). Simulation results shows a relative base-band error of 6.8 dB for traditional and 3.8 dB for feed forward which clearly reflects the less insensitivity of feed forward topology to circuit constraints like $'\alpha'$ when compared to the traditional one.

5.6.2 Finite and Non-linear dc Gain

The open-loop dc gain of the amplifier is not only finite but can be nonlinear also. Such non-linearities occur, when the integrator implementation is based on an amplifier with input-dependent gain. The consequence of these non-linearities is harmonic distortion that limits the peak SNR achievable at large signal levels. Figure 5.13 shows the open-loop dc gain as a function of the output voltage.

The non-linear open loop gain of the amplifiers introduces error components as harmonic distortion in the modulator output spectrum. The non-linearity of the gain is manifested by its dependency on the amplifier output. In reality, all the amplifiers experience a non-linear gain because the transition between the linear and saturation output region is gradual. The dependency of the open-loop gain of the amplifier in the first integrator on the output voltage can be approximated by the polynomial as shown in equation 5.8, where the second-order non-linear coefficient is negative and of a module quite large than that of the first order.

$$A_v = A_0(1 + a_1 v + a_2 v^2 + \cdots) \tag{5.8}$$

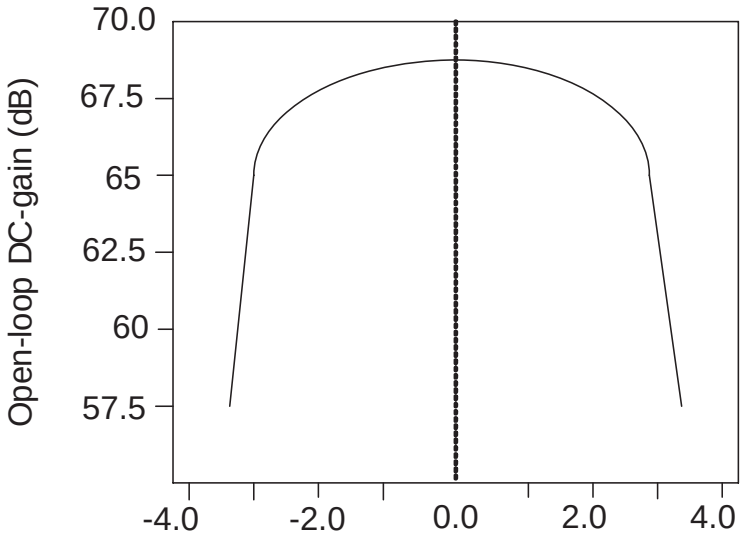

Figure 5.13: Open-loop dc gain as a function of the output voltage

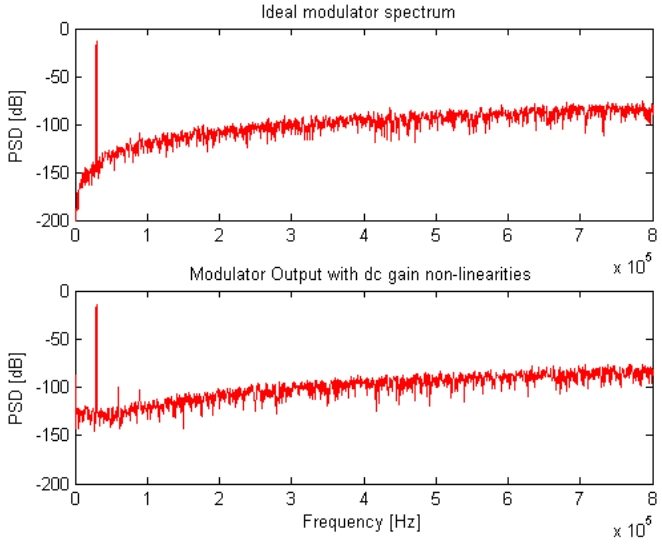

Figure 5.14: Simulated influence of dc gain non-linearities on the output spectrum

Figure 5.14 shows the harmonic distortion generated when due to dc gain non-linearities with first-order coefficient of 0.1% and second-order coefficient of 1% for a dc gain of 1000, when the ideal blocks are replaced with real integrator blocks.

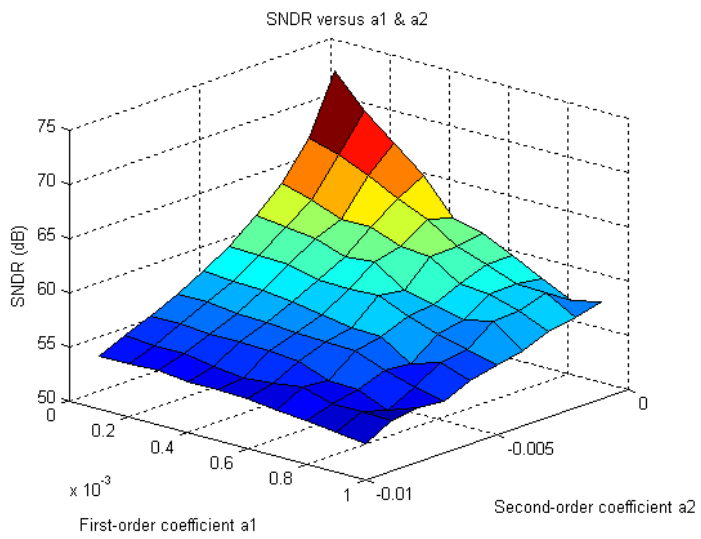

Figure 5.15: Simulated coefficient variation : Traditional modulator

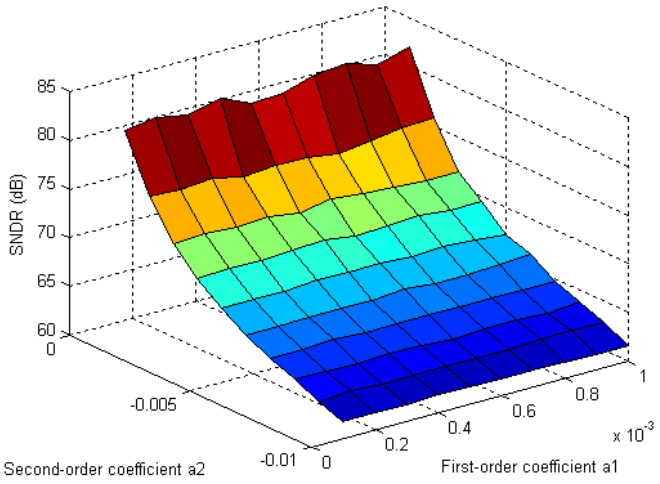

Figure 5.16: Simulated coefficient variation : Feed forward topology

Figure 5.15-5.16 shows the 3-D simulation result of coefficient mismatch, where the first-order coefficient (a_1) changes from 0.01% to 0.1% and second-order coefficient (a_2) changes from 0.1% to 1%, keeping the DC gain at 1000. The achieved SNDR for traditional is 74 dB, whereas 81 dB for the feed forward

topology. Another observation which can be made from the two plots is that feed forward topology is less sensitive to variations in first-order and second-order non-linearities, which is not the case for traditional.

5.6.3 BW and SR

The finite BW and the SR of the operational amplifier are modelled as in Figure 5.11 with a building block placed in front of the integrator which implements a Matlab function (80). Slew rate and BW are related to each other. SR and BW limitation can lead to a non-ideal transient response within each clock cycle, thus producing an incomplete or inaccurate charge transfer to the output at the end of the integration period.

In typical sampled-data analog filter, the unity gain bandwidth of the operational amplifier should often be at least an order of magnitude greater than the sampling rate. In other words, the time constant of the integrator which is given by $1/2\pi GBW$ should be kept smaller than the sampling period T_s for the modulator to be stable. But it is found that this constraint for the settling of the integrator output is acceptable, provided that the settling process is linear. That is, the settling must not be slew-rate limited. The SR and BW limitations produce harmonic distortion reducing the total SNDR of the sigma-delta modulators.

Matlab simulations were carried out to determine the requirements of OTA to meet both the WCDMA/WLAN specifications which are more stringent. Figures 5.17, 5.18 and 5.19 shows the peak SNR for various values of OTA DC gain, bandwidth and slew rate. Based on these results, OTA needs to have more than 60 dB DC gain, at least 350 MHz closed loop bandwidth and more than 300 V/us slew rate. The SNRs are then checked with OTA gain of 1000, bandwidth of 350 MHz and slew rate of 300 V/us in the WLAN mode.

5.6.4 Saturation

The saturation levels of the operational amplifier used is an important factor in limiting the dynamic range of signals in a sigma-delta modulator. This can be

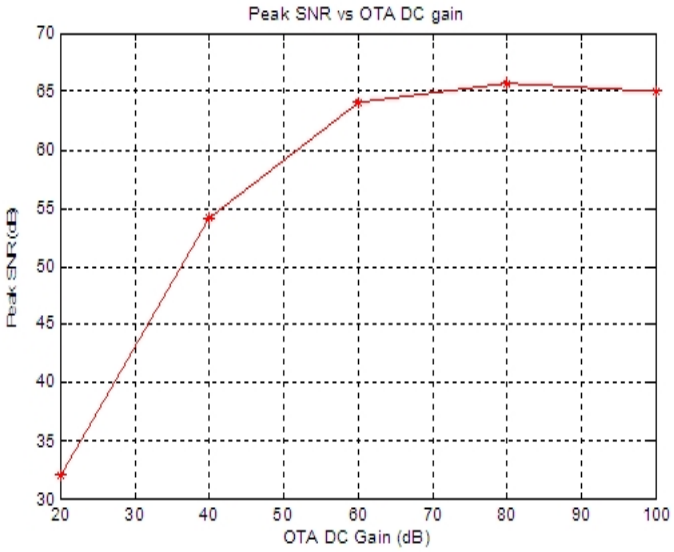

Figure 5.17: Peak SNR vs. OTA dc gain

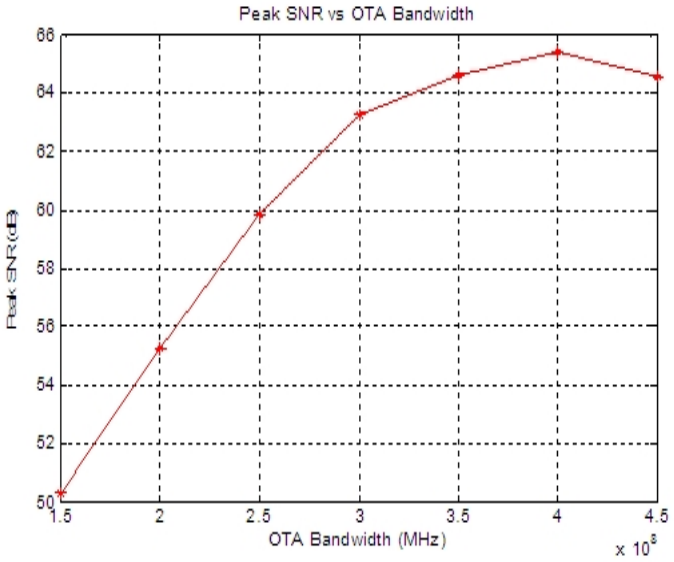

Figure 5.18: Peak SNR vs. OTA bandwidth

done using the Simulink^{TM} model of the saturation block inside the feedback loop of the integrator as shown in Figure 5.10.

The effect of the operational amplifier saturation voltage (Amax) on the performance of the sigma-delta modulator is illustrated in Figure 5.20, by plotting

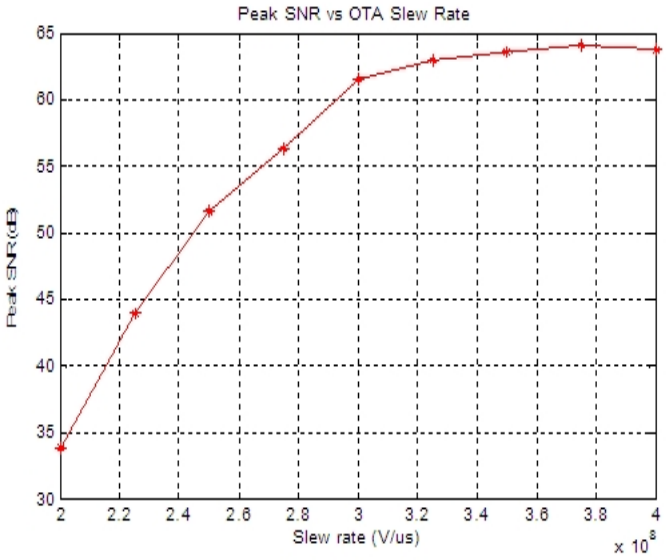

Figure 5.19: Peak SNR vs. OTA slew rate

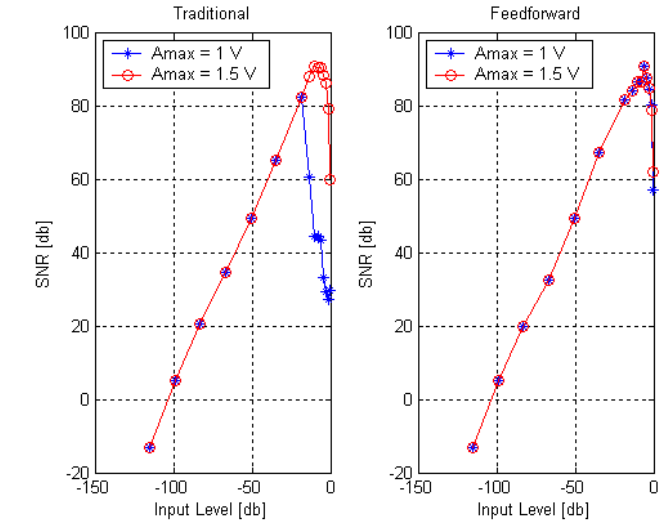

Figure 5.20: SNR as a function of the input signal amplitude for different values of the operational amplifier saturation voltage (Amax)

the simulated SNR as a function of the input signal amplitude for different values of Amax. For the traditional one, a saturation voltage of Amax = 1.5 V with a reference voltage of 1 V, does not degrade the performance significantly upto

a signal amplitude of -6dB, whereas a significant degradation occurs for a signal amplitude of -16 dB when the saturation voltage Amax = 1 V due to the saturation of the operational amplifiers and not able to track the input signal. For feed forward, this almost have no impact on the performance as the integrators process only the quantization noise and the signal range is comparatively small.

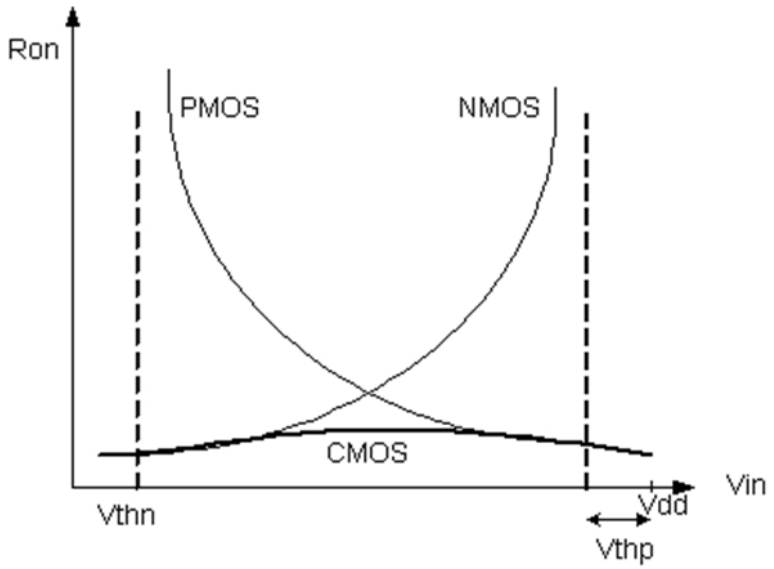

Figure 5.21: Switch on-resistance as a function of the input voltage.

5.7 Circuit-related Non-idealities

5.7.1 Switch Non-linearity

Linearity is an important factor in the design of switches (67). It is desirable to operate in a region where the on resistance of the switch is independent of the input voltage. Therefore, the switches used in the integrator are implemented with complementary MOS devices. In CMOS switches, the sizing of the NMOS and PMOS devices is critical. The parallel combination of the NMOS and PMOS

devices yields an effective resistance given by equation 5.9.

$$R_{ON\_CMOS} = \left[\mu_N C_{ox}\left(\frac{W}{L}\right)_N (V_{GSN} - V_{THN}) + \mu_P C_{ox}\left(\frac{W}{L}\right)_P (V_{GSP} - |V_{THP}|)\right]^{-1} \tag{5.9}$$

Figure 5.21 shows the switch on-resistance as a function of input voltage. The input signal amplitude, switch size and harmonic distortion statistics are compiled to minimize the distortion introduced by the switches. Figure 5.22 shows the statistical result of the signal to distortion ratio (SDR) vs. switch size with various input signal amplitudes. SDR can be increased either by increasing the switch size or by reducing the input signal amplitude. Although increasing the switch can reduce the harmonic distortion, it causes the parasitic capacitance to increase and thus the clock feed-through noise is increased. There is a trade off between the switch size and the distortions. It is found that the optimum value of the switch size can be chosen as 30 um without much degradation in SDR.

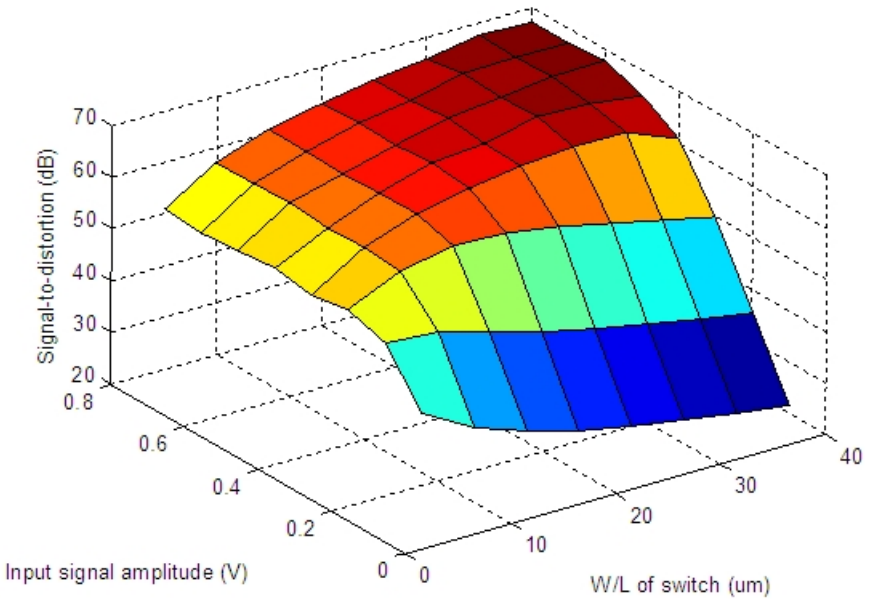

Figure 5.22: Distortion of the sampling phase of an integrator

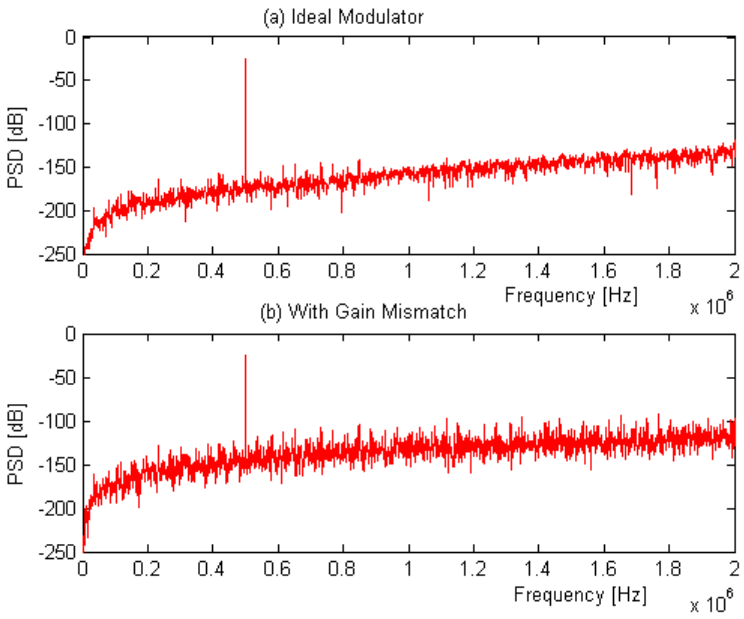

Figure 5.23: Output spectrum of the modulator with and without mismatch

5.7.2 Gain Mismatch

In cascaded modulators, the successive stages serve to randomise the quantization error. If the cancellation of quantization error is complete, then the coloration in the output of the first stage is eliminated. The quantization error of the final stage approaches white noise. Unfortunately, owing to gain mismatch, quantization error from the first stage leaks into the output of the cascade. A major limitation of cascaded modulators is the leakage of spectral tones from the 1^{st} stage into the output as a result of gain mismatch. For example, with a cumulative matching error of 5%, the following spectrum is obtained for a sinusoidal input of -6 dB as in Figure 5.23.

Matching between analog (g_1,g_2) and digital (g_5) gains is an important factor which can result in the quantization error from the first stage not fully cancelled. Figures 5.24 and 5.25 depicts the sensitivity of matching between analog and digital gains on the performance of the modulator. The 3-D plot shows the influence in signal-to-noise ratio as the percentage of mismatch between the analog (g_1,g_2) and digital (g_5) coefficients when they are varied from 0 to 10%. It is

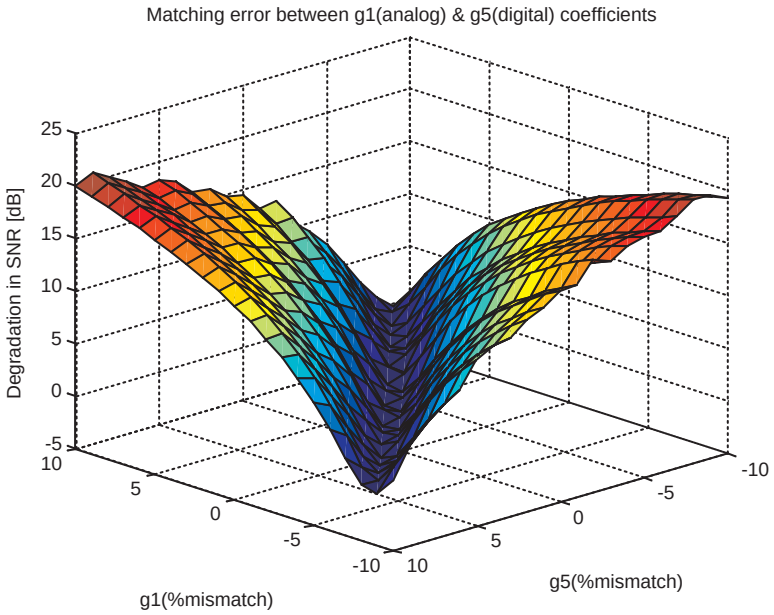

Figure 5.24: Degradation in SNR versus g_1 and g_5

observed that there is a degradation of almost 20 dB in the peak signal-to-noise ratio totally.

5.8 DAC Non-linearity

The modulators with more than two internal quantization levels, also called multi-bit modulators, are to a large extent insensitive to the quantizer non-idealities. However, the D/A conversion of the signals in the feedback loop, when two or more bits are handled, can be affected by non-linearity error. The D/A conversion error are directly added to the modulator input and it appears at the output, generally, as distortion. Since such errors are not attenuated, the linearity of the sigma-delta converter is affected by that internal DAC which degrades its performance.

The errors of DAC can be divided into three types: offset, gain error and non-linearity. The first two do not cause severe problem to real performance, while the non-linearity degrades the performance severely. It is represented by its

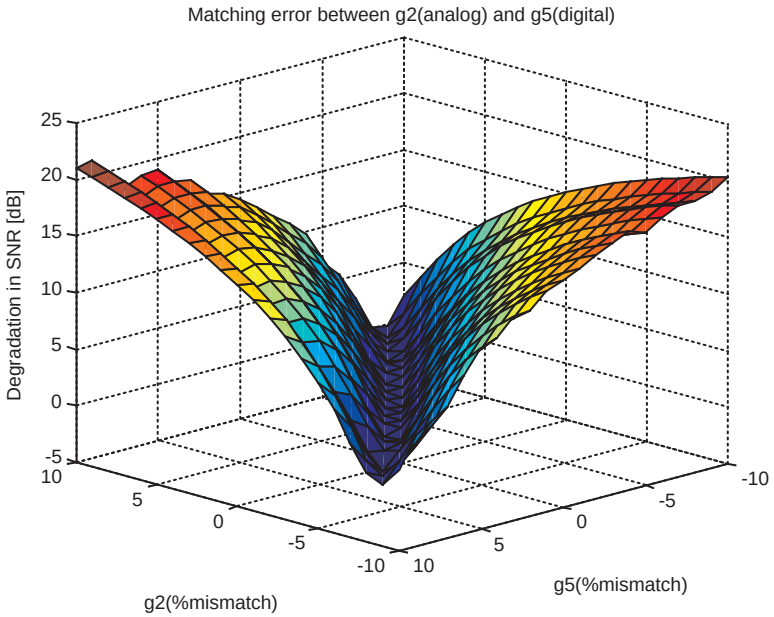

Figure 5.25: Degradation in SNR versus g_2 and g_5

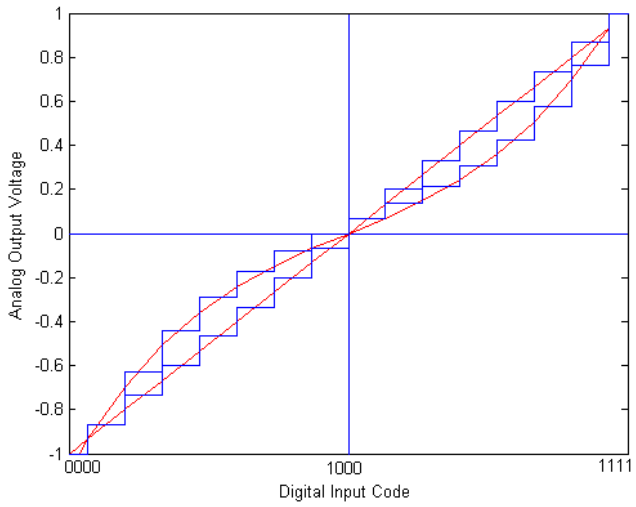

Figure 5.26: Nonlinear D/A model

integral non-linearity (INL) which is defined as the maximum difference between the actual output analog value and its ideal value, once the offset and gain errors

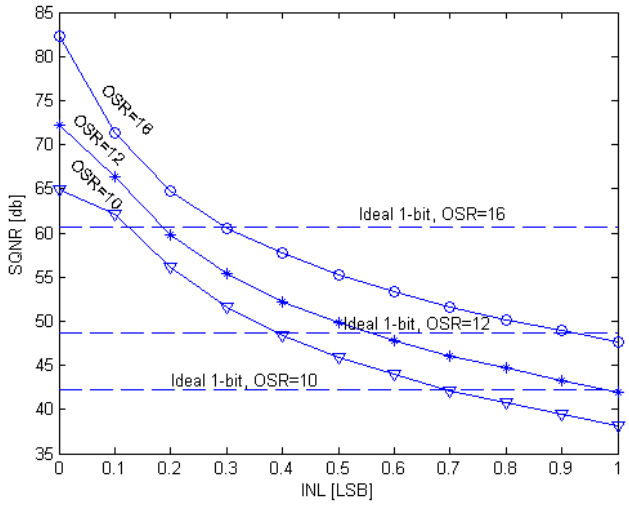

Figure 5.27: SQNR vs. INL for a 4th-order cascaded sigma-delta modulator using 1-bit D/A in the first stage and 4-bit D/A in the second stage.

have been corrected.

The nonlinear equation relating the quantizer input and output can be written in the form:

$$Y(t) \;=\; x(t) + a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) + \cdots \tag{5.10}$$

Figure 5.26 shows the non-linear D/A model which represents a transfer function where the maximum INL is at the maximum and minimum input values. In the following analysis, the impact of non-linearity to SQNR of the D/A converter is quantified as INL, which is the maximum deviation from the ideal 1-bit structures. When the SQNR with non-linear multi-bit structure is worse than the SQNR of the 1-bit case, then it is obvious that extra circuit complexity and power consumption associated with the multi-bit structure cannot be motivated.

The plot of SQNR vs. INL for a 4th-order cascaded sigma-delta modulator using 1-bit D/A in the first stage and 4-bit D/A block in the second stage is shown in Figure 5.27. The dotted lines indicate the SQNR for OSRs 16,12 and 10, for the same modulator using 1-bit D/A block in the second stage. The point where the error curve crosses the ideal 1-bit line is the maximum acceptable INL

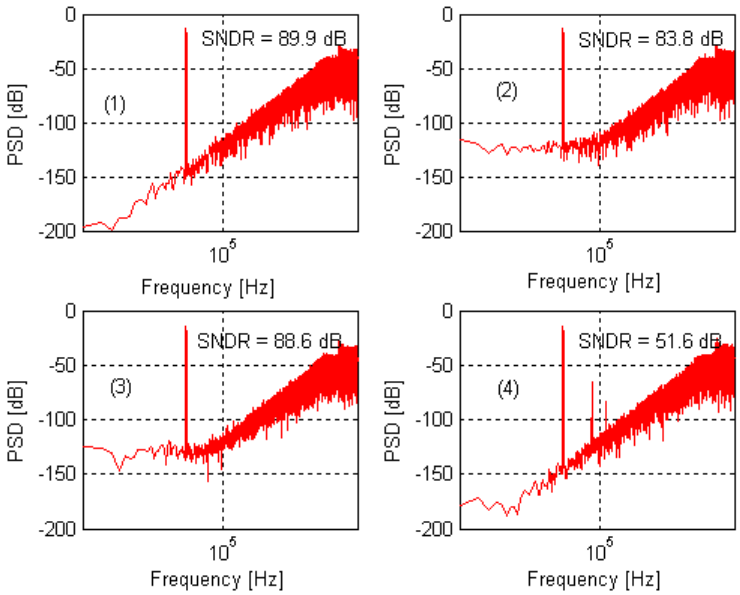

Figure 5.28: PSD of (1) the ideal modulator; (2) with sampling jitter, τ= 4 ns; (3) with kT/C noise, C_s = 1.25 pF; (4) with SR = 50 V/μs

for each case. The acceptable INL for OSRs of 16,12 and 10 are 0.3 LSB, 0.55 LSB and 0.7 LSB respectively. The INL error in form of LSBs indicate that higher error is tolerable for lower OSR compared to the $N_1 = 1$, $N_2 = 1$ converter. LSB refers to the voltage difference between the adjacent code steps.

5.9 Performance Analysis

Behavioral simulations were performed using the Matlab Simulink^{TM} models (80) which includes the various non-idealities affecting the operation of a SC sigma-delta modulator on a 2nd-order feed forward modulator. Here only the non-idealities of the first integrator were considered, since their effects are not attenuated by noise shaping. Figure 5.28 compares the power spectral densities (PSD) at the output of the modulator, when two of the most significant non-idealities in the first integrator are taken into account, with the PSD of the ideal modulator. The spectra put in evidence how the sampling jitter and kT/C noise increases the

Table 5.1: Performance summary for GSM, WCDMA and WLAN Mode

Parameters	**GSM**	**WCDMA**	**WLAN**
Order	2	2-2	2-2-2
Bandwidth (MHz)	0.2	5	10
OSR	128	16	8
Sampling frequency (MHz)	51.2	160	160
Input Signal frequency (MHz)	0.1	2.5	5
Quantizer Bits	1	1-2	1-2-4
SNR (dB)	86	72	62
Resolution (in bits)	14	11	10

in-band noise floor, while the slew-rate produces harmonic distortion. It must be noted from the results that the non-ideal effects resulting from practical circuit limitations add up and contribute to increase the in-band noise-plus-distortion and, therefore can become a severe limitation to the performance achievable from a given architecture.

Table 5.1 gives the performance summary of the designed multi-standard sigma-delta modulator toolbox for the three wireless standards namely GSM, WCDMA and WLAN. The individual stages of the 2-2-2 cascaded multi-mode sigma delta modulator are designed to attain high linearity with low distortion over the targeted bandwidth, thereby minimizing the area and power consumption. A low-distortion swing suppression topology is adopted for all the three cascaded stages which are less sensitive to circuit imperfections, especially at very low oversampling ratios.

5.10 Chapter Summary

In this chapter, a toolbox for the design of multi-standard sigma-delta modulator for three wireless standards is presented. The toolbox is developed using Matlab^{TM} Simulink models. This is a powerful tool as the user can perform a

quick design and analysis without a thorough understanding of the underlying methods. The toolbox incorporates most of the significant non-idealities like finite and nonlinear dc gain, slew rate and gain-bandwidth limitations, amplifier saturation voltage, capacitor mismatch, opamp input referred noise, kT/C noise, clock jitter and DAC capacitor mismatch. Behavioral simulation results indicate that the feedforward topology is less sensitive to circuit imperfections when compared to the traditional topology. These simulations help us to examine the trade-offs between the different parameters and choose the best solution to fulfil the application requirements.

Chapter 6

GA-based Optimization of Sigma-delta Modulators

6.1 Motivation

In this chapter we explore efficient optimization for sigma-delta modulator, in particular application to wireless design is considered. In sigma-delta modulator design, the scaling coefficients determine the peak signal-to-noise ratio. Therefore, selecting the optimum value of the coefficient is very important. To this end, this chapter addresses the design of a fourth-order multi-bit sigma-delta modulator suitable for Wireless Local Area Networks (WLAN) receivers with feed forward path and the optimum coefficients were selected using genetic algorithm (GA)-based search method. In particular, the proposed converter makes use of low-distortion swing suppression SDM architecture which is highly suitable for low oversampling ratios to attain high linearity over a wide bandwidth. A second-order traditional topology has been chosen as the second design example to validate our proposed method. The aim of this chapter is the identification of the best coefficients suitable for the proposed topology in order to achieve the desired signal-to-noise ratio. GA-based search engine is a stochastic search method which can find the optimum solution within the given constraints.

6.2 Introduction

Genetic algorithms (GAs) have been successfully applied to a wide range of optimization problems including design, scheduling, routing, and signal processing (40), (17), (52), (15), (90), (69), (2), (28), (12), (31). In sigma-delta ($\Sigma\Delta$) modulator design, GA can be effectively used to optimize the scaling coefficients in order to achieve the desired signal-to-noise ratio (62), (96), (97). $\Sigma\Delta$ modulators were traditionally used for audio applications where the over-sampling ratio is high and a high resolution can be achieved with a realizable clock frequency. Recently $\Sigma\Delta$ modulators are exploited for wideband applications like WLAN, thus preventing the excess increase in the OSR and resorting to higher order modulators. Higher order modulators with low OSR requires the optimization of system parameters in order to achieve the required dynamic range. The requirements that the ADC has to fulfill are set by both the standard characteristics and the receiver architecture. This work focuses on a zero-IF WLAN 802.11b receiver, presented in Figure 6.1 (32).

The zero-IF architecture shows excellent multi-standard capabilities, making our system easy to upgrade to multi-mode operation. The radio specifications of WLAN 802.11b (44) are summarized in Table 6.1. This together with the link budget, sets the minimum requirements for the ADC. Our architecture choice leads to a minimum dynamic range of 50dB for the ADC for a 10 MHz bandwidth.

This chapter presents the design and optimization of a highly linear sigma-delta modulator for wireless applications. The proposed architecture employs a multi-bit 2-2 modified cascaded sigma-delta modulator suitable for WLAN receivers. It also describes the genetic optimization algorithm used to find the optimal scaling coefficients for the proposed modulator. The simulation results for the two design examples are also presented at the end of the chapter.

6.3 Modulator Architecture

This Section explores tradeoffs among the wide variety of $\Sigma\Delta$ modulator architectures that can be used to implement a $\Sigma\Delta$ A/D converter suitable for low power

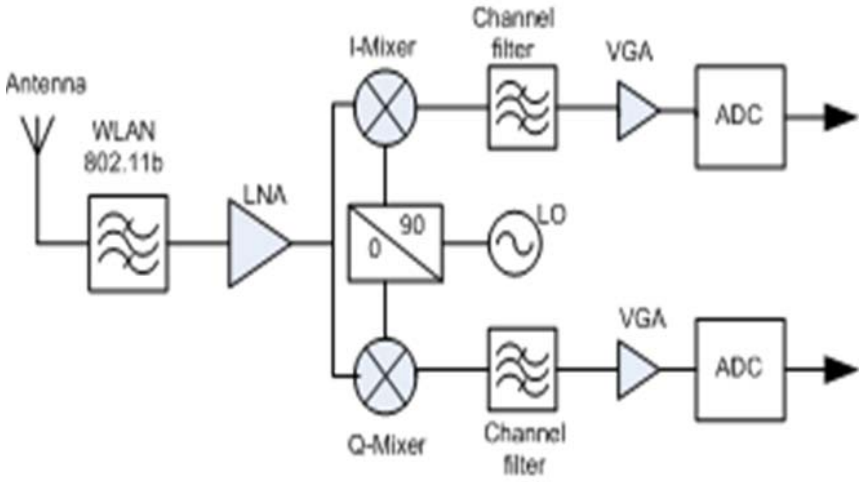

Figure 6.1: Zero-IF receiver architecture

and high integration WLAN standard receiver. The search for an optimal wide-band $\Sigma\Delta$ topology has been performed by varying the order L, the oversampling ratio M and the number of bits B in the quantizer (102).

The target specifications for the $\Sigma\Delta$ modulator were defined to be 50 dB DR over 10 MHz bandwidth at minimum power dissipation. For signals of very wide bandwidth, such as in WLAN receiver, oversampling ratio cannot be very high (4 or 5) because the achievable clock frequency is constrained by the process technology. Therefore the only solution is by increasing the order L and quantizer bits B in order to achieve the required resolution. The dynamic range DR (64), (38)

Table 6.1: Radio specifications for WLAN 802.11b

Frequency Band	2.412-2.484 GHz
Channel Spacing	25 MHz
Channel Bandwidth	20 MHz
Sensitivity	-76 dBm
Maximum Input Signal	-10 dBm
Input Noise	-104 dBm
Required SNR	14 dB

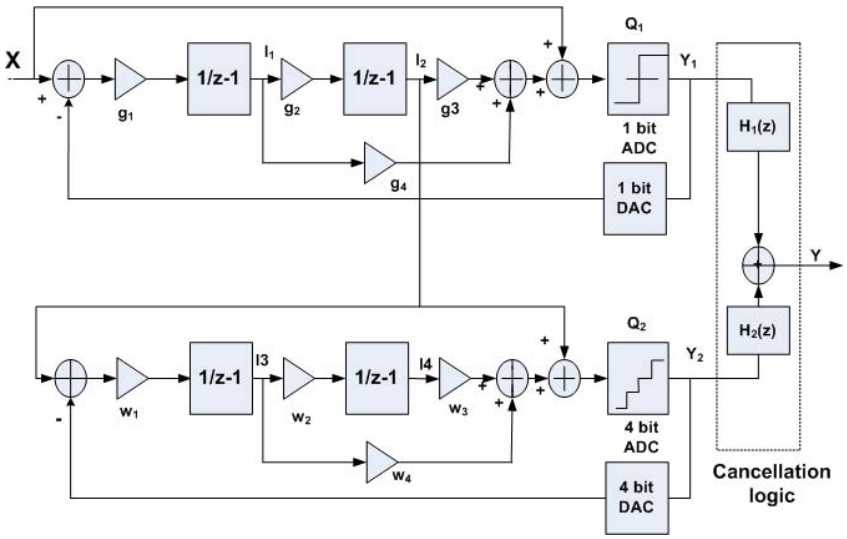

Figure 6.2: Modified cascaded sigma-delta modulator for WLAN

of a $\Sigma\Delta$ modulator is given by

$$DR = \left(\frac{2}{3}\right)\left(\frac{2L+1}{\pi^{2L}}\right) M^{(2L+1)} \left(2^B - 1\right)^2 \tag{6.1}$$

For low-data rate applications, such as GSM receiver, where bandwidth is relatively smaller, oversampling ratio (M) can be made higher, which will increase the circuit complexity and power consumption. For higher order or multi-bit modulators the complexity becomes higher, and for higher sampling frequency the requirements of analog building blocks becomes more demanding. Alternatively, the increased quantizer resolution enables us to use a lower oversampling ratio or a lower noise-shaping order for a given dynamic range bandwidth target. Unfortunately, the higher quantizer resolution will lead to a large area of internal flash ADC and switched-capacitor DAC and increased power consumption. An OSR of 8 has been chosen as a compromise between the technologically feasibility sampling frequency and bandwidth requirements. Once the OSR was established, a 2-2 modified cascaded modulator architecture has been adopted which can provide comparable dynamic ranges. The next key issue in the design of a low-power $\Sigma\Delta$ modulator is the quantizer resolution. Thus B plays an important role in the power-performance design of the modified cascaded sigma-delta modulator. A multi-bit quantizer with multi-bit feedback digital-to-analog

converter (DAC) has to be used to attain the WLAN specifications. The main drawback of multi-bit ΣΔ modulator is the high linearity that is required of the feedback DAC. Thus the overall sigma-delta converter linearity and resolution are limited by the precision of the multi-bit DAC. Reducing the quantizers resolution to 1 bit may eliminate the dependence on feedback DAC linearity. One way to achieve further reduction of quantization noise is to use a multi-bit quantizer only in the final stage to eliminate the necessity of DEM techniques to improve the linearity of multi-bit DAC. Therefore we have adopted a single bit quantizer in the first stage and 4-bit quantizer in the second stage.

Figure 6.2 shows the block diagram of the proposed modified cascaded sigma-delta modulator. The 4^{th} order modified cascaded ΣΔ modulator architecture employs two key design approaches. One is the 2^{nd} order sigma-delta modulator with feedforward signal path (21), (34), which has a high linearity even at low OSR. The other is the structural approach, which combines the merits of modified cascaded topology and multibit quantization in the last stage to make all quantization noise sources negligible at low oversampling (OSR). The scaling coefficients have been used to achieve the peak signal-to-noise and distortion ratio (SNDR), to control the input of the second stage and to utilize the full dynamic range of the next stage. By combining these techniques the performance improvements of the ΣΔ modulator are significant. The output of the first stage of the modulator is given by

$$Y_1(z) = X(z) + \frac{(1-z^{-1})^2}{(1+g_1g_4-2)z^{-1} + (1+g_1g_2g_3-g_1g_4)z^{-2}} Q_1(z) \tag{6.2}$$

The output of the integrators, I_1 and I_2 are given by

$$I_1(z) = \frac{g_1 z^{-1}(1-z^{-1})}{1+(g_1g_4-2)z^{-1} + (1+g_1g_2g_3-g_1g_4)z^{-2}} Q_1(z) \tag{6.3}$$

$$I_2(z) = \frac{g_1g_2 z^{-2}}{1+(g_1g_4-2)z^{-1} + (1+g_1g_2g_3-g_1g_4)z^{-2}} Q_1(z) \tag{6.4}$$

From equations 6.3 and 6.4, it is observed that the integrators process only the quantization noise. Therefore, the integrator output swings of the proposed architecture are reduced compared with the traditional one and then the operational amplifier requirements are greatly relaxed. Since the output of the second

integrator (I_2) contains only quantization noise, this output has been used as input for the second stage. Therefore, the output of the second stage is given by

$$Y_2(z) = \frac{g_1 g_2 z^{-2}}{1 + (g_1 g_4 - 2)z^{-1} + (1 + g_1 g_2 g_3 - g_1 g_4)z^{-2}} Q_1(z) + T(z) \tag{6.5}$$

where

$$T(z) = \frac{(1 - z^{-1})^2}{1 + (w_1 w_4 - 2)z^{-1} + (1 + w_1 w_2 w_3 - w_1 w_4)z^{-2}} Q_2(z) \tag{6.6}$$

and $Q_1(z)$ and $Q_2(z)$ are the quantization errors of the first and second stages respectively and g_1, g_2, g_3, g_4, w_1, w_2, w_3, w_4 are the analog coefficients. The final modulator output after the cancellation logic is given by equation 6.7

$$Y(z) = z^{-2} X(z) + T_1(z) \tag{6.7}$$

where

$$T_1(z) = \frac{1}{g_1 g_2} \frac{(1 - z^{-1})^4}{1 + (w_1 w_4 - 2)z^{-1} + (1 + w_1 w_2 w_3 - w_1 w_4)z^{-2}} Q_2(z) \tag{6.8}$$

where the digital coefficient is $g_5 = 1/g_1 g_2$ and the digital transfer functions are $H_1(z) = z^{-2}$ and $H_2(z) = g_5(1 - z^{-1})^2$. The coefficients selected randomly for generating the maximum peak signal to noise and distortion ratio (SNDR) were: $g_1 = g_2 = w_1 = w_2 = 0.5, g_3 = g_4 = w_3 = w_4 = 4$.

6.4 GA-Based Coefficient Optimization

6.4.1 Genetic Algorithm

GAs are search and optimization algorithms based on the mechanics of natural selection and natural genetics (21). They make use of structured but randomized information exchange and concept of the survival of the fittest. The algorithm starts with an initial population which consists of a collection of chromosomes i.e. possible solutions coded in the form of strings. The chromosome which produces the minimum error function value represents the best solution. The chromosomes which represent the better solutions are selected using roulette wheel selection technique. Genetic operators like crossover, mutation, elitism etc. are applied

over the selected chromosomes. As a result a new set of chromosome is produced. This process is repeated until a fit solution appears. In essence, a population of chromosomes is always available to get the desired result. Occasionally a new part is added to a chromosome to make it more robust. Genetic algorithms exploit past to extrapolate new search points to provide improved performance.

A robust method like GA works well across a wide range of problems and also is more efficient. The traditional derivatives based approach, enumerative schemes and simple random walks are not that good for all classes of problems. On the other hand, heuristics approaches, such as genetic algorithms (GAs), differ from the traditional ones in that there exists a high probability that the global optimal solution will be reached. Figure 6.3 shows the flowchart of the binary GA.

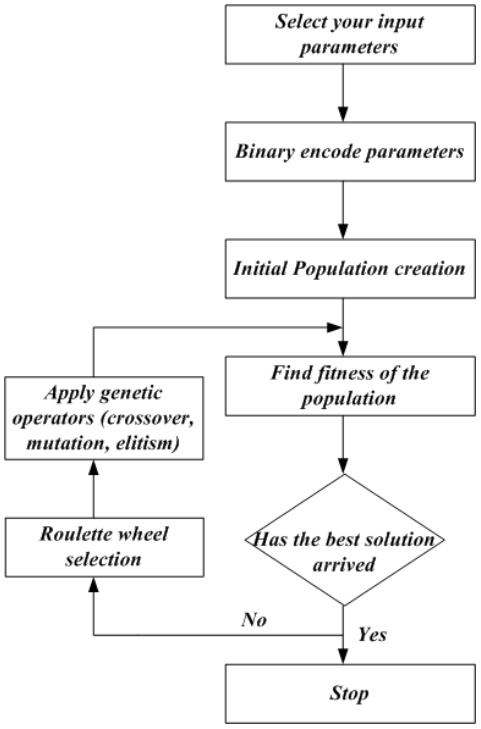

Figure 6.3: Flow chart of binary GA

6.4.2 Using GA in ΣΔ ADC Design

In the design of ΣΔ ADCs, we need to optimize a large set of parameters including the overall structures and the performance of the building blocks to achieve the required signal-to-noise ratio. Therefore, behavioral simulations were carried out using a set of Simulink^{TM} models (80), (57) in Matlab Simulink^{TM} environment in order to verify the performance for a WLAN system, to investigate the circuit non-idealities effect, to optimize the system parameters and to establish the specifications for the analog cells. The most important parameter to be optimized in a sigma-delta modulator are the gain coefficients in order to achieve the desired signal-to-noise ratio. GA is one of the best optimization technique which finds a global optimum solution without taking much of the computational power.

The steps involved in the process of optimization using GA is shown in Figure 6.3. There are two general schemes for coding the solutions: (i) binary coding (ii) decimal coding. In our work, binary coding has been used where 0s and 1s are used to form a chromosome of length l depending on the precision needed. After defining the chromosome, an initial population is obtained by randomly producing N number of chromosomal solutions called the first generation.

The next step, called pairing, consists of selecting the chromosomes that will pair together to reproduce the offsprings. This is done by using roulette wheel selection technique. These pairs will be used for reproduction. Reproduction ensures that chromosomes with higher fitness will have a higher probability of reproduction than chromosomes with lower fitness. Reproduction is the application of crossover, mutation and elitism operators over the selected chromosomes. In this work single point crossover has been used as shown in Figure 6.4.

Mutation rate (MR) is set to a very low value. A high MR introduces high diversity but might cause instability. However, a very low MR makes it difficult for the GA to find a global optimal solution. In addition to crossover and mutation the best chromosome present in a particular generation is passed on to the next generation so that it will not be lost until the next best arrives. In this way the stability of the GA is improved. A fitness function or objective function has to be obtained to evaluate the performance of the chromosomes and compare

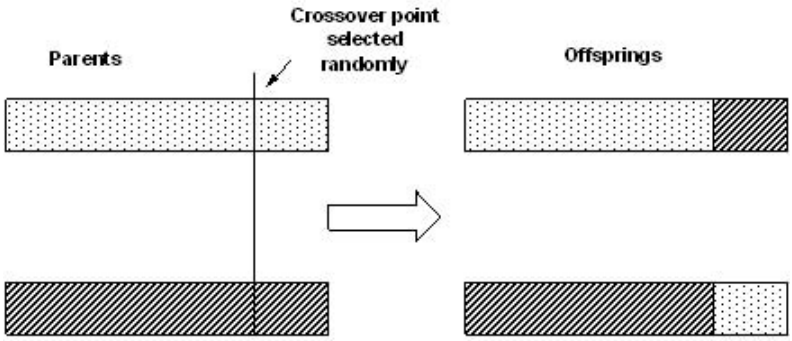

Figure 6.4: Single-point crossover process

their performance. In the design of sigma-delta modulator we need to optimize the coefficients for a maximum signal-to-noise ratio (SNR). Hence the fitness function is formulated as

$$fitness = \frac{1}{Error} \tag{6.9}$$

$$where \quad Error \; = \; DesiredSNR \; - \; ObtainedSNR \tag{6.10}$$

After evaluating the fitness function, fitness values will be assigned to each chromosome. If the best fit chromosome has arrived, the GA can be stopped and the coefficient values can be decoded. Otherwise the chromosomes are sent back to the selection module and the whole procedure is repeated again until the best arrives or the maximum number of generation set is reached.

It is to be noted that the number of chromosomes should not be very small or very high. Too small a population size will lead to very fast convergence of GA and thus one may not obtain an optimum solution. Too high a population size will take a lot of computation time for the GA to converge which needs sufficient computing power.

6.5 Simulation Results

6.5.1 Case A

A fourth-order sigma-delta feed forward topology has been chosen as the first design example in which simulations were performed for both using ideal and real integrator blocks. Real integrator block takes into account the main circuit non-idealities like opamp finite dc gain, slew rate, gain-bandwidth product and amplifier saturation voltage. In this work a population of 20 binary chromosomes for a precision of 3 decimal places has been run for 20 generations to get the optimum value of the coefficients. Crossover rate and mutation rate were chosen as 0.7 and 0.8/l respectively where l is the length of the chromosome. At the end of the 20^{th} generation, the optimum values of the coefficients were obtained as $g_1 = 0.325$, $g_2 = 0.7646$, $g_3 = 4.023$, $g_4 = 6.1538$. Figure 6.5 shows the convergence plot for the first coefficient g_1 which is the most critical one. After 20 generations, the optimum value for g_1 was found to be 0.325 for which the peak SNDR was 64 dB. Table 6.2 shows that there is almost a 6dB increase or 1-bit resolution in both SNR and SNDR after using GA-based optimization technique.

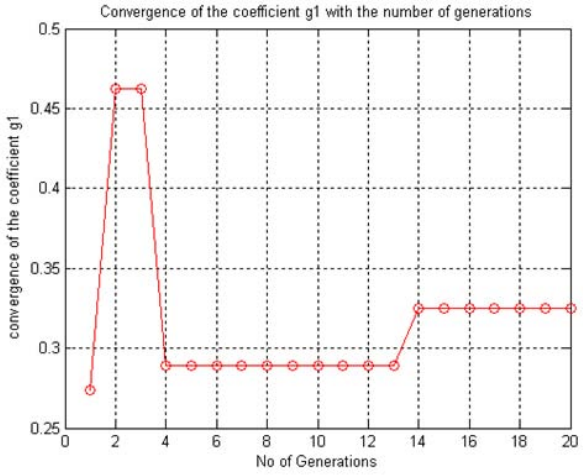

Figure 6.5: Convergence of coefficient g_1 with number of generations

Simulations were performed using an OSR of 8 for a bandwidth of 10 MHz. Figure 6.6 shows the modulator output spectrum for a 0.5V/2.5MHz input signal.

Table 6.2: Comparison of gain coefficients with and without GA

	Coefficients	Peak SNR	Peak SNDR
Without GA	$g_1 = 0.5,\ g_2 = 0.5$ $g_3 = 4,\ g_4 = 4$	64 dB	59 dB
With GA	$g_1 = 0.325,\ g_2 = 0.7646$ $g_3 = 4.023,\ g_4 = 6.1538$	69 dB	64 dB

As shown in Figure 6.6, the peak SNDR achieved was found to be 64 dB with a finite dc gain of 60 dB, slew rate of at least $300V/\mu s$ and a gain-bandwith product of 350 MHz.

Figure 6.7 presents the simulated SNDR versus input signal amplitude for WLAN. Simulation results show a peak SNDR of 59 dB @ -6dBFS without using GA and 64 dB @ -4dBFS after optimizing the coefficients using GA in the WLAN mode.

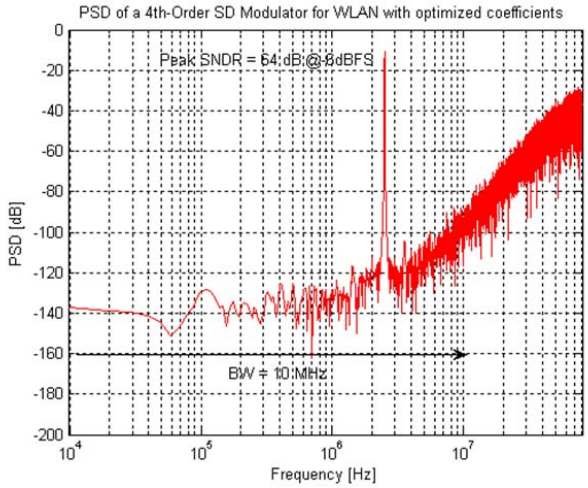

Figure 6.6: Modulator output spectrum for WLAN

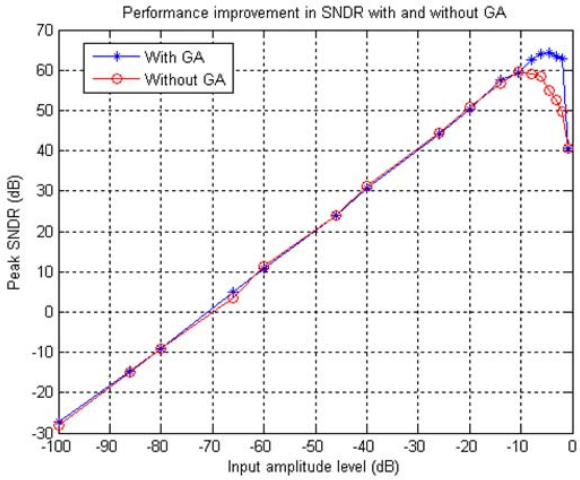

Figure 6.7: SNDR versus input signal amplitude with and without GA

6.5.2 Case B

A traditional second-order sigma-delta topology has been chosen as the second design example which is shown in Figure 6.8. In the design of the modulator, integrator signal swings should be limited within the linear region, in order to maximize the dynamic range. In order to reduce the signal swings, integrator gains otherwise called scaling coefficients are employed for each of the integrator inputs. In a switched-capacitor circuit implementation these gains are easily realized by appropriately sizing the input sampling capacitors.

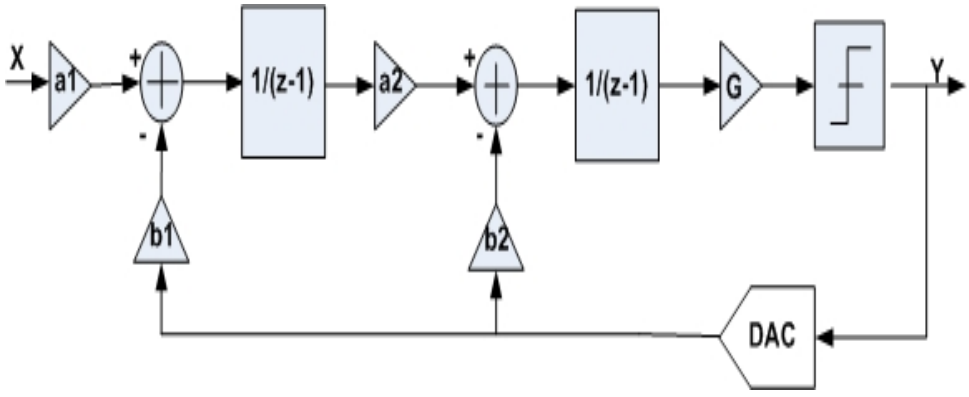

Figure 6.8: A traditional second-order sigma-delta topology

According to the unity gain approximation, the equivalent quantizer gain G in the topology of Figure 6.8 is given by

$$G = (1/b_1 a_2) \tag{6.11}$$

The integrator gains in the modulator should satisfy the following constraint:

$$(b_2/b_1 a_2) = 2 \tag{6.12}$$

In this example, we apply our method to design a traditional 2^{nd} order sigma-delta modulator. The bandwidth was selected to be 200 KHz with an over sampling ratio of 64. The simulation was performed using $Matlab^{TM}$ Simulink environment which achieves a peak SNR of 76 dB with 1-bit quantization. With traditional topology, $G = 2/a_2$ and it is stable when the input amplitude is less than 0.5. First we focus on searching for solutions with large peak SNR and good stability (i.e., stable input range is about (0, 0.5). In addition, we want to avoid designs with overly large spread of coefficients. With these goals in mind we set $a_1 = 0.5$ and $b_1 = 0.5$. In the first run of the GA, a satisfactory solution with a peak SNR of 72.9 dB was obtained in 10 generations, which is called solution A as shown in Table 6.3. This corresponds to $a_2 = b_2 = 0.68957$. The convergence curve for a_2 (b_2) is shown in Figure 6.9. It can be seen that a_2 (b_2) converged in the 6^{th} generation and remains the same afterwards. In the second run of the GA based search algorithm another good solution B was found within 10 generations. In comparison to solution A, solution B has slightly higher SNR of 74.1 dB with a quantizer gain G = 1.6339. Its stable input range is (0, 0.7). The search algorithm was run repeatedly many times and the results of some of the runs are shown in Table 6.3. It can be seen from Table 6.3 that each time the algorithm is run the solution converges to either a different or same maxima. Solution C was the best solution having a peak SNR of 76 dB with a stable input range of (0, 0.5) with G = 1.7946, and coefficient $a_2 = b_2 = 1.1144$ which is very close to the theoretical dynamic range of 79 dB calculated using equation 6.1.

Then, we challenge ourselves to search for solutions by varying the coefficients (a_1, b_1) such that $a_1 = b_1$ within the range (0.6, 1). It was found that the modulator became more and more unstable as the scaling factors are moved closer

to unity. Therefore, we searched for solutions by limiting the coefficients within the stable range of (0.1, 0.5). This example demonstrate that our proposed GA based search engine can explore a much broader design space and find good solutions with different characteristics in terms of peak SNR, stable input range and spread of coefficients. This enables designers to make tradeoffs between different objectives and/or constraints, and to accommodate different design requirements.

Table 6.3: Second example: Coefficients

Solutions	$a_1(b_1)$	$a_2(b_2)$	$G = \frac{2}{a_2}$	SNR (dB)
A	0.5	0.68957	2.9003	72.9
B	0.5	1.22404	1.6339	74.1
C	0.5	1.1144	1.7946	76.3
D	0.5	1.21452	1.6467	74.1
E	0.5	1.11835	1.7883	76.2

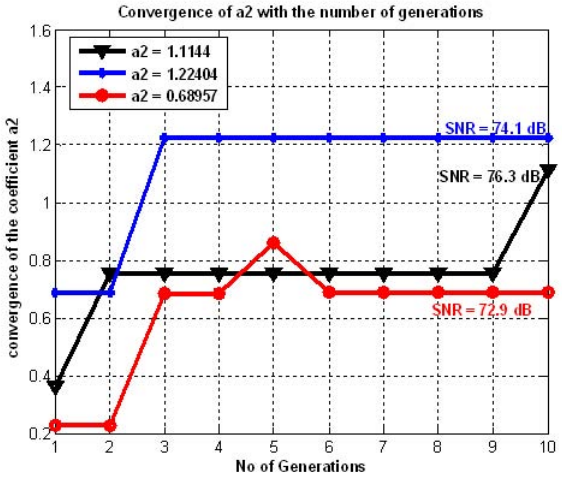

Figure 6.9: Convergence of a_2 with the number of generations

The plot in Figure 6.9 shows the convergence of a_2 with the number of generations for 3 runs of GA (Solutions A, B & C as shown in Table 6.3). It can be seen that in most of the cases, optimum solution arrived within 10 generations. All

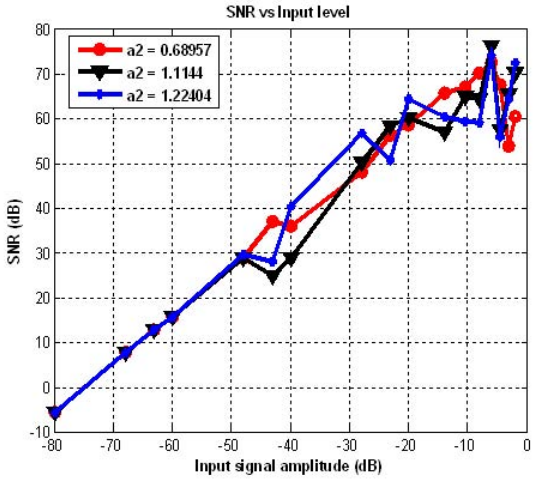

Figure 6.10: SNR vs. input amplitude for a second-order traditional topology

the solutions provided peak SNR values closer to the theoretical dynamic range and the solution C was found to be the closest. Figure 6.10 shows SNR vs. input signal amplitude for the first 3 runs of GA in Table 6.3. It shows that a peak SNR of 76 dB is achieved for a coefficient $a_2 = b_2 = 1.1144$.

We have provided two design examples and numerical results to demonstrate the effectiveness of our proposed method. The choice of the scaling coefficients g_1 and a_2 affects the shape of the search space and the solution the search algorithm will lead us to. Proper selection of the scaling coefficients is required to limit the integrator signal swings and to maximize the dynamic range.

6.6 Chapter Summary

A GA-based search engine is developed for the quick and easy design of sigma-delta modulators. The genetic algorithm based search engine can effectively search for solutions with different characteristics and enables tradeoffs between different design considerations. It has been successfully used to improve the performance of a 2-2 cascaded feed forward sigma-delta ADC which is proposed for WLAN applications. The coefficients were optimized using GA which results in extended dynamic range. It has also been applied to a traditional second order

feedback topology to find peak SNR values with good stability. Design examples and numerical results demonstrate the effectiveness of our proposed method.

Chapter 7

Conclusions and Future Work

This chapter concludes the thesis by giving a summary of the previous chapters. An overview of future work is given from a perspective based on the results presented in this thesis.

7.1 Summary of the Thesis

The main contribution of the thesis are summarized as follows.

- First, at the system level, a full feedforward topology is introduced and its unique features compared to the traditional topology are presented. Then a dual-mode sigma-delta $\Sigma\triangle$ architecture which uses the low-distortion swing suppression topology is proposed to meet the design specifications of GSM and WCDMA applications. The modulator achieves a peak SNDR of 83 dB for GSM and 75 dB for WCDMA in the presence of circuit non-idealities. Then the dual-mode design has been extended to a triple-mode architecture which uses a 2-2-2 reconfigurable sigma-delta modulator that can handle GSM, WCDMA and WLAN standards. Special measures are taken to switch-off the unused blocks of second and third stages to reduce the power consumption. The configurable sigma-delta modulator has been designed in TSMC 0.18um CMOS technology, operating from 1.8V supply voltage. The proposed sigma-delta modulator for GSM/WCDMA/WLAN

receiver was implemented as a fully-differential switched-capacitor (SC) circuit which has been simulated using SPICE. The design of the individual circuit blocks like operational transconductance amplifier (OTAs), switches, capacitors and comparators has been done based on behavioral simulation results. The modulator achieves a peak SNDR of 82/68/54 dB for GSM/WCDMA/WLAN standards respectively in the presence of circuit non-idealities.

- Secondly, to expedite the handling of complicated design calculations, a Graphical User Interface GUI based design tool is also proposed. In particular, multi-standard sigma-delta modulator design for three wireless communication standards consisting of GSM, WCDMA and WLAN is considered. A 2-2-2 reconfigurable sigma-delta modulator is proposed which can meet the design specifications of the three standards. The sigma-delta modulator design tool is developed using the Graphical User Interface Development Environment (GUIDE) in MATLAB. A systematic study of the various $\Sigma\triangle$ non-idealities to optimize the system parameters and to establish the specifications of the analog building blocks to achieve the required signal-to-noise ratio is also investigated. The main non-idealities considered here are finite and nonlinear dc gain, slew rate and gain-bandwidth limitations, amplifier saturation voltage, capacitor mismatch, opamp input referred noise, kT/C noise, clock jitter and DAC capacitor mismatch.

- In sigma-delta modulator design, the scaling coefficients determine the peak signal-to-noise ratio. Therefore, selecting the optimum value of the coefficient is very important. Towards this, the design of a fourth-order multi-bit sigma-delta modulator suitable for Wireless Local Area Networks (WLAN) receivers with feed forward path is selected as an example. Further, a Genetic Algorithm(GA) based search method is introduced. In particular, the proposed converter makes use of low-distortion swing suppression SDM architecture which is highly suitable for low oversampling ratios to attain high linearity over a wide bandwidth. A second-order traditional topology has been chosen as the second design example to validate our proposed method. The basic aim is the identification of the best coefficients suitable

for the proposed topology in order to achieve the desired signal-to-noise ratio. GA-based search engine is a stochastic search method which can find the optimum solution within the given constraints.

7.2 Future Work

This section discusses future directions of our research by pointing out some of the possible forms to improve and extend the work presented in this thesis. Higher data transferring rate, seamless integration between various wireless infrastructures, such as cellular networks and IP networks, form the scenario of the fourth generation (4G) wireless system. For such a system, a multi-standard reconfigurable sigma-delta modulator, which is able to support various standards for the 4G of mobile communication systems, is essential for the next mobile systems

- In this thesis, we concentrated only on the design and implementation of low-pass $\Sigma\triangle$ modulators. Depending on the frequency band of interest, there is another type of $\Sigma\triangle$ modulator, band-pass $\Sigma\triangle$ modulator, widely used in wireless transceivers (85) (88), (91). By applying different loop filters inside the $\Sigma\triangle$ modulator, a high attenuation of quantization noise in a certain frequency band can be realized. This type of modulator is useful in digitizing signals within a certain frequency range and finds its applications in wireless transceivers.

- The non-linearity of the feedback DAC connected with a multibit quantizer is another area which needs attention to increase the dynamic range. This can be done by using dynamic element matching (DEM) techniques. Of all DEM techniques, the data weighted averaging (DWA) algorithm is an effective and simple technique to realize the DEM.

- A two stage optimization approach using Genetic Algorithm (GA) both at the system-level and circuit-level for the design of $\Sigma\triangle$ modulators can be investigated. A high-level simulation-based GA can quickly find an optimum topology given the input specifications. Circuit-level simulation-based

GA can simplify and automate the circuit design process for designers significantly reducing the overall time consumed. Genetic Algorithm can also be extended for the design and optimization of the noise transfer function in higher-order $\Sigma\triangle$ modulators so that the resulting A/D or D/A converter is stable.

- A challenge to practical utilization of the multi-standard design technique is to create of an effective computer aided design tool that will automatically generate the coefficient of the modulator given it order and other design parameters. Although some of the concepts and algorithms necessary for such a package have been presented, a significant amount of research remains to be done to make it competitive with standard computer aided design (CAD) package.

- Behavioural Modelling and Simulation of $\Sigma\triangle$ Modulators Using Hardware Description Languages is an alternative to the costly electrical simulation of $\Sigma\triangle$ modulators. An important benefit derived from the use of these description languages is that HDL simulators are already included in many commercial design environments (22). In this way, $\Sigma\triangle$ modulators modelled with VHDL can be simulated together with other VHDL-modelled blocks and even continuous-time descriptions of blocks, modeled using VHDL-AMS.

- Until recently, reconfigurable logic and Field Programmable Gate Array (FPGA) chips have been used primarily for prototyping. However, it is now being realized that reconfigurable architectures are a separate family in their own right, just as processors and ASIC are with unique properties that can be used for easy re-configuration. The basic building block of reconfigurable logic is a reconfigurable cell which is implemented using Look-Up-Table (LUT), Programmable Logic Array (PLA) or Memory. LUT or memory-based cell is configured by writing the result of the combinational logic to the cell. Apart from the modulator which is described in thesis, decimation filter (18), (9), (41), (61) is an integral part of the complete ADC design. Therefore designing re-configurable filter structures is key to to the effective

use of multi-standard architectures. Hence, this is one of the areas for future research.

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